Low Dropout, Two-Bank LED Driver with PWM Brightness Control

FEATURES

- **Regulated Output Current with 2% LED-to-LED Matching**
- **Drives Up to Four LEDs at 25mA Each in a Common Cathode Topology**
- **28mV Typical Dropout Voltage Extends Usable Supply Range in Li-Ion Battery Applications**
- **Brightness Control Using PWM Signals**
- **Two 2-LED Banks with Independent Enable and PWM Brightness Control per Bank**
- **No Internal Switching Signals—Eliminates EMI**
- **Default LED Current Eliminates External Components**
  - **Default values from 3mA to 10mA (in 1mA increments) available using innovative factory EEPROM programming**
  - **Optional external resistor can be used for high-accuracy, user-programmable current**
- **Over-Current and Over-Temperature Protection**
- **Available in Wafer Chip-Scale Package or 2,5mm × 2,5mm SON-10**

APPLICATIONS

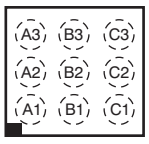
- **Keypad and Display Backlighting**
- **White and Color LEDs**
- **Cellular Handsets**
- **PDAs and Smartphones**

DESCRIPTION

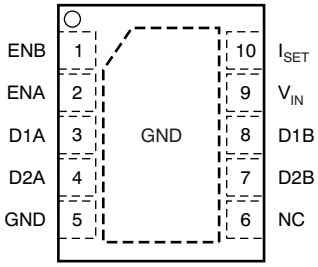
The TPS7510x linear low dropout (LDO) matching LED current source is optimized for low power keypad and navigation pad LED backlighting applications. The device provides a constant current to up to four unmatched LEDs organized in two banks of two LEDs each in a common-cathode topology. Without an external resistor, the current source defaults to factory-programmable, preset current level with ±0.5% accuracy (typical). An optional external resistor can be used to set initial brightness to user-programmable values with higher accuracy. Brightness can be varied from off to full brightness by inputting a pulse width modulation (PWM) signal on each Enable pin. Each bank has independent enable and brightness control, but current matching is done to all four channels concurrently. The input supply range is ideally suited for single-cell Li-Ion battery supplies and the TPS7510x can provide up to 25mA per LED.

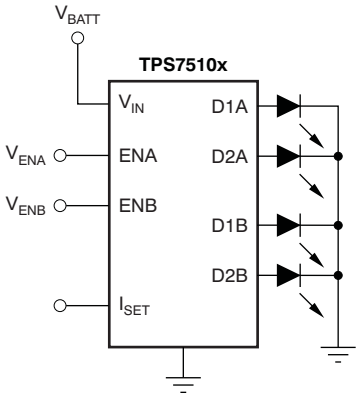
No internal switching signals are used, eliminating troublesome electromagnetic interference (EMI). The TPS7510x is offered in an ultra-small, 9-ball, 0.4mm ball-pitch wafer chip-scale package (WCSP) and a 2,5mm × 2,5mm, 10-pin SON package, yielding a very compact total solution size ideal for mobile handsets and portable backlighting applications. The device is fully specified over T_J = –40°C to +85°C.

TPS7510x YFF 9-Ball WCSP (Top View)



TPS7510x DSK 2,5mm x 2,5mm SON-10 (Top View)





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT ID	OPTIONS(2)
TPS7510**x** ***yyyz***	**X** is the nominal default diode output current (for example, 3 = 3mA, 5 = 5mA, and 0 = 10mA). **YYY** is the package designator. **Z** is the reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Default set currents from 3mA to 10mA in 1mA increments are available through the use of innovative factory EEPROM programming. Minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted).

PARAMETER	VALUE
V_{IN} range	–0.3V to +7.0V
V_{ISET}, V_{ENA}, V_{ENB}, V_{DX} range	–0.3V to V_{IN}
I_{DX} for D1A, D2A, D1B, D2B	35mA
D1A, D2A, D1B, D2B short circuit duration	Indefinite
Continuous total power dissipation	Internally limited
Junction temperature (T_J)	–55°C to +150°C
Storage temperature	–55°C to +150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C	T_A = +70°C	T_A = +85°C
Low-K(1)	YFF	55°C/W	208°C/W	4.8mW/°C	480mW	264mW	192mW
High-K(2)	YFF	55°C/W	142°C/W	7.0mW/°C	704mW	387mW	282mW
	DSK	40°C/W	60.6°C/W	17mW/°C	1650mW	908mW	660mW

(1) The JEDEC low-K (1s) board used to derive this data was a 3 inch × 3 inch, two-layer board with 2 ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3 inch × 3 inch, multi-layer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	2.7		5.5	V
I_{DX}	Operating current per LED	3		25	mA
t_{PWM}	On-time for PWM signal	33			µs
T_J	Operating junction temperature range	–40		+85	°C

ELECTRICAL CHARACTERISTICS

Over operating junction temperature range (T_J = –40°C to +85°C), V_{IN} = 3.8V, DxA and DxB = 3.3V, R_{SET} = 32.4kΩ, and ENA and ENB = 3.8V, unless otherwise noted. Typical values are at T_A = +25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SHDN}	Shutdown supply current	$V_{ENA,B}$ = 0V, V_{DX} = 0V			0.03	1.0	µA
I_{GND}	Ground current	DSK package	I_{DX} ≤ 5mA, V_{IN} = 3.8V		170	230	µA
			I_{DX} > 5mA, V_{IN} = 3.8V		250	300	µA
		YFF package	I_{DX} ≤ 5mA, V_{IN} = 4.5V		170	200	µA
			I_{DX} > 5mA, V_{IN} = 4.5V		250	300	µA
ΔI_D	Current matching ($I_{DXMAX} - I_{DXMIN}/I_{DXMAX}$) × 100%	T_A = +25°C		0	2	4	%
		T_A = –40°C to +85°C	YFF package	0		5	%
			DSK package	0		6	%
$\Delta I_{DX}\%/\Delta V_{IN}$	Line regulation	3.5V ≤ V_{IN} ≤ 4.5V, I_{DX} = 5mA			2.0		%/V
$\Delta I_{DX}\%/\Delta V_{DX}$	Load regulation	1.8V ≤ V_{DX} ≤ 3.5V, I_{DX} = 5mA			0.8		%/V
V_{DO}	Dropout voltage of any DX current source (V_{DX} at I_{DX} = 0.8 × $I_{DX,\ nom}$)	I_{DXnom} = 5mA			28	100	mV
		I_{DXnom} = 15mA			70		
V_{ISET}	Reference voltage for current set			1.183	1.225	1.257	V
I_{OPEN}	Diode current accuracy(1)	I_{SET} = open, V_{DX} = V_{IN} – 0.2V	YFF package		0.5	3	%
			DSK package		0.5	4	%
I_{SET}	I_{SET} pin current range			2.5		62.5	µA
k	I_{SET} to I_{DX} current ratio(1)				420		
V_{IH}	Enable high level input voltage			1.2			V
V_{IL}	Enable low level input voltage					0.4	V
I_{INA}	Enable pin A (V_{ENA}) input current	V_{ENA} = 3.8V			5.0	6.1	µA
		V_{ENA} = 1.8V			2.2		
I_{INB}	Enable pin B (V_{ENB}) input current	V_{ENB} = 3.8V			4.0	4.9	µA
		V_{ENB} = 1.8V			1.8		
t_{SD}	Shutdown delay time	Delay from ENA and ENB = low to reach shutdown current (I_{DX} = 0.1 × $I_{DX,\ nom}$)		5	13	30	µs
T_{SD}	Thermal shutdown temperature	Shutdown, temp increasing			+165		°C
		Reset, temp decreasing			+140		

(1) Average of all four I_{DX} outputs.

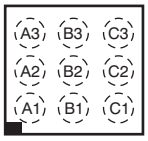
Table 1. Recommended (1% Tolerance) Set Resistor Values

R_{SET} (kΩ)	I_{SET} (µA)	I_{DX} (mA)(1)
511	2.4	1.0
255	4.8	2.0
169	7.2	3.0
127	9.6	4.1
102	12.0	5.0
84.5	14.5	6.1
73.2	16.7	7.0
64.9	18.9	7.9
56.2	21.8	9.2
51.1	24.0	10.1
46.4	26.4	11.1
42.2	29.0	12.2
39.2	31.3	13.1
36.5	33.6	14.1
34.0	36.0	15.1
32.4	37.8	15.9
30.1	40.7	17.1
28.7	42.7	17.9
26.7	45.9	19.3
25.5	48.0	20.2
24.3	50.4	21.2
23.2	52.8	22.2
22.1	55.4	23.3
21.5	57.0	23.9
20.5	59.8	25.1

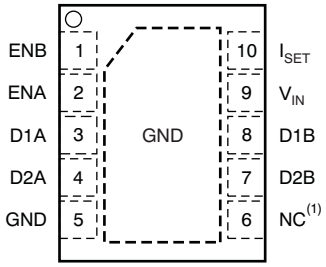
(1) $I_{DX} = (V_{SET}/R_{SET}) \times k$.

PIN ASSIGNMENTS

YFF PACKAGE
9-BALL WCSP
(TOP VIEW)



DSK PACKAGE
2,5mm × 2,5mm SON-10
(TOP VIEW)

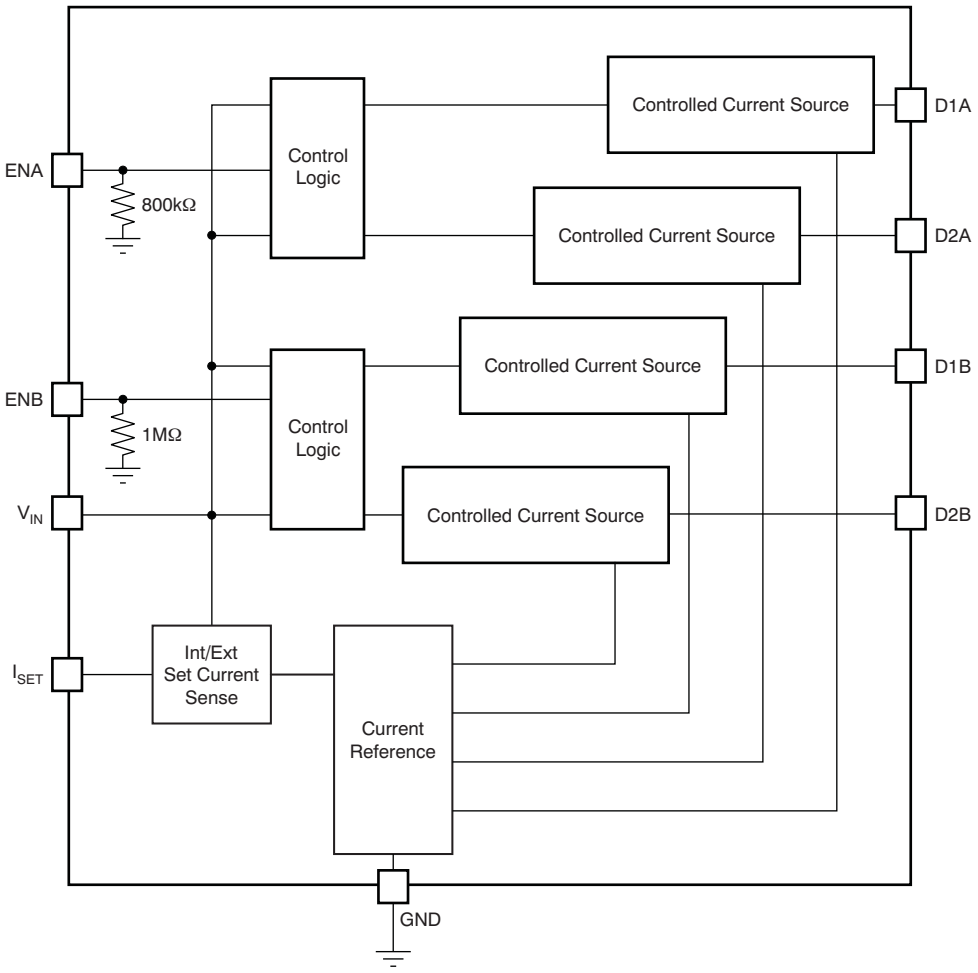


NOTE (1): Not connected

TERMINAL FUNCTIONS

NAME	WCSP	SON	INPUT/ OUTPUT	DESCRIPTION
ENA	A3	2	I	Enable pin, Bank A. Driving this pin high turns on the current source to Bank A outputs. Driving this pin low turns off the current source to Bank A outputs. An applied PWM signal reduces the LED current (between 0mA and the maximum current set by I_{SET}) as a function of the duty cycle of the PWM signal. ENA and ENB can be tied together. ENA can be left OPEN or connected to GND if not used. See the Application Information section for more details.
D1A	B3	3	O	Diode source current output, Bank A. Connect to LED anode.
D2A	C3	4	O	Diode source current output, Bank A. Connect to LED anode.
ENB	A2	1	I	Enable pin, Bank B. Driving this pin high turns on the current source to Bank B outputs. Driving this pin low turns off the current source to Bank B outputs. An applied PWM signal reduces the LED current (between 0mA and the maximum current set by I_{SET}) as a function of the duty cycle of the PWM signal. ENA and ENB can be tied together. ENB can be left OPEN or connected to GND if not used. See the Application Information section for more details.
V_{IN}	B2	9	I	Supply Input
GND	C2	5, Pad	—	Ground
I_{SET}	A1	10	O	An optional resistor can be connected between this pin and GND to set the maximum current through the LEDs. If no resistor is connected, I_{SET} defaults to the internally-programmed value.
D1B	B1	8	O	Diode source current output, Bank B. Connect to LED anode.
D2B	C1	7	O	Diode source current output, Bank B. Connect to LED anode.
NC	—	6	—	Not connected.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Over operating junction temperature range (T_J = –40°C to +85°C), V_{IN} = 3.8V, DxA and DxB = 3.3V, R_{SET} = 32.4kΩ, and ENA and ENB = high, unless otherwise noted. Typical values are at T_A = +25°C.

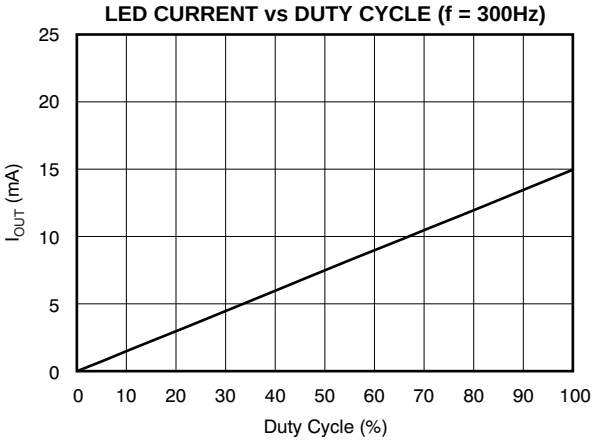


Figure 1.

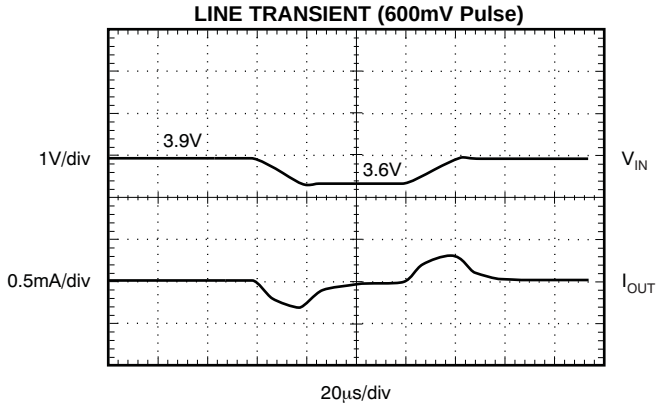


Figure 2.

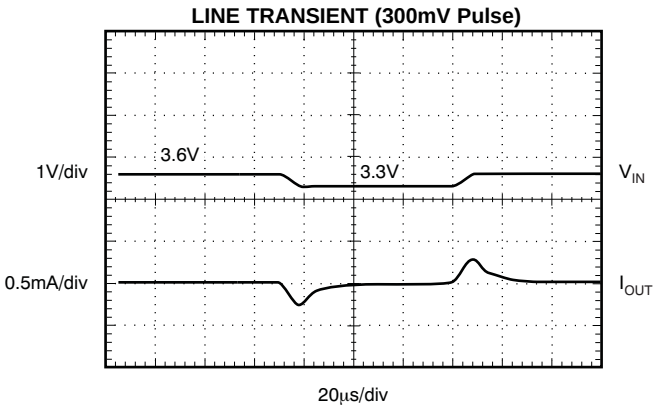


Figure 3.

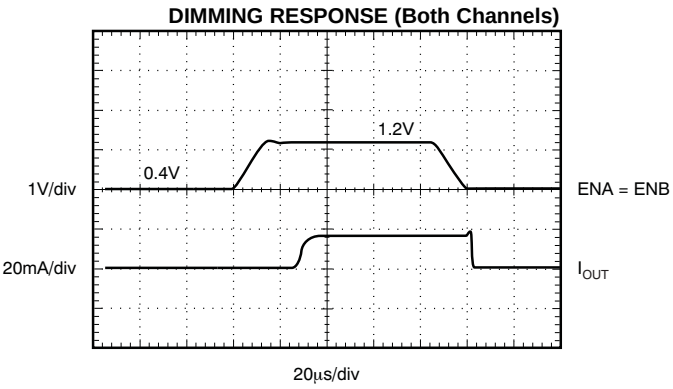


Figure 4.

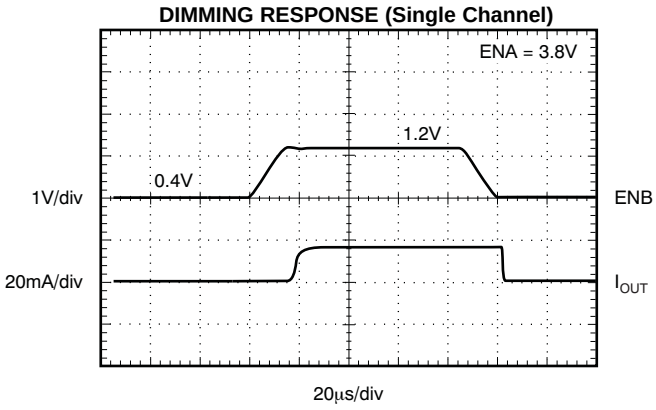


Figure 5.

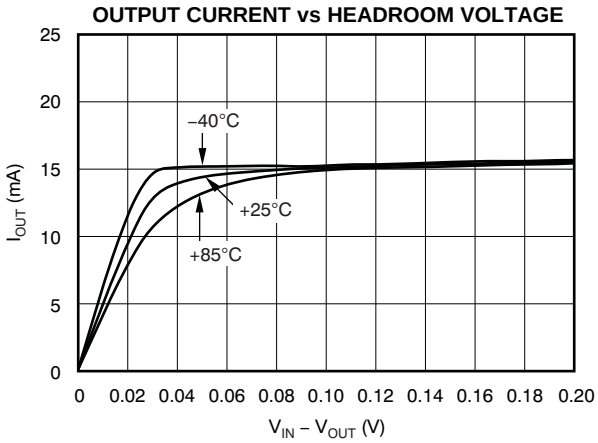


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Over operating junction temperature range (T_J = –40°C to +85°C), V_{IN} = 3.8V, DxA and DxB = 3.3V, R_{SET} = 32.4kΩ, and ENA and ENB = high, unless otherwise noted. Typical values are at T_A = +25°C.

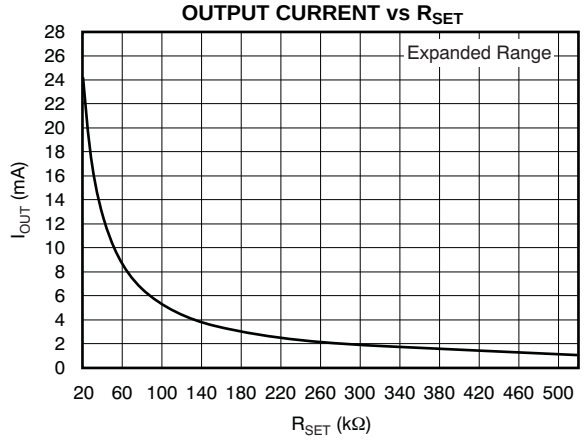


Figure 7.

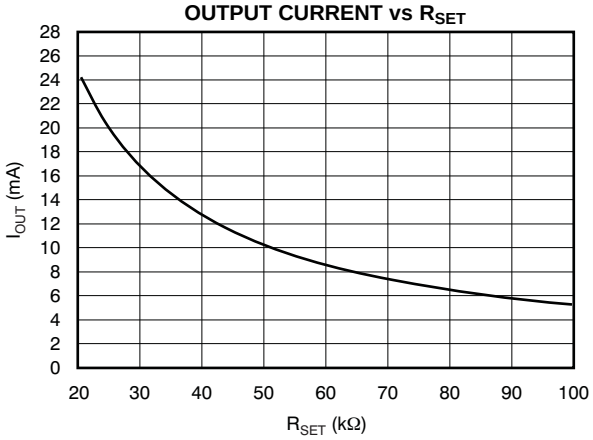


Figure 8.

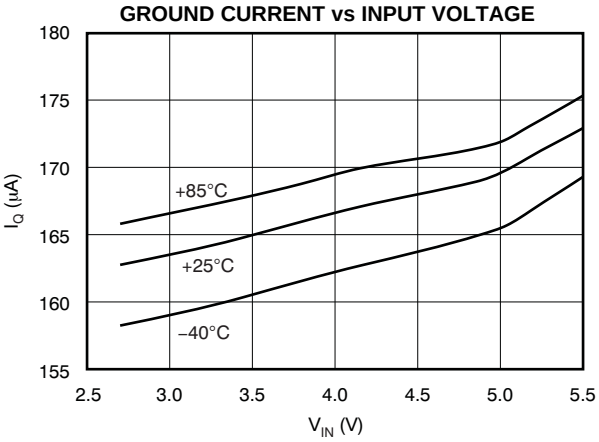


Figure 9.

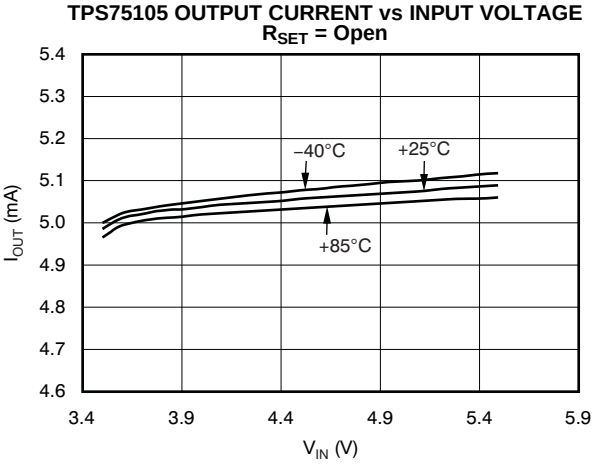


Figure 10.

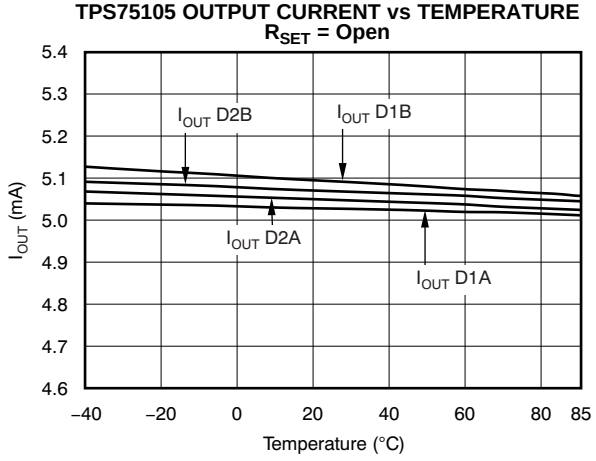


Figure 11.

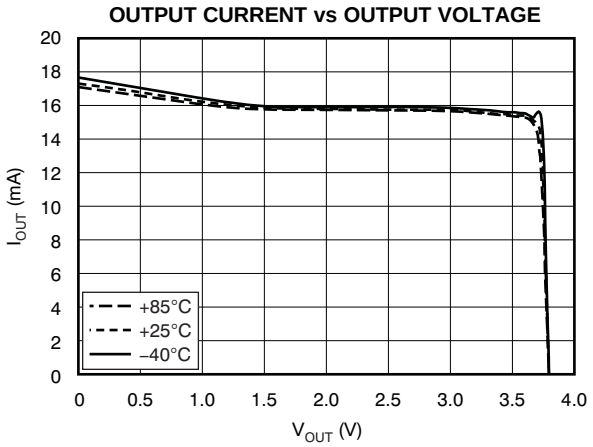


Figure 12.

APPLICATIONS INFORMATION

SETTING THE OUTPUT CURRENT LEVEL

The TPS7510x is a quad matched current source. Each of the four current source output levels is set by a single reference current. An internal voltage reference of 1.225V (nominal) in combination with a resistor sets the reference current level. This reference current is then mirrored onto each of the four outputs with a ratio of typically 420:1. The resistor required to set the LED current is calculated using Equation 1:

$$R_{ISET} = \frac{K \times V_{ISET}}{I_{LED}} \quad (1)$$

where:

- K is the current ratio
- V_{ISET} is the internal reference voltage
- I_{LED} is the desired LED current

For example, to set the LED current level to 10mA, a resistor value of 51.1kΩ is required. This value sets up a reference current of 23.9μA (1.22V/51.1kΩ). In turn, this reference current is mirrored to each output current source, resulting in an output current of 10mA (23.9μA × 420).

The TPS7510x offers two methods for setting the output current levels. The LED current is set either by connecting a resistor (calculated using Equation 1) from the I_{SET} pin to GND, or leaving I_{SET} unconnected to employ the factory-programmed R_{SET} resistance. The internal programmed resistance is implemented using high-precision processing and yields a reference current accuracy of 0.5%, nominal. Accuracy using external resistors is subject to the tolerance of the external resistor and the accuracy of the internal reference voltage.

The TPS7510x automatically detects the presence of an external resistor by monitoring the current out of the I_{SET} pin. Current levels in excess of 3μA signify the presence of an external resistor and the device uses the external resistor to set the reference current. If the current from I_{SET} is less than 3μA, the device defaults to the preset internal reference set resistor. The TPS7510x is available with eight preset current levels, from 3mA to 10mA (per output) in 1mA increments. Solutions using the preset internal current level eliminate an external component, thereby increasing accuracy and reducing cost.

LIMITATIONS ON LED FORWARD VOLTAGES

The TPS7510x is a linear current source implementing LDO regulator building blocks. Therefore, there are some limitations to the forward (output) voltages that can be used while maintaining accurate operation. The first limitation is the maximum LED forward voltage. Because LDO technology is employed, there is the dropout voltage to consider. The TPS7510x is an ultra-low dropout device with typical dropouts in the range of 30mV at 5mA. Care must be taken in the design to ensure that the difference between the lowest possible input voltage (for example, battery cut-off) and the highest possible forward voltage yields at least 100mV of headroom. Headroom levels less than dropout decrease the accuracy of the current source (see Figure 6).

The other limitation to consider is the minimum output voltage required to yield accurate operation. The current source employs NMOS MOSFETs, and a minimum forward LED voltage of approximately 1.5V on the output is required to maintain highest accuracy. The TPS7510x is ideal for white LEDs and color LEDs with forward voltages greater than 1.5V. This range includes red LEDs that have typical forward voltages of 1.7V.

USE OF EXTERNAL CAPACITORS

The TPS7510x does not require the use of any external capacitors for stable operation. Nominal stray and/or power-supply decoupling capacitance on the input is adequate for stable operation. Capacitors are not recommended on the outputs because they are not needed for stability.

USE OF UNUSED OUTPUTS OR TYING OUTPUTS TOGETHER

Unused outputs may be left unconnected or tied to the V_{IN} supply. While open outputs are acceptable, tying unused outputs to the V_{IN} supply increases ESD protection. Connecting unused output to ground violates the minimum recommended output voltage, results in current levels that potentially exceed the set/preset LED current and should be avoided.

Connecting outputs in parallel is an acceptable way of increasing the amount of LED current drive. This configuration is a useful trick when the higher current level is a multiple of the preset value.

USE OF ENABLE PINS FOR PWM DIMMING

The TPS7510x divides control of the LED outputs into two banks of two current sources each. Each bank is controlled by the use of an independent, active-high enable pin (ENA and ENB). The enable pin can be used for standard ON/OFF operation of the current source, driven by standard logic levels from processor GPIO pins, for example. Drive EN high to turn on the bank of LEDs; drive EN low to turn off the bank of LEDs.

Another use of the enable pin is for LED dimming. LED brightness is a function of the current level being driven across the diode and the time that current is being driven through the diode. The perceived brightness of an LED can be changed by either varying the current level or, more effectively, by changing the time in which that current is present. When a PWM signal is input into the enable pin, the duty cycle (high or ON time) determines how long the fixed current is driven across the LEDs. Reducing or increasing that duration has the effect of dimming or brightening the LED, without having to employ the more complex method of varying the current level. This technique is particularly useful for reducing LED brightness in low ambient light conditions, where LED brightness is not required, thereby decreasing current consumption. The enable pins can also be used for LED blinking, varying blink rates based on system status.

Although providing many useful applications, PWM dimming does have a minimum duty cycle required to achieve the required current level. The recommended minimum on time of the TPS7510x is approximately 33µs. On times less than 33µs result in reductions in the output current by not allowing enough time for the output to reach the desired current level. Also, having both enables switching together, asynchronously, or having one enable on at all times, impacts the minimum recommended on time (see Figure 4 and Figure 5). If one enable is already on, the speed at which the other channel turns on is faster than if both channel were turning on together or if the other channel is off. Therefore, connecting one enable on allows for approximately 10µs to 12µs shorter minimum on times of the switching enable channel.

Unused enable pins can be left unconnected or connected to ground to minimize current consumption. Connecting unused enable pins to ground increases ESD protection. If connected to V_{IN}, a small amount of current drains through the enable input (see the Electrical Characteristics table).

LOAD REGULATION

The TPS7510x is designed to provide very tight load regulation. In the case of a fixed current source, the output load change is a change in voltage. Tight load regulation means that output voltages (LED forward voltages) with large variations can be used without impacting the fixed current being sourced by the output or the output-to-output current matching. The permissible variation on the output not only allows for large variations in white LED forward voltages, but even permits the use of different color LEDs on different outputs with minimal effect on output current.

LINE REGULATION

The TPS7510x is also designed to provide very tight line regulation. This architecture allows for voltage transient events to occur on the power supply (battery) without impacting the fixed output current levels or the output to output current matching. A prime example of such a supply transient event is the occurrence of a transmit pulse on the radio of a mobile handset. These transient pulses can cause variations of 300mV and 600mV on the supply to the TPS7510x. The line regulation limitation is that the lower supply voltage level of the event does not cause the input to output voltage difference to drop below the dropout voltage range.

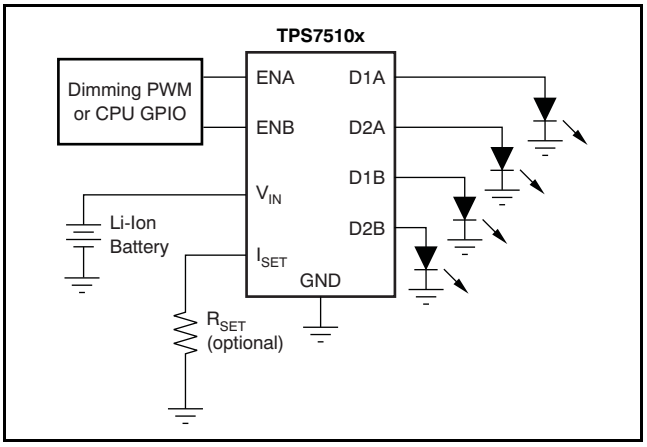


Figure 13. Typical Application Diagram

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (January 2010) to Revision I **Page**

- Changed test conditions for ground current parameter in the Electrical Characteristics 3
- Deleted Figure 14; duplicate mechanical image. 10

Changes from Revision G (March 2009) to Revision H **Page**

- Added DSK package dissipation information to Dissipation Ratings table 2
- Revised ground current parameter, Electrical Characteristics; changed symbol from I_Q to I_{GND}; added specifications for YFF and DSK packages 3
- Added YFF and DSK package specifications for current matching parameter, Electrical Characteristics 3
- Changed diode current accuracy parameter, Electrical Characteristics, to reflect YFF and DSK package specifications 3
- Deleted operating junction temperature range specification from Electrical Characteristics table to eliminate redundancy 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS75100DSKR	ACTIVE	SON	DSK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SKX	Samples
TPS75100DSKT	ACTIVE	SON	DSK	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SKX	Samples
TPS75100YFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	FB	Samples
TPS75100YFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	FB	Samples
TPS75100YZR	PREVIEW	DSBGA	YZ	9		TBD	Call TI	Call TI	-40 to 85		
TPS75103YFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		FC	Samples
TPS75103YFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		FC	Samples
TPS75105DSKR	ACTIVE	SON	DSK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CHH	Samples
TPS75105DSKT	ACTIVE	SON	DSK	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CHH	Samples
TPS75105YFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	FE	Samples
TPS75105YFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	FE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

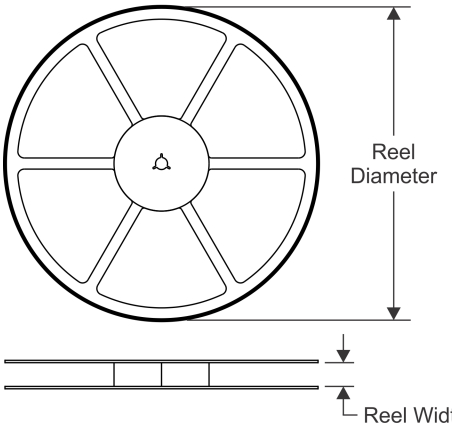
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

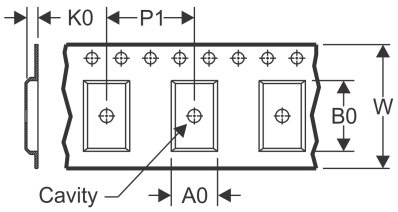
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

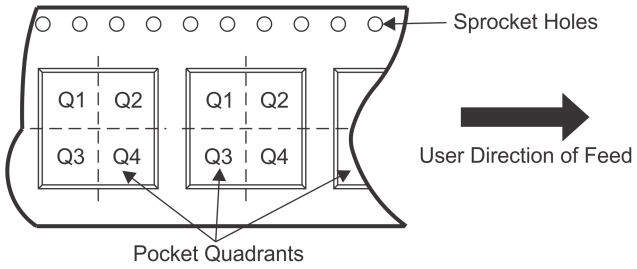


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

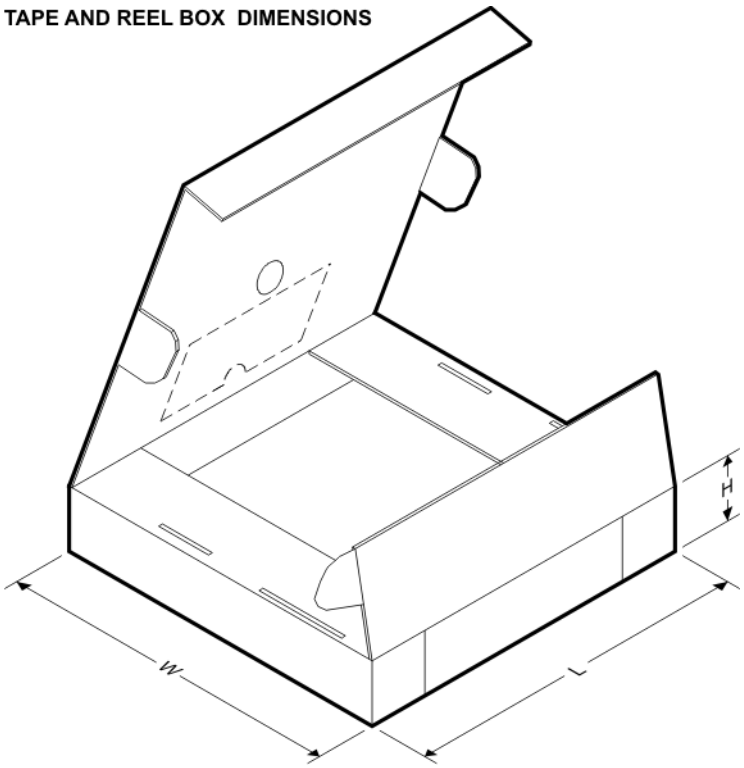
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS75100DSKR	SON	DSK	10	3000	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2
TPS75100DSKT	SON	DSK	10	250	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2
TPS75100YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.34	1.34	0.81	4.0	8.0	Q1
TPS75100YFFT	DSBGA	YFF	9	250	180.0	8.4	1.34	1.34	0.81	4.0	8.0	Q1
TPS75103YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1
TPS75103YFFT	DSBGA	YFF	9	250	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1
TPS75105DSKR	SON	DSK	10	3000	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2
TPS75105DSKT	SON	DSK	10	250	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2
TPS75105YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1
TPS75105YFFT	DSBGA	YFF	9	250	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1

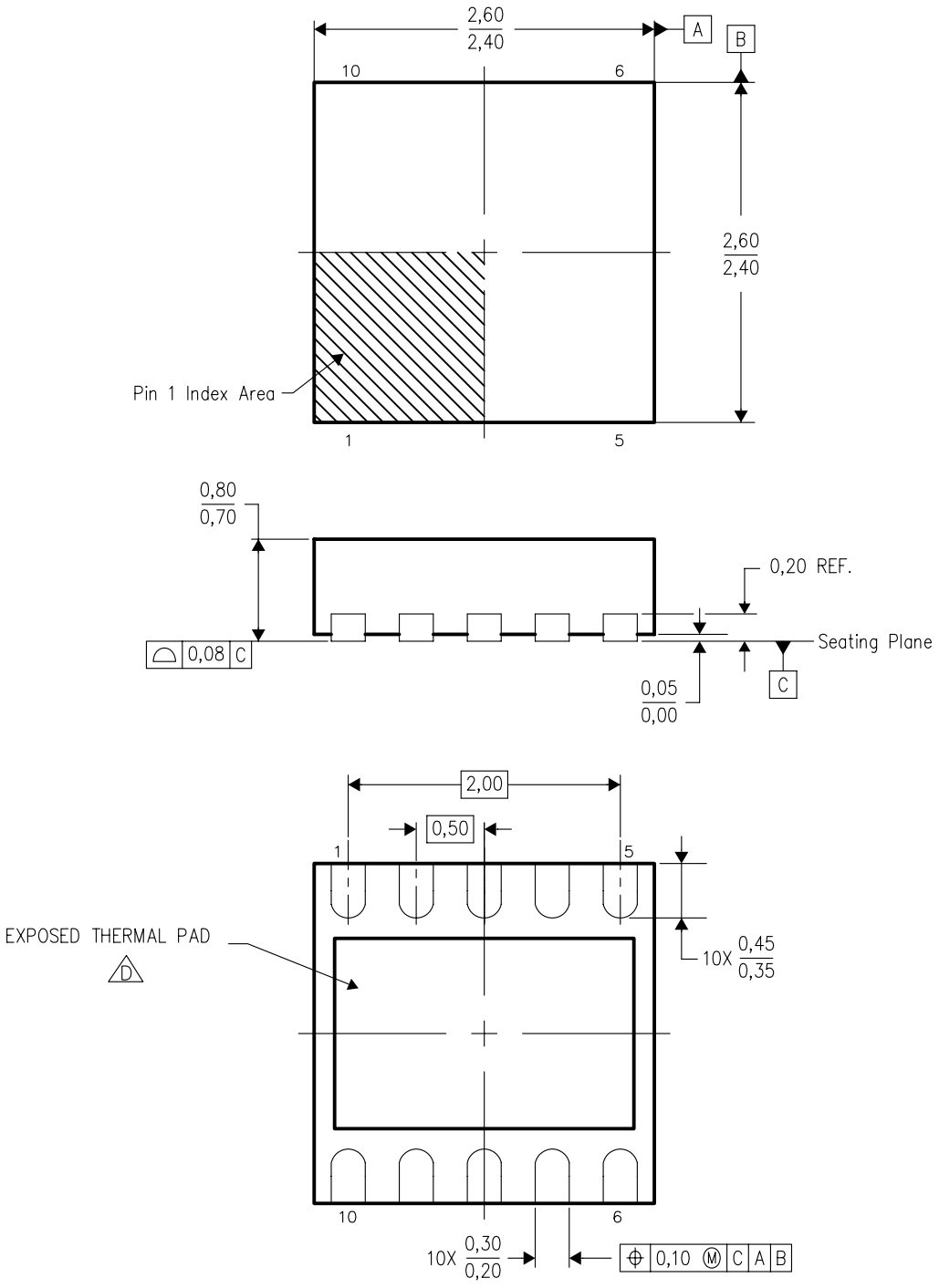
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS75100DSKR	SON	DSK	10	3000	203.0	203.0	35.0
TPS75100DSKT	SON	DSK	10	250	203.0	203.0	35.0
TPS75100YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS75100YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS75103YFFR	DSBGA	YFF	9	3000	210.0	185.0	35.0
TPS75103YFFT	DSBGA	YFF	9	250	210.0	185.0	35.0
TPS75105DSKR	SON	DSK	10	3000	203.0	203.0	35.0
TPS75105DSKT	SON	DSK	10	250	203.0	203.0	35.0
TPS75105YFFR	DSBGA	YFF	9	3000	210.0	185.0	35.0
TPS75105YFFT	DSBGA	YFF	9	250	210.0	185.0	35.0

DSK (S–PDSO–N10) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

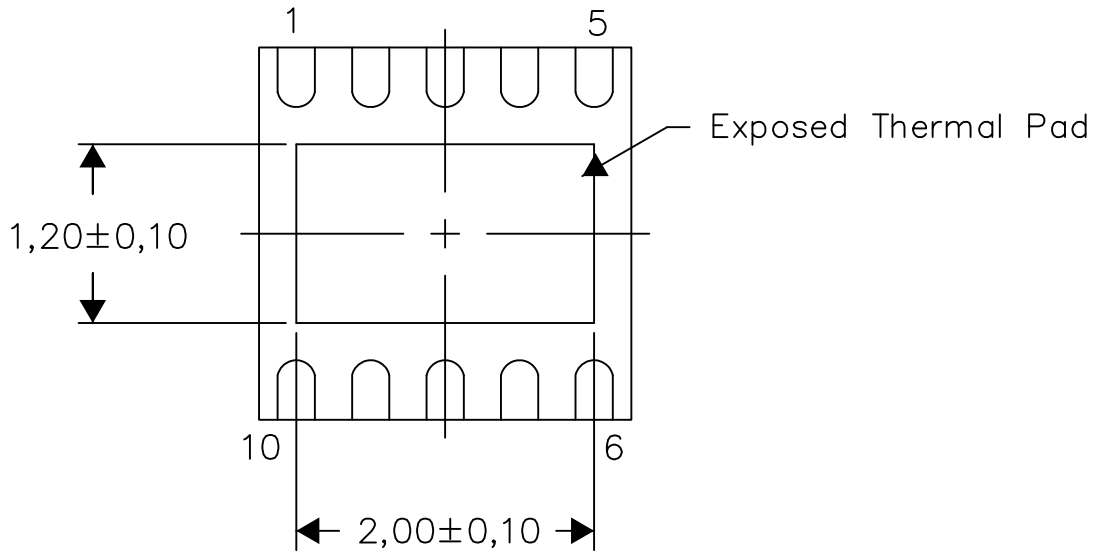
DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



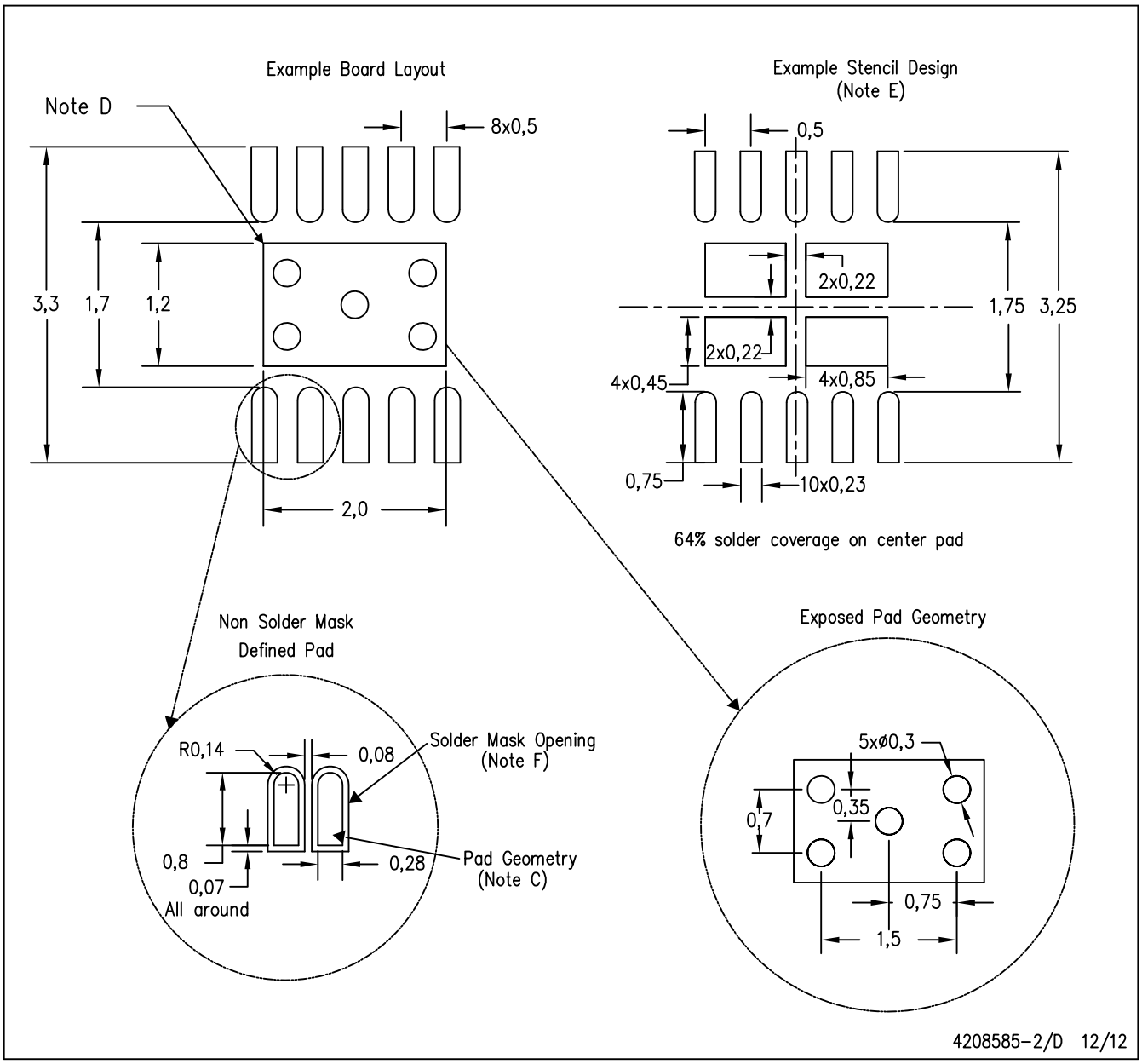
Bottom View

Exposed Thermal Pad Dimensions

4208579–2/E 12/12

NOTE: All linear dimensions are in millimeters

DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



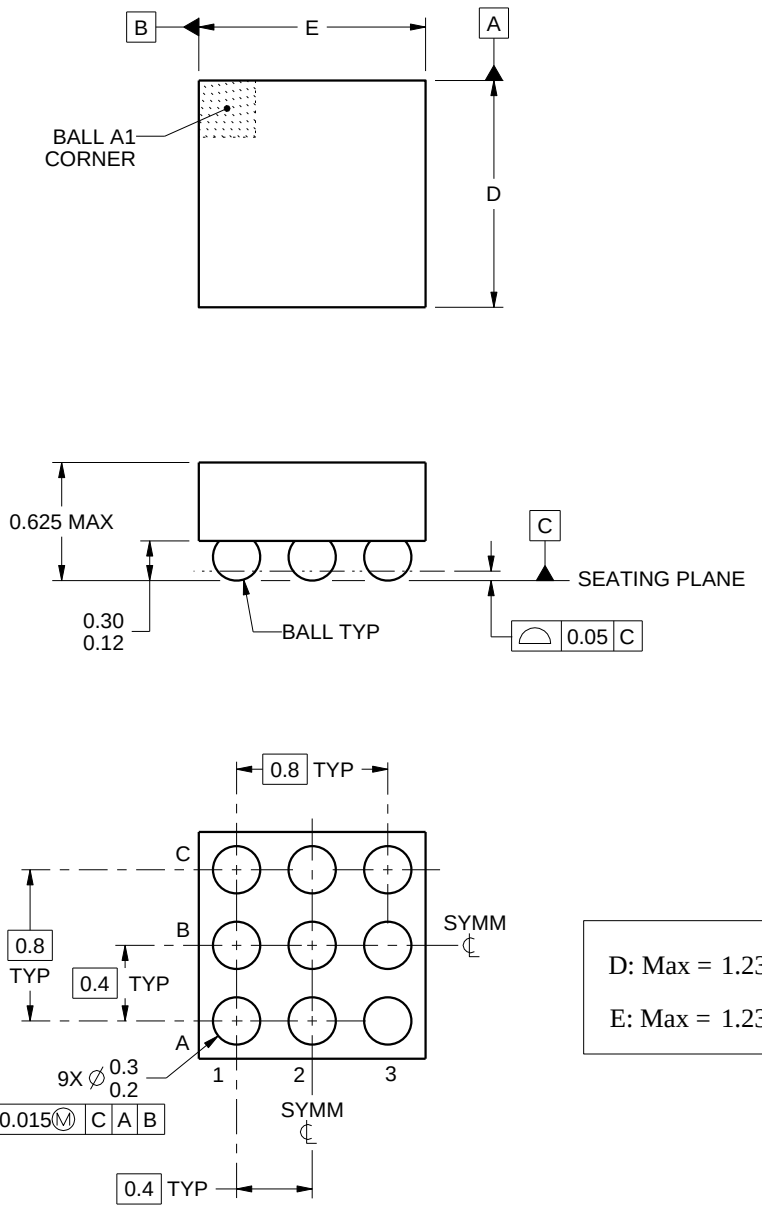
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

PACKAGE OUTLINE

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.238 mm, Min =1.178 mm

E: Max = 1.238 mm, Min =1.178 mm

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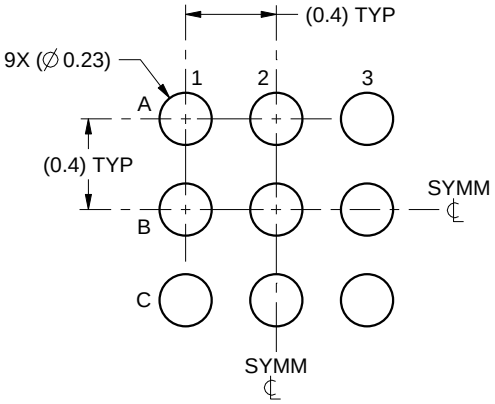
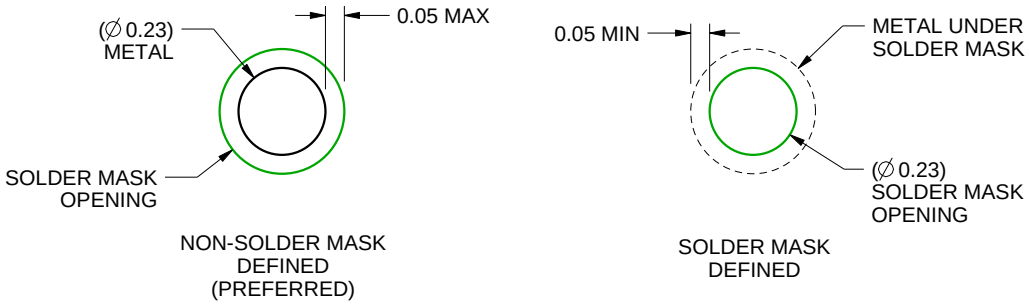
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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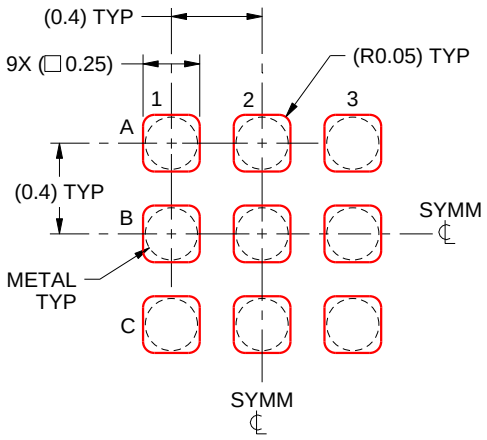
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219552/A 05/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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