General Description

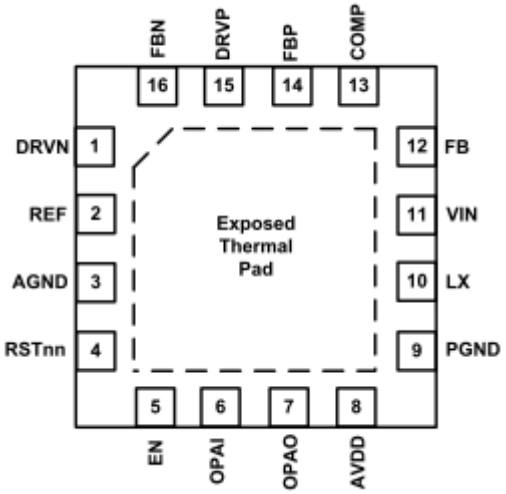
TheEC9223 is an integrated power supply solution optimized for small to medium size thin- film transistor (TFT) liquid crystal displays (LCD's). The boost converter operates at a fixed frequency of 1.2MHz. The integrated N-channel FET has a current limit of 1.8A. The positive and negative charge pumps provide regulated TFT LCD gate-on and gate-off supplies. Both outputs can be adjusted by external resistive voltage dividers.

The integrated operational amplifier is typically used for LCD VCOM driving; the output can sink or source up to 150mA short-circuit current. A built-in voltage detector generates a reset signal when the input voltage drops below 2.6V. The reset signal is active low and has a 123ms blanking time during power-on. The EC9223 is available in a thin 16-pin 3x3 mm WQFN green package.

Features

- 2.5V to 5.5V input supply
- Active-high Enable Control
- Current-mode boost regulator
  - 1.2MHz switching frequency
  - Integrated 20V/1.8A 700mΩ FET
  - Fast transient response to pulsed load
  - High efficiency up to 90%
  - Adjustable high-accuracy output voltage(±1%)
- VGH positive charge pump
- VGL negative charge pump
- Integrated unity-gain V_{COM} buffer
  - ±150mA output current limit
  - 12V/us slew rate
  - 12MHz Bandwidth
- Low-voltage detection circuit
- Soft-start and timed delay fault latch for all outputs
- Thermal shutdown
- Thin 3x3 mm 16-lead WQFN package

QFN-16 Pin Configuration



Applications

- TFT LCD for Notebooks
- Tablet Personal Computer Display
- Car Navigation Display
- Portable equipment

PIN DESCRIPTION

Number	Name	Pin Description
1	DRVN	Negative charge pump driver output.
2	REF	Reference output. All power outputs are disabled until REF exceeds its UVLO
3	AGND	Analog ground.
4	RSTnn	Voltage detector output. RSTnn is an active-low open-drain output.
5	EN	Enable control input pin. This pin has a 4uA pull-down current source.
6	OPAI	Unity-gain buffer input pin.
7	OPAO	Unity-gain buffer output pin.
8	AVDD	Charge pump and unity-gain buffer supply.
9	PGND	Boost converter power ground (source of the internal NMOS switch).
10	LX	Boost converter switching node (drain of the internal NMOS switch).
11	VIN	Supply for PWM, reference and other circuits.
12	FB	Boost converter feedback voltage input.
13	COMP	Boost converter error amplifier compensation node.
14	FBP	Positive charge pump feedback input.
15	DRVP	Positive charge pump driver output.
16	FBN	Negative charge pump feedback input.
-	TP	Thermal Pad, connect to AGND.

Ordering Information

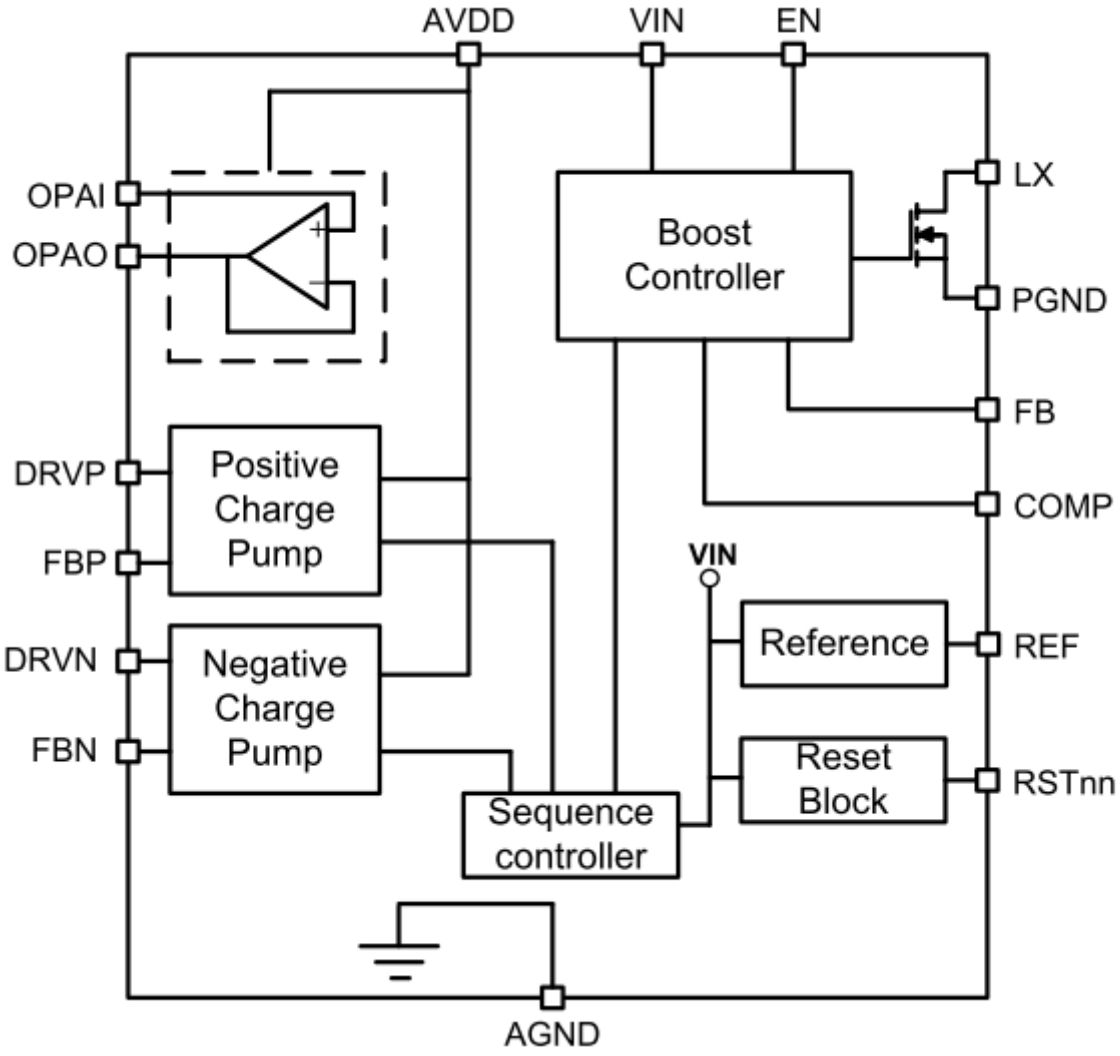
EC9223 NN XX X

R:Tape & Reel

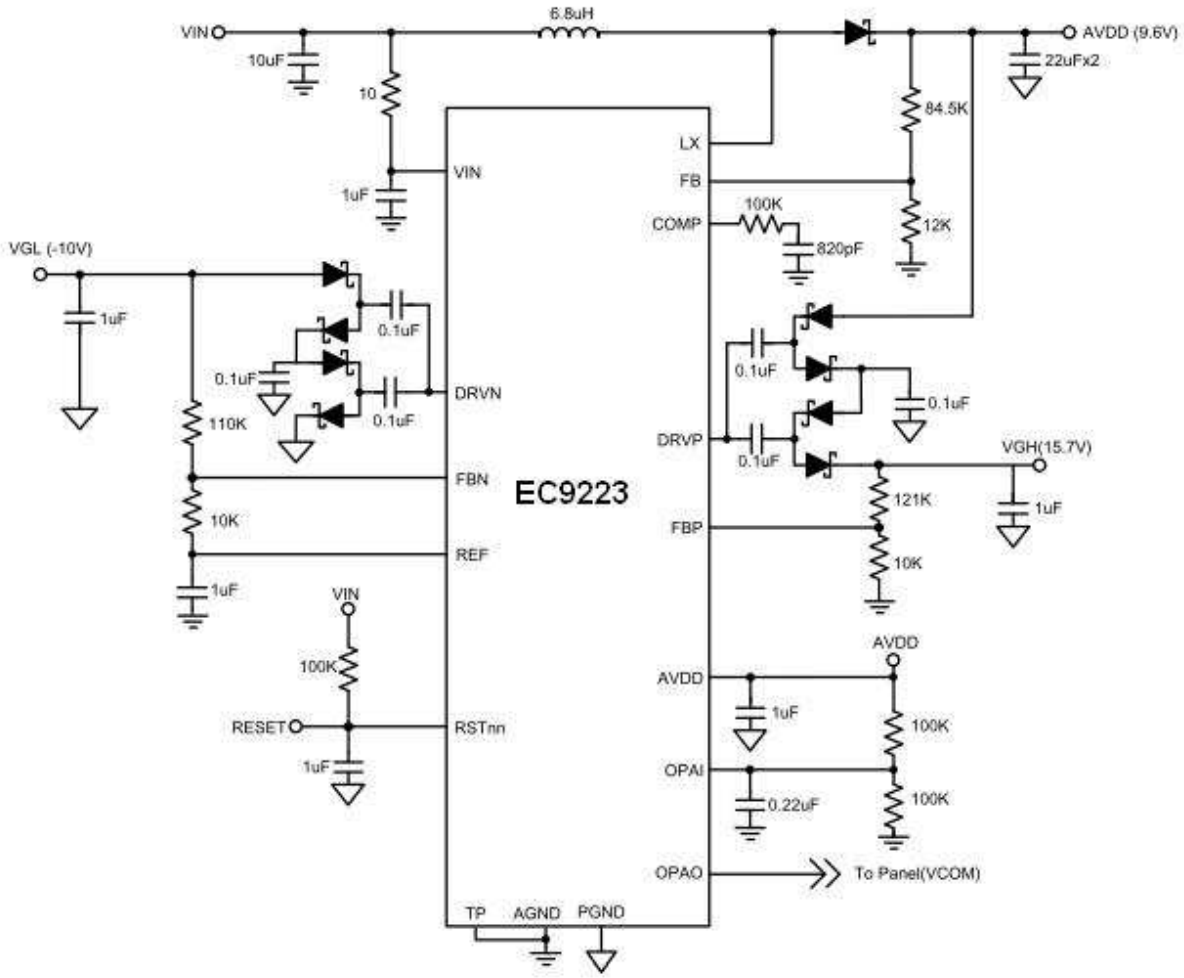
Q1:WQFN

Part Number	Package	Marking	Marking Information
EC9223NNQ1R	WQFN 16L	9223 LLLLL	1. LLLLL：Lot No

Function Block Diagram



Typical Application Diagram



Absolute Maximum Ratings

Input Supply Voltage, VIN	-0.3V to 6.5V
Voltages on EN, RSTnn	-0.3V to 6.5V
Voltages on AVDD, LX	-0.3V to 22V
Voltages on FB, FBP, FBN, COMP, REF	-0.3V to (VIN+0.3V)
Voltages on DRVP, DRVN, OPAI, OPAO	-0.3V to (AVDD+0.3V)
Storage temperature range	-65℃ to 150℃
Lead temperature (soldering, 10s maximum)	260℃
ESD, Human body mode	2kV
ESD, Machine mode	200V

Note1: All voltages are referenced to ground with PGND and AGND pins grounded.
Note2: “ABSOLUTE MAXIMUM RATINGS” indicate limits beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. For guaranteed specifications and test conditions, see the “ELECTRICAL SPECIFICATIONS”.

Recommended Operation Conditions

Junction temperature range	-40℃ to 125℃
Ambient temperature range	-40℃ to 85℃

Power Dissipation Ratings

Package	Thermal Resistance, Θ_{JA}	Power Rating (T_A < 25 ℃)	Power Rating (25 < T_A < 85 ℃)	Power Rating (T_A = 85℃)
16-ld QFN	103℃ /W	1.25W	(125 - T_A) / 103 W	0.39W

Electrical Specifications

(V_{IN}=3.3V, AV_{DD} = 8.5V, T_A=25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
System Supply						
Input Supply Voltage	V_{IN}		2.5	--	5.5	V
VIN Under Voltage Lockout	V_{UVLO}	V_{IN} rising	1.8	2.0	2.2	V
VIN Under Voltage Lockout	V_{UVLO}	Hysteresis	--	0.1	--	V
VIN Quiescent current	I_Q	V_{FB} = 1.35V, LX no switching	--	0.3	--	mA
VIN Quiescent current	I_Q	V_{FB} = 1.15V, LX switching	--	0.8	--	mA
EN Threshold	V_{IH}		2	--	--	V
EN Threshold	V_{IL}		--	--	0.8	
Thermal shutdown	T_{SHDN}		--	150	--	℃
Main Boost Regulator						
FB Regulation Voltage	V_{FB}		1.188	1.2	1.212	V
FB Fault Trip Level		Falling edge		0.95		V
FB Load Regulation		0< I_{LOAD} < full		-1		%
FB Line Regulation		V_{IN} = 2.5 to 5.5V		0.15	0.25	%/V
FB Input Bias Current		V_{FB} = 1.25V	-40	0	40	nA
FB Transconductance	G_m	ΔI=±5uA at COMP, FB = COMP		70		uA/V
FB Voltage Gain	A_V	FB to COMP		1500		V/V
LX Current Limit		V_{FB} =1.1V, duty cycle = 75%	1.4	1.8	2.2	A
LX On-Resistance	R_{ds_LX}	I_{LX} = 200mA		0.7		Ω
LX Leakage Current		V_{LX} = 19V, T_A = +25℃		0.1	10	uA
Current-Sense Transresistance				0.35		V/A
Maximum Duty Cycle	DUTY		85	90	94	%
Soft-Start Period	T_{SS1}			7		ms
Reference						
REF OUTPUT Voltage	V_{REF}	I_{REF}=50uA	1.176	1.20	1.224	V
REF Load Regulation	I_{REF}	0<I_{LOAD} <100uA		1	5	mV
REF Line Regulation		I_{REF} = 100uA V_{IN}=2.5V to 5.5V		2	5	mV
Oscillator and Timing						
Frequency	F_{OSC}		900	1200	1500	KHz
Duration to Trigger Fault Condition		FB or FBP or FBN below threshold		100		ms

Positive Charge-Pump Regulator						
AVDD Supply Range	V_{AVDD}		6		16	V
Operating Frequency	F_{OSC_CP}			600		KHz
FBP Regulation Voltage	V_{FBP}		1.176	1.2	1.224	V
FBP Input Bias Current	I_{FBP_BIAS}	V_{FBP} =1.5V, T_A = +25℃	-40	-	40	nA
DRVP P-Ch On-Resistance	R_{DRVPP}	V_{AVDD}=10V,I_{DRVP}=20mA		20		Ω
DRVP N-Ch On-Resistance	R_{DRVPN}			20		Ω
FBP Fault Trip Level		Falling edge		0.95		V
Soft-Start Period	T_{SS2}			5		ms
Negative Charge-Pump Regulator						
AVDD Supply Range	V_{AVDD}		6		16	V
Operating Frequency	F_{OSC_CP}			600		KHz
FBN Regulation Voltage	V_{FBN}		210	240	270	mV
FBN Input Bias Current	I_{FBN_BIAS}	V_{FBN} = 0V, T_A = +25℃	-40	-	40	nA
DRVN P-Ch On-Resistance	R_{DRVNP}	V_{AVDD}=10V,I_{DRVN}=20mA		20		Ω
DRVN N-Ch On-Resistance	R_{DRVNN}			20		Ω
FBN Fault Trip Level		Rising edge		0.45		V
Soft-Start Period	T_{SS3}			5		ms
Operational Amplifier						
AVDD Supply Range	V_{AVDD}		6		16	V
AVDD Supply Current	I_{AVDD}	V_{OPAI}= V_{AVDD}/2, no load		0.6	1.2	mA
Input Offset Voltage	V_{OS}	V_{OPAI} =V_{AVDD}/2, T_A = +25℃	-15	0	15	mV
Input Bias Current	I_{BIAS}	V_{OPAI} =V_{AVDD}/2, T_A = +25℃	-100		100	nA
Input Common-Mode Voltage Range			0		VAVDD	V
Output-Voltage-Swing High	VOH	OPAO I_{OUT} = 100μA	V_{AVDD} - 20	V_{AVDD} - 5		mV
		OPAO I_{OUT} = 5 mA	V_{AVDD} - 200	V_{AVDD} - 150		mV
Output-Voltage-Swing Low	VOL	OPAO I_{OUT} = -100μA		5	20	mV
		OPAO I_{OUT} = -5 mA		150	200	mV
Slew Rate	SR	V_{OPAO} 20% to 80% with CL=10pF, RL=10k	8	12		V/us
-3dB Bandwidth	BW	CL=10pF, RL=10k		12		MHz
Short-Circuit Current	ISCC	V_{OPAI}=V_{AVDD}/2 , short output to GND (sourcing)	100	150		mA
		V_{OPAI}=V_{AVDD}/2 , short output to AVDD (sinking)	100	150		mA

Low-Voltage Detector						
Reset Threshold	V_{RST_TH}	Falling edge at V_{IN}		2.6		V
	V_{RST_HYST}			100		mV
RSTnn Output Voltage	V_{RST}	I_{SINK} = 1mA			0.4	V
Reset Blanking Time	T_{BLK}			120		ms

Application Information

The EC9223 offers an all-in-one solution for TFT LCD. The chip includes a high-efficiency boost converter with a 20V/1.8A on-chip N-channel transistor for biasing of the LCD, a regulated positive charge pump, a regulated negative charge pump, and a unity-gain VCOM buffer. A voltage detector circuit generates a reset signal when the input voltage falls below 2.6V.

TFT LCD Boost Converter (AVDD)

The LCD panel AVDD supply is generated from a high-efficiency PWM boost converter operating with current mode control, and the switching frequency is 1.2MHz. During the on-period, TON, the synchronous FET connects one end of the inductor to ground, therefore increasing the inductor current. After the FET turns off, the inductor switching node, LX, is charged to a positive voltage by the inductor current. The freewheeling diode turns on and the inductor current flows to the output capacitor. The converter operates in the continuous conduction mode (CCM) when the average input current IIN is at least one-half of the inductor peak- to-peak ripple current, ΔI_{LPP}.

$$I_{IN} \geq \frac{\Delta I_{LPP}}{2}$$

$$\Delta I_{LPP} = \frac{(AVDD - V_{IN}) \times V_{IN}}{L \times F_{OSC} \times AVDD}$$

The output voltage, AVDD, is determined by the duty cycle, D, of the power FET on-time and the input voltage, V_{IN}.

$$AVDD = \frac{V_{IN}}{1 - D}$$

The average load current, I_{LOAD}, can be calculated from the power conservation law.

$$\eta \times V_{IN} \times I_{IN} = AVDD \times I_{LOAD}$$

where η is the power conversion efficiency. For a lower load current, the inductor current would decay to zero during the free-wheeling period and the output node would be disconnected from the inductor for the remaining portion of the switching period. The converter would operate in the discontinuous conduction mode (DCM). Current mode control is well known for its robustness and fast transient response. An inner current feedback loop sets the on-time and the duty cycle such that the current through the inductor equals to the current computed by the compensator. This loop acts within one switching cycle. A slope compensation ramp is added to suppress sub-harmonic oscillations. An outer voltage feedback loop subtracts the voltage on the FB pin from the internal reference voltage and feeds the difference to the compensator operational transconductance (Gm) amplifier. This amplifier is compensated by an external R-C network to allow the user to optimize the transient response and loop stability for the specific application conditions.

Compensation

This current mode boost converter has a current sense loop and a voltage feedback loop. The current sense loop does not need any compensation. The voltage feedback loop is compensated by an external series R-C network R_{COMP} and C_{COMP} from COMP pin to ground. R_{COMP} sets the high-frequency loop gain and the unity gain bandwidth of the loop which determines the transient response. C_{COMP} together with R_{COMP} determine the phase margin which relates to loop stability.

Output Capacitor Selection

The output voltage ripple due to converter switching is determined by the output capacitor total capacitance, C_{OUT}, and the output capacitor total effective series resistance, ESR.

$$AVDD_{RIPPLE} = \frac{D \times I_{LOAD}}{F_{OSC} \times C_{OUT}} + I_{PK} \times ESR$$

$$I_{PK} = I_{IN} + \frac{\Delta I_{LPP}}{2}$$

The first ripple component can be reduced by increasing C_{OUT}. Changing C_{OUT} may require adjustment of compensation R and C in order to provide adequate phase margin and loop bandwidth.
The second ripple component can be reduced by selecting low-ESR ceramic capacitors and using several smaller capacitors in parallel instead of just one large capacitor.

Inductor Selection

To prevent magnetic saturation of the inductor core the inductor has to be rated for a maximum current larger than I_{PK} in a given application. Since the chip provides current limit protection of 1.8A (typ) it is generally recommended that the inductor be rated at least for 1.8A. Selection of the inductor requires trade-off between the physical size (footprint x height) and its electrical properties (current rating, inductance, resistance). Within a given footprint and height, an inductor with larger inductance typically comes with lower current rating and often larger series resistance. Larger inductance typically requires more turns on the winding, a smaller core gap or a core material with a larger relative permeability. An inductor with a larger physical size has better electrical properties than a smaller inductor.

It is desirable to reduce the ripple current ΔILPP in order to reduce voltage noise on the input and output capacitors. In practice, the inductor is often much larger than the capacitors and it is easier and cheaper to increase the size of the capacitors. The ripple current ΔILPP is then chosen the largest possible while at the same time not degrading the maximum input and output current that the converter can operate with before reaching the current limit of the chip or the rated current of the inductor.

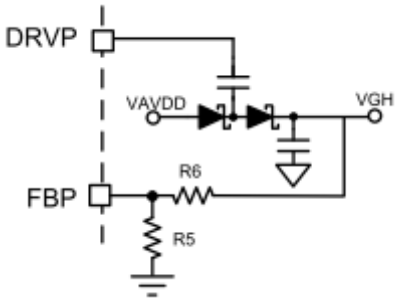
$$I_{PK} = I_{IN} + \frac{\Delta I_{LPP}}{2} \le I_{MAX}$$

For example, ΔI_{LPP} could be set to 20% of I_{MAX}.

Positive Charge Pump (VGH)

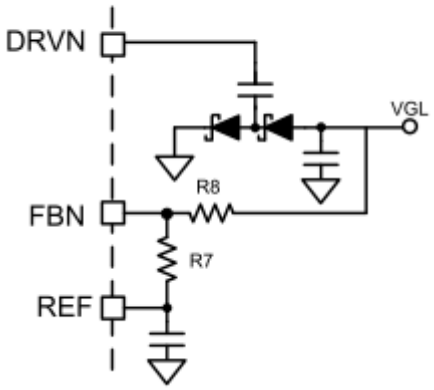
The positive charge pump is used to generate the TFT LCD gate on voltage. The output voltage, VGH, can be set by an external resistive divider. Voltage V_{FBP} is 1.2V. A single stage charge pump can produce an output voltage less than approximately twice the charge pump input voltage AVDD. The output voltage VGH is regulated as the following equation.

$$VGH = V_{FBP} \times \frac{R5 + R6}{R5}$$



The negative charge pump is used to generate the TFT LCD gate off voltage. The output voltage, VGL, is set with an external resistive divider from its output to REF with the midpoint connected to FBN. The error amplifier compares the feedback signal from FBN with an internal reference 240mV. The output voltage VGL is regulated as the following equation. V_{REF} is 1.2V.

$$VGL = V_{FBN} - \frac{R8}{R7}(V_{REF} - V_{FBN})$$



VCOM Buffer

The V_{COM} buffer generates the bias supply for the back plane of an LCD screen which is capacitively coupled to the pixel drive voltage. The purpose of the V_{COM} buffer is to hold the bias voltage steady while pixel voltage changes dynamically. The buffer is designed to sustain up to ±75mA of output current. In transients, it can deliver up to 150mA at which point the over current protection circuit limits the output current. Excessive current draw over a period of time may cause the chip temperature to rise and set off the over temperature protection circuit.

Under Voltage Protection

During normal operation (after completing the soft start sequence) EC9223 constantly monitors feedback pins FB, FBP and FBN. A fault condition occurs if FB falls below 0.95V or FBP falls below 0.95V or FBN rises above 0.45V. If any of the fault conditions persist for longer than 100ms, the chip sets a fault latch and shuts down. To turn the power supplies back on requires cycling of VIN supply below the UVLO level or toggling the EN pin low and high. This will clear the fault latch and restore normal operation.

Over Current Protection

The EC9223 has Over-Current Protection (OCP) that limits the peak inductor current in every switching cycle. It prevents large current from damaging the inductor and diode. Once the inductor current exceeds the current limit, the internal switch turns off immediately and shortens the duty cycle. The output voltage drops if the over-current condition occurs. Current limit is affected by the input voltage, duty cycle, and inductor value.

Thermal-Overload Protection

The EC9223 boost converter provides Thermal-overload Protection to prevents excessive power dissipation from overheating the IC. When the junction temperature exceeds T_J = 150℃, a thermal sensor activates the fault protection, which shuts down all outputs. To resume normal operation the chip internal temperature must drop at least by 15℃. In addition, either the inpu t supply must be cycled below the UVLO level or the EN pin must be toggled low and high to clear the fault latch.

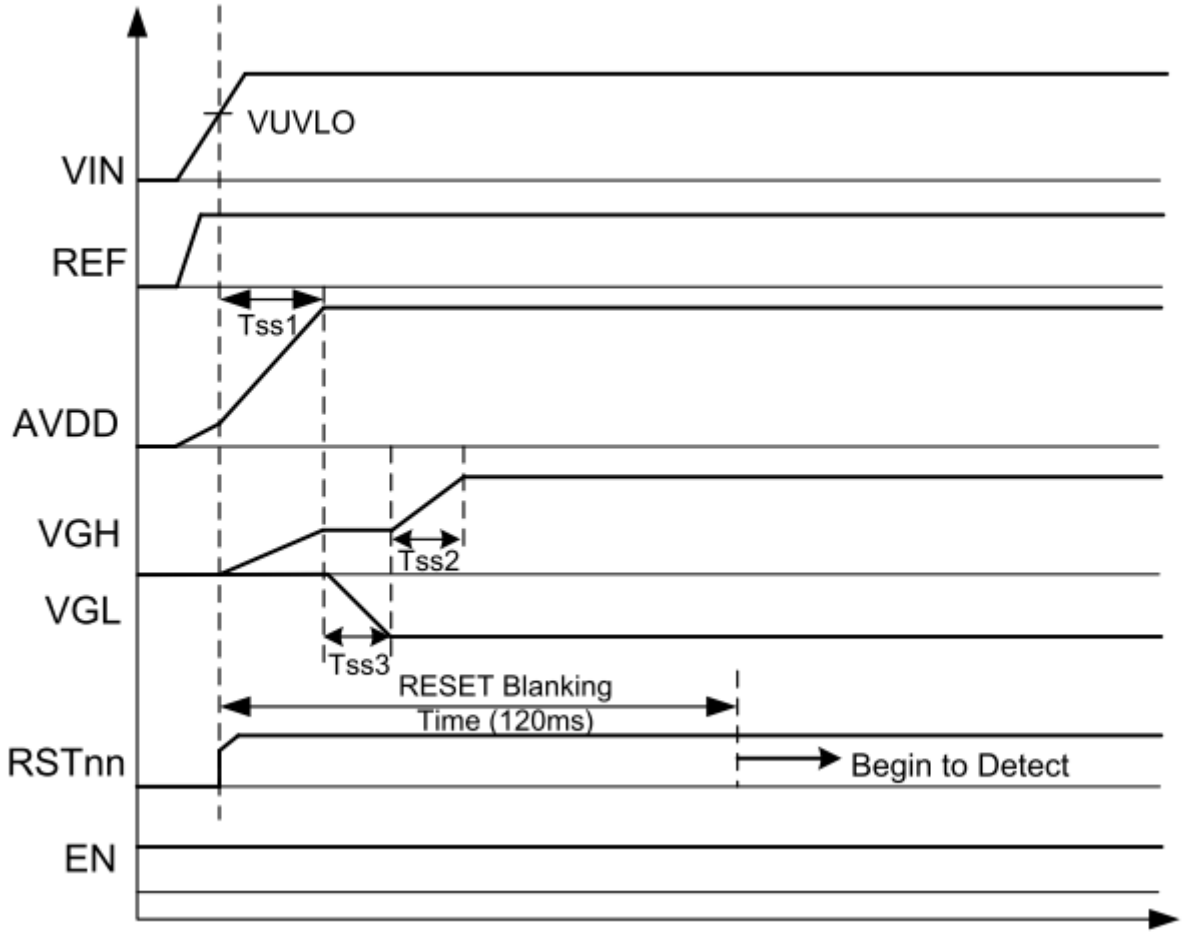
Voltage Detector Circuit

The internal voltage detector circuit monitors the chip input voltage V_{IN}. The chip can either drive RSTnn pin low or leave it floating. While floating, RSTnn is pulled high by an external pull up resistor. When VIN drops below 2.6V the chip pulls RSTnn pin low. In order to release RSTnn the V_{IN} voltage must rise above 2.7V. The voltage detector circuit is disabled and RSTnn is floating while the chip is disabled and for 123ms from the time the chip is enabled (V_{IN}>UVLO and EN is high).

Start-Up and Power-Off Control

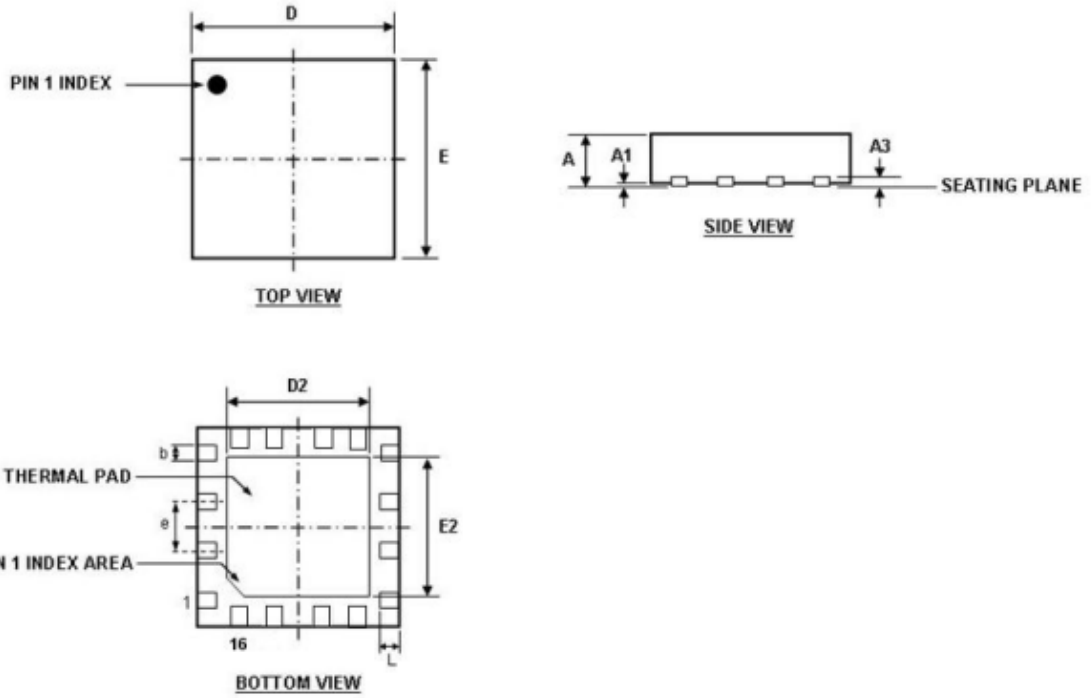
The EC9223 employs EN pin to control the whole chip. Pulling EN high enables this device. When EN goes high, once reference voltage is ready, the boost convertor starts operating. To limit the supply inrush current during start up conditions, an internal soft-start circuitry is implemented. The soft-start circuitry will slowly ramp up the output voltage during soft-start period, the soft-start period is 7ms for AVDD and 5ms for VGH and VGL. The EC9223 shuts down to reduce the supply current when EN is low. In this mode, all the internal blocks turn off, and the n-channel MOSFET is turned off as well. The boost convertor's output is connected to VIN by the external inductor and rectifier diode.

Startup Sequence



Package Information

(WQFN-16 3x3 mm)



DIMENSION	MIN (mm)	MAX (mm)
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.60	1.80
E	3.00 BSC	
E2	1.60	1.80
e	0.50 BSC	
L	0.30	0.45

Notes:
1) All dimensions are in millimeters.