CLP: PLL LVDS SERIES: ULTRA HF CLOCK OSCILLATOR, LVDS, +3.3 VDC

DESCRIPTION: A crystal controlled, high frequency, highly stable oscillator, adhering to Low Voltage Differential Signaling (LVDS) Standards. The output can be Tri-stated to facilitate testing or combined multiple clocks. The device is contained in a sub-miniature, very low profile, leadless ceramic SMD package with 6 gold contact pads. This miniature oscillator is ideal for today's automated assembly environments.

APPLICATIONS AND FEATURES:

- **Infiniband; Fiber Channel; SATA; 10GbE; Network Processors; SOHO Routing; Switches;**
- **Common Frequencies: 150 MHz; 156.25 MHz; 155.52 MHz; 161.1328 MHz; 212.5MHz; 312.5MHz**
- **+3.3 VDC LVDS**
- **Frequency Range from 750KHz to 800 MHz**
- **PLL multiplication (F>25MHz)**
- **Miniature Ceramic SMD Package Available on Tape and Reel**
- **Lead Free and ROHS Compliant**

■ ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNIT
Operating temperature range	Ta	-40…+85	°C
Storage temperature range	T(stg)	-55…+90	°C
Supply voltage	Vcc	+4.6	VDC
Maximum Input Voltage	Vi	Vss-0.5…Vcc+0.5	VDC
Maximum Output Voltage	Vo	Vss-0.5…Vcc+0.5	VDC

■ ELECTRICAL PARAMETERS:

PARAMETER	SYMBOL	TEST CONDITIONS[*1]		VALUE	UNIT
Nominal Frequency	fo			0.75~ 800.00**	MHz
Supply Voltage	Vcc			+3.3 ±5%	VDC
Supply Current	Is			80.0 MAX	mA
Output Logic Type				LVDS	
Load		Connected between Out and Complementary Out		100	Ω
Output Voltage Levels	Voh	Output logic high		1.43 Typ, 1.6 Max	VDC
	Vol	Output logic low		0.9 Min, 1.10 Typ	VDC
	Vod	Differential output		247 Min, 330 Typ, 454 Max	mV
		Differential output error		50 Max	mV
	VOS	Offset Voltage		1.125 Min, 1.25 Typ, 1.375 Max	VDC
	OS	Offset error		25 Max	mVDC
Duty Cycle	DC	Measured at 50% of Vcc		40/60 to 60/40 or 45/55 to 55/45	%
Rise / Fall Time	tr / tf	Measured at 20/80% and 80/20% Vcc Levels		0.7 TYP 1.0 MAX[*2]	ns
Jitter	J	Integrated Phase tji RMS, Fj = 12 kHz…20 MHz[5]	Fo=155.52MHz	2.6 TYP**	ps
			Fo=622.08MHz	2.5 TYP**	
		Random period Jitter Rj using wavecrest analyzer [4]	Fo=155.52MHz.	4 TYP **	ps
			Fo=622.08MHz	6 TYP **	
		Acumm. Peak to Peak Jitter Tp-p using wavecrest analyzer[*4]	Fo=155.52MHz.	30 TYP**	ps
			Fo=622.08MHz	40 TYP**	
Phase Noise	£(Δf)	typ. @155.52MHz[6]	Δf=10 Hz Δf=100 Hz Δf=1 KHz Δf=10 KHz Δf=100 KHz Δf=1M Hz Δf=10M Hz Δf≥20M Hz	-60 -90 -120 -125 -121 -121 -140 -145	dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Overall Frequency Stability	Δf/fc	Op. Temp., Aging, Load, Supply and Cal. Variations		±20, ±25, ±50, or ±100 MAX[*3]	ppm
Enable High Option; Pin 1 Output Enabled Output Disabled	 En Dis	 High Voltage or No Connect Ground		 0.7•Vcc MIN 0.3•Vcc MAX	 VDC VDC
Enable Low Option; Pin 1 Output Disabled Output Enabled	 Dis En	 High Voltage Ground or No Connect		 0.7•Vcc MIN 0.3•Vcc MAX	 VDC VDC

*1 Test Conditions Unless Stated Otherwise: Nominal Vcc, Nominal Load, +25 ±3°C
*2 Frequency Dependent
*3 Not All Stabilities Available With All Temperature Ranges—Please Consult Factory For Availability
*4 Measured with Wavecrest SIA-3000A 10,000, Cycles no filtering
*5 Calculated from Agilent 5500 phase noise measurements
*6 Measured with Agilent 5500

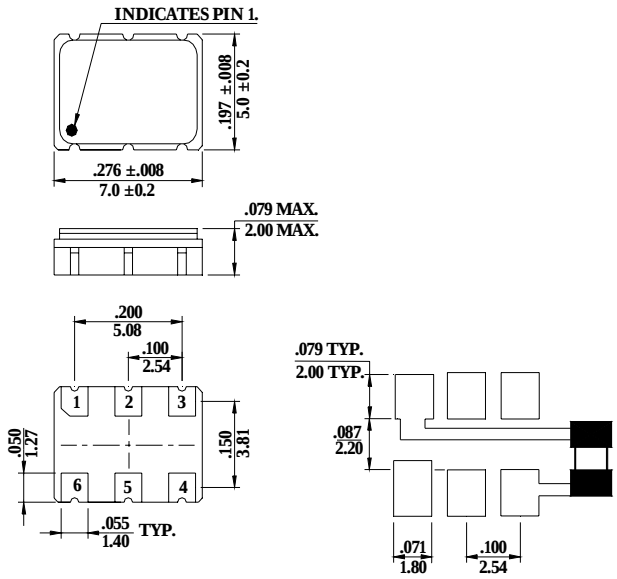
■ PART NUMBERING SYSTEM:

SERIES	SYMMETRY	TEMPERATURE RANGE (°C)	FREQUENCY STABILITY (Overall)	FREQUENCY (MHz)	Enable/Disable
CLP: UHF +3.3Vdc Clock with LVDS Comp. Output	A: 40/60 to 60/40% T: 45/55 to 55/45%	R: 0…+50 S: 0…+70 U: -20…+70 V: -40…+85**	K: ±20 ppm** I: ±25 ppm H: ±50 ppm J: ±100 ppm	0.75…800.000	Enable High – standard (Omit Suffix) EL; Enable Low

EXAMPLE: -155.520
Clock Oscillator, 7x5mm Package, +3.3 VDC Supply Voltage, LVDS Output, Standard Symmetry, 0…+70°C Operating Temperature Range, ±50 ppm Total Frequency Stability, 155.520 MHz

** ±20ppm stability may not be available at all combinations, please consult the factory for any custom requirements.

■ MECHANICAL PARAMETERS:



SOLDER PATTERN

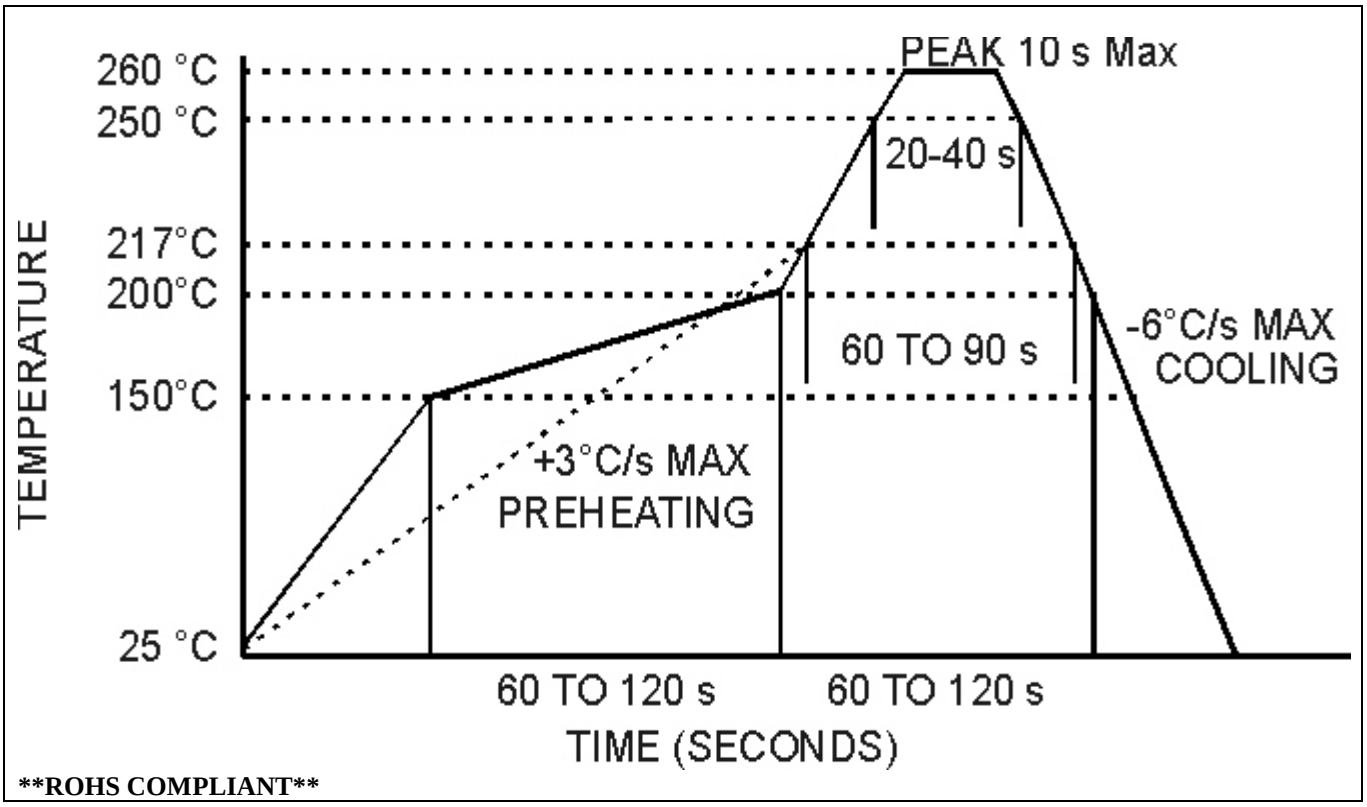
OUTLINE TOLERANCE:
±0.006" / 0.15mm
(Unless otherwise specified)

PIN FUNCTIONS:
[1] ENABLE/ DISABLE
[2] NO CONNECT
[3] CASE GROUND
[4] OUTPUT
[5] COMP. OUTPUT
[6] SUPPLY VOLTAGE

MARKING:
CLPASH
155.52
RAL D/C

***0.01µF external by-pass filter is recommended as seen on solder pattern.**

■ **REFLOW PROFILE:**



****ROHS COMPLIANT****