Document Number: AFT09S220-02N
Rev. 0, 9/2015

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 54 W RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 850 to 960 MHz.

900 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 54 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
920 MHz	19.5	35.8	7.0	–36.7	–13
940 MHz	19.3	35.4	7.0	–36.8	–12
960 MHz	19.0	35.3	7.0	–36.9	–12

880 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 54 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

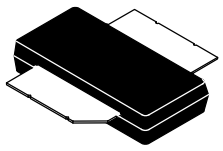
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
865 MHz	20.3	35.8	7.0	–36.2	–14
880 MHz	20.1	35.8	7.0	–36.5	–14
895 MHz	19.7	35.5	7.0	–36.0	–11

Features

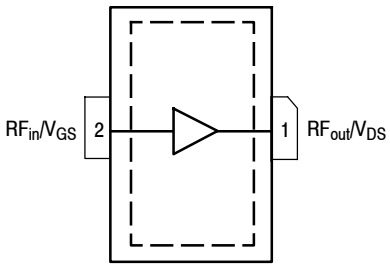
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications

AFT09S220-02NR3

850–960 MHz, 54 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



OM-780-2L PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +70	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 74°C, 54 W CW, 28 Vdc, I_{DQ} = 1400 mA, 940 MHz	$R_{\theta JC}$	0.30	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 70 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 135 μAdc)	$V_{GS(th)}$	0.8	1.3	1.8	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1400 mA)	$V_{GS(Q)}$	—	2.2	—	Vdc
Fixture Gate Quiescent Voltage (4) (V_{DD} = 28 Vdc, I_D = 1400 mA, Measured in Functional Test)	$V_{GG(Q)}$	4.0	4.4	4.8	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.35 Adc)	$V_{DS(on)}$	0.05	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf and search for AN1955.
4. $V_{GG} = 2 \times V_{GS(Q)}$. Parameter measured on Freescale test fixture, due to resistor divider network on the board. Refer to test circuit schematic.

(continued)

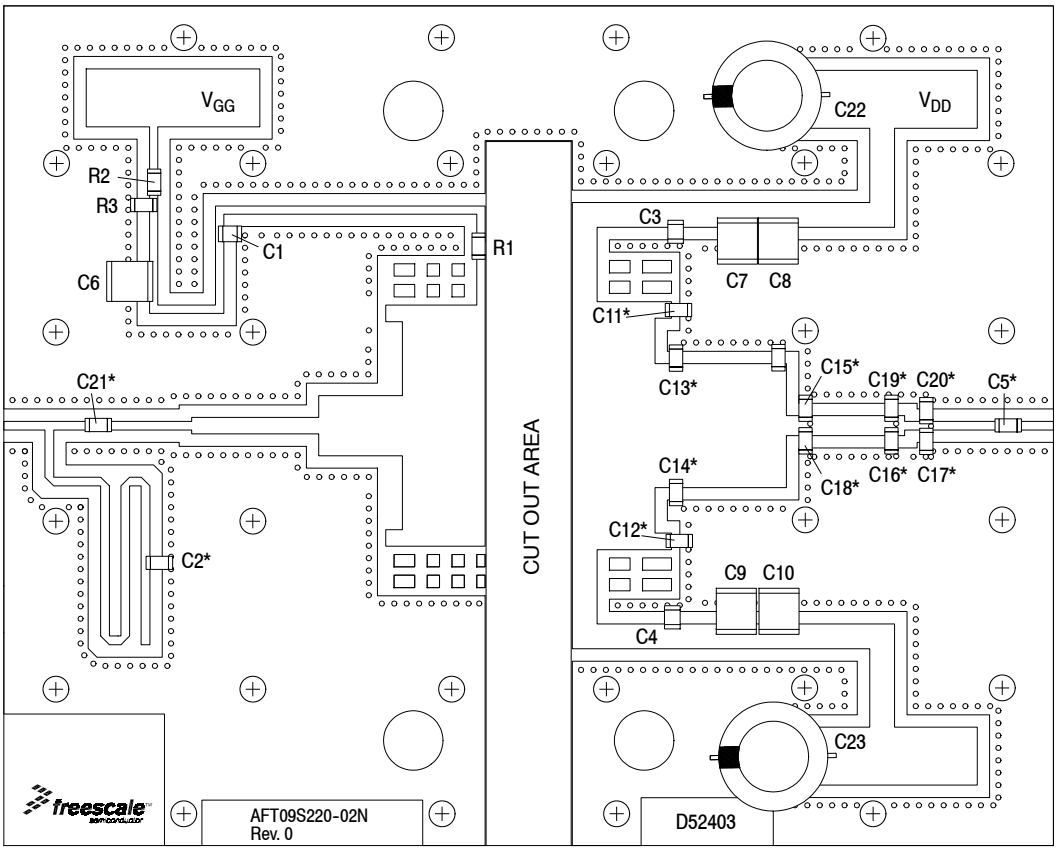
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 54 W Avg., f = 920 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	18.0	19.5	21.0	dB
Drain Efficiency	η_D	34.4	35.8	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.5	7.0	—	dB
Adjacent Channel Power Ratio	ACPR	—	–36.7	–34.2	dBc
Input Return Loss	IRL	—	–13	–9	dB
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 1400 mA, f = 940 MHz, 100 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 30 Vdc, 240 W Pulsed CW Output Power (3 dB Input Overdrive from 220 W Pulsed CW Rated Power)		No Device Degradation			
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, 920–960 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	220	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 920–960 MHz frequency range)	Φ	—	–10.6	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	70	—	MHz
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 54 W Avg.	G_F	—	0.5	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.013	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.002	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
AFT09S220-02NR3	R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel	OM-780-2L

1. Part internally matched both on input and output.



*C2, C5, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20 and C21 are mounted vertically.

Figure 2. AFT09S220-02NR3 Test Circuit Component Layout

Table 7. AFT09S220-02NR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C6, C7, C8, C9, C10	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C11, C12	6.2 pF Chip Capacitors	ATC100B6R2BT500XT	ATC
C13, C14, C15, C16	1.7 pF Chip Capacitors	ATC100B1R7BT500XT	ATC
C17	2.2 pF Chip Capacitor	ATC100B2R2JT500XT	ATC
C18	2.0 pF Chip Capacitor	ATC100B2R0BT500XT	ATC
C19	1.1 pF Chip Capacitor	ATC100B1R1BT500XT	ATC
C20	0.2 pF Chip Capacitor	ATC100B0R2BT500XT	ATC
C21	6.8 pF Chip Capacitor	ATC100B6R8CT500XT	ATC
C22, C23	470 μF, 63 V Electrolytic Capacitors	477CKS050M	Illinois Capacitor
R1	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay
R2, R3	10 kΩ, 1/4 W Chip Resistors	CRCW120610K0FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D52403	MTL

TYPICAL CHARACTERISTICS

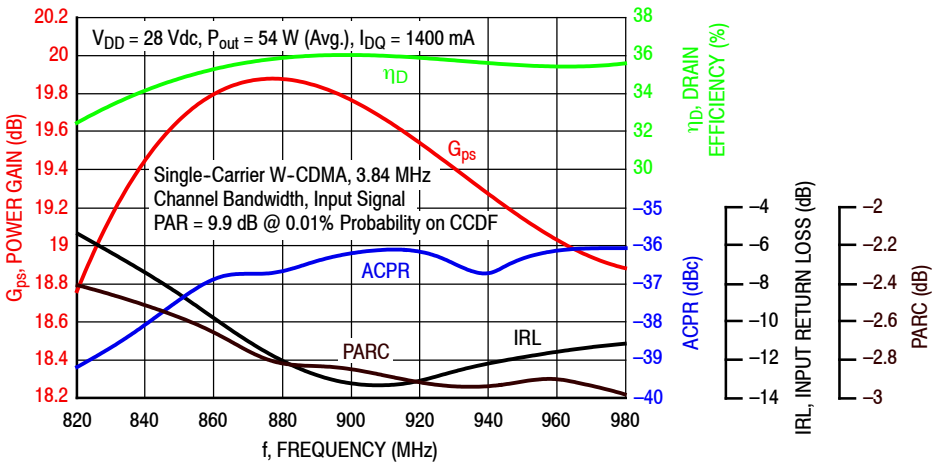


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 54 Watts Avg.

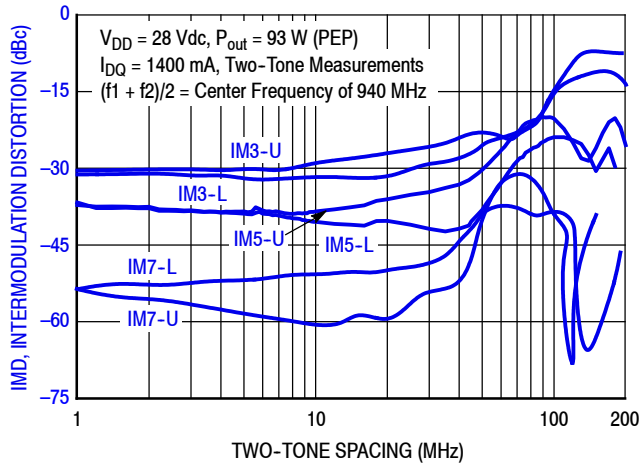


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

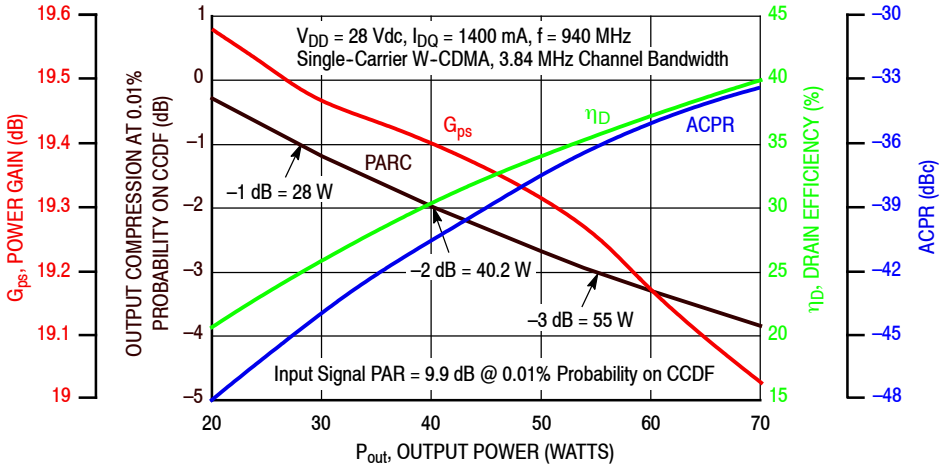


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

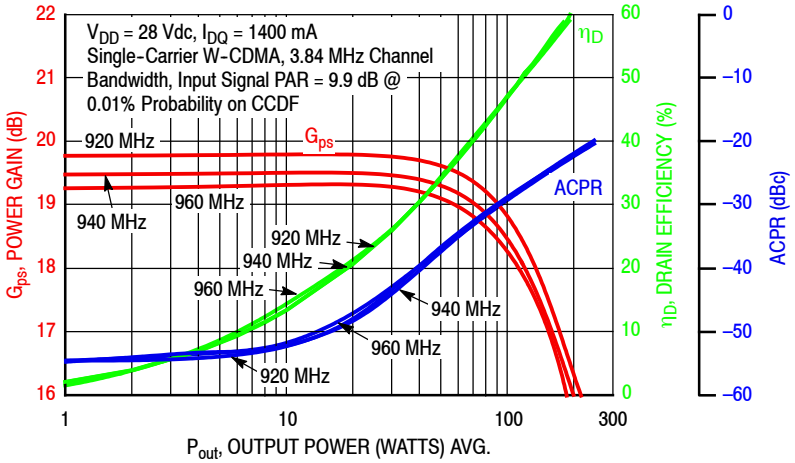


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

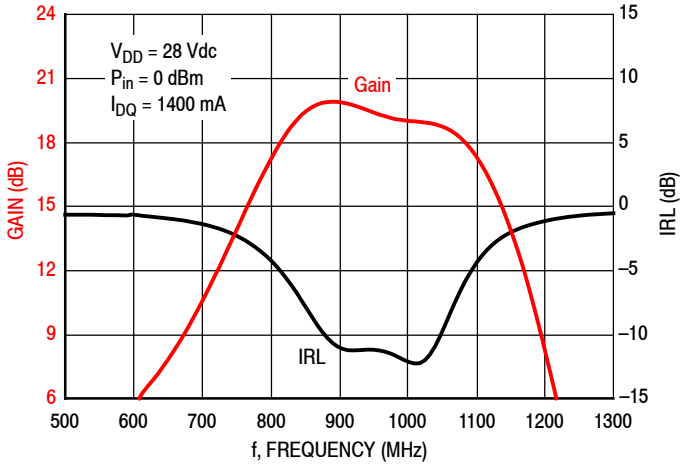


Figure 7. Broadband Frequency Response

Table 8. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.43 – j5.36	2.30 + j5.40	3.95 – j2.04	17.4	54.9	306	55.7	–4.5
940	2.73 – j5.85	2.65 + j5.83	4.58 – j1.60	17.2	54.8	303	55.2	–4.2
960	3.29 – j6.47	3.10 + j6.30	5.04 – j1.02	17.0	54.9	311	56.5	–4.7

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.43 – j5.36	2.38 + j5.49	4.63 – j1.21	15.1	55.9	387	59.5	–7.3
940	2.73 – j5.85	2.74 + j5.91	4.95 – j0.67	15.0	55.8	384	59.2	–7.0
960	3.29 – j6.47	3.23 + j6.37	5.12 + j0.16	14.7	55.9	392	60.3	–7.4

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

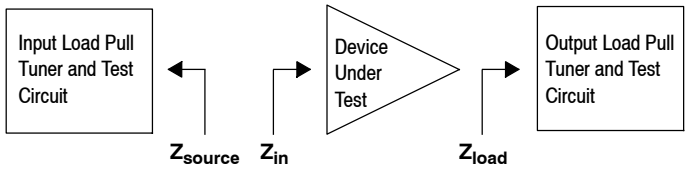
Table 9. Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.43 – j5.36	2.29 + j5.33	1.15 – j1.10	20.7	52.1	164	70.0	–13
940	2.73 – j5.85	2.67 + j5.75	1.18 – j1.16	20.7	51.8	151	69.5	–13
960	3.29 – j6.47	3.17 + j6.24	1.45 – j1.23	20.2	52.3	169	71.1	–12

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.43 – j5.36	2.36 + j5.44	1.50 – j1.06	18.2	53.7	232	73.1	–16
940	2.73 – j5.85	2.75 + j5.86	1.55 – j1.09	18.2	53.4	221	73.0	–16
960	3.29 – j6.47	3.30 + j6.34	1.40 – j1.20	18.3	52.9	193	74.5	–19

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL LOAD PULL CONTOURS — 940 MHz

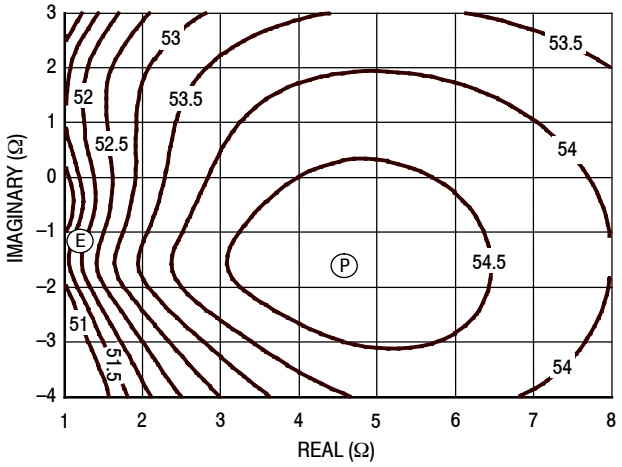


Figure 8. P1dB Load Pull Output Power Contours (dBm)

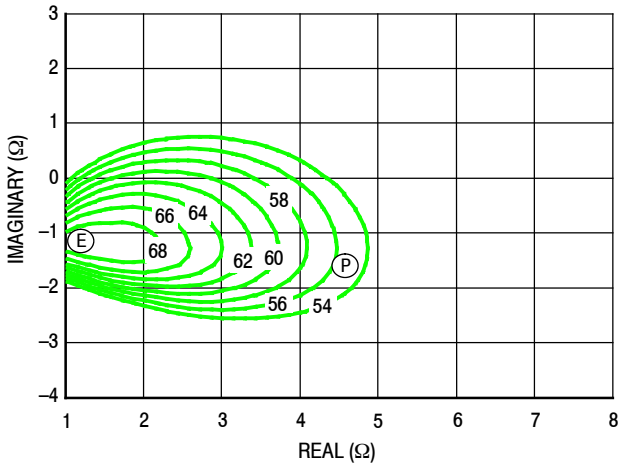


Figure 9. P1dB Load Pull Efficiency Contours (%)

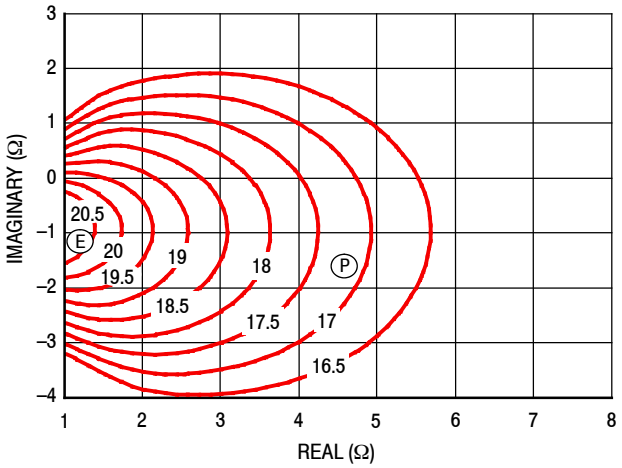


Figure 10. P1dB Load Pull Gain Contours (dB)

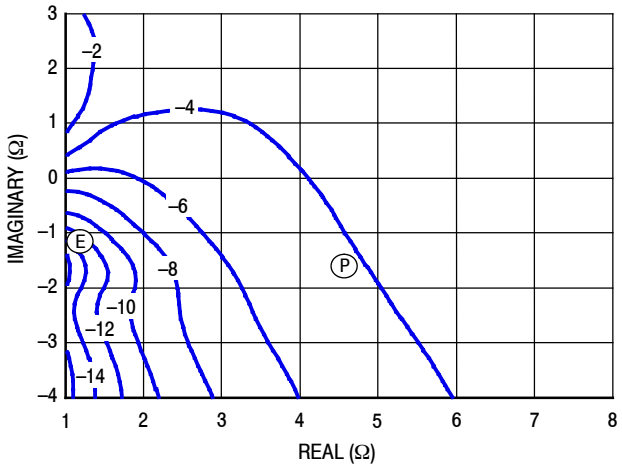


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 940 MHz

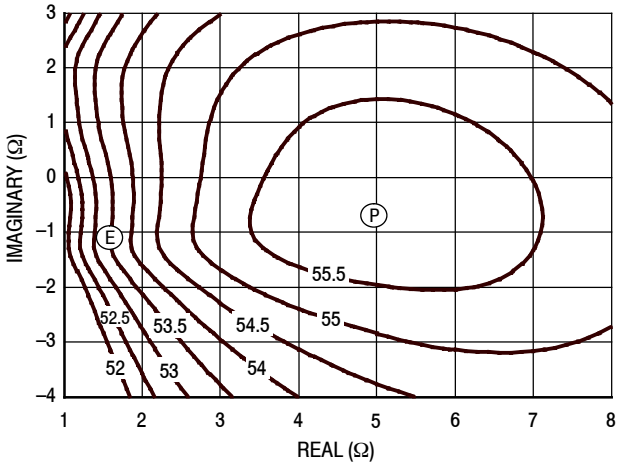


Figure 12. P3dB Load Pull Output Power Contours (dBm)

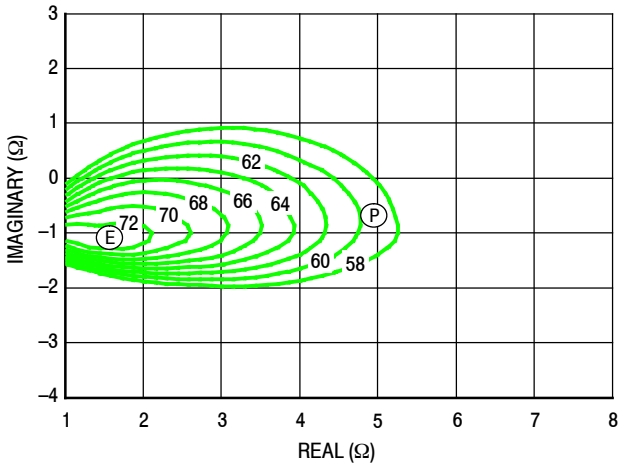


Figure 13. P3dB Load Pull Efficiency Contours (%)

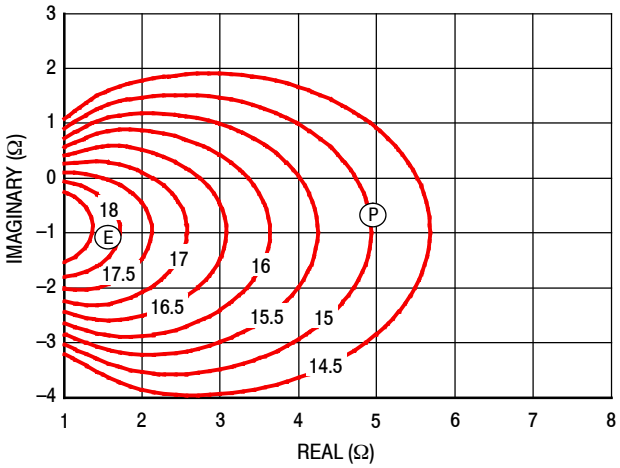


Figure 14. P3dB Load Pull Gain Contours (dB)

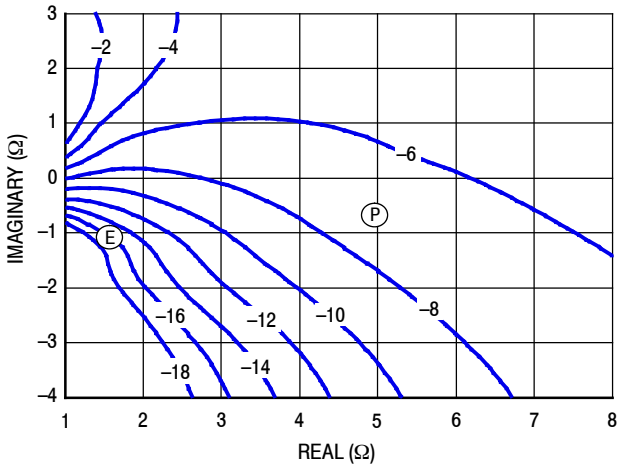


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

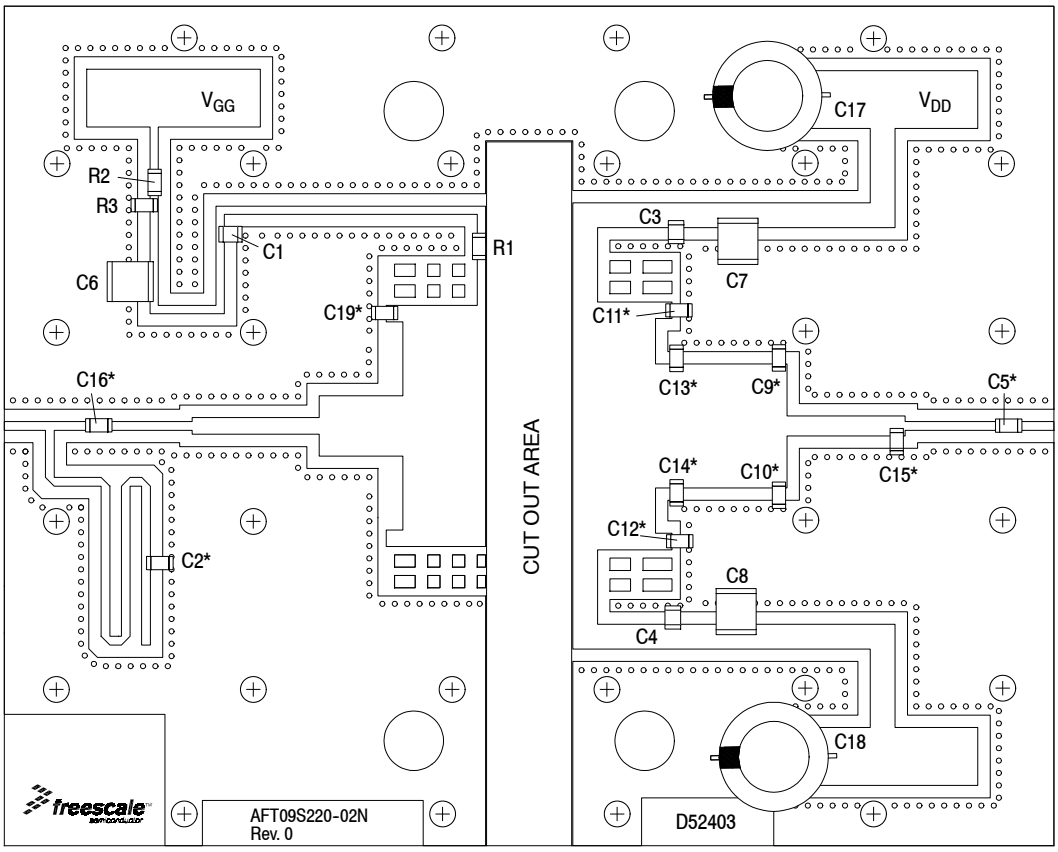
Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power



*C2, C5, C9, C10, C11, C12, C13, C14, C15, C16 and C19 are mounted vertically.

Figure 16. AFT09S220-02NR3 Test Circuit Component Layout — 865–895 MHz

Table 10. AFT09S220-02NR3 Test Circuit Component Designations and Values — 865–895 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5	56 pF Chip Capacitors	ATC100B560CT500XT	ATC
C6, C7, C8	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C9	1.1 pF Chip Capacitor	ATC100B1R1BT500XT	ATC
C10	1.5 pF Chip Capacitor	ATC100B1R5BT500XT	ATC
C11, C12	3.9 pF Chip Capacitors	ATC100B3R9CT500XT	ATC
C13, C14	5.1 pF Chip Capacitors	ATC100B5R1CT500XT	ATC
C15	5.6 pF Chip Capacitor	ATC100B5R6CT500XT	ATC
C16	10 pF Chip Capacitor	ATC100B100JT500XT	ATC
C17, C18	470 μF, 63 V Electrolytic Capacitors	477CKS050M	Illinois Capacitor
C19	3.6 pF Chip Capacitor	ATC100B3R6CT500XT	ATC
R1	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay
R2, R3	10 kΩ, 1/4 W Chip Resistors	CRCW120610K0FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D52403	MTL

TYPICAL CHARACTERISTICS — 865–895 MHz

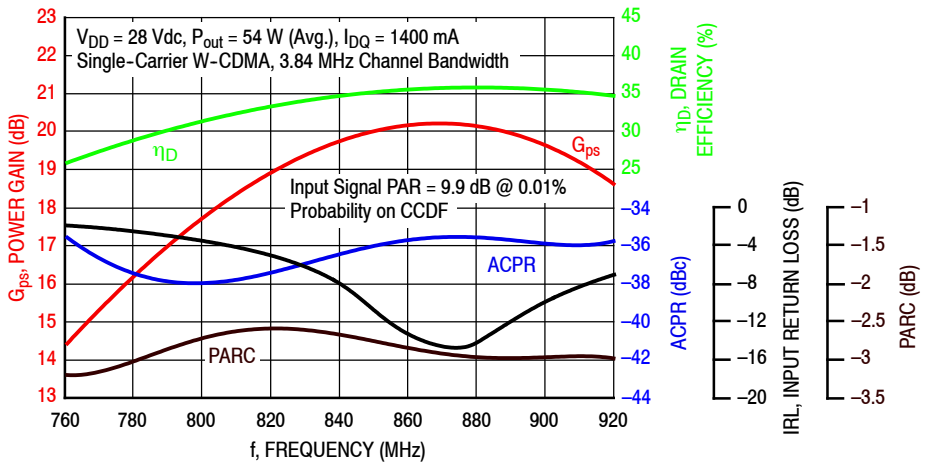


Figure 17. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 54 Watts Avg.

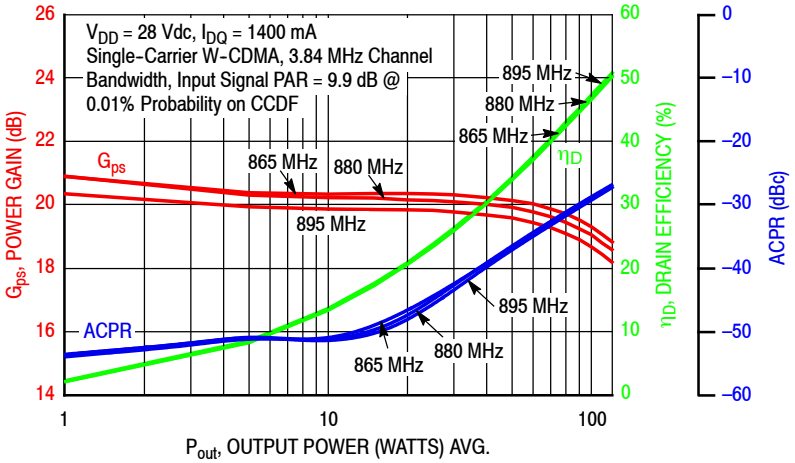


Figure 18. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

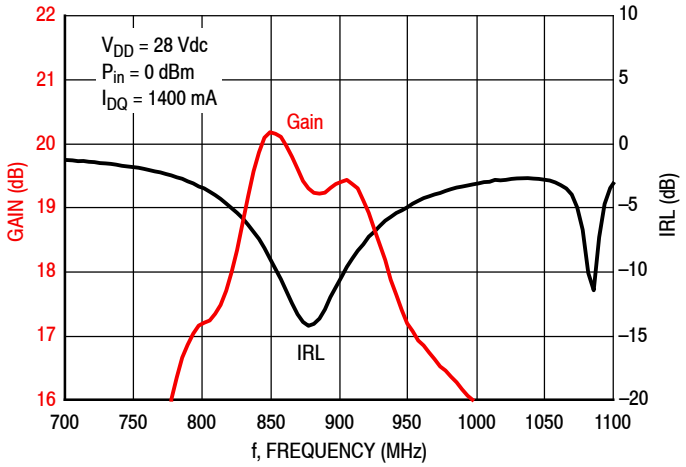


Figure 19. Broadband Frequency Response

Table 11. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
865	1.59 – j4.58	1.62 + j4.38	2.93 – j2.36	17.6	54.7	293	52.6	–4.2
880	1.76 – j4.85	1.77 + j4.63	3.10 – j2.26	17.6	54.8	303	55.2	–4.8
895	1.91 – j5.04	1.95 + j4.91	3.45 – j2.18	17.6	54.9	310	56.3	–4.3

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
865	1.59 – j4.58	1.65 + j4.47	3.54 – j2.02	15.5	55.7	374	57.7	–7.5
880	1.76 – j4.85	1.82 + j4.73	3.77 – j1.91	15.4	55.8	384	59.2	–8.0
895	1.91 – j5.04	2.01 + j5.00	4.09 – j1.75	15.3	56.0	394	60.8	–7.4

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

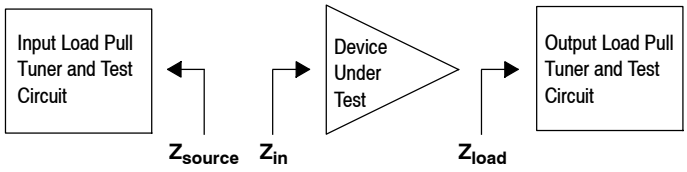
Table 12. Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
865	1.59 – j4.58	1.56 + j4.30	1.20 – j0.95	20.7	52.8	189	68.2	–10
880	1.76 – j4.85	1.73 + j4.56	1.17 – j1.06	20.6	52.7	188	69.7	–11
895	1.91 – j5.04	1.91 + j4.82	1.04 – j1.03	21.0	52.2	167	71.3	–13

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
865	1.59 – j4.58	1.59 + j4.40	1.21 – j0.82	18.8	53.4	220	71.7	–16
880	1.76 – j4.85	1.77 + j4.66	1.30 – j0.91	18.6	53.6	231	73.1	–16
895	1.91 – j5.04	1.97 + j4.94	1.35 – j0.96	18.5	53.7	235	74.8	–16

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL LOAD PULL CONTOURS — 880 MHz

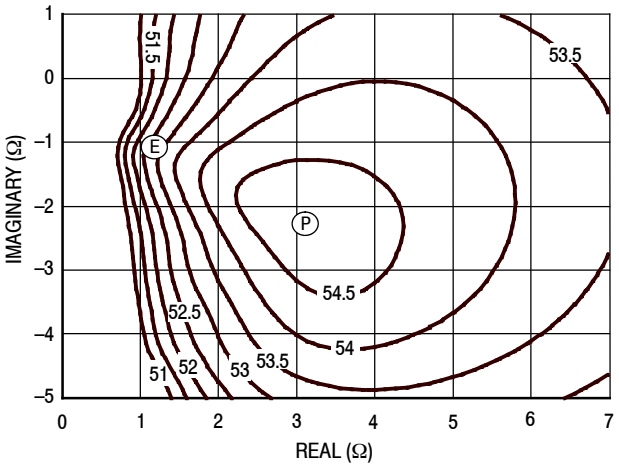


Figure 20. P1dB Load Pull Output Power Contours (dBm)

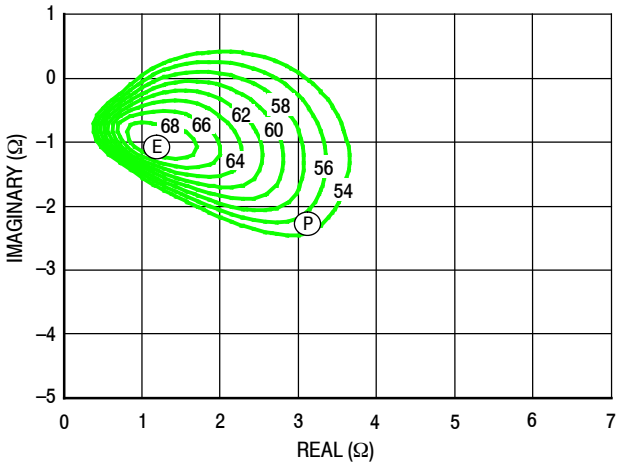


Figure 21. P1dB Load Pull Efficiency Contours (%)

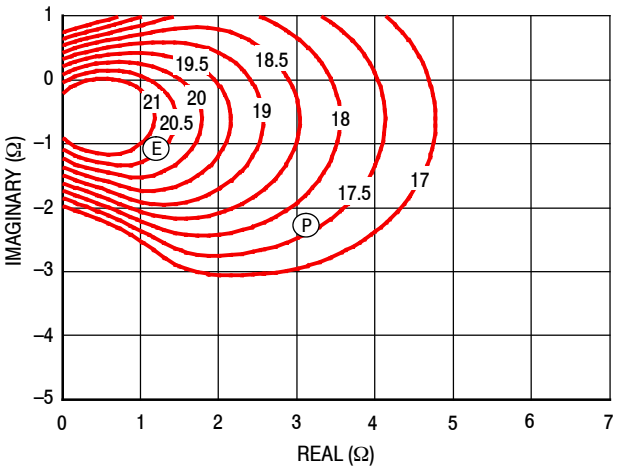


Figure 22. P1dB Load Pull Gain Contours (dB)

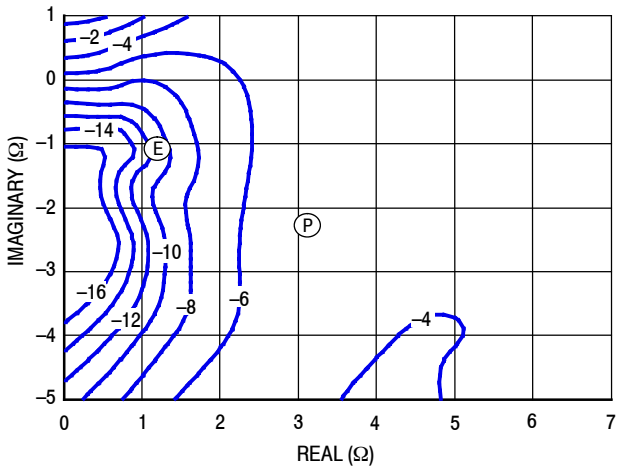


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 880 MHz

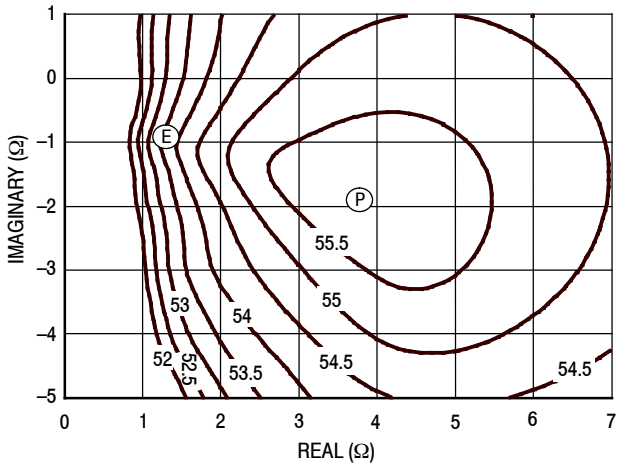


Figure 24. P3dB Load Pull Output Power Contours (dBm)

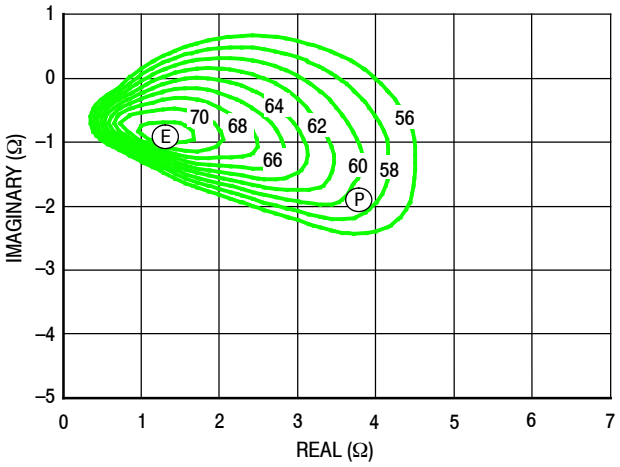


Figure 25. P3dB Load Pull Efficiency Contours (%)

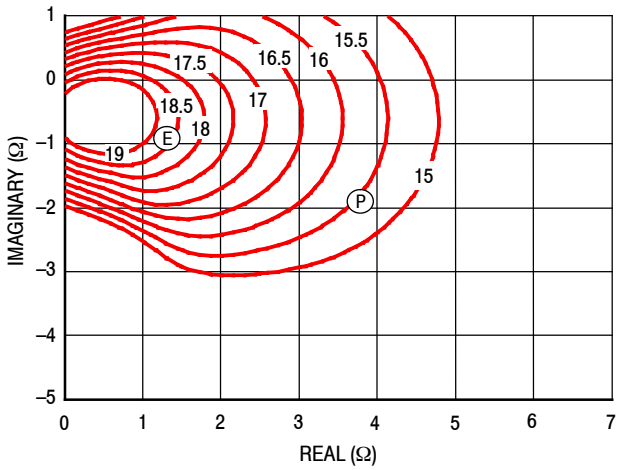


Figure 26. P3dB Load Pull Gain Contours (dB)

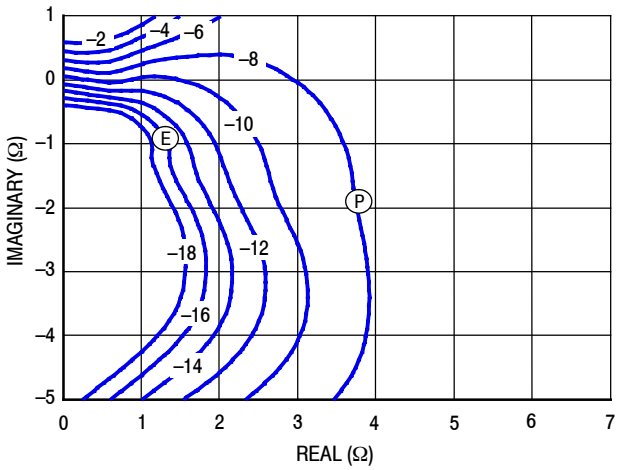
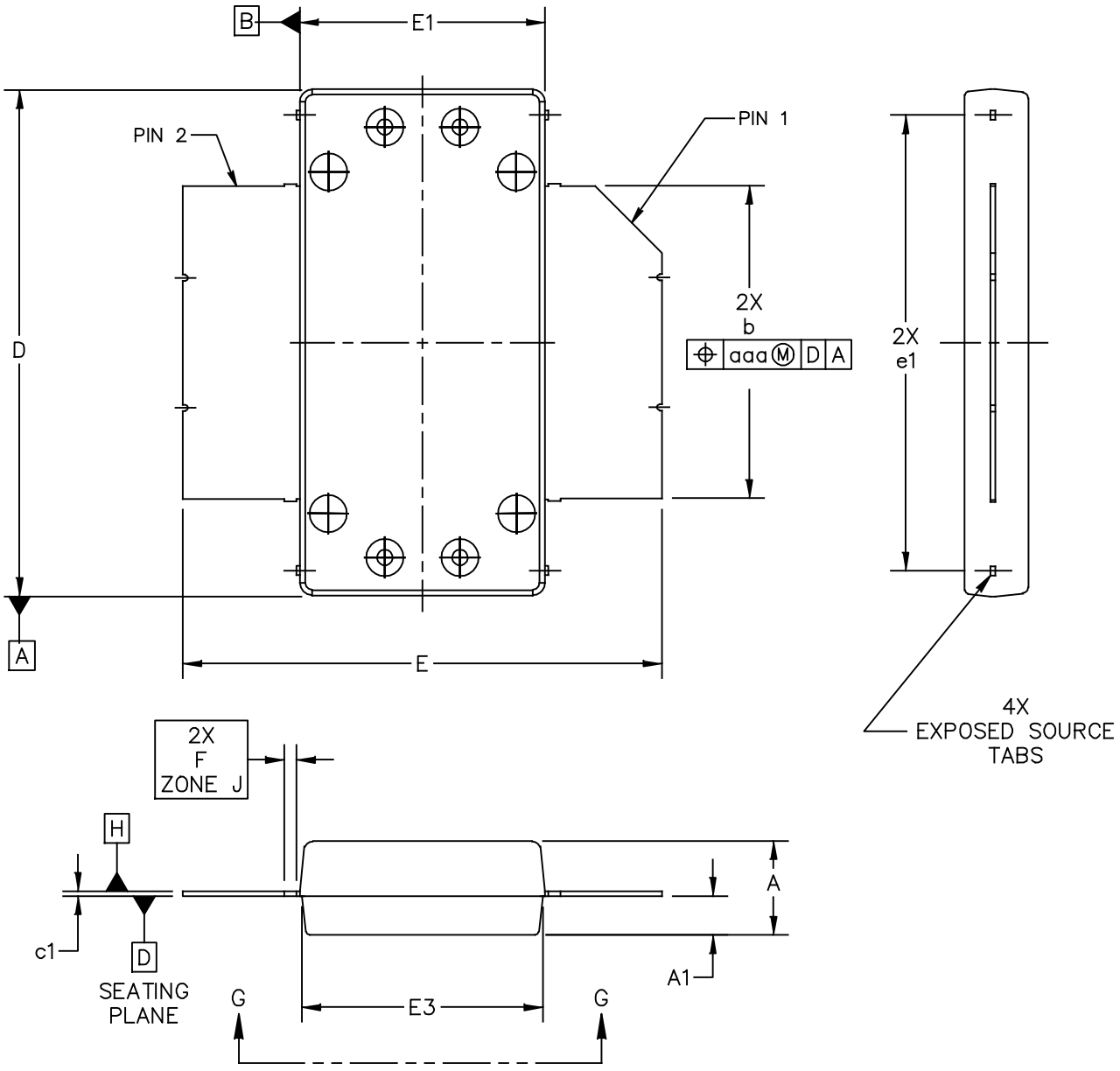


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

PACKAGE DIMENSIONS



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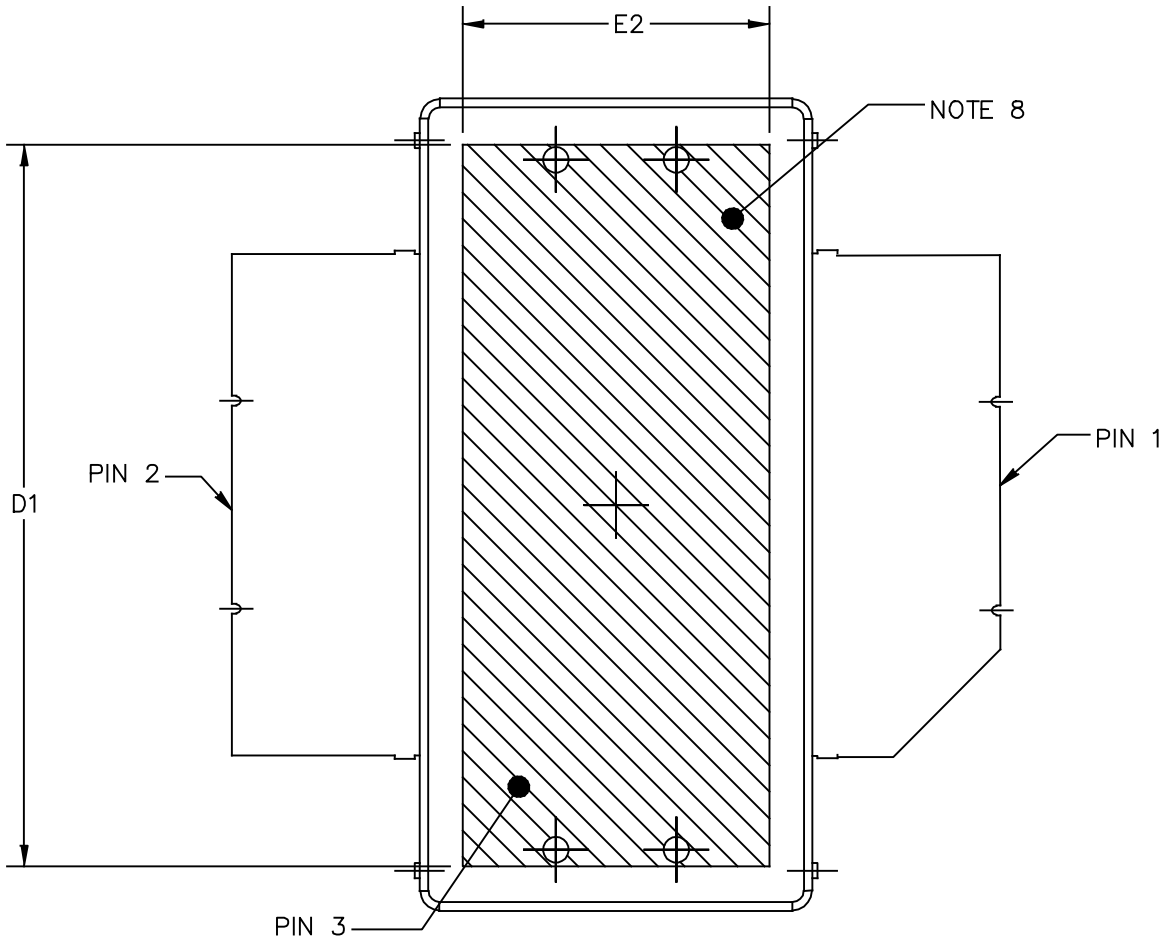
	CASE NUMBER: 2021–03	22 OCT 2009
	STANDARD: NON–JEDEC	



BOTTOM VIEW
VIEW G–G

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	CASE NUMBER: 2021–03	22 OCT 2009
	STANDARD: NON–JEDEC	

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

STYLE 1:
PIN 1 – DRAIN
PIN 2 – GATE
PIN 3 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	0.148	.152	3.76	3.86	b	.497	.503	12.62	12.78
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e1	.721	.729	18.31	18.52
D1	.720	----	18.29	----					
E	.762	.770	19.36	19.56	aaa	.004		0.10	
E1	.390	.394	9.91	10.01					
E2	.306	----	7.77	----					
E3	.383	.387	9.73	9.83					
F	.025 BSC		0.635 BSC						

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TITLE:	DOCUMENT NO: 98ASA10831D	REV: B
OM780–2 STRAIGHT LEAD	CASE NUMBER: 2021–03	22 OCT 2009
	STANDARD: NON–JEDEC	

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.freescale.com/rf
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2015	• Initial Release of Data Sheet

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