EPSON

S1C88650

8-bit Single Chip Microcomputer

Low Voltage Operation Products

- Original Architecture Core CPU
- Large-capacity Font ROM for Kanji, Simplified Chinese and Hangul (896K bytes)
- Dot-matrix LCD Driver (126 × 32)

■ DESCRIPTION

The S1C88650 is an 8-bit microcomputer for portable equipment with an LCD display that has a built-in LCD controller/driver and a character generator (kanji) ROM. This microcomputer features low-voltage (1.8V) and high-speed (8.2MHz) operations as well as low-current consumption (2.5µA during standby). The LCD controller/driver contains an LCD drive power supply circuit and can drive an maximum of 126 × 32-dot LCD panel in low-power consumption. An 896K-byte large-capacity font ROM is embedded in the S1C88650. This allows applications to contain fonts for Simplified Chinese characters, Hangul characters and user-defined characters as well as 11 × 12-dot JIS level-1, JIS level-2 and other kanji fonts without an external expanded font ROM. This 8-bit CPU has up to 16MB accessible address space allowing easy implementation of a large data processing application. The S1C88650 is suitable for display modules, portable CD/MD, solid audio players, PDA, data bank and other applications that required an exclusive LCD driver in conventional systems.

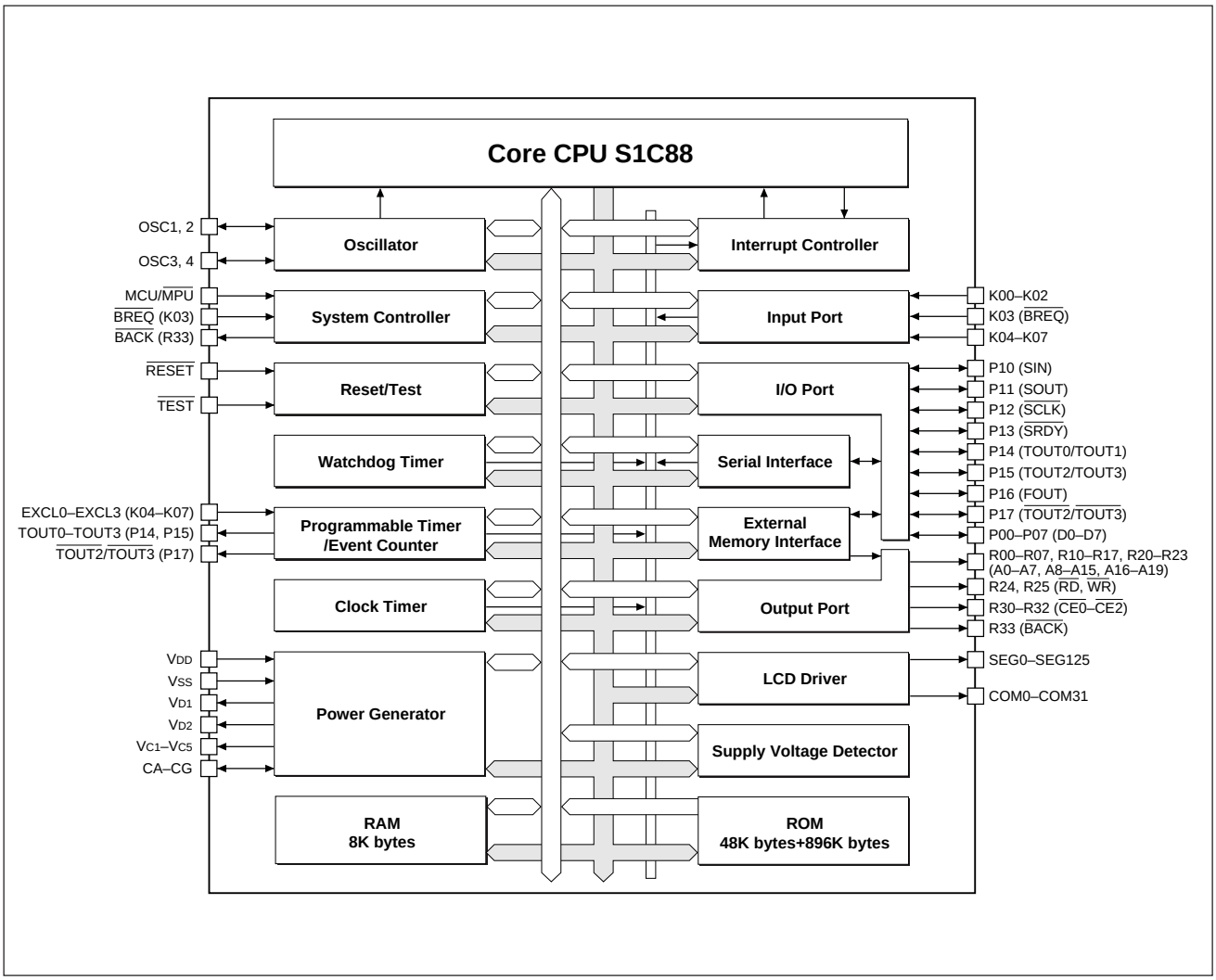
■ FEATURES

- Core CPU ..... S1C88 (MODEL3) CMOS 8-bit core CPU
- Main (OSC3) oscillation circuit ..... Crystal oscillation circuit/ceramic oscillation circuit 8.2MHz (Max.) or CR oscillation circuit 2.2MHz (Max.) (∗1)
- Sub (OSC1) oscillation circuit ..... Crystal oscillation circuit 32.768kHz (Typ.) or CR oscillation circuit 200kHz (Max.) (∗1)
- Instruction set ..... 608 types (usable for multiplication and division instructions)
- Min. instruction execution time 0.244µsec/8.2MHz (2-clock)
- Internal ROM capacity ..... Program ROM: 48K bytes
  Font ROM: 896K bytes (can be used for a program/data ROM)
- Internal RAM capacity ..... RAM: 8K bytes
  Display memory: 768 bytes
- Bus line ..... Address bus: 20 bits (also usable as a general output port when not used as a bus)
  Data bus: 8 bits (also usable as a general I/O port when not used as a bus)
  $\overline{CE}$ signal: 3 bits
  $\overline{WR}$ signal: 1 bit
  $\overline{RD}$ signal: 1 bit
  (also usable as a general output port when not used as a bus)
- Input port ..... 8 bits (4 bits can be used as the source clock inputs for PWM timers and 1 bit as a bus request signal input)
- Output port ..... 0–3 bits (when the external bus is used)
  26 bits (when the external bus is not used)
  (1 bit can be configured for the bus acknowledge signal output)
- I/O port ..... 8 bits (when the external bus is used)
  16 bits (when the external bus is not used)
  (shard with serial interface, FOUT and TOUT terminals)
- Serial interface ..... 1 ch. (optional clock synchronous system or asynchronous system)
- Timer ..... Programmable timer: 16 bits (8 bits × 2) 4 ch. (with PWM function)
  Clock timer: 1 ch.

- LCD driver ..... Dot matrix type (16 × 16/5 × 8 or 12 × 12 dot fonts)
  126 segments × 32, 16 or 8 commons (∗2) (1/5 bias)
  Built-in LCD power supply circuit (booster type, 5 potentials)
- Watchdog timer ..... Built-in (0.5–4 second cycles)
- Supply voltage detection (SVD) circuit .... 13 value programmable (1.8V to 2.7V)
- Interrupt ..... External interrupt: Input port interrupt 1 system (8 types)
  Internal interrupt: Timer interrupt 2 systems (16 types)
  Serial interface interrupt 1 system (3 types)
- Supply voltage ..... 1.8V to 3.6V
- Current consumption (Typ.) ..... SLEEP mode: 1µA
  HALT mode (32kHz crystal oscillation, LCD OFF): 2.5µA
  HALT mode (32kHz CR oscillation, LCD OFF): 10µA
  Run (32kHz crystal oscillation, LCD OFF): 9µA
  Run (32kHz CR oscillation, LCD OFF): 15µA
  Run (8.2MHz ceramic oscillation, LCD OFF): 1700µA
  Run (2.2MHz CR oscillation, LCD OFF): 600µA
- Supply form ..... QFP8-256pin or chip

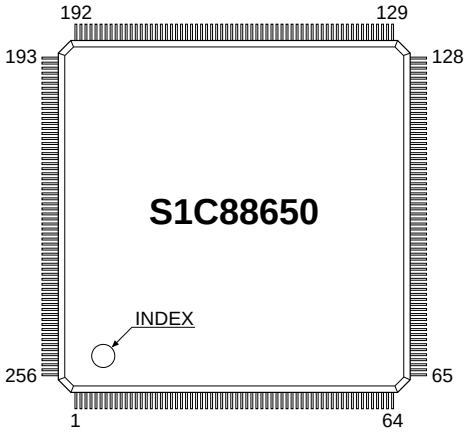
∗1: Can be selected with mask option ∗2: Can be selected with software

■ BLOCK DIAGRAM



■ PIN LAYOUT DIAGRAM

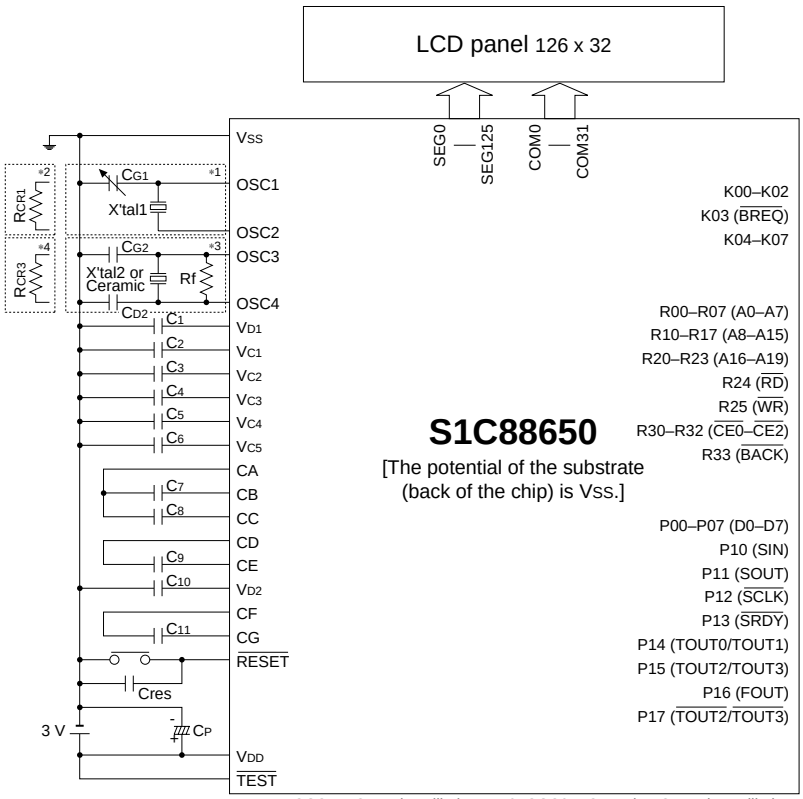
QFP8-256pin



■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	131, 189	–	Power supply (+) terminal
V_{SS}	67, 134, 195, 253	–	Power supply (GND) terminal
V_{D1}	135	–	Internal logic system and oscillation system voltage regulator output terminals
V_{D2}	113	–	LCD circuit power voltage booster output terminal
V_{C1}–V_{C5}	125–121	–	LCD drive voltage output terminals
CA–CG	120–114	–	LCD and power voltage booster capacitor connection terminals
OSC1	136	I	OSC1 oscillation input terminal (select crystal/CR oscillation by mask option)
OSC2	137	O	OSC1 oscillation output terminal
OSC3	132	I	OSC3 oscillation input terminal (select crystal/ceramic/CR oscillation by mask option)
OSC4	133	O	OSC3 oscillation output terminal
MCU/$\overline{\text{MPU}}$	140	I	MCU/MPU mode setup terminal
K00–K02	148–146	I	Input terminals (K00–K02)
K03/$\overline{\text{BREQ}}$	145	I	Input terminal (K03) or bus request signal input terminal ($\overline{\text{BREQ}}$)
K04/EXCL0	144	I	Input terminal (K04) or programmable timer external clock input terminal (EXCL0)
K05/EXCL1	143	I	Input terminal (K05) or programmable timer external clock input terminal (EXCL1)
K06/EXCL2	142	I	Input terminal (K06) or programmable timer external clock input terminal (EXCL2)
K07/EXCL3	141	I	Input terminal (K07) or programmable timer external clock input terminal (EXCL3)
R00–R07/A0–A7	165–172	O	Output terminals (R00–R07) or address bus (A0–A7)
R10–R17/A8–A15	173–180	O	Output terminals (R10–R17) or address bus (A8–A15)
R20–R23/A16–A19	181–184	O	Output terminals (R20–R23) or address bus (A16–A19)
R24/$\overline{\text{RD}}$	185	O	Output terminal (R24) or read signal output terminal ($\overline{\text{RD}}$)
R25/$\overline{\text{WR}}$	186	O	Output terminal (R25) or write signal output terminal ($\overline{\text{WR}}$)
R30–R32/$\overline{\text{CE0}}$–$\overline{\text{CE2}}$	187, 188, 196	O	Output terminals (R30–R32) or chip enable signal output terminals ($\overline{\text{CE0}}$–$\overline{\text{CE2}}$)
R33 ($\overline{\text{BACK}}$)	197	O	Output terminal (R33) or bus acknowledge signal output terminal ($\overline{\text{BACK}}$)
P00–P07/D0–D7	164–157	I/O	I/O terminals (P00–P07) or data bus (D0–D7)
P10/SIN	156	I/O	I/O terminal (P10) or serial I/F data input terminal (SIN)
P11/SOUT	155	I/O	I/O terminal (P11) or serial I/F data output terminal (SOUT)
P12/$\overline{\text{SCLK}}$	154	I/O	I/O terminal (P12) or serial I/F clock I/O terminal ($\overline{\text{SCLK}}$)
P13/$\overline{\text{SRDY}}$	153	I/O	I/O terminal (P13) or serial I/F ready signal output terminal ($\overline{\text{SRDY}}$)
P14/TOUT0/TOUT1	152	I/O	I/O terminal (P14) or programmable timer underflow signal output terminal (TOUT0/TOUT1)
P15/TOUT2/TOUT3	151	I/O	I/O terminal (P15) or programmable timer underflow signal output terminal (TOUT2/TOUT3)
P16/FOUT	150	I/O	I/O terminal (P16) or clock output terminal (FOUT)
P17/$\overline{\text{TOUT2}}$/$\overline{\text{TOUT3}}$	149	I/O	I/O terminal (P17) or programmable timer underflow inverted signal output terminal ($\overline{\text{TOUT2}}$/$\overline{\text{TOUT3}}$)
COM0–COM31	198–213, 112–97	O	LCD common output terminals
SEG0–SEG125	214–252, 4–61, 68–96	O	LCD segment output terminals
$\overline{\text{RESET}}$	139	I	Initial reset input terminal
$\overline{\text{TEST}}$	138	I	Test input terminal
TEST	3	–	Test terminal (open during normal operation)

■ BASIC EXTERNAL CONNECTION DIAGRAM



∗1: OSC1 = Crystal oscillation ∗3: OSC3 = Crystal or Ceramic oscillation
∗2: OSC1 = CR oscillation ∗4: OSC3 = CR oscillation

Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI(Max.) = 35 kΩ
C_{G1}	Trimmer capacitor	0–25 pF
R_{CR1}	Resistor for CR oscillation	1.5 MΩ
X'tal2	Crystal oscillator	4 MHz
Ceramic	Ceramic oscillator	4 MHz
Rf	Feedback resistor	1 MΩ
C_{G2}	Gate capacitor	15 pF (Crystal oscillation) 30 pF (Ceramic oscillation)
C_{D2}	Drain capacitor	15 pF (Crystal oscillation) 30 pF (Ceramic oscillation)
R_{CR3}	Resistor for CR oscillation	40 kΩ
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{C1}	0.1 µF
C_3	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C3}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_7–C_9	Booster capacitors	0.1 µF
C_{10}	Capacitor between V_{SS} and V_{D2}	0.1 µF
C_{11}	Booster capacitor	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{RESET}$ terminal	0.47 µF

Note: The above table is simply an example, and is not guaranteed to work.

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