Preliminary Data Sheet, DS 1, Nov. 2001

SWITI
Switching IC

PEF 20451 HTSI
PEF 20471 HTSI-L
PEF 24471 HTSI-XL
Version 1.3

Wired
Communications

Never stop thinking.

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PRELIMINARY
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Page	Content
20	**Table 6** updated
35	**Chapter 3.4.4** updated, added **Figure 14**
43	**Chapter 3.7.1** and **Chapter 3.7.2** updated
49	**Chapter 4.3** reworked
68	Description of Configuration Command Register 1 and 2 (**CMD1** and **CMD2**) updated
78	Description of Interrupt Status Register 1 (**ISTA1**) reworked
79	Description of Interrupt Error Status Register 1 and 2 (**IESTA1** and **IESTA2**) reworked
83	Description of Interrupt Error Mask Register (**INTEM2**) reworked
91	Description of Source Address (**SA**) and Destination Address (**DA**) Registers updated
97	**Chapter 6.2** reworked
112	**Chapter 6.8.3** reworked
128	**Chapter 7.1** and **Table 27** “PCM timing” updated
131	**Table 28** “PCM Parallel Mode Timing”
144	**Table 35** and **Figure 57** updated
146	Added **Chapter 7.8, “Hardware Reset Timing”**

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PRELIMINARY

PRELIMINARY

Preface

The Switching IC (SWITI) is a family of switching devices for a wide area of telecommunication and data communication applications. This document provides complete reference information according to chip interfaces, programming, internal architecture and applications.

Organization of this Document

This Preliminary Data Sheet is divided into 9 chapters. It is organized as follows:

- **Chapter 1, Overview**
  Gives a general description of the product and of the SWITI family, lists the key features, and presents some typical applications.

- **Chapter 2, Pin Description**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3, Architectural Description**
  Rough overview of the internal architecture and clock fallback feature.

- **Chapter 4, Description of Interfaces**
  Short introduction of used interfaces.

- **Chapter 5, Register Description**
  Gives information about all registers accessible via the microprocessor interface according to address, short name, access, reset value and value range.

- **Chapter 6, Programming the Device**
  Gives a variety of examples how to programm the device, lists all available command and parameter values.

- **Chapter 7, Timing Diagrams**
  Contains timing diagrams.

- **Chapter 8, Electrical Characteristics**
  Specification of the electrical parameters.

- **Chapter 9, Package Outlines**
  Outlines of the available packages (P-BGA-217-1).

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Table 1 Who should read what?

Addressed Person	Relevant Chapters
Programmer	3, 5, 6
Board Designer	2, 3, 4, 7, 8, 9

Related Documentation

H.100 Hardware Compatibility Specification: CT Bus, revision 1.0

H.110 Hardware Compatibility Specification: CT Bus, revision 1.0

PCI Specification, revision 2.1, PCI special interest group

Compact PCI Specification - PICMG 2.0, revision 2.1

Compact PCI Hot Swap Specification - PICMG 2.1, revision 1.0

H-MVIP Standard, Release 1.1a, GO-MVIP Inc., January 1997

MVIP-90 Standard, Release 1.1, GO-MVIP Inc., October 1994

SC-Bus Specification, ANSI/VITA 6-1994

1 Overview

The new switching family, called SWITI, provides a complete and cost-effective solution for all switching systems. The family is divided in two sub-families, the MTSI family and the HTSI family. The Preliminary Data Sheet describes the functionality and characteristic of the HTSI devices.

The devices can be used in today's switching applications, e.g. conventional PBXs and central offices (CO's), as well as in H.100/H.110 applications (only the HTSI family), which are the key to high performing CTI- and Voice-over-IP-applications, one of the most important future technologies in telecommunications.

The main requirements of today's switching applications are met by the following features:

- Constant delay e.g. to support wide band data switching, or channel bundling
- Bit switching/subchannel switching to support applications such as mobile base stations, DECT, computer telephony

In addition, the SWITI family provides new features to ensure a broad range of configurations to make it possible to adapt the device to all switching applications:

- A compliant H.100/H.110 interface (HTSI)
- 8-channel stream-to-stream switching capability (HTSI)
- Message mode, which allows to assign a preset value to any output time-slot
- GPIO (General Purpose I/O) port, which is controlled from the external µP

SWITI family. The SWITI family consists of 6 ICs with different switching capacities. The possible configurations are shown in **Table 2**. The HTSI versions provide an additional H.100 / H.110 interface, while the MTSIs are standard switching devices. All devices can be programmed easily, thus helping the designer/programmer to integrate the device into his application comfortably.

Table 2 SWITI Family Tree

Name	Package	Sales code	Connec-tions	Local bus IN/OUT	H-Bus I/O
HTSI-XL (H-Mode)	P-BGA-217-1	PEF24471 HTSI-XL	2048	16/16	32
HTSI-XL (M-Mode)		PEF24471 HTSI-XL		32/32	-
HTSI-L (H-Mode)	P-BGA-217-1	PEF20471 HTSI-L	1024	16/16	32
HTSI-L (M-Mode)		PEF20471 HTSI-L		32/32	-

Table 2 SWITI Family Tree (cont'd)

Name	Package	Sales code	Connec-tions	Local bus IN/OUT	H-Bus I/O
HTSI (H-Mode)	P-BGA-217-1	PEF20451 HTSI	512	16/16	32
HTSI (M-Mode)		PEF20451 HTSI		32/32	-
MTSI-XL	P-MQFP-100-2	PEF24470 MTSI-XL	2048	16/16	-
MTSI-L	P-MQFP-100-2	PEF20470 MTSI-L	1024	16/16	-
MTSI	P-MQFP-100-2	PEF20450 MTSI	512	16/16	-

HTSI devices.

The HTSI devices can be operated in two different modes, H-Mode and M-Mode.

In H-Mode the device offers 16 local I/Os and additionally a compliant H.100/H.110 interface (32 bidirectional I/Os). The complete number of available connections can be assigned as H-bus to H-bus, local bus to local bus connection, or mixed.

In M-Mode all lines are configured as local I/Os, so that in total 32 local I/Os are provided. Thus e.g. the HTSI-XL device can be used as 2K non-blocking switch operating with all 32 I/Os at 4.096 Mbit/s.

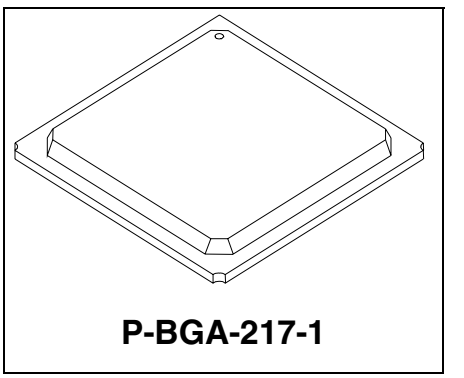
PRELIMINARY

Switching IC
SWITI

PEF 20451 / 20471 / 24471

Version 1.3 **CMOS**

1.1 Overview of Features



P-BGA-217-1

General

- Switching capacity of 512, 1024, or up to 2048 connections of different types between different buses
- Programmable data rates of 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, and 16.384 Mbit/s on per stream basis
- Constant delay or minimum delay programmable on per connection basis
- Subchannel switching ability of 1-bit, 2-bit, 4-bit wide time-slots
- Programmable clock shift for local bus
- 8-channel stream-to-stream switching for H.100/H.110 and interoperability bus
- Automatic data rate adaption
- Optional 8-bit parallel input and/or 8-bit parallel output for first 8 lines of local bus
- Broadcast capabilities
- Multipoint switching ability
- Read and write access to all time-slots
- Message mode (time-slot write access)
- Programmable framing group
- GPIO port
- 8-bit µP-interface supports both Intel and Motorola mode
- Optional 16-bit µP interface mode (instead of GPIO port)
- On chip PLL for H.100/H.110, SCbus, MVIP, MVIP-H clock operation (master/slave) and for local bus clock operation (master/slave)
- JTAG interface
  – Boundary scan according to IEEE 1149.1
- 3.3 V power supply
- 5 V tolerant inputs/outputs

Type	Package
PEF 20451 / 20471 / 24471	P-BGA-217-1

HTSI in H-Mode

- H.100/H.110 compliant interface with all mandatory signals
- Local bus of up to 16 PCM ports (16 In/16 Out)
- Hot swapping

HTSI in M-Mode

- Local bus of up to 32 PCM ports (32 In/32 Out).

1.2 Features in Detail

Flexible Data Rates

Each input and each output line of the local bus is programmable to operate at different data rates. The possible data rates are 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, and 16.384 Mbit/s. Even for the HTSI in M-Mode all of the 32 input lines and 32 output lines are configureable, except for the bit rate of 16.384 Mbit/s.

In case of 16.384 Mbit/s only 24 lines can be used.

The possible data rate for the data lines of the H-Bus are 2.048 Mbit/s, 4.096 Mbit/s and 8.192 Mbit/s.

Constant and Minimum Delay

Each connection independent of the addressed buses can be determined to be a constant delay or minimum delay connection. Constant delay means that any input time-slot or subchannel is available on the programmed output after 2 frames. Minimum delay means that the time-slot or subchannel appears at the output as soon as possible. The minimum delay depends on the chosen connections and the possible range is between 0 and 2 frames.

Subchannel Switching

Each connection can be a 1-bit, 2-bit, 4-bit, or 8-bit connection. Subchannel switching is applicable to both the local bus and the H-Bus and has a constant delay of 2 frames. Sub-Channel switching is supported only for data rate of 2.048 Mbit/s, 4.096 Mbit/s and 8.192 Mbit/s.

Programmable Clock Shift

The position of time-slot 0 of each local bus input line can be programmed within the time-slot before and after the PFS rising edge in half clock steps. Also the position of time-slot 0 of all local bus output lines can be programmed within the first time-slot after the PFS rising edge.

8-Channel Stream-to-Stream Switching

This feature offers the possibility to efficiently switch one data stream to another at the same or different data rates without occupying switching memory capacity. It mainly supports interoperability between CT-bus (Computer Telephony) devices such as SCbus and MVIP-90 running at different data rates. It is possible to use up to 8 lines from the H.1x0 data lines to establish the connections. Input and output frequency can be configured differently.

Automatic Data Rate Adaption

Connections are also possible between lines operating at different data rates. The programmer just specifies input and output line, time-slot, and if necessary, the subchannel.

Parallel Mode

The first 8 local bus input and output lines can be configured to one parallel input or output port respectively. In serial mode a time-slot is determined by 8 consecutive data clock cycles according to each line. In parallel mode a time-slot is determined by 1 data clock cycle according to the first 8 lines.

Broadcast

With this feature it is possible to distribute one incoming time-slot to different output time-slots.

Multipoint

Multipoint connections can be seen as the opposite of broadcast connections. Here it is possible to generate one output time-slot consisting of several input time-slots. The specified input time-slots are logically AND or OR connected (selectable) and have a constant delay of 2 frames.

Read Access

The programmer has access to any input time-slot. After issuing an appropriate command the arrival of the time-slot will be reported by interrupt. The value can be read from a dedicated register. For every read request the command has to be issued again.

Message Mode (Write Access)

This feature allows a constant value to be sent to any given output time-slot.

Framing Group

It is possible to specify up to 8 different framing signals of 8 kHz. The position of the rising edge and the pulse width can be programmed for each signal. The reference frame is determined by the PFS signal. The pulse parameters are programmed in half step resolution according to a 16.384 MHz clock.

General Purpose Clocks

All 8 GPCLK lines can be configured as individual clock outputs with 8 kHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz and for test purposes with the internal frequency or the input frequency of the analog PLL (APLL).

GPIO Port

Each line of the general purpose input/output port can be configured to be either input or output. According to an input an edge causes an interrupt. The outputs can be influenced by write access via the microprocessor interface. Thus the user has the possibility to observe and influence additional signals for his application.

Microprocessor Interface

All devices provide a standard 8-bit microprocessor interface operating in either Intel or Motorola mode. Optionally it is possible to configure the GPIO port as additional data lines to provide a 16-bit microprocessor interface. The use of the 16-bit µP interface reduces the number of write cycles required to configure a connection from 7 (in case of 8-bit µP interface) to 3 write cycles.

Input/Output Tolerance

The HTSI can be used in a 5 V environment with two additional 5 V (VDD) power supply pins. Local input and outputs are 3.3 V and 5 V tolerant. The outputs have TTL level driving capability. The H-Bus lines of the HTSI can be used in a 3.3 V signaling PCI environment.

1.3 Logic Symbol

The HTSI is dedicated to perform time-slot switching between the local bus and the H-Bus or to offer a solution for applications with a high number of local I/Os. The HTSI operates in two modes. In H-Mode (**Figure 1**) it works with the H-Bus and in M-Mode (**Figure 2**) it operates without the H-Bus.
The HTSI in H-Mode provides 16 PCM input lines and 16 PCM output lines and the complete H-Bus with 32 bidirectional H.100/H.110 data lines.

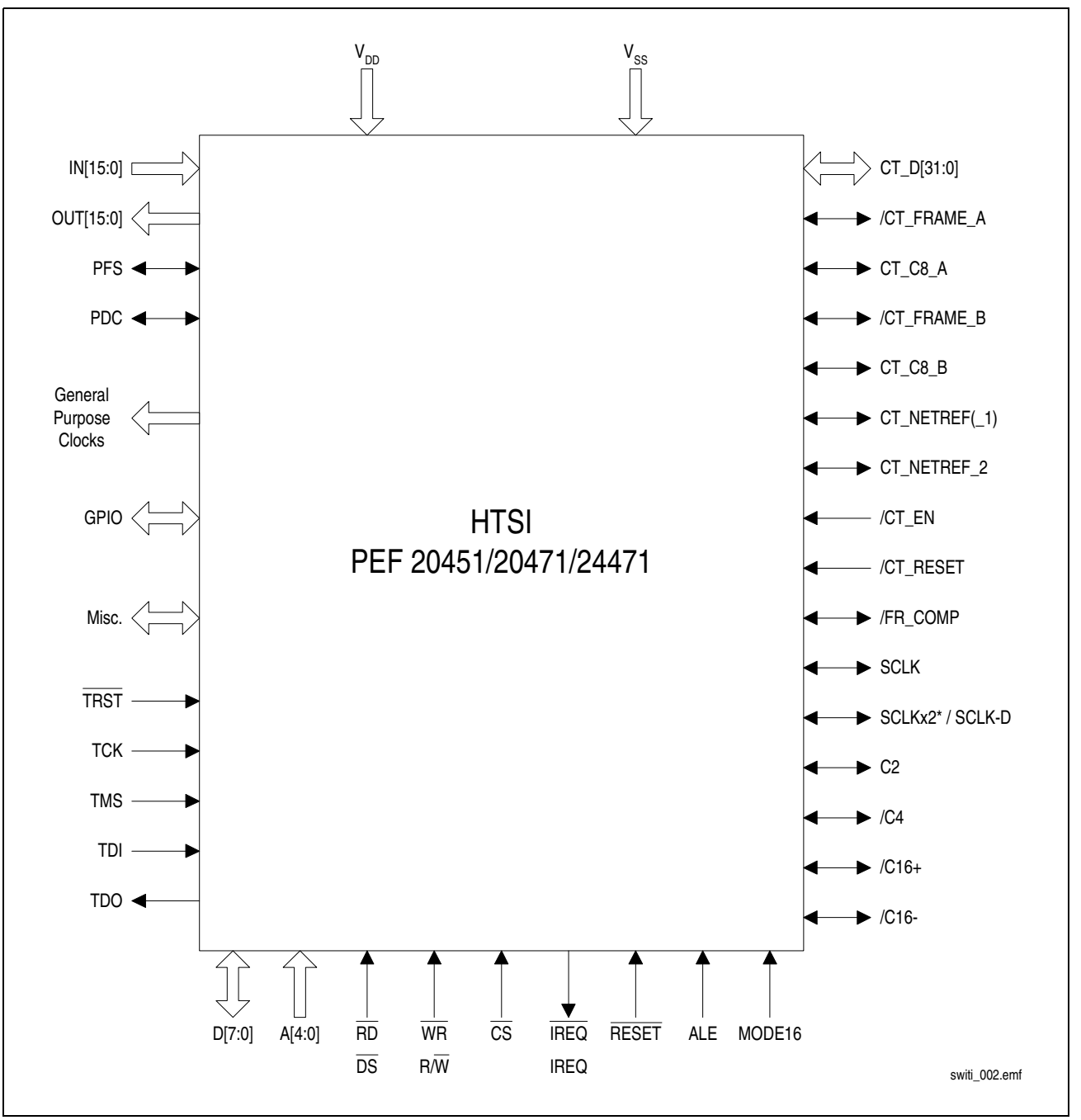


Figure 1 Logic Symbol: HTSI in H-Mode

If no H-Bus is needed it is possible to configure the HTSI in M-Mode. In this mode, the HTSI provides 32 PCM input lines and 32 PCM output lines.

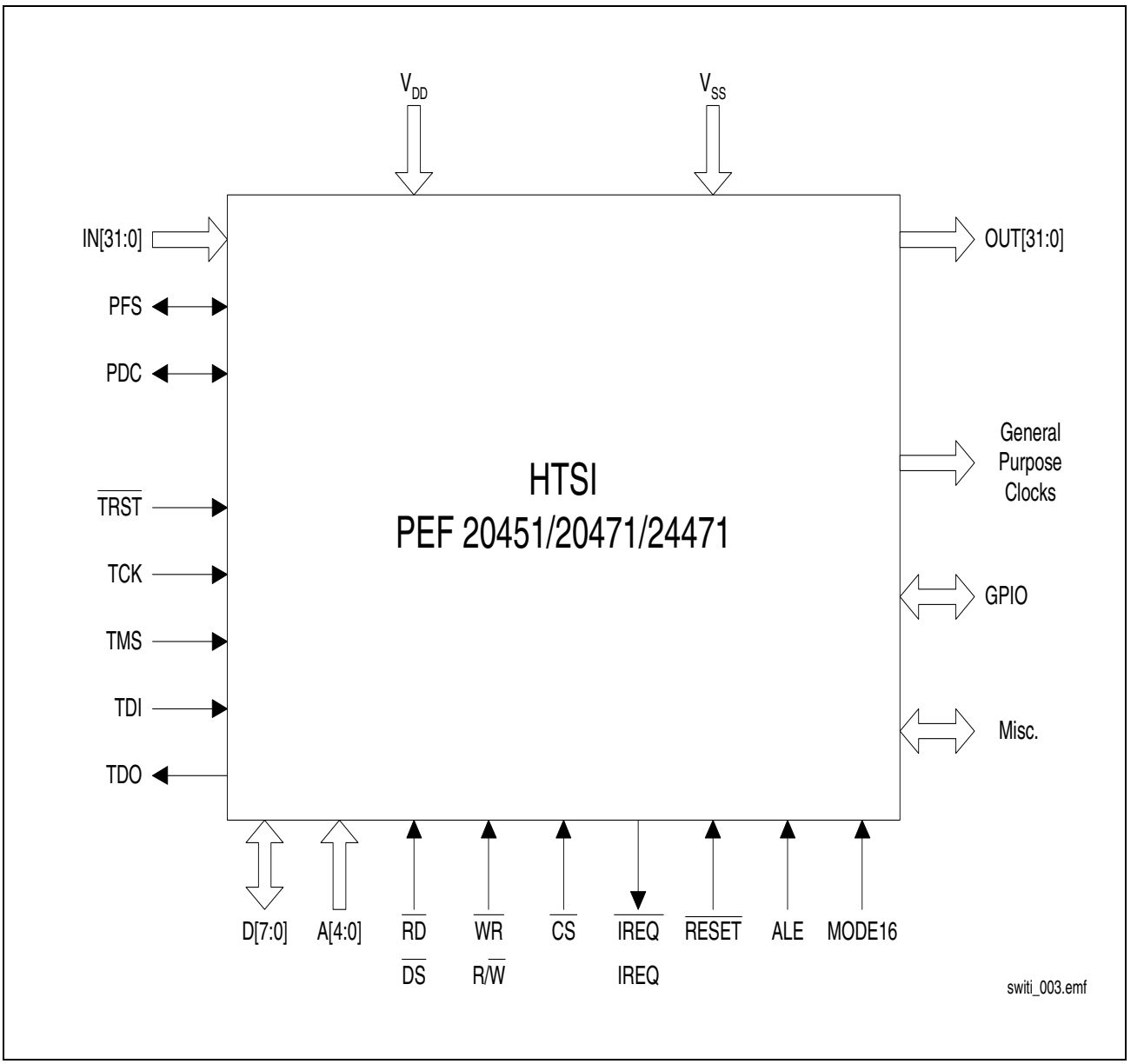


Figure 2 Logic Symbol: HTSI in M-Mode

1.4 Typical Applications

Typical applications of the SWITI family are:

- PCM switch, concentrator or multiplexer in PBXs, COs or mobile base stations
- H.100/H.110 interface in
  - Computer telephony systems
  - Internet telephony systems
  - LAN/WAN access devices
  - Enhanced service platforms

The following sections give a general overview of the system integration of the SWITI family.

1.4.1 Standard PBX or CO Application

The MTSI or the HTSI in M-Mode can be used, just as the MTSC or MTSL, in standard private branch exchange or central office applications (**Figure 3**), e.g. in the switching network.

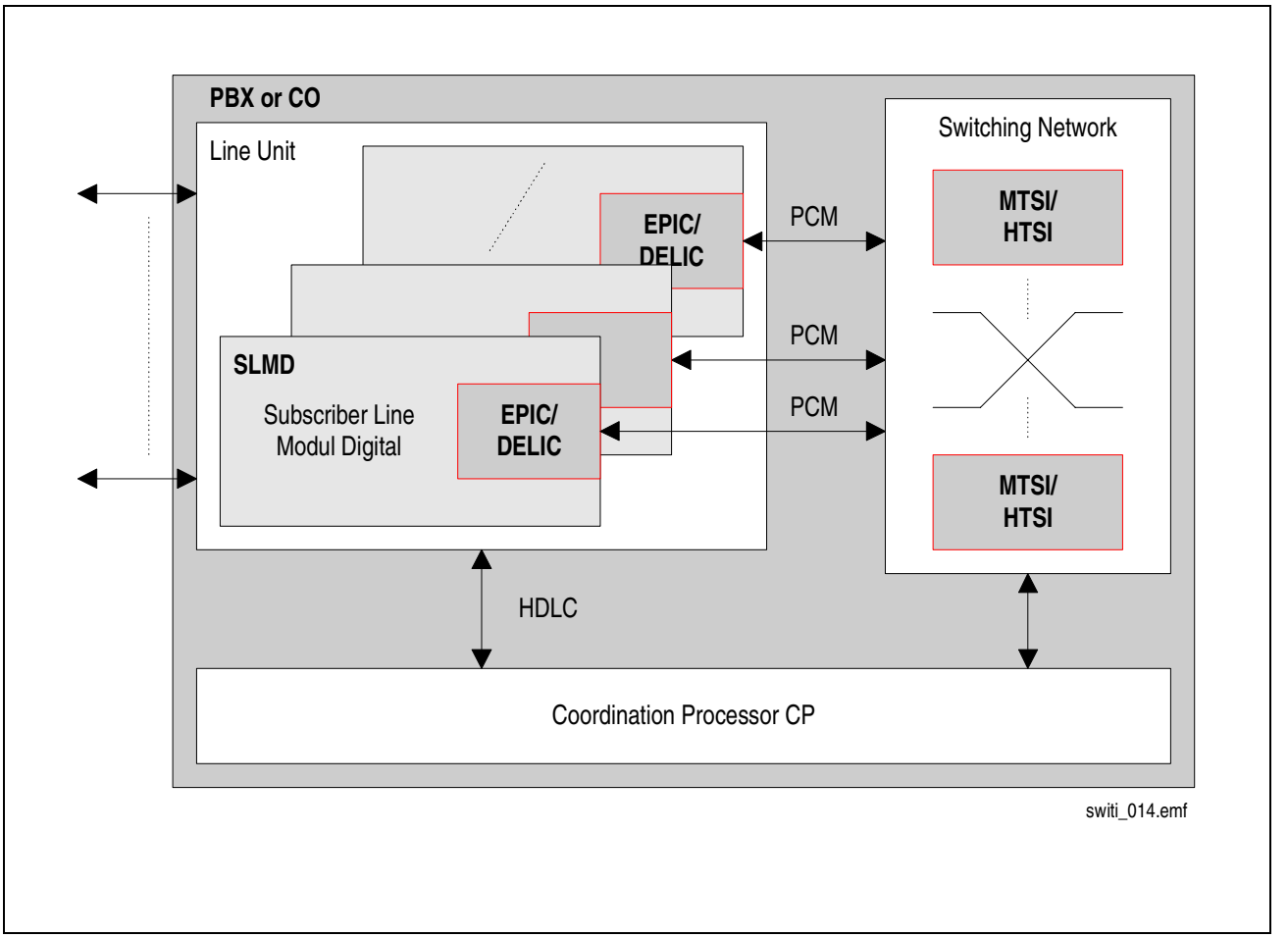


Figure 3 Standard PBX or CO Application

1.4.2 Computer Telephony Application

In Computer Telephony Integration (CTI) applications, resources such as the analog telephone line cards, ISDN ports, switching controllers, FAX firmware, or voice processing modules are in the form of plug-in cards that sit on the ISA or PCI slots of a PC. Resource sharing is established by connecting the top of the plug-in cards with cables. This Time Division Multiplex (TDM) bus has evolved from the original H-MVIP, MVIP-90, Dialogic's SC-Bus, into the latest H.100/H.110 bus or H-Bus developed by the Enterprise Computer Telephony Forum (ECTF). By connecting to the H.100/H.110 interface devices, system modules may send and receive data to and from any one of the 4096 TDM time-slots of the H-Bus. The H-Bus also offers the ideal solution for routers to provide a bridge between the data communication and telecommunication system modules.

In Computer Telephony (CT) environment, resource sharing is accomplished by passing data back and forth through the H.100/H.110 bus. **Figure 4** shows the example.

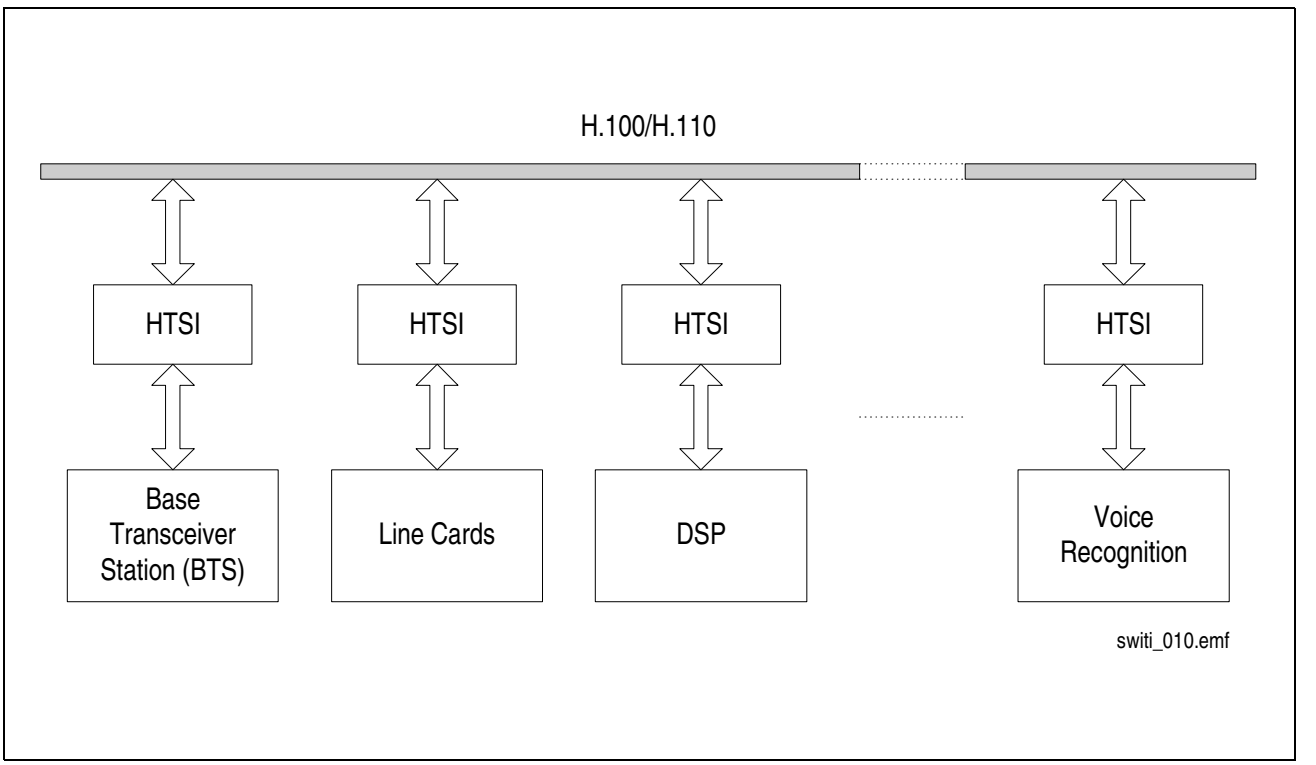


Figure 4 CT Application

1.4.3 Router / Remote Access Application

The HTSI (H-Mode) or also the MTSI (if no H-Bus interface is used in the system) is used in multivoice applications as the bridge connecting the data communication modules to the telecommunication modules in a router/remote access design. **Figure 5** shows the example.

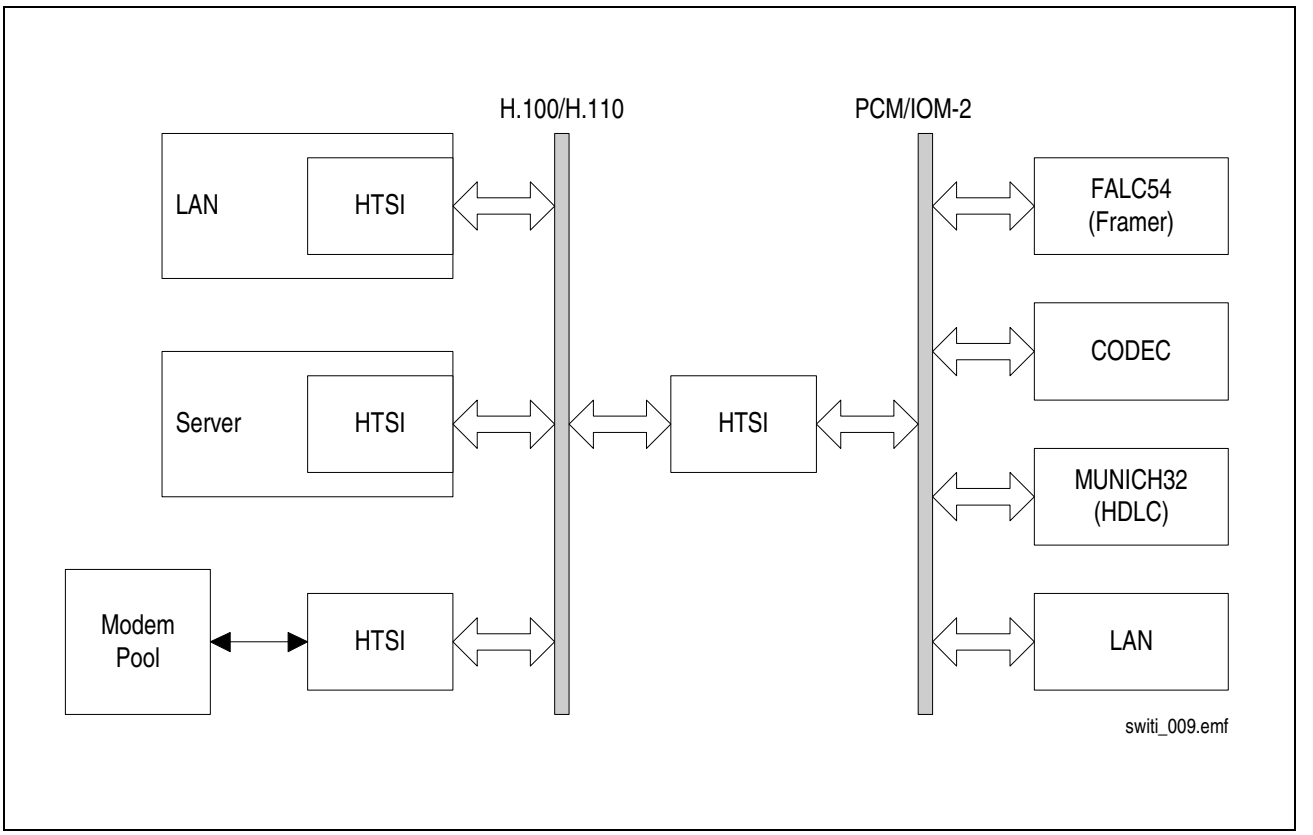


Figure 5 Router / Remote Access Applications

1.4.4 Voice over IP Application

In a voice over IP application (**Figure 6**) the HTSI (in H-Mode) may be used to connect a conventional PBX to the H-Bus. A Vocoder card, also connected to the H-Bus, performs speech compression and decompression whereas an Ethernet card transmits and receives the compressed data over the network.

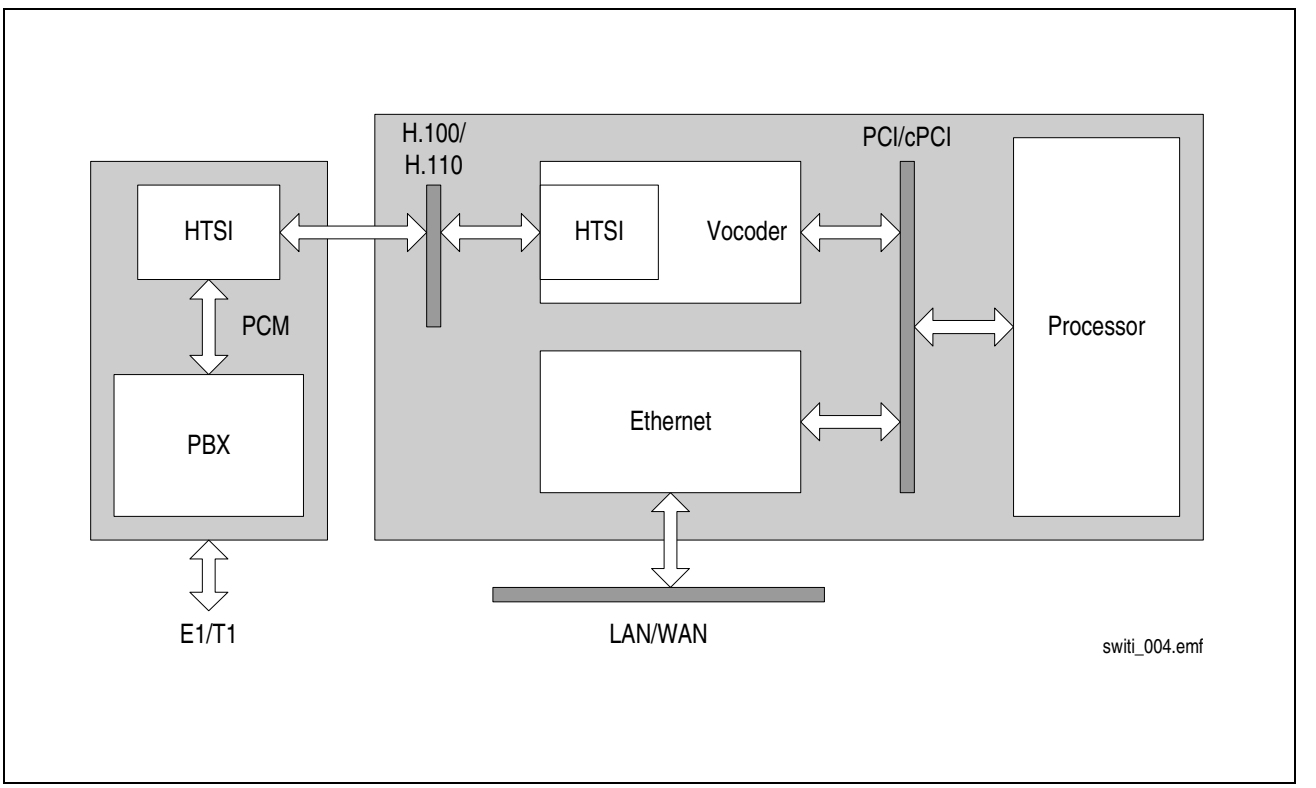


Figure 6 Voice over IP Application

2 Pin Description

The pin description gives an overview of the pin numbers, names, direction, position and function ordered by the different interfaces.

Note: All unused input or I/O pins should be connected to V_{SS} to avoid leakage current.

2.1 Pin Diagram

P-BGA-217-1

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
NC	NC	CT_D_0 /IN_16	CT_D_2/ IN_18	IN_3	IN_5	VSS	CT_D_6/ IN_22	CT_D_7/ IN_23	CT_D_8/ IN_24	IN_9	IN_11	VDD	CT_D_12 /IN_28	CT_D_14/ IN_30	NC	NC	A
NC	VSS	VDD	IN_1	VDD5	CT_D_3/ IN_19	CT_D_5/ IN_21	IN_6	IN_7	VDD5	CT_D_9 /IN_25	CT_D_11 /IN_27	IN_12	IN_14	NC	VSS	NC	B
GPCLK_2	NC	VSS	VSS	IN_2	VSS	IN_4	VDD	IN_8	VSS	CT_D_10 /IN_26	VSS	CT_D_13 /IN_29	CT_D_15/ IN_31	VSS	VDD	WR R/W	C
VDD	/CT_ FRAME_A	GPCLK_0	VSS	IN_0	CT_D_1/ IN_17	CT_D_4/ IN_20	VDD	VSS	VDD	IN_10	IN_13	IN_15	VSS	VSS	C2	A_1	D
GPCLK_5	VSS	GPCLK_3	GPCLK_1										RD/DS	A_0	A_2	VDD	E
GPCLK_7	GPCLK_6	CT_C8_A	GPCLK_4										ALE	/C4	VSS	/C16+	F
VSSA	VDDA	/CT_ FRAME_B	CT_C8_B										A_4	A_3	D_0	D_2	G
ECLKO	M-MODE	CT_ NETREF2	VDD										VDD	D_1	D_3	/C16-	H
ECLKI	RESERV.	RESERV.	VSS										VSS	D_4	VDD	VSS	J
H110- MODE	/CT_ RESET	NTWK_2	VDD										VDD	D_6	/FR_ COMP	D_5	K
NTWK_1	VDD	RESET	IREQ										GPIO_1	SCLK	GPIO_0	D_7	L
VSS	MODE16	VDD	CT_ NETREF1										GPIO_5	GPIO_3	VSS	VDD	M
CS	VSS	PFS	TDO										VDD	GPIO_6	SCLKx2* SCLK-D	GPIO_2	N
PDC	TRST	TMS	VSS	VSS	CT_D_17/ OUT_17	CT_D20/ OUT20	VDD	VSS	VDD	OUT_10	OUT_13	CT_D_30/ OUT_30	VSS	VSS	GPIO_7	GPIO_4	P
TDI	TCK	VSS	VDD	OUT_1	VDD5	OUT_4	VDD	CT_D22/ OUT22	VSS	CT_D_26 /OUT_26	VDD	CT_D_28/ OUT_28	OUT_15	VSS	NC	/CT_EN	R
NC	VSS	NC	CT_D_16/ OUT_16	CT_D_18/ OUT_18	OUT_3	OUT_5	VSS	CT_D_23 /OUT_23	CT_D_24 /OUT_24	OUT_9	OUT_11	VSS	CT_D_29/ OUT_29	CT_D_31 /OUT_31	VSS	NC	T
NC	NC	OUT_0	OUT_2	VSS	CT_D_19/ OUT_19	CT_D_21 /OUT_21	OUT_6	OUT_7	OUT_8	VDD5	CT_D_25/ OUT_25	CT_D_27/ OUT_27	OUT_12	OUT_14	NC	NC	U

P-BGA- 217-1

VSS	VSS	VSS
VSS	VSS	VSS
VSS	VSS	VSS

Bottom View

switi_076.emf

Figure 7 Pin Configuration

2.2 Pin Definitions and Functions

2.2.1 H-Bus Interface

The following table (**Table 3**) is only applicable for the H-mode except the CT_D (IN/OUT) lines.

Table 3 H.100/H.110 Bus Interface (H-mode only)

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
D16	$\overline{\text{CT\_FRAME\_A}}$	I/O	H.1x0 only Frame Sync - driven by the "A" clock master. This is a negative true pulse, nominally 122 ns wide that straddles the beginning of the first bit of the first time slot. It has a period of 125 µs.	High Z
F15	CT_C8_A	I/O	H.1x0 only Bit Clock - driven by "A" clock master. The clock frequency is 8.192 MHz. The duty cycle of this signal is nominally 50%.	High Z
G15	$\overline{\text{CT\_FRAME\_B}}$	I/O	H.1x0 only Redundant Frame Sync - driven by the "B" clock master. This is a negative true pulse, nominally 122 ns wide that straddles the beginning of the first bit of the first time slot. It has a period of 125 µs.	High Z
G14	CT_C8_B	I/O	H.1x0 only Redundant Bit Clock - driven by "B" clock master. The clock frequency is 8.192 MHz. The duty cycle of this signal is nominally 50%.	High Z
T3, P5, T4, R5, U5, R7, U6, T8, T9, R9, U11, P11, U12, T13, P12, T14, C4, A3, C5, A4, B6, C7, B7, A8, A9, A10, B11, D11, B12, A14, D12, A15	CT_D[31:0][1)]	I/O	H-Mode Serial Data lines that can be driven by any board in the system. However, only one board can drive the bus at any given time slot on each stream. Each signal contains 128 time slots per frame at a clock frequency of 8.192 MHz. These 32 signals collectively are referred to as the CT_D bus. CT Bus devices may connect to subsets of the CT_D bus.	High Z
			M-mode	
	CT_D[15:0] as IN[31:16]	I	PCM Receive Data Port 16 to 31 (PCM mode only)	
	CT_D[31:16] as OUT[31:16]	O	PCM Transmit Data Port 16 to 31 (PCM mode only)	High Z

Table 3 H.100/H.110 Bus Interface (H-mode only) (cont'd)

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
M14	CT_NETREF_1	I/O	H.1x0 Additional Network Timing Reference - driven by any (single) CT Bus digital trunk interface to provide network synchronization to the CT Bus. This signal can have any duty cycle as long as the period is 125 µs (8 kHz), 647 ns (1.544 MHz), or 488 ns (2.048 MHz) and is network synchronized. There is no specified phase relation to CT_NETREF_2 and the other clocks. It has a minimum high of 90 ns and a minimum low time of 90 ns.	High Z
H15	CT_NETREF_2	I/O	H.1x0 Additional Network Timing Reference - driven by any (single) CT Bus digital trunk interface to provide network synchronization to the CT Bus. This signal can have any duty cycle as long as the period is 125 µS (8 kHz), 647 ns (1.544 MHz), or 488 ns (2.048 MHz) and is network synchronized. There is no specified phase relation to CT_NETREF_1 and the other clocks. It has a minimum high time of 90 ns and a minimum low time of 90 ns.	High Z
R1	$\overline{\text{CT\_EN}}$	I	H.110 only Logic low signal to indicate that J4 of a CT Bus card is fully seated.	
K16	$\overline{\text{CT\_RESET}}$	I	H.110 only Logic low signal used to reset all CT Bus cards that do not have access to the PCI RST# reset from J1/P1.	
K2	$\overline{\text{FR\_COMP}}$	I/O	H.1x0 Compatibility frame pulse - driven by current clock master. This is a negative true pulse, nominally 122 ns wide, that straddles the beginning of the first bit of the first time slot. It has a period of 125 µs. This signal serves as the frame synchronization signal for SCbus (Fsync*) and MVIP (/F0).	High Z
L3	SCLK	I/O	H.1x0 SCbus System clock - driven by current clock master. The clock is selectable. It can be either 2.048 MHz, 4.096 MHz, or 8.192 MHz. It is used to identify the data bit positions on the SCbus. The positive going edge indicates the beginning of the bit.	High Z
N2	SCLKx2* SCLK-D	I/O	H.100 SCbus System (SCLK) clock times two - driven by current clock master. The clock frequency is exactly twice that of SCLK. Transitions of SCLK occur on the falling edge of SCLKx2* for SCbus operating at 2.048 MHz, 4.096 MHz, or 8.192 MHz. H.110 Inter-operability clock - driven by current clock master. The clock frequency is 8.192 Mhz. It is used to identify the data bit positions on the ANSI VITA 6, SCbus. The positive going edge indicates the sample point of the bit.	High Z

Table 3 H.100/H.110 Bus Interface (H-mode only) (cont'd)

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
D2	C2	I/O	H.1x0 MVIP-90 bit clock - driven by current clock master. The clock frequency is 2.048 MHz, nominally symmetrical. The positive going edge indicates the beginning of the bit.	High Z
F3	$\overline{C4}$	I/O	H.1x0 MVIP-90 bit clock times two - driven current by clock master. The clock frequency is exactly twice C2, and transitions of C2 are synchronous with the falling edge of $\overline{C4}$.	High Z
F1	$\overline{C16}$+	I/O	H.1x0 H-MVIP 16.384 MHz Positive active low Clock. High to low transition on frame boundary	High Z
H1	$\overline{C16}$-	I/O	H.1x0 H-MVIP 16.384 MHz Negative active low Clock. Low to high transition on frame boundary	High Z
H16	M-MODE[2)]	I	Mode Selection Pin for H-Mode or M-Mode low=H-Bus is in normal H.100/H.110 mode (H-Mode) high=H-Bus interface is additional PCM interface (port 16 to 31), (M-mode)	
K17	H110-MODE[3)]	I	Mode Selection Pin for H.100/H.110 low = the H-Bus operates in H.100 mode high = the H-Bus operates in H.110 mode ***Note: The pin must be connected to VSS in M-MODE***	

1) T3 is CT_D31, P5 is CT_D30, T4 is CT_D29..

2) Pin has to be connected to VDD or VSS as required. The pin information is sampled during reset.

3) Pin has to be connected to VDD or VSS as required The pin information is sampled during reset. The pin must be connected to VSS in M-MODE.

2.2.2 Local Bus Interface (PCM)

Table 4 Local Bus Interface

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
N15	PFS	I/O	PCM Frame Synchronization Clock of 8 kHz	High Z
P17	PDC	I/O	PCM Data Clock of 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, 16.384 Mbit/s	High Z
D5, B4, D6, B5, A6, D7, A7, C9, B9, B10, A12, C11, A13, C13, B14, D13	IN[15:0][1)]	I	PCM Receive Data Port 15 to 0	
R4, U3, P6, U4, T6, P7, T7, U8, U9, U10, T11, R11, T12, U14, R13, U15	OUT[15:0][2)]	O	PCM Transmit Data Port 15 to 0	High Z

1) D5 is IN15, B4 is IN14, D6 is IN13..

2) R4 is OUT15, U3 is OUT14, P6 is OUT13..

2.2.3 General Purpose Port

Table 5 GPIO

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
P2, N3, M4, P1, M3, N1, L4, L2	GPIO[7:0][1)] D[15:8]	I/O	General Purpose I/O port (only if 8-bit µP interface used) Upper 8 bit of 16-bit µP interface	Input

1) P2 is GPIO7, N3 is GPIO6, M4 is GPIO5..

2.2.4 Clock Signals

Table 6 Clock Pins

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
J17	ECLKI	I	External Crystal Input of 16.384 MHz, or 32.768 MHz External Oscillator Input of 16.384 MHz, or 32.768 MHz	
H17	ECLKO	O	External Crystal Output of 16.384 MHz, or 32.768 MHz	
F17, F16, E17, F14, E15, C17, E14, D15	GPCLK[7:0][1)]	O	General Purpose Clock Output (Framing Signals)	High Z
L17	NTWK_1	I	Primary Network Timing Reference Input Optionally the PLL can be synchronized to this input which can be 8 kHz, 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz	
K15	NTWK_2	I	Secondary Network Timing Reference Input Optionally the PLL can be synchronized to this input which can be 8 kHz, 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz	

1) F17 is GPCLK7, F16 is GPCLK6, E17 is GPCLK5..

2.2.5 JTAG Interface

Table 7 JTAG Interface

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
R16	TCK	I	Test Clock Single rate test data clock.	
P15	TMS	I	Test Mode Select A ’0’ to ’1’ transition on this pin is required to step through the TAP controller state machine.	
P16	$\overline{\text{TRST}}$	I	Test Reset Resets the TAP controller state machine (asynchronous reset).	
N14	TDO	O	Test Data Out In the appropriate TAP controller state test data or a instruction is shifted out via this line.	High Z
R17	TDI	I	Test Data Input In the appropriate TAP controller state test data or a instruction is shifted in via this line.	

2.2.6 Microprocessor Interface

Table 8 Microprocessor Interface

Pin No.	Symbol	In (I) Out (O)	Function	Reset Behavior
N17	$\overline{CS}$	I	Chip Select Active low. A "low" on this line selects all registers for read/ write operations.	
E4	$\overline{RD}$ $\overline{DS}$	I	Read (Intel/Infineon Mode) Indicates a read access. Data Strobe (Motorola Mode) During a read cycle, DS indicates that the device should place valid data on the bus. During a write access, DS indicates that valid data is on the bus.	
C1	$\overline{WR}$ R/$\overline{W}$	I	Write (Intel/Infineon Mode) Indicates a write access. Read/Write (Motorola Mode) Indicates the direction of the data transfer on the bus.	
F4	ALE	I	Address Latch Enable Controls the on-chip address latch in multiplexed bus mode. While ALE is 'high', the latch is transparent. The falling edge latches the current address. ALE is also evaluated to determine the bus mode (ALE fix 'low' = Motorola, fix 'high' = Intel/Infineon)	
M16	MODE16	I	Microprocessor Bus 8/16-Bit Interface Selection ('low' = 8 bit, 'high' = 16 bit)	
L14	IREQ/ $\overline{IREQ}$	O OD	Interrupt Request This pin is programmable to push/pull (active high or low) or open-drain. This signal is activated when SWITI requests an µP interrupt. When operated in open drain mode, multiple interrupt sources may be connected.	High Z
G4, G3, E2, D1, E3	A[4:0][1)]	I	Address Bus When operated in address/data multiplex mode, the address pins are externally connected to the D bus.	
L1, K3, K1, J3, H2, G1, H3, G2	D[7:0][2)]	I/O	Data bus	Input
L15	$\overline{RESET}$	I	System Reset SWITI is forced to go into reset state.	

1) G4 is A4, G3 is A3, E2 is A2..

2) L1 is D7, K3 is D6, K1 is D5..

2.2.7 Power Supply

Table 9 Power Supply Pins

Pin No.	Symbol	In (I) Out (O)	Function
C2, E1, J2, M1, N4, R6, R10, R14, M15, D17, B15, C10, A5, D8, D10, H4, H14, K4, P8, P10, K14, L16	V_{DD}	I	Power Supply 3.3 V
B8, B13, R12, U7	V_{DD5}	I	I/O Reference Voltage 5,0 V for 5 V tolerant I/Os. Pins must be connected at 3,3 V in a 3,3 V signal environment
D3, F2, J1, M2, P3, T5, R8,T10, U13, P13, N16, M17, E16, C14, C12, A11, C8, C6, B2, B16, C3, C15, D4, D9, D14, H8, H9, H10, J4, J8, J9, J10, J14, K8, K9, K10, P4, P9, P14, R3, R15, T2, T16	V_{SS}	I	Digital Ground (0 V)
G16	V_{DDA}	I	Power Supply Analog Logic 3.3 V Used for PLL
G17	V_{SSA}	I	Analog Ground (0 V)
J16	R		Reserved. Must be connected to VSS
J15	R		Reserved. Must be connected to VSS
B1, R2, U2,T15, T17, C16, A16, B3, A1, T1, U1, U16, U17, B17, A17, A2	NC		Not Connected

3 Architectural Description

The following sections give a short overview of the functionality of the SWITI.

3.1 Functional Block Diagram

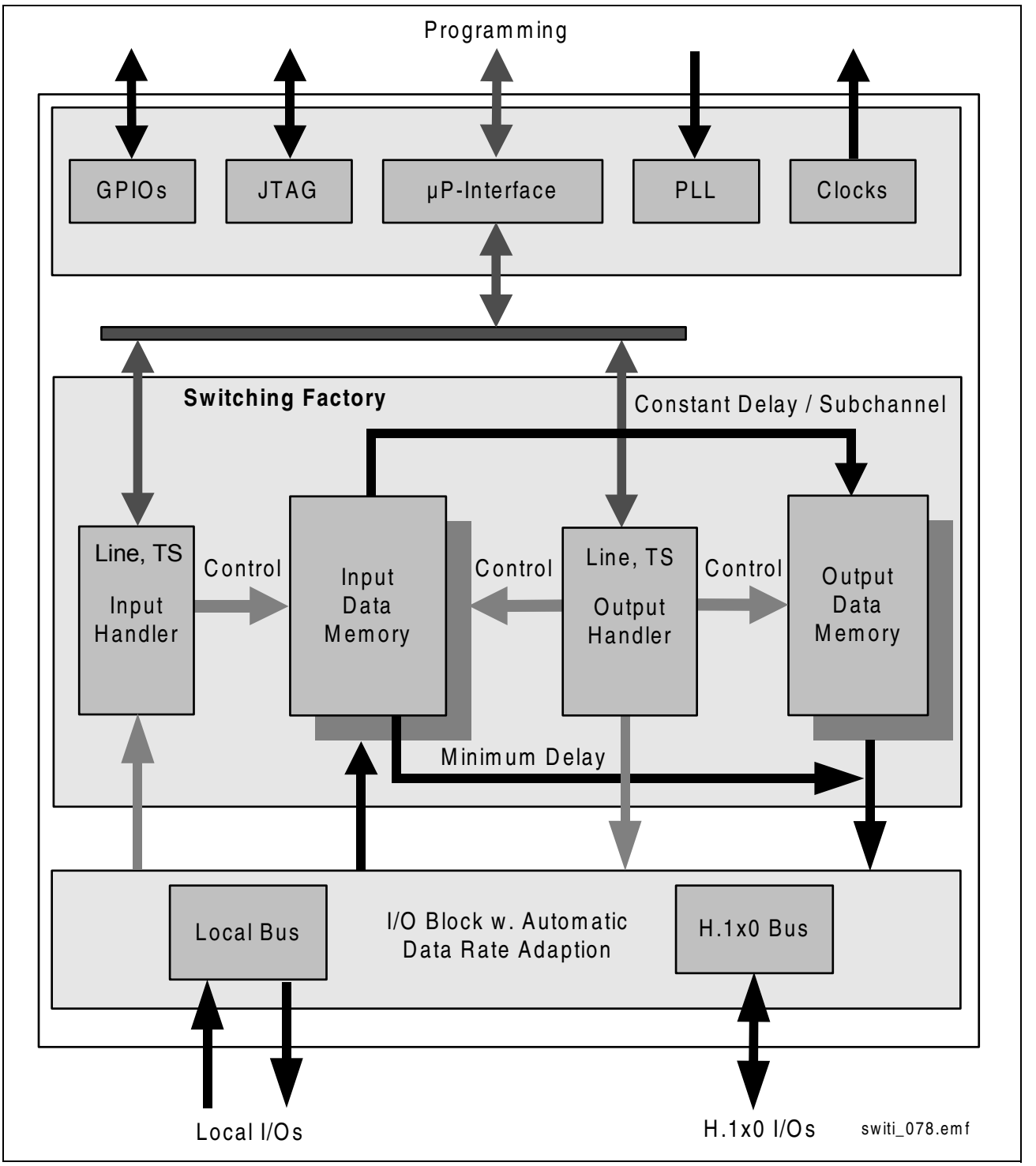


Figure 8 Block Diagram

3.2 Overview of Functional Blocks

Switching Factory

The switching factory is responsible for transferring and handling the incoming data streams to the assigned output channels and time-slots. The block includes a 512, 1024, or 2048 byte input and output data memory as far as an input and output connection memory.

Local bus and H-Bus I/O Block

The block is designed to handle the conversion of the data provided via the switching block and the external PCM and H.1x0 interface. It performs the PCM and H.1x0 timing, the data rate selection and the tristate control.

Microprocessor Interface Block

A standard 8-bit multiplexed or de-multiplexed µP interface is provided, compatible to Intel/Infineon Tech. (e.g. 80386EX, C166) and Motorola (e.g. 68040, 68340, 68360, 801) bus systems. If the GPIO port is not needed it can be used to provide a 16-bit µP interface.

GPIO Block

This block supports up to 8 external port lines each one configurable as input or output. A change on an input line may cause an interrupt (if not masked). The user has access to the port configuration and information via the appropriate registers of the µP interface.

PLL and Clock Block

The PLL generates all frequencies supporting the H.1x0, SCbus, MVIP, H-MVIP busses. The internal phase-locked loop (PLL) generates all bus frequencies synchronized to a selected reference signal. The output frequency tolerance is equal to the input frequency tolerance. The PLL operates from a 16.384 MHz, or 32.768 MHz external crystal, oscillator. According to the H.1x0 specification the input frequency tolerance must be ±32 ppm or less.

3.3 Switching Factory

As shown in **Figure 8** the switching factory comprises the input/output data memory and the input/output data handler with the programmed connections. The I/O controller handles all lines operating at the same or different data rate. To establish a connection the user must only program the source line with time-slot and the destination line with the time-slot. The internal controller (data handler) writes the connection in a connection descriptor list and stores this list in the connection data handler. The programming procedure is described in **Chapter 6**. The incoming time-slot will be stored in the input data memory controlled by the input handler. The output handler controls the constant, minimum delay and subchannel switching.

3.3.1 Switching Modes

The SWITI family supports a various number of switching modes. All modes are described in the following chapters.

3.3.1.1 Minimum and Constant Delay

Each connection independent of the addressed buses can be determined to be a constant delay or minimum delay connection. Constant delay means that any input time-slot or subchannel is available on the programmed output after 2 frames. Minimum delay means that the time-slot or subchannel appears at the output as soon as possible. The minimum delay depends on the chosen connections and the possible range is between 0 and 2 frames, up to 3 frames in rare cases.

An application note which describes the possible connection and minimum delays is available.

3.3.1.2 Subchannel Switching

Subchannel switching is applicable to both the local bus and the H-Bus and has a constant delay of 2 frames. Every connection can be 1-bit, 2-bit, 4-bit, or normal 8-bit connection. It is possible to combine every kind of subchannel connection, e.g. two 1-bit time-slots with one 4-bit time-slot to one output time-slot. Please refer to **Chapter 6.11.2** for a detailed description about the programming.

3.3.1.3 Multipoint Switching

As described in the overview the multipoint-switching allows to switch several input time-slots to one output time-slot. All input data are logical AND or OR connected. This mode is selectable with the multipoint connection command. The setup (logical AND or OR) for the last connection determines all other previous programmed multipoint connections. Multipoint switching has always a constant delay. Subchannel switching is not supported.

3.3.1.4 Broadcast Switching

Broadcast switching allows to distribute one incoming time-slot to different output time-slots. The input and output mechanism is the same as the normal constant delay connection mode with subchannel switching. Minimum delay is also supported without subchannel switching.

A table with the possible connections and minimum delays will be provided.

The broadcast connection is programmed in the same way as a normal connection. The output time-slots can be released with the disconnect part of broadcast command. The last connection must be released with the normal disconnect command.

Subchannel Broadcast

It is possible to program one input time-slot as broadcast subchannel connections. That means the bits from the input time-slot are used in several broadcast connections related to one ore more output time-slots.

The output time-slots must be released with the disconnect part of broadcast command. The last subchannel connection must be released with the normal disconnect command. (Please refer to **Chapter 6.11.4** for an example)

3.3.1.5 Bidirectional Switching

The input and output mechanism is the same as the normal constant delay or minimum delay connection. The exception for the internal data handling is explained in the following figure. Since the internal state machine has to calculate the belonging connection the time to program a bidirectional connection is twice as the time to program a normal connection. There is a special command to program a bidirectional connection. A bidirectional connection can only be programmed on a available time-slot and input/output line.

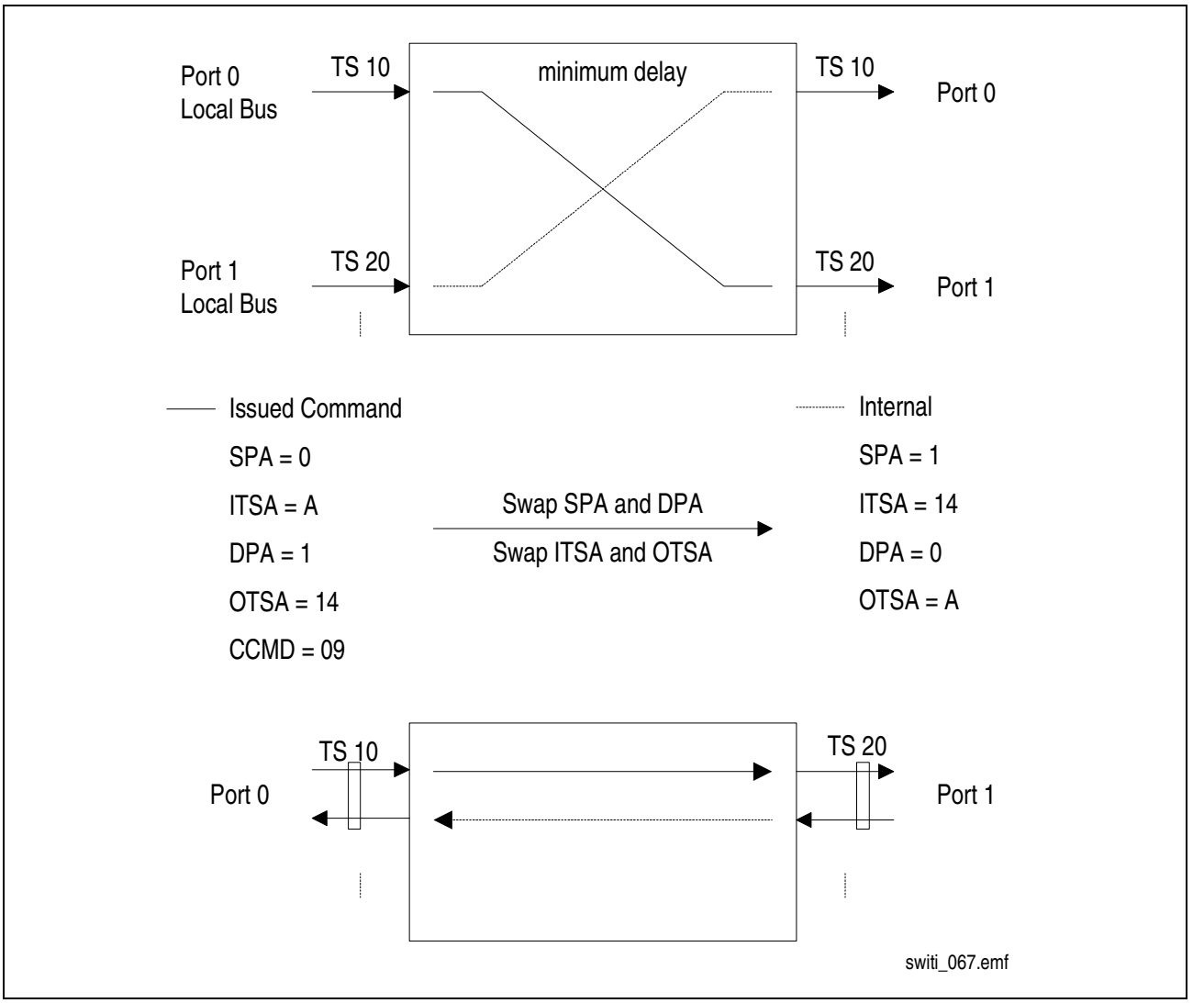


Figure 9 Bidirectional Mode

3.3.1.6 Stream-to-Stream Switching

The stream-to-stream switching connection supports the interoperability for the H.1x0 bus with the MVIP and SCbus, it doesn't support the local bus lines.

Every dataline can be selected for the operation. The maximum number of switching channels is eight. The following example on **page 29** is using two switching channels. The stream-to-stream connection can not be established parallel to the normal connections. The output of the stream-to-stream switch is multiplexed with the output of the switching factory, with the stream-to-stream having priority.

Every stream-to-stream connection must be programmed with the special command in the **CMD1** register. To establish the connection the bit I2 must be set to 1 and to release the connection the bit I2 must be set to 0. If the bit I3 is set to 1 all stream-to-stream connections will be released. The STR bit in the **ISTA1** register indicates that one or more stream-to-stream connections are set (see also **Chapter 6.2**). A internal control

logic avoids a wrong selection of the possible stream-to-stream connections and thus prevents bus collisions.

The main application of the stream switch is to provide an inter-rate exchange highway allowing legacy bus devices to exchange data even though they operate at different rates with a minimum delay of zero frames.

The stream-to-stream connections starts with the first frame and the switching possibilities are determined by the highest bit rate and can be seen as a repetition of same time-slot (TS) connections from one data line to another data line. If the first TS switching sequence is finished it starts with the same sequence from the next available time-slots.

Table 10 shows the possible time-slot connections.

Table 10 Stream-to-Stream Connection Mapping

Input Data Stream Rate	Output Data Steam Rate	Mode Partition	Time-Slot Connection
2.048 Mbit/s	2.048 Mbit/s	0	0 to 1, 1 to 2, 2 to 3, 3 to 4,....., 31 to 0
	4.096 Mbit/s	0	0 to 2, 1 to 4, 2 to 6, 3 to 8,....., 31 to 0
		1	0 to 3, 1 to 5, 2 to 7, 3 to 9,....., 31 to 1
	8.192 Mbit/s	0	0 to 4, 1 to 8, 2 to 12, 3 to 16,...., 31 to 0
		1	0 to 5, 1 to 9, 2 to 13, 3 to 17,...., 31 to 1
		2	0 to 6, 1 to 10, 2 to 14, 3 to 18,...., 31 to 2
		3	0 to 7, 1 to 11, 2 to 15, 3 to 19,...., 31 to 3
4.096 Mbit/s	2.048 Mbit/s	0	0 to 1, 2 to 2, 4 to 3, 6 to 4,....., 62 to 0
		1	1 to 1, 3 to 2, 5 to 3, 7 to 4,....., 63 to 0
	4.096 Mbit/s	0	0 to 1, 1 to 2, 2 to 3, 3 to 4,....., 63 to 0
	8.192 Mbit/s	0	0 to 2, 1 to 4, 2 to 6, 3 to 8,....., 63 to 0
		1	0 to 3, 1 to 5, 2 to 7, 3 to 9,....., 63 to 1
8.192 Mbit/s	2.048 Mbit/s	0	0 to 1, 4 to 2, 8 to 3, 12 to 4,....., 124 to 0
		1	1 to 1, 5 to 2, 9 to 3, 13 to 4,....., 125 to 0
		2	2 to 1, 6 to 2, 10 to 3, 14 to 4,....., 126 to 0
		3	3 to 1, 7 to 2, 11 to 3, 15 to 4,....., 127 to 0
	4.096 Mbit/s	0	0 to 1, 2 to 2, 4 to 3, 6 to 4,....., 126 to 0
		1	1 to 1, 3 to 2, 5 to 3, 7 to 4,....., 127 to 0
	8.192 Mbit/s	0	0 to 1, 1 to 2, 2 to 3, 3 to 4,....., 127 to 0

Example:

D0 = input stream with 2.048 Mbit/s, D3 = output stream with 8.192 Mbit/s, mode 2

D3 = input stream with 8.192 Mbit/s, D1 = output stream with 4.092 Mbit/s, mode 1

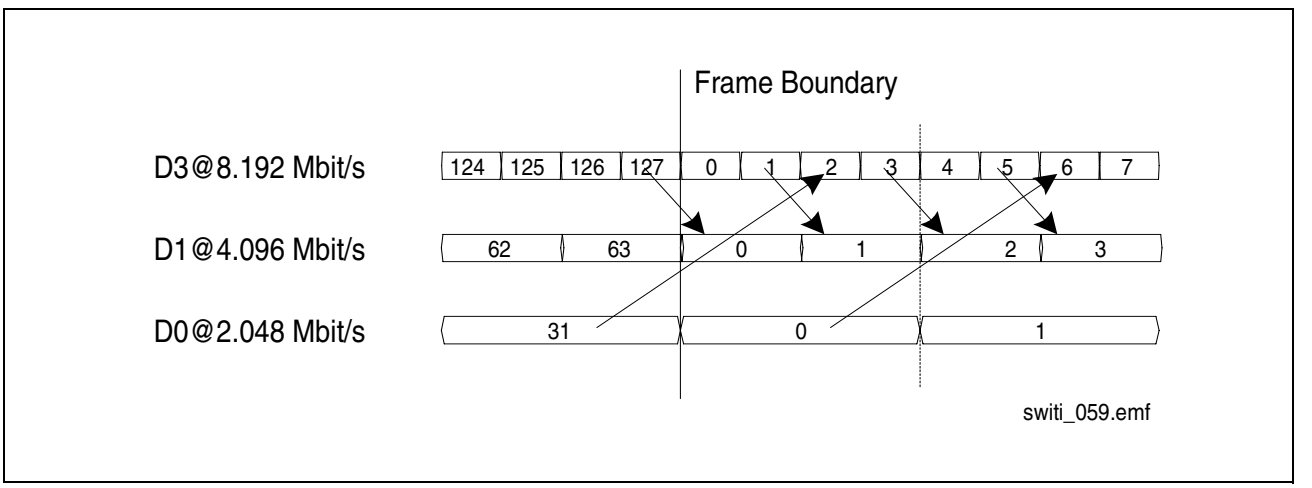


Figure 10 Example for Stream-to-Stream Switching

3.3.1.7 Message Mode

The message mode allows to send a predefined 8-bit data value in a defined time-slot on a dedicated destination port. Message mode is started or stopped via register **CCMD**. The data value to be send is predefined in register **MV**. The time-slot and the destination port is is defined in register **OTSA** and register **DPA**.

3.3.2 Parallel Mode for Local Bus

The parallel mode can be set with the 'set parallel mode' command in the configuration command register. This command set the first 8 input lines and the first 8 output lines of the local bus as parallel bus. The data rate for all lines must be 2.048 Mbit/s. If the parallel mode is enabled all included lines will be set to 2.048 Mbit/s automatically. If the parallel mode is disabled all lines will keep the data rate of 2.048 Mbit/s until a new data rate will be programmed for the selected line.

The internal S/P-converter is bypassed. The 8 bit data stream per time-slot is distributed on 8 data lines, one bit for every line. The least significant bit is assigned to line 0 and the most significant bit is assigned to line 7. To program a connection line 0 must be used for this special parallel data port. The bit shift value must only be programmed for port 0 and this value will be assigned to the other 7 ports automatically. The initialize sequence is described in **Chapter 6**. The switching data handling is the same as the data handling for constant delay or minimum delay mode. A timing diagram is provided in the timing diagram chapter (see "PCM Parallel Mode Timing" on page **131**).

3.3.3 Switching Block Error Handling

The normal procedure to establish a connection is explained in **Chapter 6**. The way to program a new connection for a specific time-slot and data line is to release the connection and to program the new connection. The SWITI switching concept provides an internal error handling to detect errors in the switching chain caused by a programming error. A programming error can occur because of noises on the data lines, software errors, etc.

A programming error is defined as follows:

– if a non existing connection (minimum, constant delay, or message) will be released.
– or if a existing minimum delay connection will be established.

If a programming error or a connection memory overflow is detected the interrupt bit CON in the **IESTA2** register will be set. In this case the last connection which was tried to establish or to release is not valid. The switching mechanism is not affected and will continue with the switching process.

For debug purposes the SWITI has the capability to write out the content of the complete connection memory and data memory via the microprocessor interface. This procedure is described in **Chapter 3.3.4**.

It is recommended to track all established and connections with the specific customer application software. For debug purpose it is useful to compare the contents of the switching memory with the virtual connections in the application software.

3.3.4 Analyze Connection and Data Memory

With the special command "memory dump enable" in the connection command register (**CCMD**) it is possible to read the complete memory in a defined sequence from the **CON** register with a 8-bit µP access. This feature can be used only for analyze purposes.

The command disables the complete switching function as far as all data lines (PCM/ H.1x0) are set to high impedance. If the command is set and after the specific recovery time (200 ns) the connection chain and data memory can be read sequentially by a µP access to the **CON** register. The internal controller writes the next 8-bit memory data in the **CON** register if the µP read access is finished. That means there is a specific recovery time for the µP to the next **CON** read access.

The internal memory dump controller reads the present memory contents of the input chain memory, data memory and output chain memory. During the memory dump the internal state machine will loose the synchronization with the external frame structure. Therefore a software reset must be issued and the device must be programmed again, except the clock configuration.

Infineon Technologies provides a software driver to recalculate the chain and to recover the current connections.

For a detailed explanation of the internal structure and the software driver please refer to the application note “Connection Memory Dump”.

3.4 Clock Generator and PLL

3.4.1 General Overview

The following figure gives an overview about the clock generator with the integrated PLL.

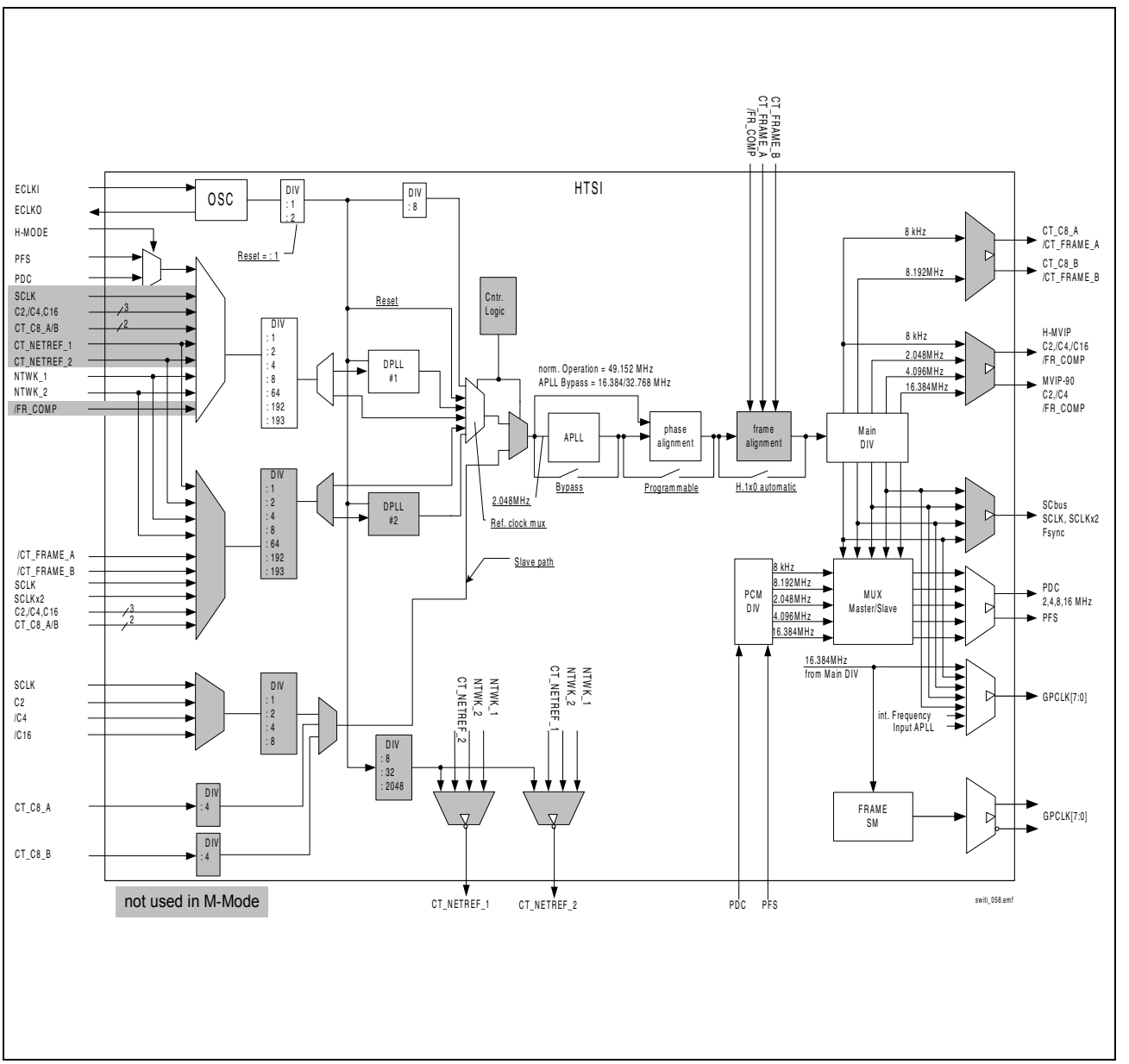


Figure 11 SWITI Clock Generator

The SWITI clock generator provides all necessary clock signals for the SWITI PCM (local bus) and H.1x0 interfaces. Since the device is a H.1x0 master capable device there are two digital PLLs which can be locked to different network reference signals. The digital PLL synchronizes the external crystal or oscillator to the selected reference clock. The digital PLL (DPLL) will be bypassed if the selected reference signal is >= 2.048 MHz. The input signal for the analog PLL (APLL) is 2.048 MHz in normal operation mode. The APLL is used for multiplying the 2.048 MHz clock into a 49.152 MHz clock and to generate all clock signals for the PCM and H.1x0, and general purpose clock signals.

The SWITI has an on-chip oscillator which allows the user to connect an external 16.384 MHz or 32.768 MHz crystal. Instead of using the crystal it is possible to assign a 16.384 MHz, or 32.768 MHz oscillator to the ECLKI pin.

After the power-on or hardware reset the APLL is bypassed. The APLL will be synchronized (after approximately 750 µs) to the external crystal or external oscillator if the command 'set external frequency' is set. This command must be used otherwise the internal working frequency is equal to the external input frequency and the SWITI will not work properly. If the APLL is locked the status bit 'APLL' in the **ISTA1** register will be set.

Note: After the reset it is necessary to program the correct crystal or oscillator value as first programming step. Otherwise the operation frequency for the SWITI is not correct.

3.4.2 Analog PLL (APLL)

Features

- Low cycle-to-cycle jitter < 1 ns
- Natural frequency f_g = 15 kHz
- Damping factor = 0.7
- Input Frequency = 2.048 MHz in any case
- Output Frequency = 49.152 MHz, duty-cycle = 50 %
- Rule behavior = change of output frequency in range of 0 - ±10% in response to changes of input frequency
- phase slope of output frequency equal to phase slope of input frequency

Note: It is necessary to provide a "noise free" analog power (V_{DDA}/V_{SSA}) to reduce the internal jitter of the APLL. These pins must be decoupled from the digital power (VDD/VSS), see also the available Application Note "Layout Notes".

3.4.2.1 Functional Description

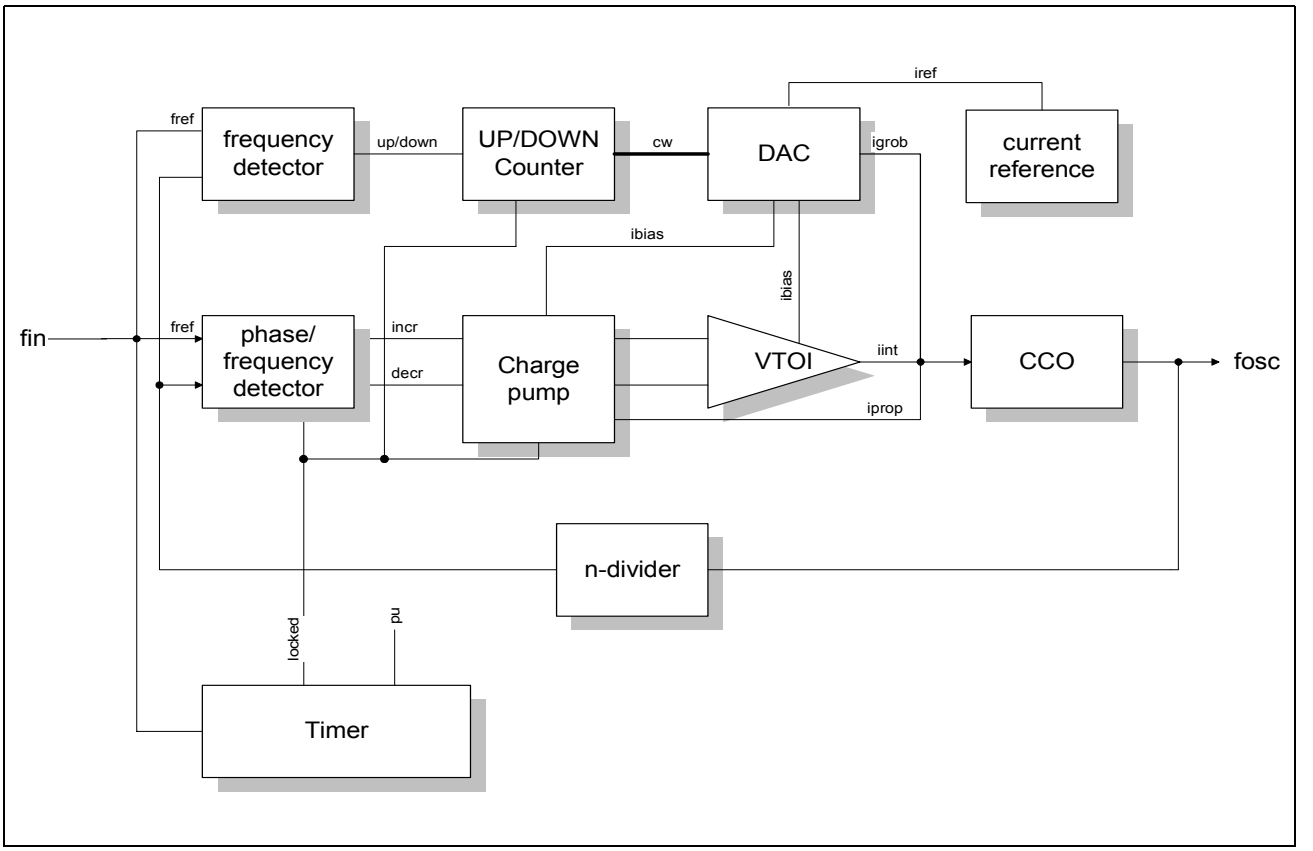


Figure 12 Block Diagram of APLL

The value of the output frequency depends of the programming of the n-divider. The chosen output frequency for the SWITI is 49.152 MHz and the input frequency is 2.048 MHz.

The macro consists of a digital and an analog PLL which are working together. During start-up only the digital one is enabled and makes a coarse adjustment, so that the technology dependency of the circuit is compensated. Afterwards the digital PLL is disabled again and the analog one is switched on for normal operation.

The digital PLL is of first order and consists of a frequency detector (FD), an up/down counter, a digital-to-analog converter (DAC) and a current controlled oscillator (CCO). The FD detects any frequency difference between the reference clock (fref: input clock fin = 2.048 MHz) and the divided oscillator clock. The output signal controls the counter. If the reference frequency is higher than the divided oscillator frequency the counter is increased. The counter output drives a current steering DAC which controls the input current of the internal oscillator. Its current rises and the output frequency increases until both frequencies are equal. The digital PLL is enabled after reset or power up and is disabled after 750 µs (lock time of PLL). The counter keeps its value and the DAC output current **irough** is constant until the digital PLL is reseted.

The second order analog PLL consists of a phase/frequency detector (PFD), a charge pump (CP), a loop filter and the CCO. The PFD which is sensitive to the rising edge detects any phase or frequency difference between the input clock **(fref**) and the divided output clock **(feedback**) and generates a control signal proportional to the phase difference. The output signals **up** and **down** cause the charge pump to modulate the amount of charge in the low pass filter (VTOI) for the integral part **(iint**) and to feed current into the CCO for the proportional part **(iprop**). With these two currents and the DAC output **irough** the CCO is controlled. If **feedback** is leading **fre**f, the oscillator is too fast. The **down** signal is activated and the CP subtracts some current **ipro**p. When **fref** is in phase with the **feedback** the PLL will hold the control current at that level and phase lock will be achieved. Thus through this negative feedback arrangement, the PLL causes the **feedback** and **fref** signals to be equal with minimum phase offset. If the analog PLL becomes unstable, a signal **pllko** is generated which resets the digital PLL.

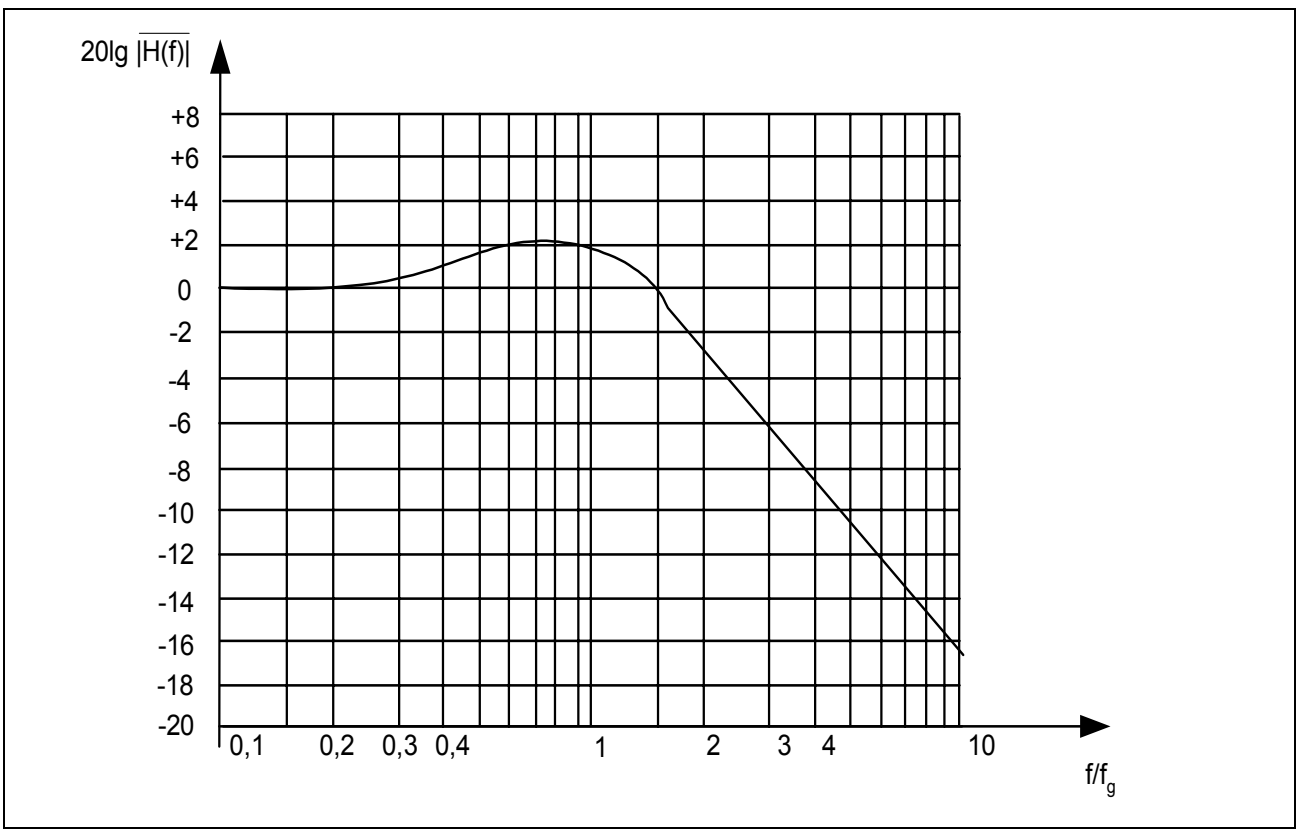


Figure 13 APLL - Jitter Transfer Function

3.4.2.2 Jitter-Transfer-Function

Jitter transfers or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

Figure 13 shows the jitter transfer function of the SWITI device. The cutoff frequency of the integrated low pass filter is f_g = 15 kHz.

3.4.3 Master-Slave Selection

For a proper working PLL and clock fallback mechanism it is necessary to select the part as master or slave with the "select master/slave" command in the **CMD1** register. If the M-Mode is used it is not allowed ot use the special master command. As described in **Chapter 3.4.6** this command must be used to finish the clock generator configuration and/or to finish the H.1x0 fallback configuration. The PLL reference source can be selected with the "PLL Primary Reference for Master Selection" command, or with the "PLL Source Selection" command.

3.4.4 Phase Alignment

If the phase alignment function is enabled all PLL output signals and the main divider are edge synchronized with the PLL clock input. If the selected reference signal is less than 2.048 MHz the edge synchronization resolution depends on the selected external crystal/oscillator frequency. If the phase alignment function is disabled the PLL output frequency (49.152 MHz) is edge synchronized with the PLL input frequency and the main divider output frequencies are edge synchronized with PLL output frequency.

An example of phase alignment functionality is shown in **Figure 14**.

Phase alignment is required to keep the output signals in phase relative to the input signals (e.g. C8A relative to C8B). After reset phase alignment is automatically activated in secondary master and slave mode and turned off in master mode.

Note: The phase alignment should be disabled for all reference frequencies < 2.048 MHz.

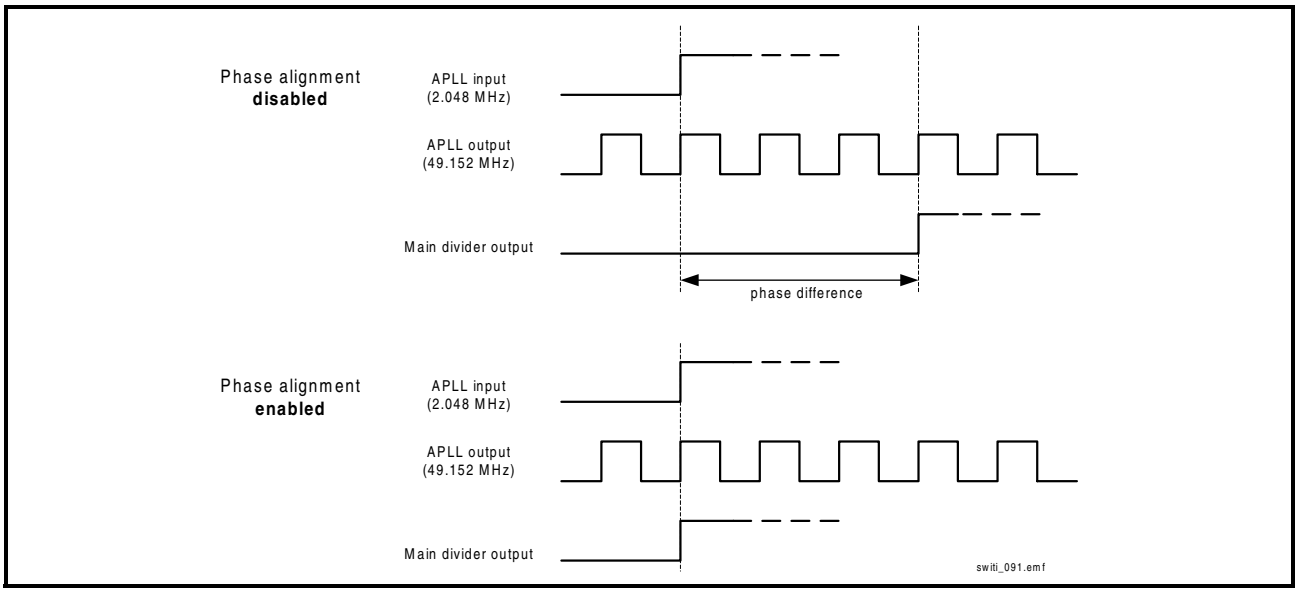


Figure 14 Example of Phase Alignment

3.4.5 PLL Synchronization

As shown in **Figure 11** there are several possibilities to synchronize the PLLs. For the synchronization it is necessary to distinguish between the different operational modes (H.1x0 with PCM, only PCM). The PLL needs approximately 750 µs to lock to the selected reference frequency. For the frame synchronization the clocking unit needs additionally two frames to synchronize the incoming frame with the generated frame. This frame synchronization will be enabled if the device is configured as H.1x0 slave, H.1x0 secondary master, and compatibility bus slave.

3.4.5.1 PLL Synchronization H-Mode

The following operational modes apply to the HTSI H-Mode.

– H.1x0 Master and PCM Master

In this mode the reference frequency must be selected by software according the H.1x0 specification. The H.1x0 and PCM clock synchronization is guaranteed by the fact, that the synchronized 2.048 MHz clock, generated from one of the digital PLLs, is used as input clock for the analog PLL, used for the generation of all necessary clocks. If the reference frequency is equal or higher than 2.048 MHz the digital PLL is bypassed and the reference signal is connected with analog PLL. The beginning of the PCM frame is equal with the beginning of the H.1x0 frame.

– H.1x0 Slave and PCM Master

For the H.1x0 Slave mode both digital PLLs are bypassed and the input signal for the analog PLL comes from one of the selected slave path clock sources. The PCM clock signals are synchronized to the H.1x0 selected input reference clock signal and there isn't a phase difference between the signals. The beginning of the PCM frame is equal with the beginning of the H.1x0 frame. This is guaranteed by the fact, that the related frame signal to the selected clock signal is used for the frame synchronization.

– H.1x0 Master and PCM Slave

This mode is not allowed, since the PCM frame start is not synchronized with the H.1x0 frame start.

– H.1x0 Slave and PCM Slave

The PDC and PFS signals must be equal to the highest selected PCM datarate and must be sourced. The incoming PCM clock/frame signals must be derived from the same clocking source as the H.1x0 clocks or from a master with the same reference clock as the H.1x0 master. Since there isn't a elasticity switching buffer in the SWITI the incoming clock must be synchronized, must have the same phase and the H.1x0 frame start must be equal to the PCM frame start.

3.4.5.2 PLL Synchronization M-Mode

The PLL reference source can be selected from the primary reference master source (PFS, PDC, NTWK_1/_2). If the selected reference signal is less than 2.048 MHz the main digital PLL is used to synchronize the analog PLL. The digital PLL is sourced from the external oscillator, or crystal. In this case the analog PLL output frequency tolerance is equal to the external oscillator/crystal frequency tolerance.

Furthermore the analog PLL can be sourced directly from the external oscillator, or crystal, or from the PDC input. All generated output frequencies will have the same tolerance as the selected input frequency.

3.4.6 PLL Error Handling

The SWITI in H-mode has an integrated control logic to detect possible PLL configuration errors. If one of the errors (see below) occurred the clock fallback mechanism and the PLL functionality is not guaranteed. The control mechanism starts with the command 'Set as H.1x0 Master/Slave (HTSI H-Mode)' in the **CMD1** register. That means that the mentioned command finished the clock generator configuration.

As shown in **Figure 11** there is a cntr. logic for the two APLL multiplexer implemented. The first multiplexer is used to select one reference source for the master mode and the second multiplexer is used to decide between the slave or master path. The main task for this control logic is to make sure that the input signal for the APLL derives from the internal oscillator (external oscillator) after the reset.

The second task is to control the input signal for the APLL during the normal operation and to decide whether the programmed combination is correct. If one of the following combinations occur, the control logic selects the internal oscillator, resets the complete clock generator configuration and an interrupt will be generated (-> wrong PLL source programming).

Configuration errors which will be detected:

HTSI H-Mode Master configuration

– PLL2 source was selected (slave path)

HTSI H-Mode Slave configuration

– PLL main **or** secondary master reference was selected

Furthermore the fallback state machine controls the logic to multiplex the necessary signal for the fallback mechanism.

Since there are redundant paths for the reference clock and also for the slave clocks the clock fallback time depends only on the multiplexer delay time.

3.4.7 Clock Fallback

This chapter must be read if the SWITI is used as H.1x0 device (H-mode).

3.4.7.1 Clock Signal Monitoring

To support the clock fallback mechanism the SWITI has the capability to monitor the CT_CA (CT_C8_A, $\overline{\text{CT\_FRAME\_A}}$), CT_CB (CT_C8_B, $\overline{\text{CT\_FRAME\_B}}$) clocks additional with the selected primary PLL reference, and to monitor the interoperability clock signals. The SWITI reports every clock failure to the host with a interrupt if it is not masked. If the interrupt is masked the status of the clock errors can be read from the **IESTA1** and **IESTA2** registers (polling). The H.1x0 clock signal monitoring will start immediately after programming a new reference clock. The process is finished with the command 'master slave' from the **CMD1** register.

The following monitoring requirements for H.1x0 must be meet:

– A received rising edge of CT_C8_A/B (both signals must controlled independently) doesn't arrive within 35ns of the expected edge.

or

– There are not exactly 1024 clock periods per frame.

If one of these requirements are not meet an interrupt will be generated (if not masked) to inform the system software that one of the clock circuits (A or B) is failed.

The following monitoring requirements for the interoperability clock signals must be meet. The $\overline{\text{FR\_COMP}}$ is monitored in conjunction with the selected primary PLL reference (master) signal or with the selected PLL source (slave).

MVIP

– A received rising edge of C2, $\overline{\text{C4}}$, or C8, or $\overline{\text{C16}}$ doesn't arrive within 40 ns of the expected edge.

or

– There are not exactly 256, or 512, or 1024, or 2048 clock periods per frame

SCbus

– A received rising edge of SCLK doesn't arrive within 40 ns of the expected edge.

or

– There are not exactly 256 (SCLK=2.048 MHz), 512, or 1024 clock periods per frame.

NTWK Signals

A received rising edge of the NTWK signal doesn't arrive within 80 ns of the expected edge.

3.4.7.2 Clock Fallback Mechanism

The clock fallback mechanism can be switched on with the special command "H.1x0 Fallback Mechanism and Clock Monitoring" and the related instruction bits. As described in the H.1x0 specification there are two different fallback path's in the fallback state machine.

The instruction "fallback from main to secondary reference (primary master)" in conjunction with the command "automatic switch back to main ref." covers the "primary NTWK link fails" path. The correct reference (main and secondary) as described in the H.1x0 specification must be programmed, e.g. NTWK or CT_NETREF.

The instruction "fallback from main to secondary reference (secondary master)" and "from A clock to B clock (Slave)" covers the "primary master clock circuit fails" path in the fallback state machine.

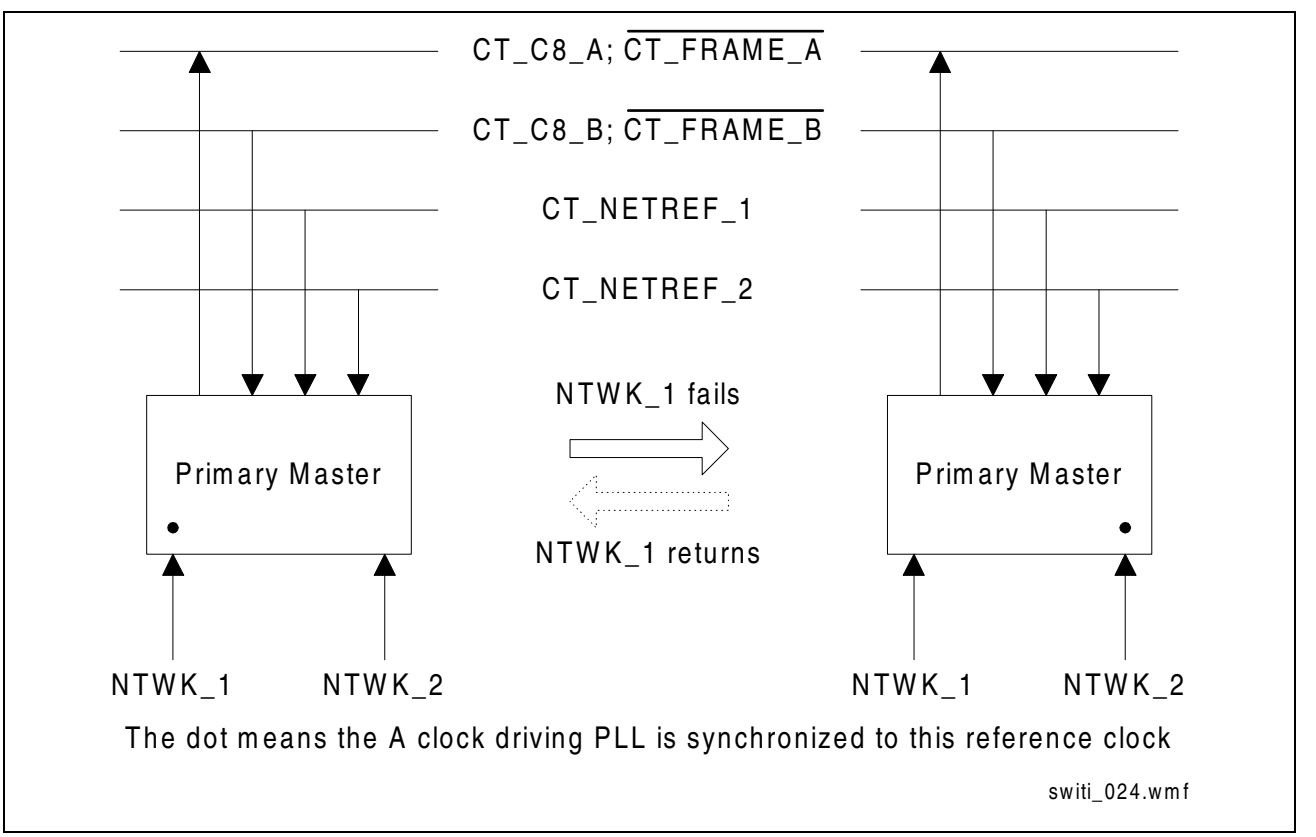


Figure 15 Clock Fallback of Primary Master

The primary master is synchronized to a reference clock (NTWK or CT_NETREF) and drives the CT_C8_A and CT_FRAME_A clocks. **Figure 15** shows a configuration example. If the primary network reference clock (NTWK_1) fails the device automatically synchronizes to the secondary network reference clock (NTWK_2). If the primary reference clock returns the device may synchronize to it again automatically or by software command (depends on configuration). If not masked the failure is reported by an interrupt.

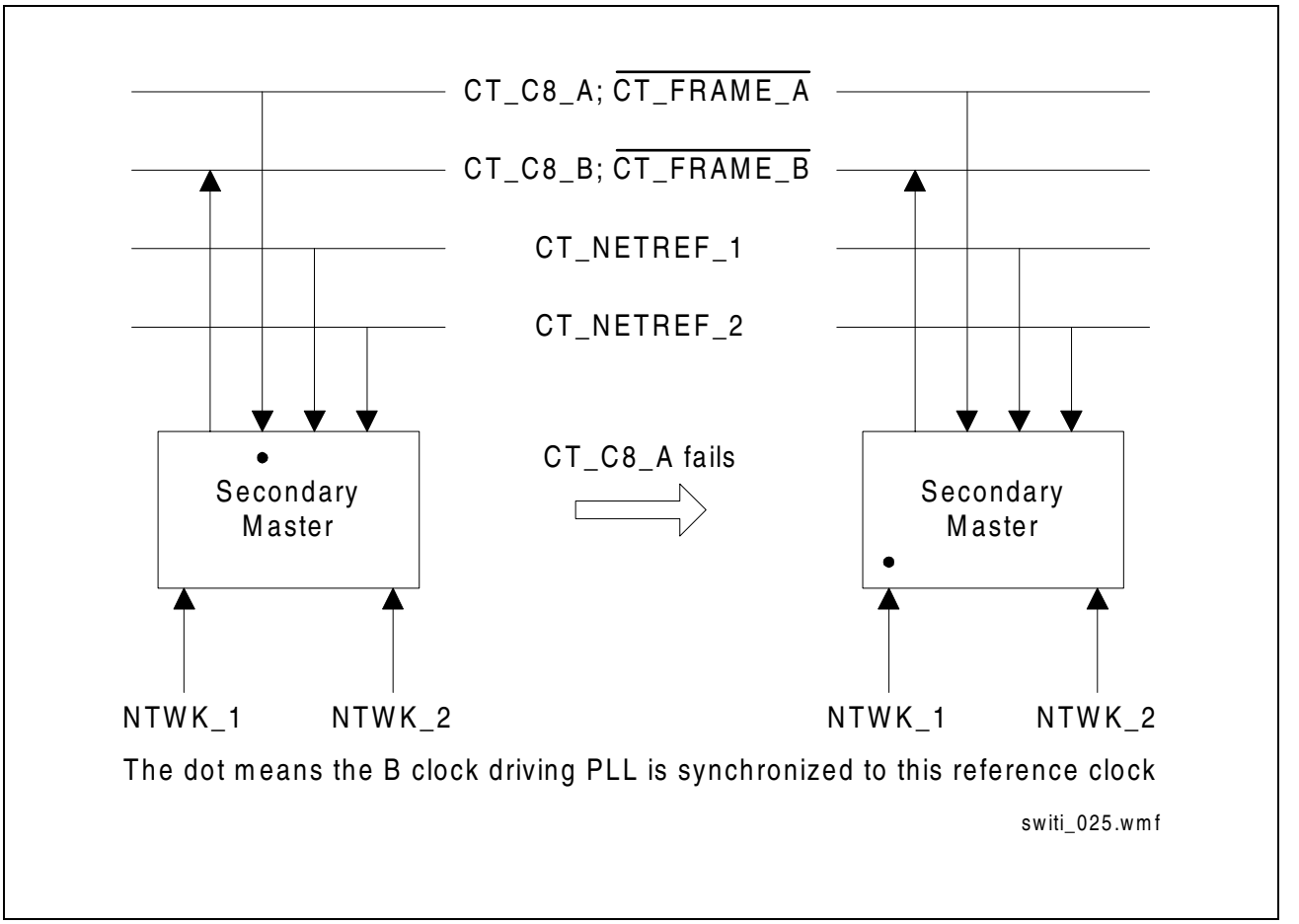


Figure 16 Clock Fallback of Secondary Master

The secondary master is synchronized to CT_C8_A, $\overline{\text{CT\_FRAME\_A}}$ and drives CT_C8_B and $\overline{\text{CT\_FRAME\_B}}$. If one of the CT_A clocks fail the device may synchronize automatically or by software command (depends on configuration) to another reference clock (NTWK or CT_NETREF). **Figure 16** shows a configuration example. If not masked the failure is reported by interrupt.

The reference and the fallback must be programmed again if the automatic fallback to the new reference was performed. Any fallback and re-programming will be performed without data loss in the device.

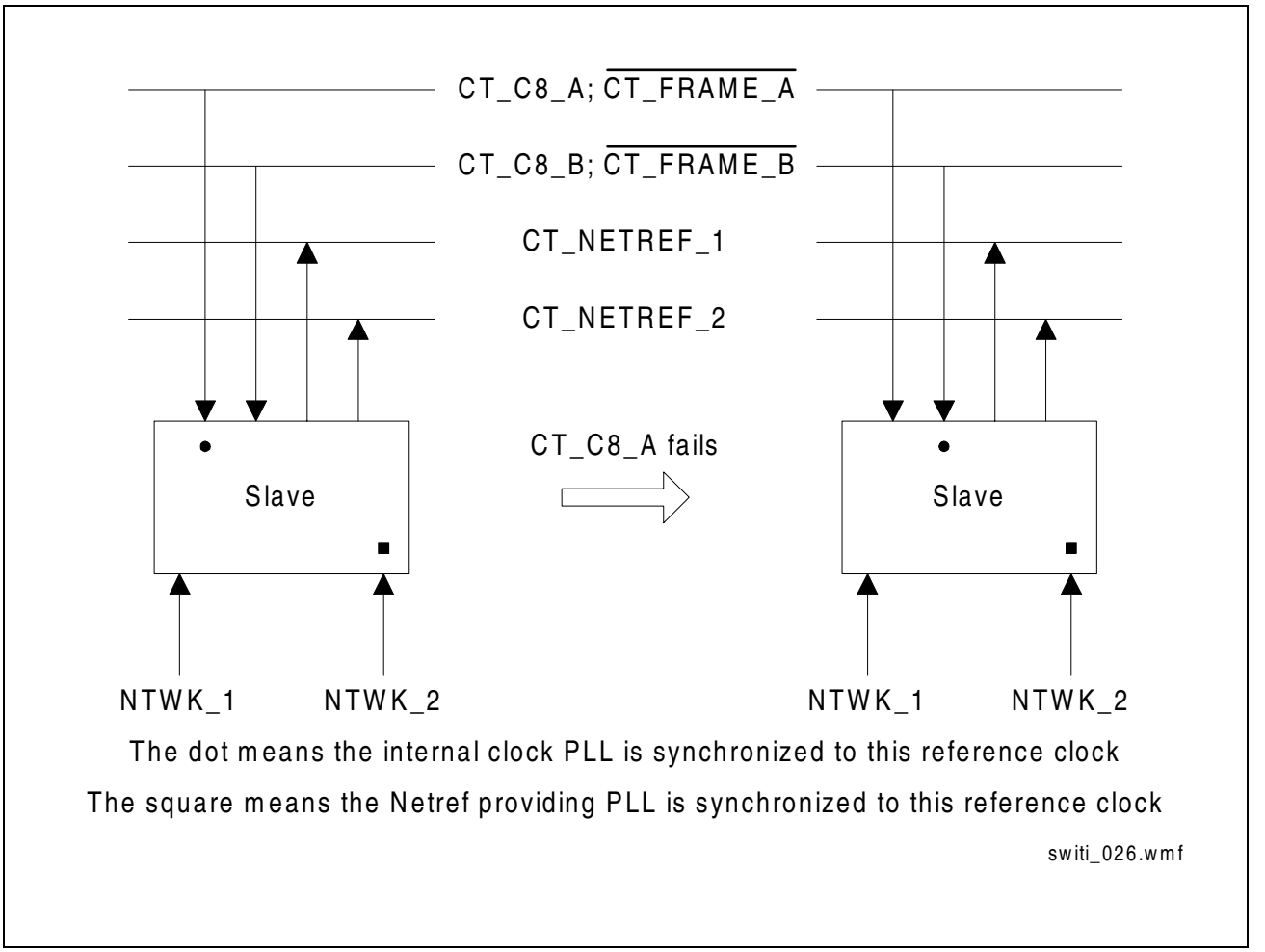


Figure 17 Clock Fallback of Slave

The slave is synchronized to CT_C8_A and $\overline{\text{CT\_FRAME\_B}}$. If the clock fails the slave synchronizes automatically or by software command to CT_C8_B and $\overline{\text{CT\_FRAME\_B}}$. If not masked the failure is reported by interrupt.

In the case of an automatic fallback to the CT_CB or CT_CA clocks the new reference must be programmed. The fallback and the re-programming of the source will be done without any data loss regarding the Stratum 4e specification. Additionally the fallback must be issued again if needed.

3.5 Loops

The loop command in the configuration command register **CMD2** provides support for automatic PCM-PCM and H.1x0-H.1x0 loops.

– PCM-PCM loop

All input lines are pad connected with the corresponding output line.

H.1x0-H.1x0 loop

The first 16 H-bus lines are pad connected with the corresponding upper 16 H-bus lines.

e.g. H0 -> H16; H1 -> H17; .....

After the loop disable command was set the lines will be set in high-impedance after approximately two frames.

3.6 Read SWITI Configuration with Indirect Register Addressing

Since the SWITI configuration can be programmed with defined instructions in the **CMD1** and **CMD2** registers it is possible to read the current configuration through the indirect access registers. The indirect addressing is started by writing one of the five read configuration commands in the **CMD2** register. The five commands can be separated in two groups, internal configuration and external line configuration. The internal configuration, e.g. clock generator, IREQ pin can be read with command "Read Configuration". The internal settings are decoded with the instruction bits I3..0. The data rate for the PCM and H.1x0 interface can be read with the "Read PCM / H.1x0 Line Configuration" commands and to get the GPCLK line configuration and the bit shift value the "Read GPCLK Configuration" and "Read Bit/Clock Shift Configuration" must be issued. The **TSV** and **CON** registers contain the required information after the internal read process is complete. The recovery time is 240 ns. To read the correct configuration data from the **TSV** register it is not allowed to use the command "Read Time-Slot Value" before the **TSV** register has been read.

3.7 Power-On and Reset Behavior

3.7.1 Hardware Reset

There are three independent low active reset pins: $\overline{\text{RESET}}$, $\overline{\text{CT\_RESET}}$ and $\overline{\text{TRST}}$.

If the $\overline{\text{RESET}}$ or $\overline{\text{CT\_RESET}}$ (in conjunction with the mode pins M-Mode and H.110 Mode) pin is activated, it immediately places all outputs and I/O ports into tri-state, except the ECLKO pin. After the reset process the correct external frequency must be set with the command 'Set external frequency' accordingly. This command starts the configuration process for the APLL. The APLL is locked after 750 µs. During this period the APLL is bypassed and the internal frequency is 2.048 MHz. If the APLL is locked the internal frequency will be 49.152 MHz.

Individual output sections must be enabled by setting the command in the configuration command register **CMD1**, or **CMD2**. Internally all state machines, counters and registers are cleared and set to their defined reset value. The H.110 controller is in the reset state and all H.110 I/O pins are tri-stated as long as the $\overline{\text{CT\_RESET}}$ pin is asserted. (see "CT_RESET" on page **48**)

The $\overline{\text{RESET}}$ and $\overline{\text{CT\_RESET}}$ pins don't control the boundary scan register and TAP-controller. If the $\overline{\text{TRST}}$ pin is asserted the TAP-controller will go into the Test-Logic-Reset state and all boundary scan elements are bypassed. All outputs and I/O-pins are controlled by the core logic and are tristated according to the programmed functionality or the core reset condition (pin $\overline{\text{RESET}}$).

The hardware reset must be issued for a minimum of 1 µs, for more details please refer to the chapter **"Hardware Reset Timing" on Page 146**.

3.7.2 Software Reset

The software reset is accomplished by setting the 'Set Software Reset' command in the **CMD2** register. The software reset clears the complete device except the clocking unit and the temporary microprocessor registers (e.g. **CMD1**).

The software reset can be deactivated with the 'Set Software Reset' command.

During software reset the microprocessor interface doesn't accept any other commands for a minimum of 1 µs.

4 Description of Interfaces

4.1 Local Bus Interface (PCM)

The local bus is a PCM interface consisting of input and output data lines (IN, OUT), a PCM data clock PDC and a frame synchronization signal PFS.

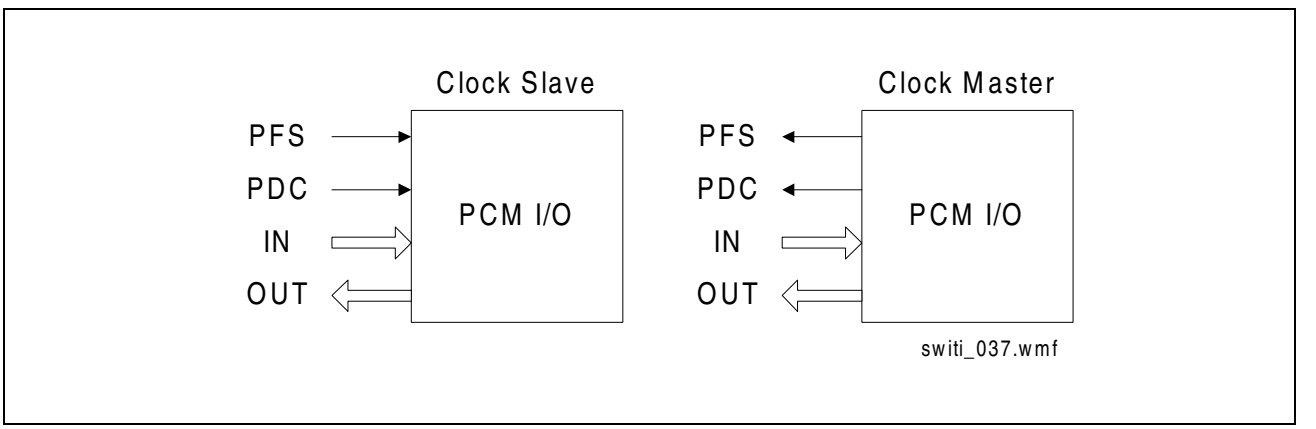


Figure 18 PCM Interface Configurations

The **PFS Frame Sync** is a 8 kHz signal and delimiting the frame. This input signal is used by the SWITI to determine the start of a frame. A frame is divided into 8-bit wide time-slots. The amount of time-slots within a frame depends on the selected data rate of PDC which can be 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, 16.384 Mbit/s. The PFS input has a Schmitt-Trigger characteristic.

The **PDC Data Clock** input supply the SWITI with a data clock. It can be operated with 2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz data rate clock depending on the selected **highest** data mode. The PDC clock signal must be equal or higher as the highest data rate. The PDC input has a Schmitt-Trigger characteristic.

A clock slave **must** receive PFS and PDC whereas a clock master drives these signals. To enable or disable the signals for the clock master the command ’PCM Clock Input/ Output Selection’ must be issued.

The time-slots are transmitted and received via 16 input and 16 output lines **(IN[15:0], OUT[15:0])**. The input lines have a Schmitt-Trigger characteristic. The output lines have tristate outputs with push-pull characteristic. For every time-slot not participating to a connection the output is high impedance.

With the special command "Local Bus (PCM) Standby" in the **CMD2** register it is possible to set all PCM lines in a high impedance state during the normal operation mode. All PCM lines are in high impedance state after the reset process and must be enabled with the "Local Bus (PCM) Standby" command. All lines which are not participating on a switching operation are in high impedance state and the time-slot information on the input lines are discarded automatically.

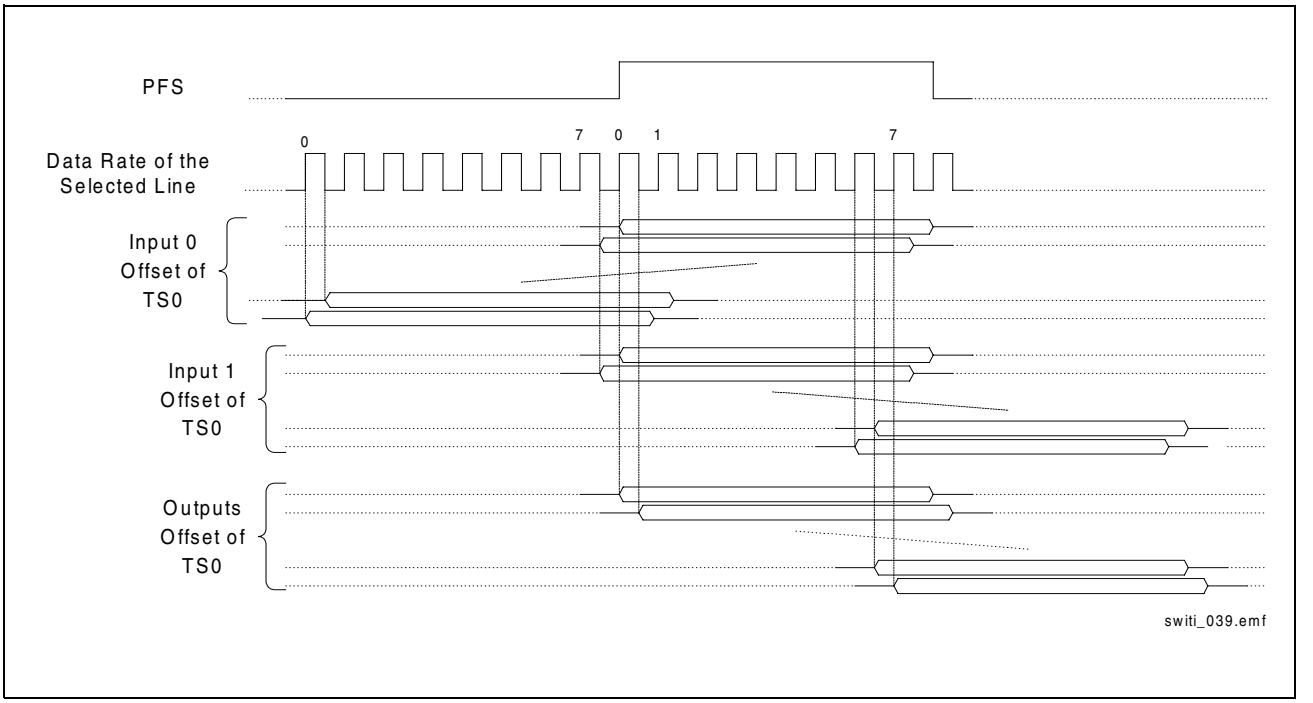


Figure 19 PCM Bit Shifting

For **each** PCM input line the offset of time-slot zero can be adjusted in a range from 0 to 7 bit in half clock resolution before or after the PFS rising edge. For **all** output lines the offset of time-slot zero can be adjusted in a range from 0 to 7 bit in half clock resolution after the PFS rising edge.

The resolution depends on the selected data rate that means the resolution doesn't depend on the PDC signal.

After the reset process the bit shift is disabled for all lines. That means the time-slot 0 starts with the rising edge of PFS. All input data will be sampled with falling edge of the selected data rate and the output data are valid with the rising edge of the selected data rate.

4.2 H-Bus Interface

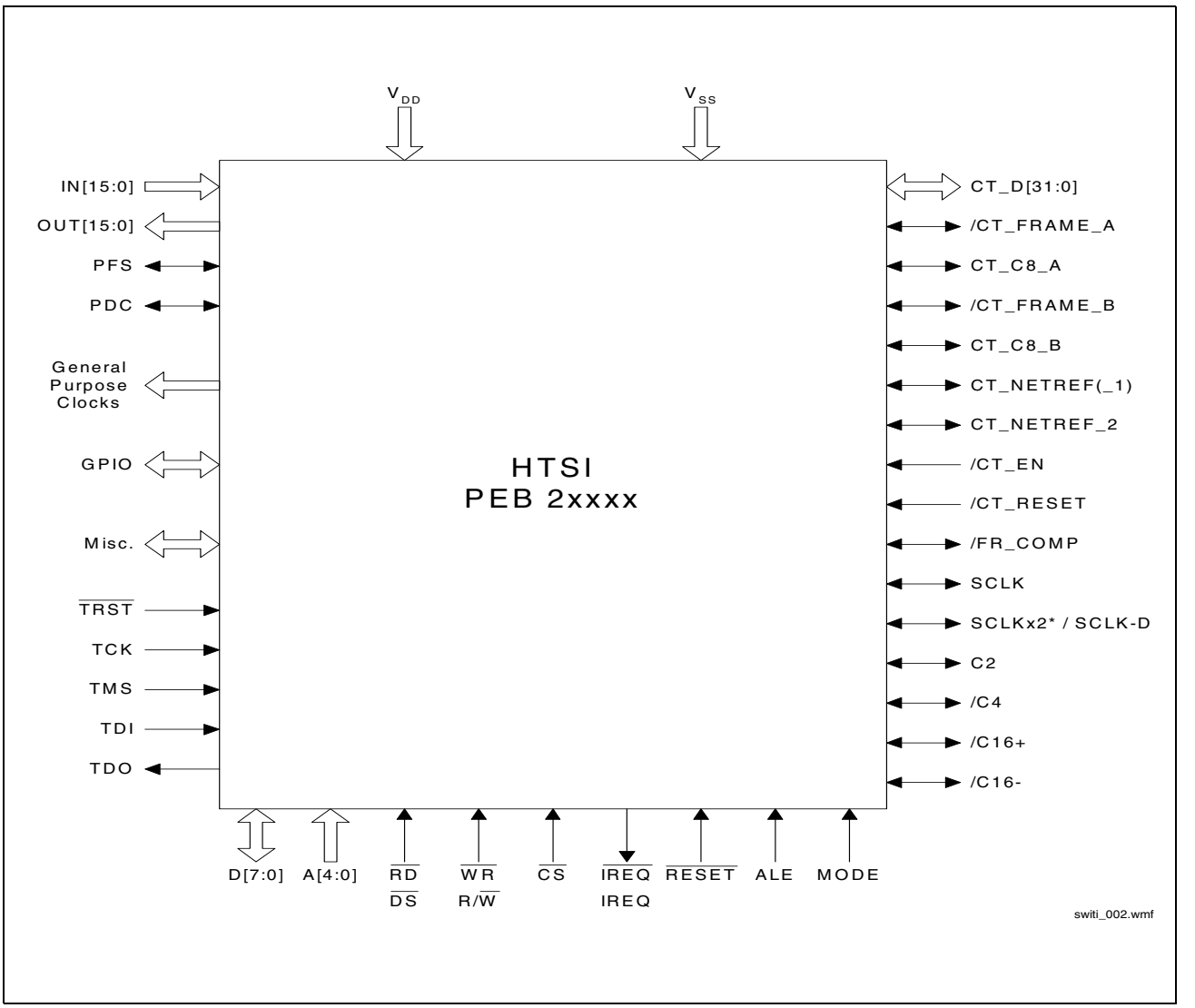


Figure 20 H-Bus Interface in H.100 Mode

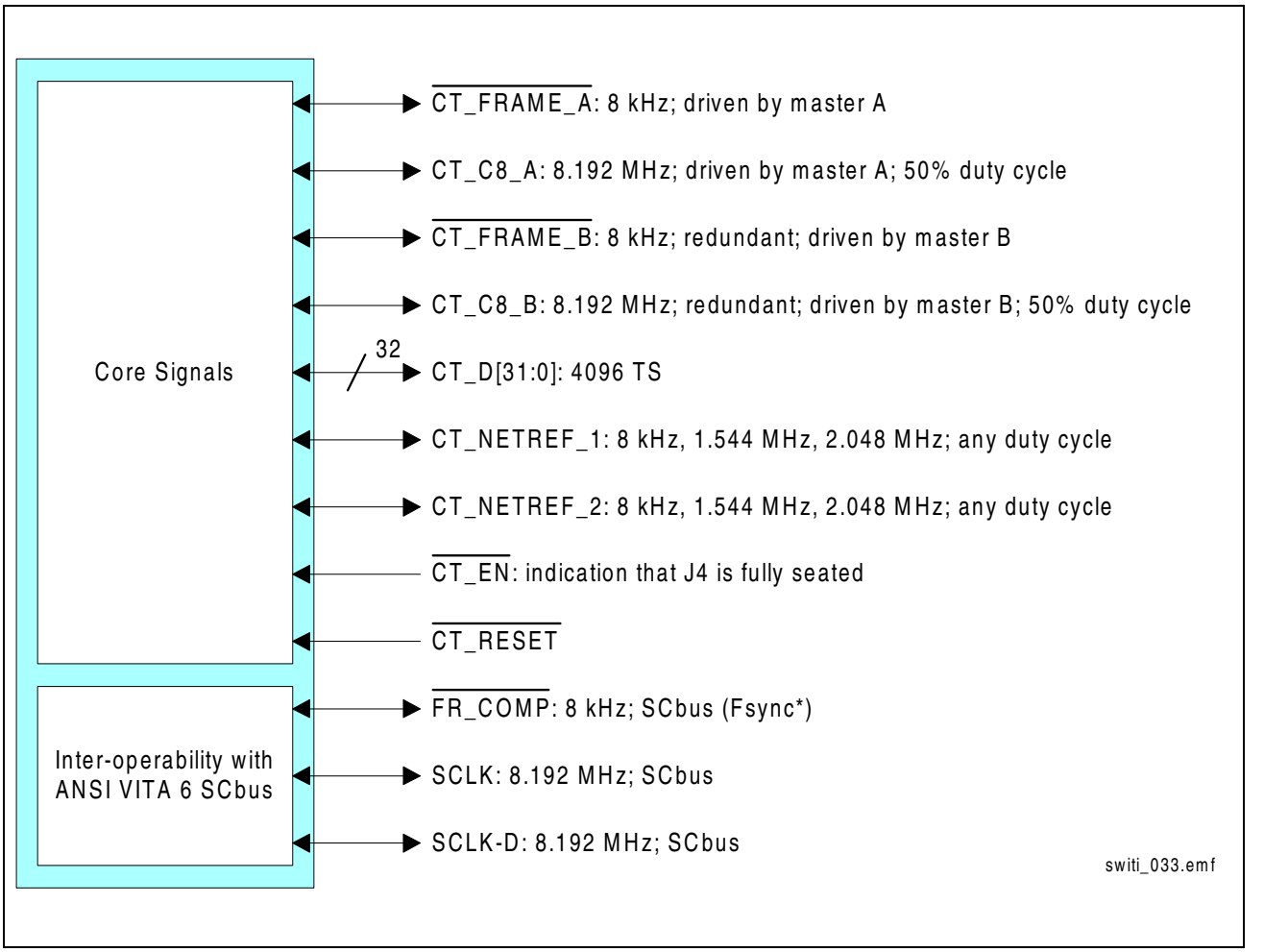


Figure 21 H-Bus Interface in H.110 Mode

Note: The frequency of SCLK in H.110 mode is 8.192 MHz only.

4.2.1 CT_C8(A/B) and CT_FRAME(A/B)

The functional timing relationship of the CT Bus clocks can CT_FRAME can be found in the chapter **“H-Bus and PCM (Local Bus) Frame Structure” on page 132**.

The **CT_FRAME** is a 8 kHz signal and delimiting the frame. The negative pulse, nominally 122 ns wide marks the beginning of the first bit of the first time-slot.

The **CT_C8** is the 8.192 MHz bit clock. The duty cycle of this signal is nominally 50%.

A H.1x0 slave **must** receive CT_C8 and CT_FRAME whereas a clock master drives these signals.

4.2.2 Dataports

There are 32 bidirectional pins available for accessing the H-bus. The frame structure is shown in **Chapter 7.3**. For every pin there is a tri-state controller. The CT_EN signal enables the tri-state controller for the H.110 data lines. With the special command "PCM

and H.1x0 Standby" in the **CMD2** register it is possible to set all H.1x0 lines in a high impedance state during the normal operation mode. All H.1x0 lines are in high impedance state after the reset process and must be enabled with the "PCM and H.1x0 Standby" command. All lines which are not participating on a switching operation are in high impedance state.

The default data rate is 8.192 Mbit/s in accordance to the H.100/H.110 specification. With the configuration command register it is possible to select a individual data rate from 2.048 Mbit/s, 4.096 Mbit/s, and 8.192 Mbit/s in accordance to support the interoperabilitiy busses.

4.2.3 $\overline{\text{CT\_EN}}$

The $\overline{\text{CT\_EN}}$ signal must be implemented in an identical manner to the implementation of the BD_SEL# signal as specified in the PICMG 2.1 CompactPCI Hot Swap specification by connecting $\overline{\text{CT\_EN}}$ to a logic high (de-asserted) through a 1.2K ±5% resistor or current source equivalent. The $\overline{\text{CT\_EN}}$ signal indicates that a PCI board is fully seated. The H.110 interface logic is enabled if the $\overline{\text{CT\_EN}}$ signal is active (logic low level enables all H.110 ports, PCM ports, and clock signals).

4.2.4 $\overline{\text{CT\_RESET}}$

The CT_RESET must be functionality and electrically equivalent to the CompactPCI signal RST#. The device must respond to the $\overline{\text{CT\_RESET}}$ signal when it is asserted. All H.110 outputs and I/Os are high impedance until the $\overline{\text{CT\_RESET}}$ is released as well as the related PCM outputs and I/Os. No clocking signal can influence the internal logic during the reset state. All internal state machines and counters are in a defined reset state after the $\overline{\text{CT\_RESET}}$ signal is released and the connection memory is in the reset state. After the $\overline{\text{CT\_RESET}}$ signal is released the device has to be configured with the configuration command register 1 and 2 (**CMD1**, **CMD2**).

The $\overline{\text{RESET}}$ and $\overline{\text{CT\_RESET}}$ (in conjunction with the mode pins M-Mode and H.110 Mode) signals are logical or connected.

4.2.5 H-MVIP $\overline{\text{C16}}$ Signals

The differential signal is driven by the clock master and used to read and write bits on the serial data lines. Time-slot boundaries align with the falling edge of $\overline{\text{C16+}}$. The $\overline{\text{C16}}$ signal is differential. The SWITI doesn't have a integrated differential receiver/ transceiver with the required thresholds of the EIA standard RS-485. Nevertheless the differential $\overline{\text{C16+}}$, $\overline{\text{C16-}}$ input signals are logical decoded to one internal /C16 signal if the SWITI is configured as clock slave. The $\overline{\text{C16-}}$ is the inverted $\overline{\text{C16+}}$ signal if the SWITI shall generate the $\overline{\text{C16+}}$, $\overline{\text{C16-}}$ signals.

4.3 Data Rate

The SWITI provides the programming of data rates on a per line basis for the local bus as well as for the H.100/H.110 bus. To support the H.100/H.110 bus and the interoperability bus systems all 32 H.100/H.110 data lines can operate with 2.048 MHz, 4.096 MHz, and 8.192 MHz independently.

The following table shows the possible data rates for the different lines.

Table 11 Data Rates for Local and H-Bus

	PCM0..7 (IN/OUT)	PCM8..15 (IN/OUT)	PCM16..31 (IN/OUT)	H0..31
HTSI-M	2/4/8/16 Mbit/s	2/4/8 Mbit/s	2/4/8/16 Mbit/s	x
HTSI-H	2/4/8/16 Mbit/s	2/4/8 Mbit/s	x	2/4/8 Mbit/s

All local bus lines can operate with 2.048 MHz, 4.096 MHz, and 8.192 MHz independently and up to 24 local bus lines for the HTSI in M-mode or 8 local bus lines for the HTSI in H-mode can operate with 16.384 MHz as well. Having 16.384 Mbit/s in any of the PCM0..7 lines, the corresponding (PCM0..7 + 8) lines will be deactivated (tri-state). Using all PCM0...7 lines with 16.384 Mbit/s all the PCM8...15 will be then deactivated.

The input and output lines are independent of each other, i.e. for a given bus line the input and the output lines can be programmed with different data rates.

For the HTSI the maximum aggregate data rate supported at the input and output bus lines is 393.216 Mbit/s, (e.g. 24 lines x 16.384 Mbit/s per line = 393.216 Mbit/s, as input and/or output). The following tables show some possible configurations for the local and H-bus lines, with the highest data rate allowed.

Table 12 Maximum possible data rates for HTSI in M-mode

PCM0..7 (IN/OUT)	PCM8..15 (IN/OUT)	PCM16..31 (IN/OUT)	H0..31
8 x 16.384 Mbit/s	x	16 x 16.384 Mbit/s	x
8 x 16.384 Mbit/s	x	16 x 8.192 Mbit/s	x
8 x 8.192 Mbit/s	8 x 8.192 Mbit/s	16 x 16.384 Mbit/s	x
8 x 8.192 Mbit/s	8 x 8.192 Mbit/s	16 x 8.192 Mbit/s	x

Table 13 Maximum possible data rates for HTSI in H-mode

PCM0..7 (IN/OUT)	PCM8..15 (IN/OUT)	PCM16..31 (IN/OUT)	H0..31
8 x 16.384 Mbit/s	x	x	32 x 8.192 Mbit/s
8 x 8.192 Mbit/s	8 x 8.192 Mbit/s	x	32 x 8.192 Mbit/s

*Note: **Table 12** and **Table 13** show all possibile combinations with only 8.192 Mbit/s and/or 16.384 Mbit/s for all available bus lines*

4.4 Microprocessor Interface

A standard 8-bit multiplexed or non-multiplexed µP interface is provided, compatible to Intel/Siemens (e.g. 80386EX, C166) and Motorola (e.g. 68040, 68340, 68360, 801) bus systems. If the GPIO port is not needed it can be used to provide a 16-bit µP interface. The 16-bit mode is determined according to MODE16 input pin.

MODE16 = ’0’ -> 8-bit interface

MODE16 = ’1’ -> 16-bit interface

This chapter describes how to configure the µP interface to each mode.

4.4.1 Intel/Siemens or Motorola Mode

The Intel/Siemens or Motorola mode for the µP interface can be configured during the hardware reset process in conjunction with the ALE pin.

– ALE permanently driven to ’low’ => Motorola mode
– ALE permanently driven to ’high’ => Intel/Siemens mode
– Edge on ALE => Intel/Siemens multiplexed mode

A falling or rising edge on ALE during the normal operation selects the multiplexed mode immediately. With the hardware reset and the tied ALE pin it is possible to return to the Motorola or Intel/Siemens mode.

4.4.2 De-multiplexed or Multiplexed Mode

In both modes, the A-bus and the D-bus are used in parallel. The A-bus should be connected to the LSBs of AD-bus, coming from the µP, also in multiplexed mode.

The next figure describes the connection to the address and data buses in the different modes.

Note: Motorola mode is used only with de-multiplexed AD bus. Intel/Siemens mode may be used with both, multiplexed or de-multiplexed AD bus.

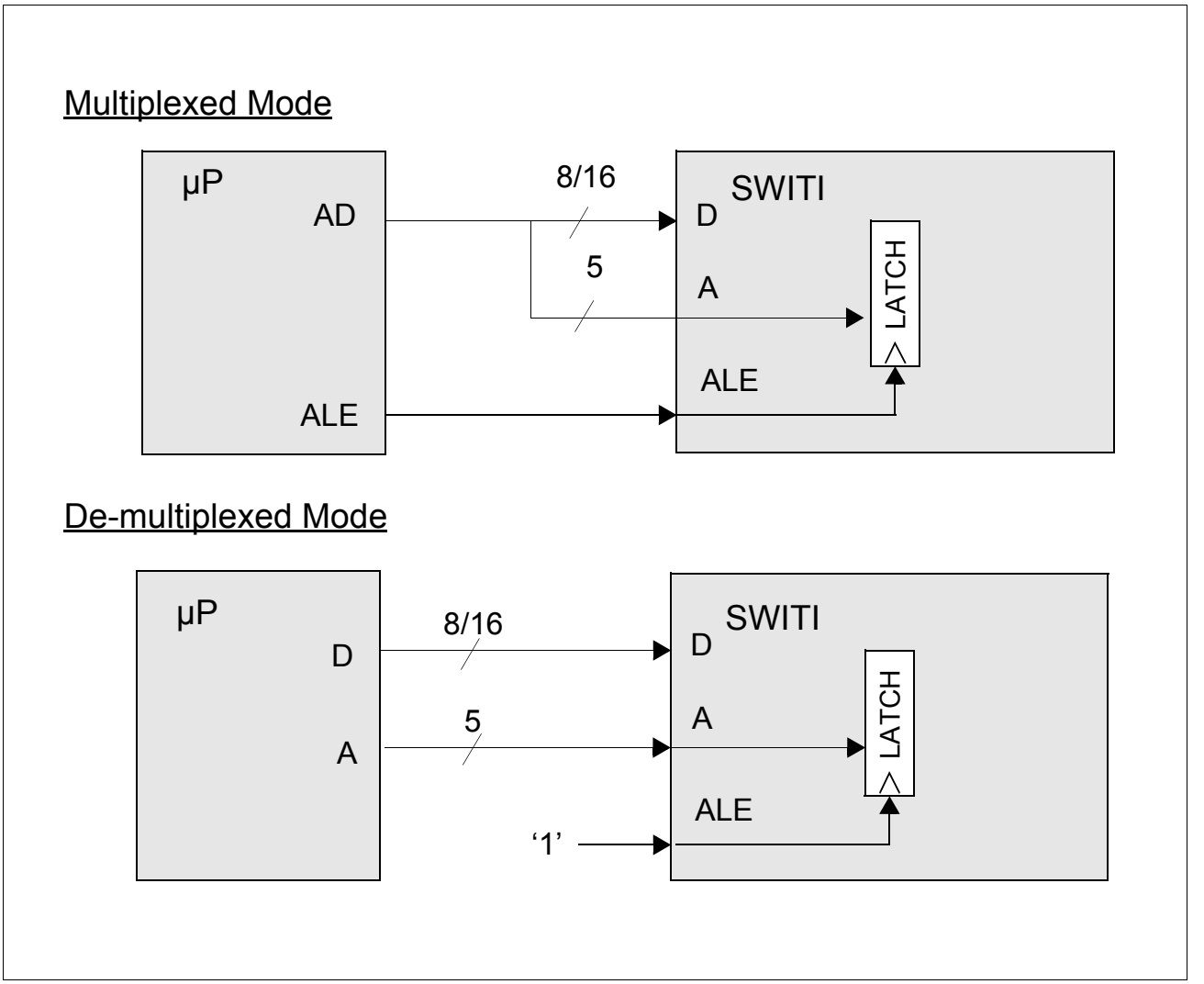


Figure 22 Multiplexed and in De-multiplexed Bus Mode

Note: In both modes only the 5 LSBs of A-bus or AD/bus are connected to the Address inputs.

4.5 General Purpose Port (GPIO)

This port consists of 8 lines each one configurable as input or output. A change on an input line may cause an interrupt (if not masked). The user has access to the port configuration and information via the appropriate registers of the µP interface.

Figure 23 shows an example.

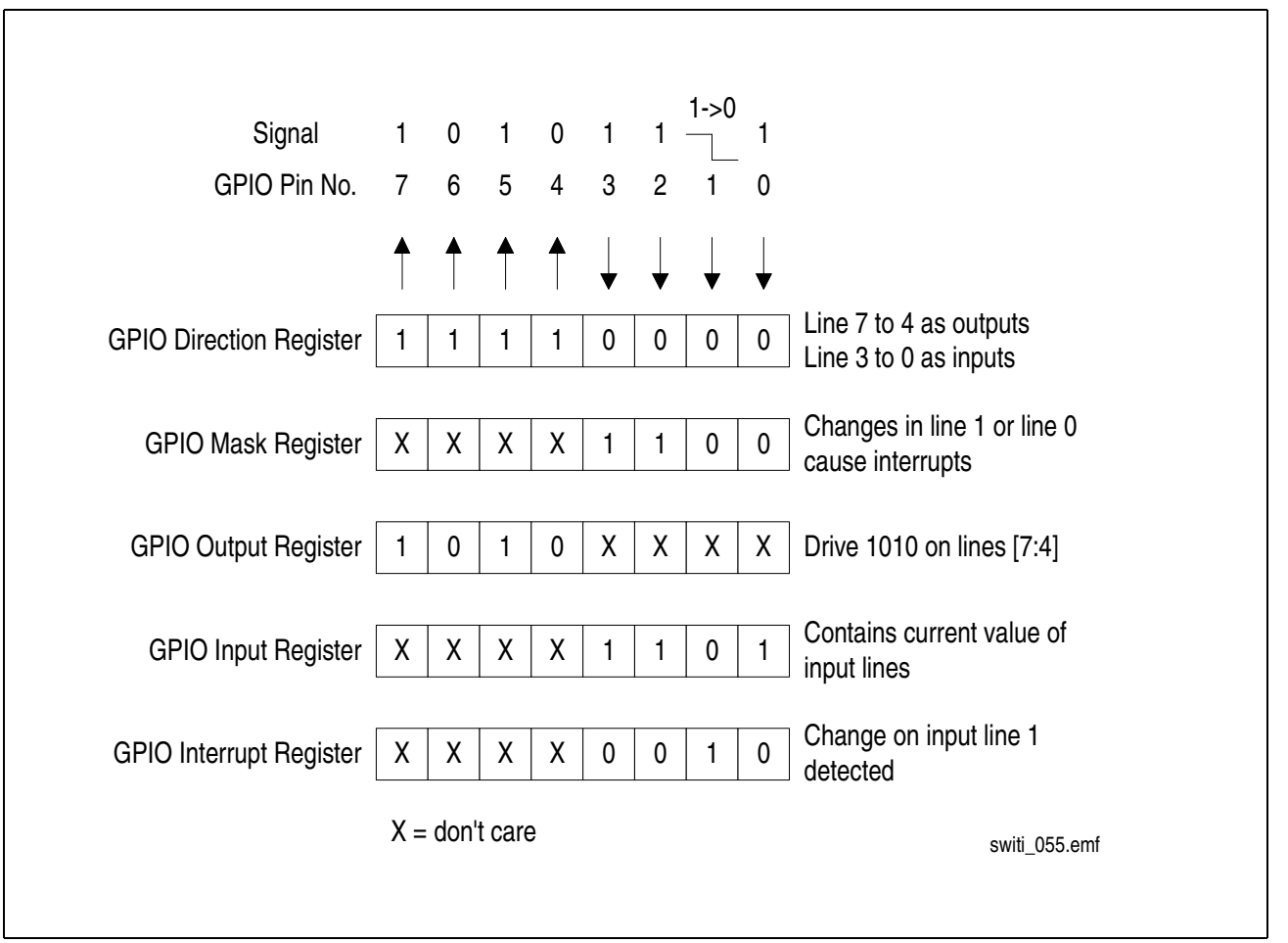


Figure 23 GPIO Port Configuration Example

4.6 General Purpose Clocks

The SWITI provides 8 general purpose clock lines. With two independent commands in the **CMD2** register the lines can be configured as frame group signals or individual clock signals. The last written command for a line is valid and controls the multiplexer.

4.6.1 Frame Group Outputs

Via 8 output lines it is possible to provide 8 different framing signals which are used for synchronization purpose. All signals have a period of 125 µs. Their offset can be programmed individually within the PFS determined frame in a resolution of 61 ns (1/ 16.384 MHz). The default start point for the offset is the beginning of a frame (rising edge of PFS and the clock signal). The start point for the offset can be shifted for a half clock cycle, that means the second start point is determined with the rising edge of PFS and the next falling edge of the clock signal (as shown in Figure 24). The high time of the signal can also be programmed in steps of 61 ns. All frame signals can be controlled as high or low active.

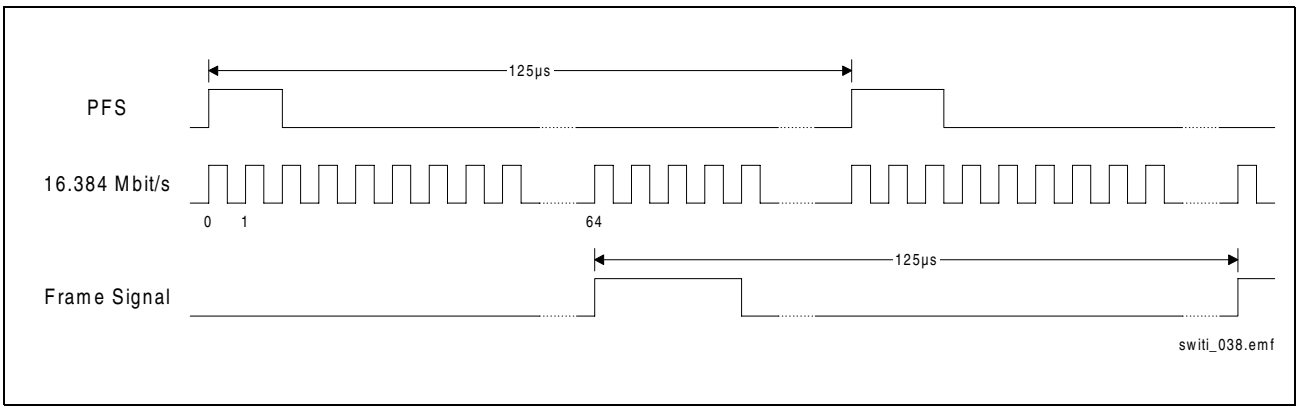


Figure 24 Frame Signal Example

Figure 24 shows an example of a frame signal beginning with the rising edge of the 64th clock cycle with a length of 4 clock cycles. Further programming examples can be found

4.6.2 GPCLK as Clock Outputs

All 8 GPCLK lines can be configured as individual clock outputs with 8 kHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz and for test purposes with the internal frequency or the input frequency of the analog PLL (APLL). All clock signals are generated from the analog PLL output frequency which is the internal frequency. The quality of all output frequency signals depends on the quality of the selected input PLL frequency.

4.7 JTAG (Boundary Scan)

The SWITI provides a fully IEEE 1149.1 compatible boundary scan support consisting of:

- a complete boundary scan chain
- a Test Access Port controller (TAP controller)
- five dedicated pins: TCK, TMS, TDI, TDO and a $\overline{\text{TRST}}$ to asynchronously reset the TAP controller
- one 32-bit IDCODE register

4.7.1 Boundary Scan

All pins except power supply and crystal are included in the boundary scan. Depending on the pin functionality one (input), two (output, enable) or three (input, output, enable) boundary scan cells are provided.

The maximum clock rate at pin TCK is 10 MHz.

4.7.2 Test-Access-Port (TAP)

The following signal pins allow the boundary scan test logic to be accessed:

- TCK
  - Test Clock input to which a central BSc test clock is applied. This BSc test clock is independent of the system clock. Clock phases are derived from this clock for test sequence control.
- TMS
  - Test Mode Select control input for which the desired status changes at the TAP controller by applying a certain level (0/1) caused by the rising edge of TCK.
- TDI
  - Test Data Input whose data is inserted into the test logic with the rising edge of the TCK.
- TDO
  - Test Data Output with tristate capability which is only active during the SHIFT-IR and SHIFT-DR controller state, and whose data is driven with the falling edge of TCK.

4.7.3 TAP Controller

The Test Access Port (TAP) controller implements the state machine defined in the JTAG standard IEEE 1149.1.

Transitions on the pin TMS cause the TAP controller to perform a state change. The possible instructions are listed in the following table.

Table 14 TAP Controller Instructions

Code	Instruction	Function
0000	EXTEST	External testing
0001	IDCODE	Reading ID code
0100	HIGHZ	High impedance state of all boundary scan outputs
0101	SAMPLE/PRELOAD	Snap-shot testing
0110	INTEST	Internal testing
0111	CLAMP	Reading outputs
1111	BYPASS	Bypass operation

The instruction length is four bit.

EXTEST is used to verify the board interconnections.

When the TAP controller is in the state “update DR”, all output pins are updated with the falling edge of TCK. When it has entered state “capture DR” the levels of all input pins are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

INTEST supports internal chip testing.

When the TAP controller is in the state “update DR”, all inputs are updated internally with the falling edge of TCK. When it has entered state “capture DR” the levels of all outputs are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction enables all signal pins (inputs and outputs) to be sampled during operation (SAMPLE) and the result to be shifted out through the shift BSc register. The function of the internal logic is not influenced by this instruction. While shifting out, the BSc cells can be serially loaded at the same time with defined values through TDI (PRELOAD). The SAMPLE/PRELOAD instruction selects the boundary scan register in normal mode. In state CAPTURE-DR data is loaded into the boundary scan register with the rising edge of TCK. In state UPDATE-DR the contents of the boundary scan register are written into the second register stage of the boundary scan register. This data becomes effective at the outputs only if an instruction has been activated that sets the BSc register to test mode: e.g. EXTEST or CLAMP.

IDCODE

The 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to ’1’..

Version	Device Code	Manufacturer Code	Output	
xxxx	xxxx xxxx xxxx xxxx	xxxx xxxx xxx	1	--> TDO

Table 15 Boundary Scan IDCODE

	Version	Device Code	Manufacture Code	Bit0
HTSI	0010	0000 0000 0110 1101	0000 1000 001	1
HTSI-L	0010	0000 0000 0110 1110	0000 1000 001	1
HTSI-XL	0010	0000 0000 0110 1111	0000 1000 001	1

CLAMP

The BSc register is in test mode. For the duration of the CLAMP instruction, the BYPASS register is selected so that a minimal shift path is created.

During SHIFT-DR data can be shifted through the BYPASS register. The contents of the BSc register does not change during the UPDATE-DR state.

HIGHZ

The HIGHZ instruction disables all outputs if switched to high impedance state. The outputs are switched to high impedance in state UPDATE-IR. The outputs are redefined according to the next new instruction if another instruction has become active with UPDATE-IR. The selected test data register is the BYPASS register.

BYPASS, a bit entering TDI is shifted to TDO after one TCK clock cycle, e.g. to skip testing of selected ICs on a printed circuit board.

4.8 Identification Code via µP Read Access

The SWITI offers two possibilities to read the identification code.

– via the JTAG port as described in **Chapter 4.7**
– or via the processor interface

After a hardware reset the identification code is stored in the **General Purpose Interrupt Register** (**GPI**) and can be read via the processor interface. The high nibble is the version number and the low nibble is equal to the low nibble of the device code shown in **Table 16**. For the 8-bit µP interface configuration the first write access to the General Purpose Mask Register (**GPM**) will reset the register **GPI** to 00_H. If the µP interface is configured as a 16-bit interface the IDCODE can always be read from the **GPI** register, that means the **GPI** register will not be reset.

The IDCODE for the µP read access is shown in **Table 16**.

Table 16 IDCODE via µP Read Access

	8-Bit IDCODE (MSB..LSB)	
	Version	**Device Code**
HTSI	0010	1101
HTSI-L	0010	1110
HTSI-XL	0010	1111

Note: The version number of the IDCODE register remains unchanged.

5 Register Description

The register description gives information about all registers accessible via the microprocessor interface according to address, short name, access, reset value and value range.

5.1 Register Overview For 8-Bit Interface

Table 17 Register Overview For 8-Bit Interface

Reg Name	Access	8-bit Address	Reset Value	Comment	Page No.
SPA	RD/WR	00_H	00_H	Source Port Address Register Value range see **Table 18**	**61**
ITSA	RD/WR	01_H	00_H	Input Time-Slot Address Register Value range see **Table 19**	**61**
DPA	RD/WR	02_H	00_H	Destination Port Address Register Value range see **Table 18**	**62**
OTSA	RD/WR	03_H	00_H	Output Time-Slot Address Register Value range see **Table 19**	**62**
SCA	RD/WR	07_H	00_H	Subchannel Address Register Value range see **Table 20**	**62**
GI1	RD/WR	04_H	00_H	General Input Register 1	**63**
GI2	RD/WR	05_H	00_H	General Input Register 2	**65**
CCMD	RD/WR	06_H	00_H	Connection Command Register	**66**
CMD1	RD/WR	08_H	00_H	Configuration Command Register 1	**68**
CMD2	RD/WR	$0A_H$	00_H	Configuration Command Register 2	**74**
MV	RD/WR	$0C_H$	00_H	Message Value Register	**78**
ISTA1	RD	$0E_H$	00_H	Interrupt Status Register 1	**78**
IESTA1	RD	10_H	00_H	Interrupt Error Status Register 1	**79**
IESTA2	RD	11_H	00_H	Interrupt Error Status Register 2	**80**
INTM1	RD/WR	12_H	$3D_H$	Interrupt Mask Register 1	**81**
INTEM1	RD/WR	14_H	$3F_H$	Interrupt Error Mask Register 1	**82**
INTEM2	RD/WR	15_H	FF_H	Interrupt Error Mask Register 2	**83**
GPPI	RD	16_H	00_H	General Purpose Port Input Register	**83**
GPPO	WR	18_H	00_H	General Purpose Port Output Register	**84**
GPD	RD/WR	$1A_H$	00_H	General Purpose Direction Register	**84**
GPM	RD/WR	$1B_H$	FF_H	General Purpose Mask Register	**84**
GPI	RD	$1C_H$	IDCODE	General Purpose Interrupt Register	**85**
TSV	RD	$1E_H$	XX_H	Time-Slot Value Register	**85**
CON	RD	$1F_H$	XX_H	Configuration Register	**89**

Table 18 Value Range for SPA/DPA

Addressed Lines	Value Range Bit4..0
Local-Bus input lines (H-Mode)	15..0
Local-Bus input lines (M-Mode)	31..0
H-Bus lines (H-Mode)	31..0

Table 19 Value Range for ITSA/OTSA

Data Rate	Range Bit7..0
2.048 Mbit/s	31..0
4.096 Mbit/s	63..0
8.192 Mbit/s	127..0
16.384 Mbit/s	255..0

Table 20 Value Range for SCA

Mode	Range
1-bit switching	0..7 for ISCA0..2; 0..7 for OSCA0..2
2-bit switching	0..3 for ISCA0..1; 0..3 for OSCA0..1
4-bit switching	0..1 for ISCA0; 0..1 for OSCA0

5.2 Detailed Register Description For 8-bit Interface

Source Port Address Register RD/WR Address: 00**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
SPA	BT	0	0	PA4	PA3	PA2	PA1	PA0

BT Bus Type (must be set to logical "0" in M-mode)

0 = Local Bus

1 = H-bus

PA4..0 Port Address

Input Time-Slot Address Register RD/WR Address: 01**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
ITSA	TSA7	TSA6	TSA5	TSA4	TSA3	TSA2	TSA1	TSA0

TSA7..0 Time-Slot Address

Destination Port Address Register RD/WR Address: 02**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
DPA	BT	0	0	PA4	PA3	PA2	PA1	PA0

BT Bus Type (must be set to logical "0" in M-mode)

0 = Local Bus

1 = H-bus

PA4..0 Port Address

Output Time-Slot Address Register RD/WR Address: 03**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
OTSA	TSA7	TSA6	TSA5	TSA4	TSA3	TSA2	TSA1	TSA0

TSA7..0 Time-Slot Address

Subchannel Address Register RD/WR Address: 07**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
SCA	0	0	OSCA2	OSCA1	OSCA0	ISCA2	ISCA1	ISCA0

OSCA2..0 Output Subchannel Address

ISCA2..0 Input Subchannel Address

General Input Register 1 RD/WR Address: 04**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
GI1	GV7	GV6	GV5	GV4	GV3	GV2	GV1	GV0

GV7..0 General Value

In case of a PLL Reference (main and secondary) Selection Command (CMD1) the content of this register is interpreted as follows:

GV2..0 Clock Frequency

000 = 8 kHz

001 = 512 kHz

010 = 1.536 MHz

011 = 1.544 MHz

100 = 2.048 MHz

101 = 4.096 MHz

110 = 8.192 MHz

111 = 16.384 MHz

In case of a CT_NETREF_1/2 Output Selection Command (CMD1) the content of this register is interpreted as follows:

GV1..0 Output CT_NETREF_1/2 Clock Frequency

00 = 8 kHz

01 = 512 kHz

10 = 2.048 MHz

In case of a Bit Shift Command (CMD1) the content of this register is interpreted as follows:

GV4 Bit shift value (only for input lines)

0 = bit shift applies before PFS rising edge

1 = bit shift applies after PFS rising edge

GV3..1 Bit shift value (range: 7 to 0)

GV0 Edge Control Bit (half clock shift)

0 = data transmit with rising edge and is sampled with falling edge

1 = data transmit with falling edge and is sampled with rising edge

In case of the GPCLK as Frame Signal Command (CMD2) the content of this register is interpreted as follows:

GV7..2 Offset within the PFS frame in number of 16.384 MHz clock cycles (lower 6 bits; refer to GI2 for the upper part)

GV1 Edge Control Bit

0 = data changes with rising edge and is sampled with falling edge

1 = data changes with falling edge and is sampled with rising edge

GV0 Reserved

In case of the GPCLK as Clock Signal Command (CMD2) the content of this register is interpreted as follows:

GV2..0 Output Frequency for the selected line

000 = 8 kHz

001 = 2.048 MHz

010 = 4.096 MHz

011 = 8.192 MHz

100 = 16.384 MHz

101 = Input Analog PLL (2.048 MHz)

110 = Internal Frequency (49.152 MHz)

General Input Register 2 RD/WR Address: 05**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
GI2	GV7	GV6	GV5	GV4	GV3	GV2	GV1	GV0

GV7..0 General Value

In case of the GPCLK as Frame Signal Command (CMD2) the content of this register is interpreted as follows:

GV7..5 Width of the pulse in number of 16.384 MHz clock cycles from 1 to 8 i.e. GV7..5 = 000 => 1 clock cycle, GV7..5 = 010 => 3 clock cycles

GV4..0 Offset within the PFS frame in number of 16.384 MHz clock cycles (upper 5 bits; refer to GI1 for the lower part)

Connection Command Register RD/WR Address: 06**H**

Reset value: 00**H**

	7	6	5	4	3	2	1	0
CCMD	I3	I2	I1	I0	CC3	CC2	CC1	CC0

CC3..0 Command Code

0000 = no operation at all

0001 = Constant Delay Connection Command (incl. Broadcast Connection)
(SPA, ITSA, DPA, OTSA, SCA are considered)

I1..0 Subchannel Mode

00 = 8-bit wide time-slots

01 = 4-bit wide time-slots

10 = 2-bit wide time-slots

11 = 1-bit wide time-slots

0010 = Minimum Delay Connection Command (incl. Broadcast Connection)
(SPA, ITSA, DPA, OTSA are considered)

0011 = Send Message Command (always Constant Delay)
(DPA, OTSA, MV are considered)

0100 = Stop Message Command
(DPA, OTSA are considered)

0101 = Disconnect Command
(SPA, ITSA, DPA, OTSA, SCA are considered)

I1..0 see I1..0 of Constant Delay Connection Command (incl. Broadcast Connection)

0110 = Disconnect Part of Broadcast Command
(SPA, ITSA, DPA, OTSA, SCA are considered)

I1..0 see I1..0 of Constant Delay Connection Command (incl. Broadcast Connection)

0111 = Multipoint Connect Command
(SPA, ITSA, DPA, OTSA are considered)

I0 Multipoint MODE

0 = logical OR connection

1 = logical AND connection

1000 = Disconnect All Command

1001 = Bidirectional Connect Command
(SPA, ITSA, DPA, OTSA are considered)

I0 Delay MODE

0 = Minimum Delay

1 = Constant Delay

1010 = Memory Dump (Connection and Data Memory)

I0 Memory Dump

0 = disable

1 = enable

Configuration Command Register 1 RD/WR Address: 08**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
CMD1	I3	I2	I1	I0	CC3	CC2	CC1	CC0

CC3..0 Command Code

0000 = no operation

0001 = Set as H.100/H.110 Master/Slave (HTSI H-Mode)
Must be programmed only after PLL input initialization and/or H.1x0 fallback command

I0 Mode Information

0 = Slave mode

1 = Master mode

0010 = PLL Primary Reference Selection Command for Master
(GI1 is considered to set the frequency)

I3..0 Synchronization Information

0000 = no synchronization = internal oscillator (default)

0001 = synchronizes the PLL to PFS (only M-Mode)

0010 = synchronizes the PLL to PDC (only M-Mode)

0011 = synchronizes the PLL to CT_NETREF_1 (only H-mode)

0100 = synchronizes the PLL to CT_NETREF_2 (only H-mode)

0101 = synchronizes the PLL to NTWK_1

0110 = synchronizes the PLL to NTWK_2

0111 = synchronizes the PLL to CT_A (CT_C8_A and $\overline{\text{CT\_FRAME\_A}}$) (only H-mode, GI1 isn't considered)

1000 = synchronizes the PLL to CT_B (CT_C8_B and $\overline{\text{CT\_FRAME\_B}}$) (only H-mode, GI1 isn't considered)

1001 = not used

1010 = not used

1011 = synchronizes the PLL to $\overline{\text{FR\_COMP}}$ (only H-mode)

1100 = synchronizes the PLL to SCLK (only H-mode)

1101 = synchronizes the PLL to C2 (only H-mode)

1110 = synchronizes the PLL to $\overline{C4}$ (only H-mode)

1111 = synchronizes the PLL to $\overline{C16}$ (only H-mode)

0011 = PLL Secondary Reference Selection Command for Master (only H-mode)
(GI1 is considered to set the frequency)

I3..0 Synchronization Information

0000 = no synchronization = internal oscillator (default)

0001 = synchronizes the PLL to CT_NETREF_1

0010 = synchronizes the PLL to CT_NETREF_2

0011 = synchronizes the PLL to NTWK_1

0100 = synchronizes the PLL to NTWK_2

0101 = synchronizes the PLL to CT_C8_A

0110 = synchronizes the PLL to CT_C8_B

0111 = synchronizes the PLL to $\overline{CT\_FRAME\_A}$

1000 = synchronizes the PLL to $\overline{CT\_FRAME\_B}$

1001 = synchronizes the PLL to $\overline{FR\_COMP}$

1010 = synchronizes the PLL to SCLK

1011 = synchronizes the PLL to SCLKx2

1100 = synchronizes the PLL to C2

1101 = synchronizes the PLL to $\overline{C4}$

1110 = synchronizes the PLL to $\overline{C16}$

1111= start special configuration register programming

0100 = PLL Source Selection Command. - Slave Path (only H-mode)

I3..0 Source/Frequency Information

0000 = not used

0001 not used

0010 not used

0011 not used

0100 not used

0101 CT_A (CT_C8_A and $\overline{CT\_FRAME\_A}$)

0110 CT_B (CT_C8_B and $\overline{CT\_FRAME\_B}$)

0111 SCLK = 2.048 MHz and $\overline{FR\_COMP}$

1000 SCLK = 4.096 MHz and $\overline{\text{FR\_COMP}}$

1001 SCLK = 8.192 MHz and $\overline{\text{FR\_COMP}}$

1010 C2 = 2.048 MHz and $\overline{\text{FR\_COMP}}$

1011 $\overline{\text{C4}}$ = 4.096 MHz and $\overline{\text{FR\_COMP}}$

1100 $\overline{\text{C16}}$ = 16.384 MHz and $\overline{\text{FR\_COMP}}$

1111 write special configuration register (GI1 is considered)

0101 = H.100/H.110 Clock Output Selection Command (only H-mode)

I1..0 Activation Information

00 = disable $\overline{\text{CT\_FRAME}}$ and CT_C8 (default)

01 = enable $\overline{\text{CT\_FRAME\_A}}$ and CT_C8_A

10 = enable $\overline{\text{CT\_FRAME\_B}}$ and CT_C8_B

I3..2 Not used must be set to ’0’

0110 = PCM Clock Input/Output Selection Command
(Default: PFS and PDC inactive)

I2..0 Frequency Information

000 = reserved

001 = enable PFS and PDC = 2.048 MHz

010 = enable PFS and PDC = 4.096 MHz

011 = enable PFS and PDC = 8.192 MHz

100 = enable PFS and PDC = 16.384 MHz

I3 Direction Information

0 = PFS and PDC as Input

1 = PFS and PDC as Output

0111 = Compatibility Clock Output Selection Command (only H-mode)

I0 MVIP-90 Activation Information

0 = disable MVIP-90 - C2, $\overline{\text{C4}}$, $\overline{\text{FR\_COMP}}$ (default)

1 = enable MVIP-90 - C2, $\overline{\text{C4}}$, $\overline{\text{FR\_COMP}}$

I1 H-MVIP Activation Information

0 = disable H-MVIP - C2, $\overline{\text{C4}}$, $\overline{\text{C16}}$, $\overline{\text{FR\_COMP}}$ (default)

1 = enable H-MVIP - C2, $\overline{\text{C4}}$, $\overline{\text{C16}}$, $\overline{\text{FR\_COMP}}$

I3..2 SCbus Activation/Frequency Information

00 = disable SCbus - SCLK, SCLKx2, Fsync* (default)

01 = enable SCbus - 2.048 MHz

10 = enable SCbus - 4.096 MHz

11 = enable SCbus - 8.192 MHz

1000 = CT_NETREF_1 Output Selection Command (only H-mode)

I0 Inversion Information

0 = normal CT_NETREF_1 output

1 = invert CT_NETREF_1 output

I3..1 Activation Information

000 = disable CT_NETREF_1 (default)

001 = enable CT_NETREF_1 - source NTWK_1

010 = enable CT_NETREF_1 - source NTWK_2

011 = enable CT_NETREF_1 - source NETREF_2

100 = enable CT_NETREF_1 - source internal oscillator (GI1 is considered to set the output frequency)

1001 = CT_NETREF_2 Output Selection Command (only H-mode)

I0 Inversion Information

0 = normal CT_NETREF_2 output

1 = invert CT_NETREF_2 output

I3..1 Activation Information

000 = disable CT_NETREF_2 (default)

001 = enable CT_NETREF_2 - source NTWK_1

010 = enable CT_NETREF_2 - source NTWK_2

011 = enable CT_NETREF_2 - source NETREF_1

100 = enable CT_NETREF_2 - source internal oscillator (GI1 is considered to set the output frequency)

1010 = H.100/H.110 Fallback Mechanism

I1..0 PLL Source (only H-mode)

00 = disable (default)

01 = from PLL Main Ref. to Secondary Ref. (If SWITI is Primary "A" Master in the system)

10 = from PLL Main Ref. to Secondary Ref. (If SWITI is Secondary "B" Master in the system)

11 = from A clock to B clock (Slave)

I2 Re-Fallback Activation Information for Primary Master (only H-mode)

0 = disable automatic switch back to main ref. (default)

1 = enable automatic switch back to main ref.

I3 PLL Phase Alignment (Please see description, **Chapter 3.4.4**)

0 = disable (default after reset)

1 = enable
Must be set for H.1x0 slave

1011 = Set Bit Rate Command Local Bus
(Default for all lines = 2.048 Mbit/s)

I1..0 Base Bit Rate Information

00 = 2.048 Mbit/s

01 = 4.096 Mbit/s

10 = 8.192 Mbit/s

11 = 16.384 Mbit/s

I2 Destination Information

0 = no effect

1 = set rate of local input lines (SPA is considered)

I3 Destination Information

0 = no effect

1 = set rate of local output lines (DPA is considered)

1100 = Set Bit Rate Command H.100/H.110 and Interoperability Bussystems
(Default for all lines = 2.048 Mbit/s)

I1..0 Base Bit Rate Information

00 = 2.048 Mbit/s (SPA is considered)

01 = 4.096 Mbit/s (SPA is considered)

10 = 8.192 Mbit/s (SPA is considered)

11 = set all lines to 8.192 Mbit/s

1101 = Read Time-Slot Command

I0 Destination Information

0 = read input time-slots(SPA, ITSA are considered)

1 = read output time-slots(DPA, OTSA are considered)

1110 = Stream to Stream Switch Command (SPA, DPA are considered)
(The value for SPA and DPA can not be equal)

The command affects H-Bus only and depends on the selected bit rate

I1..0 Connection (see **Figure 10** on page **28**) depends on the selected bit for every line

00 = Mode 0

01 = Mode 1

10 = Mode 2

11 = Mode 3

I2 Connection Information

0 = release current stream to stream connection

1 = establish current stream to stream connection

I3 Destination Information

0 = reserved

1 = release all programmed stream to stream connections

1111 = Bit Shift Command (GI1 is considered to set shift value)
(Default: Bit Shift is inactive)

I1..0 Direction Control

00 = Set shift value for input line (SPA is considered)

01 = Set shift value for all input lines

10 = Set shift value for all output lines

11 = Set shift value for all lines (input and output)

Configuration Command Register 2 RD/WR Address: 0A**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
CMD2	I3	I2	I1	I0	CC3	CC2	CC1	CC0

CC3..0 Command Code

0000 = no operation at all

0001 = External Frequency

I0 Set External Frequency **(Must be programmed first)**

0 = 32.768 MHz

1 = 16.384 MHz

I1 Fallback to Oscillator

0 = disable (and turn off “enable” status temporarily if fallback has occurred)

1 = enable

If "Fallback to Oscillator" is enabled and a fallback has occurred, the corresponding failure is indicated in the IESTA1 and/or IESTA2 registers. For all clock failures, the PLL bit ("PLL Source Failure Indication", IESTA2 register) as well as the clock source related bit (in IESTA1 or IESTA2 register) will be set to "1". With the clock valid again the previously changed bits in IESTA1 and/or IESTA2 are set back to "0", the fallback must be disabled (CMD2=01_H/11_H) for a few cycles and enabled again thereafter.

I2 APLL´s parameters

0 = default

1 = start APLL with improved parameters

The command CMD2=41_H or CMD2=51_H to start the APLL with improved parameters must only be issued only once after Power Up

0010 = Parallel Mode (local bus only)
Set the first 8 local bus input lines as 8 parallel input lines and set the first 8 local bus output lines as 8 parallel output lines.

I0 Set Parallel Mode

0 = disable

1 = enable

0011 = IREQ Pin Command

I1..0 Set IREQ Pin
(Default: IREQ is inactive)

00 = IREQ is active low

01 = IREQ is active high

10 = IREQ as open-drain pin

I2 Set Interrupt Time-Out Counter
Set the inactive time between two consecutive interrupts

0 = disable = 20 ns

1 = enable = 300 ns

0100 = PCM and H.1x0 Standby Command

I0 Set PCM to High Impedance

0 = outputs are tristated (default)

1 = outputs are enabled

I1 Set H.1x0 to High Impedance (only H-mode)

0 = I/O's are tristated (default)

1 = I/Os are enabled

I2 not used must be set to '0'

I3 Internal PCM Clock Synchronization

0 = Must be set in PCM clock master mode

1 = Must be set in PCM clock slave mode

0101 = Loop Command

I0 Set PCM-PCM Loop

0 = disable (default)

1 = enable

I1 Set H.100/H.110 Loop (only H-mode)

0 = disable (default)

1 = enable

0110 = GPCLK as Frame Signal Command (GI1, GI2 are considered)
(Default: All GPCLK's are tristated)

I2..0 GPCLK Line (7..0)

I3 Invert Mode

0 = frame signal is high active

1 = frame signal is low active

0111 = GPCLK as Clock Signal Command (GI1 is considered to set the frequency)
(Default: All GPCLK's are tristated)

I2..0 GPCLK Line (7..0)

1000 = Set Range of Data Rate Command
To avoid loss of data this command should be issued only once after reset. If the range of data rate is changed later on, loss of data must be expected for up to four frames. (Additionally for the H-mode the 8.192 Mbit/s bit must be set.)

I3..0 Range Select
To specify the range the min and max codes have to be logical OR combined.

0001 = 2.048 Mbit/s (default)

0010 = 4.096 Mbit/s

0100 = 8.192 Mbit/s

1000 = 16.384 Mbit/s

1001 = Read Configuration

I3..0 Select Configuration Command

0000 = Master/Slave Configuration (only H-mode)

0001 = PLL Primary Master Source

0010 = PLL Secondary Master Source (only H-mode)

0011 = PLL Source (Slave Path) (only H-mode)

0100 = Clock Output Selection for H.1x0 (only H-mode)

0101 = Clock Output Selection for PCM

0110 = Clock Output Selection for Interoperability Signals (only H-mode)

0111 = Output Selection for CT_NETREF_1 (only H-mode)

1000 = Output Selection for CT_NETREF_2 (only H-mode)

1001 = Fallback Mechanism and Phase Alignment

1010 = External Input Frequency

1011 = Parallel Mode

1100 = IREQ Pin

1101 = H.1x0/PCM Standby

1110 = Loop

1111 = Range of Data Rate

1010 = Read GPCLK Configuration

I2..0 GPCLK Line 7..0

1011 = Read PCM Line Configuration

I0 Destination Information

0 = Read Data Rate of Input Line (SPA is considered)

1 = Read Data Rate of Output Line (DPA is considered)

1100 = Read H.1x0 Line Configuration (SPA is considered) (only H-mode)

1101 = Read Bit Shift Configuration

I0 Destination Information

0 = Shift Value for Input Line (SPA is considered)

1 = Shift Value for all Output Lines

1110 = Reserved

1111 = Software Reset

I0 Set Software Reset

0 = Deactivate Software Reset (default)

1 = Activate Software Reset

Message Value Register RD/WR Address: 0C**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
MV	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0

MV7..0 Message Value

Interrupt Status Register 1 RD Address: 0E**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
ISTA1	APLL	STR	ER2	ER1	GPIO	TSA	NFC	RDY

APLL APLL lock indication

0 = PLL is not locked = bypassed

1 = PLL is locked

STR Stream to Stream Indication

0 = no stream to stream connection is set

1 = stream to stream connections are set

ER2 Error2 Interrupt Change Indication (not active in 16-bit mode)

0 = no change detected in the Interrupt Error Status Register 2 (IESTA2)

1 = change detected in the Interrupt Error Status Register 2 (IESTA2)

ER1 Error1 Interrupt Change Indication

0 = no change detected in the Interrupt Error Status Register 1 (IESTA1)

1 = change detected in the Interrupt Error Status Register 1 (IESTA1)

GPIO General Purpose Change Indication

0 = no change according to GP port inputs detected

1 = at least one change according to GP port inputs detected

TSA Time-Slot Arrived Indication

0 = there is no new time-slot value in the register TSV

1 = there is a new time-slot value in the register TSV

NFC No Further Connections Indication

0 = establishing of connections is possible

1 = the maximum amount of connections is reached

RDY Ready Indication

0 = CCMD is not ready to be written to

1 = CCMD is ready to be written to

Interrupt Error Status Register 1 RD Address: 10**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
IESTA1	0	0	NR2	NR1	CTB	CTA	NW2	NW1

NR2 CT_NETREF_2 Failure Indication

NR1 CT_NETREF_1 Failure Indication

CTB CT_C8_B or $\overline{\text{CT\_FRAME\_B}}$ Failure Indication

CTA CT_C8_A or $\overline{\text{CT\_FRAME\_A}}$ Failure Indication

NW2 NTWK_2 Failure Indication

NW1 NTWK_1 Failure Indication

for all these status bits the values can be

0 = no failure detected

1 = failure detected

Interrupt Error Status Register 2 RD Address: 11**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
IESTA2	CON	PLL	FRC	SC2	SC	C2	C4	C16/S

CON Connection Memory Error/Overflow Indication

PLL PLL Source Failure Indication

FRC FR_COMP Failure Indication

SC2 SCLK2 Failure Indication

SC SCLK Failure Indication

C2 C2 Failure Indication

C4 $\overline{C4}$ Failure Indication

C16/S $\overline{C16}$ Failure Indication

C16/S Secondary Reference Failure Indication (only in master mode)

for all these status bits the values can be

0 = no failure detected

1 = failure detected

Interrupt Mask Register 1 RD/WR Address: 12**H**

Reset value: 3DH

	7	6	5	4	3	2	1	0
INTM1	0	0	ER2	ER1	GPIO	TSA	0	RDY

ER2 Error2 Interrupt Change Indication Mask (not active in 16-bit mode)

0 = Do not mask the Change Indication Bit

1 = Mask the Change Indication Bit

ER1 Error1 Interrupt Change Indication Mask

0 = Do not mask the Change Indication Bit

1 = Mask the Change Indication Bit

GPIO General Purpose Change Indication Mask

0 = Do not mask the Change Indication Bit

1 = Mask the Change Indication Bit

TSA Time-Slot Arrived Indication Mask

0 = Do not mask the Time-Slot Arrived Indication Bit

1 = Mask the Time-Slot Arrived Indication Bit

RDY Ready Indication Mask

0 = Do not mask the Ready Indication Bit

1 = Mask the Ready Indication Bit

Mask = Disable the interrupt

Interrupt Error Mask Register 1 RD/WR Address: 14**H**

Reset value: 3FH

	7	6	5	4	3	2	1	0
INTEM1	0	0	NR2	NR1	CTB	CTA	NW2	NW1

NR2 CT_NETREF_2 Failure Indication Mask

NR1 CT_NETREF_1 Failure Indication Mask

CTB CT_C8_B or $\overline{\text{CT\_FRAME\_B}}$ Failure Indication Mask

CTA CT_C8_A or $\overline{\text{CT\_FRAME\_A}}$ Failure Indication Mask

NW2 NTWK_2 Failure Indication Mask

NW1 NTWK_1 Failure Indication Mask

for all these status bits the values can be

0 = Do not mask this interrupt

1 = Mask this interrupt

Mask = Disable the interrupt

Interrupt Error Mask Register 2 RD/WR Address: 15**H**

Reset value: FFH

	7	6	5	4	3	2	1	0
INTEM2	CON	PLL	FRC	SC2	SC	C2	C4	C16/S

CON Connection Memory Overflow Indication Mask

PLL PLL Source Failure Indication Mask

FRC FR_COMP Failure Indication Mask

SC2 SCLK2 Failure Indication Mask

SC SCLK Failure Indication Mask

C2 C2 Failure Indication Mask

C4 $\overline{\text{C4}}$ Failure Indication Mask

C16/S $\overline{\text{C16}}$ Failure Indication Mask

C16/S Secondary Reference Failure Indication Mask (only in master mode)

For all these status bits the values can be

0 = Do not mask this interrupt

1= Mask this interrupt

Mask = Disable the interrupt

General Purpose Port Input Register RD Address: 16**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
GPPI	GPB7	GPB6	GPB5	GPB4	GPB3	GPB2	GPB1	GPB0

GPB7..0 General Purpose Bits

General Purpose Port Output Register WR Address: 18**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
GPPO	GPB7	GPB6	GPB5	GPB4	GPB3	GPB2	GPB1	GPB0

GPB7..0 General Purpose Bits

General Purpose Direction Register RD/WR Address: 1A**H**

Reset value: 00H

	7	6	5	4	3	2	1	0
GPD	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0

DC7..0 Direction Control

0 = set line as input

1 = set line as output

General Purpose Mask Register RD/WR Address: 1B**H**

Reset value: FFH

	7	6	5	4	3	2	1	0
GPM	IM7	IM6	IM5	IM4	IM3	IM2	IM1	IM0

IM7..0 GPIO Interrupt Mask (bit 0 for line 0, bit 1 for line 1 ..)

0 = enable change detection

1 = disable change detection

General Purpose Interrupt Register RD Address: 1C**H**

Reset value: IDCODE

	7	6	5	4	3	2	1	0
GPI	IND7	IND6	IND5	IND4	IND3	IND2	IND1	IND0

IND7..0 GPIO Interrupt Indication (bit 0 for line 0, bit 1 for line 1 ..)

0 = no change detected

1 = at least one change detected on this line

Time-Slot Value Register RD Address: 1E**H**

Reset value: XXH

	7	6	5	4	3	2	1	0
TSV	TSV7	TSV6	TSV5	TSV4	TSV3	TSV2	TSV1	TSV0

For the Read Time-Slot Value Command the content of the TSV register is interpreted as:

TSV7..0 Time-Slot Value

For the Read Configuration Command the content of the TSV register is interpreted as:

Master/Slave Configuration only H-mode (page **68**)

TSV0 0 = Slave

1 = Master

PLL Primary Master Configuration

TSV3..0 See I3..0 from PLL Primary Master Reference Selection Command (page **68**)

TSV6..4 000 = 8 kHz

001 = 512 kHz

010 = 1.536 MHz

011 = 1.544 MHz

100 = 2.048 MHz

101 = 4.096 MHz

110 = 8.192 MHz

111 = 16.384 MHz

PLL Secondary Master Configuration

TSV3..0 See I3..0 from PLL Secondary Master Reference Selection Command (page 69)

TSV6..4 000 = 8 kHz

001 = 512 kHz

010 = 1.536 MHz

011 = 1.544 MHz

100 = 2.048 MHz

101 = 4.096 MHz

110 = 8.192 MHz

111 = 16.384 MHz

PLL Source Selection

TSV3..0 See I3..0 from PLL Source Selection Command (page 69)

H.1x0 Clock Output Selection only H-mode

TSV1..0 See I1..0 from H.1x0 Clock Output Selection Command (page 70)

PCM Clock Output Selection

TSV3..0 See I3..0 from PCM Clock Output Selection Command (page 70)

Compatibility Clock Output Selection only H-mode

TSV3..0 See I3..0 from Compatibility Clock Output Selection Command (page 70)

CT_NETREF_1 Output Selection only H-mode

TSV3..0 See I3..0 from CT_NETREF_1 Output Selection Command (page 71)

TSV5..4 Use TSV5..4, if TSV3..0 = 100x

00 = 8 kHz

01 = 512 kHz

10 = 2.048 MHz

CT_NETREF_2 Output Selection only H-mode

TSV3..0 See I3..0 from CT_NETREF_2 Output Selection Command (page 71)

TSV5..4 Use TSV5..4, if TSV3..0 = 100x

00 = 8 kHz

01 = 512 kHz

10 = 2.048 MHz

H.1x0 Fallback Mechanism and Phase Alignment

TSV3..0 See I3..0 from H.1x0 Fallback Mechanism and Phase Alignment Command (page 71)

External Frequency

TSV0 See I0 from Set External Frequency Command (page 74)

Parallel Mode

TSV0 See I0 from Set Parallel Mode Command (page 74)

IREQ Pin

TSV2..0 See I1..0 from Set IREQ Pin Command (page 75)

H.1x0/PCM Standby

TSV1..0 See I0 from Set H.1x0/PCM Standby Command (page 75)

Loop

TSV1..0 See I1..0 from Loop Command (page 75)

Range of Data Rate

TSV3..0 See I3..0 from Set Range of Data Rate Command (page 76)

For the Read GPCLK Configuration Command the content of the TSV register is interpreted as:

TSV0 0 = GPCLK Line as Clock Signal

1 = GPCLK Line as Frame Signal

GPCLK Line as Clock Signal

TSV3..1 000 = 8 kHz

001 = 2.048 MHz

010 = 4.096 MHz

011 = 8.192 MHz

100 = 16.384 MHz

101 = Input Analog PLL

110 = Internal Frequency

GPCLK Line as Frame Signal

TSV1 0 = Rising Edge

1 = Falling Edge

TSV7..2 Offset within the PFS frame in number of 16.384 MHz clock cycles (lower 6 bits; refer to CON for the upper part)

For the Read PCM and H.1x0 Line Configuration Command the content of the TSV register is interpreted as:

TSV1..0 00 = 2.048 MBit/s

01 = 4.096 MBit/s

10 = 8.192 MBit/s

11 = 16.384 MBit/s (only for PCM)

In case of the Read Bit Shift Configuration Command the content of the TSV register is interpreted as:

TSV0 Edge Control
- 0 = Rising Edge
- 1 = Falling Edge

TSV3..1 Bit Shift Value (Range: 7 to 0)

TSV4 Byte Shift Value (only for input lines)
- 0 = bit shift applies to byte before PFS rising edge
- 1 = bit shift applies to byte before PFS falling edge

Configuration Register RD Address: 1F**H**

Reset value: XXH

	7	6	5	4	3	2	1	0
CON	CON7	CON6	CON5	CON4	CON3	CON2	CON1	CON0

For the Memory Dump Command (CCMD) the content of the CON register is:

CON7..0 Connection and Data Memory

For the Read GPCLK Configuration Command the content of the CON register is:

CON7..5 Width of the pulse in number of 16.384 MHz clock cycles from 1 to 8
i.e. CON7..5 = 000 => 1 clock cycle, CON7..5 = 010 => 3 clock cycles

CON4..0 Offset within the PFS frame in number of 16.384 MHz clock cycles (upper 5 bits; refer to TSV for the lower part)

5.3 Register Overview For 16-Bit Interface

Table 21 Register Overview For 16-Bit Interface

Reg Name	Access	Address	Reset Value	Comment	Page No.
SA	RD/WR	00_H	0000_H	Source Address Register	91
DA	RD/WR	02_H	0000_H	Destination Address Register	91
GI	RD/WR	04_H	0000_H	General Input Register	92
CC16	RD/WR	06_H	0000_H	Connection Command Register 16-bit	92
CMD1	RD/WR	08H	00H	Configuration Command Register 1 This is a 8-bit register	68
CMD2	RD/WR	0AH	00H	Configuration Command Register 2 This is a 8-bit register	74
MV	RD/WR	0CH	00H	Message Value Register This is a 8-bit register	78
ISTA1	RD	0EH	00H	Interrupt Status Register 1 This is a 8-bit register	78
IESTA	RD	10_H	0000_H	Interrupt Error Status Register	93
INTM1	RD/WR	12H	3DH	Interrupt Mask Register This is a 8-bit register	81
INTEM	RD/WR	14_H	$FF3F_H$	Interrupt Error Mask Register	93
IDC	RD	$1C_H$	IDCODE	IDCODE Register This is a 8-bit register	94
TSVC	RD	$1E_H$	$XXXX_H$	Time-Slot Value / Configuration Register	94

5.4 Detailed Register Description For 16-Bit Interface

Source Address Register RD/WR Address: 00**H**

Reset value: 0000**H**

SA

15	14	13	12	11	10	9	8
TSA7	TSA6	TSA5	TSA4	TSA3	TSA2	TSA1	TSA0
7	6	5	4	3	2	1	0
BT	0	0	PA4	PA3	PA2	PA1	PA0

High See Input Time-Slot Address Register on page **61**

Low See Source Port Address Register on page **61**

Destination Address Register RD/WR Address: 02**H**

Reset value: 0000**H**

DA

15	14	13	12	11	10	9	8
TSA7	TSA6	TSA5	TSA4	TSA3	TSA2	TSA1	TSA0
7	6	5	4	3	2	1	0
BT	0	0	PA4	PA3	PA2	PA1	PA0

High See Output Time-Slot Address Register on page **62**

Low See Destination Port Address Register on page **62**

General Input Register RD/WR Address: 04**H**

Reset value: 0000**H**

GI

15	14	13	12	11	10	9	8
GV15	GV14	GV13	GV12	GV11	GV10	GV9	GV8
7	6	5	4	3	2	1	0
GV7	GV6	GV5	GV4	GV3	GV2	GV1	GV0

GV15..0 General Value

GV15..8 See General Input Register 2 on page **65**

GV7..0 See General Input Register 1 on page **63**

Connection Command Register 16-bit RD/WR Address: 06**H**

Reset value: 0000**H**

CC16

15	14	13	12	11	10	9	8
0	0	OSCA2	OSCA1	OSCA0	ISCA2	ISCA1	ISCA0
7	6	5	4	3	2	1	0
I3	I2	I1	I0	CC3	CC2	CC1	CC0

High See Subchannel Address Register on page **62**

Low See Connection Command Register on page **66**

Interrupt Error Status Register RD Address: 10**H**

Reset value: 0000**H**

IESTA

15	14	13	12	11	10	9	8
CON	PLL	FRC	SC2	SC	C2	C4	C16/S
7	6	5	4	3	2	1	0
0	0	NR2	NR1	CTB	CTA	NW2	NW1

High See Interrupt Error Status Register 2 on page **80**

Low See Interrupt Error Status Register 1 on page **79**

Interrupt Error Mask Register RD/WR Address: 14**H**

Reset value: FF3F**H**

INTEM

15	14	13	12	11	10	9	8
CON	PLL	FRC	SC2	SC	C2	C4	C16/S
7	6	5	4	3	2	1	0
0	0	NR2	NR1	CTB	CTA	NW2	NW1

High See Interrupt Error Mask Register 2 on page **83**

Low See Interrupt Error Mask Register 1 on page **82**

IDCODE Register RD Address: 1C**H**

Reset value: IDCODE

	7	6	5	4	3	2	1	0
IDC	IDC7	IDC6	IDC5	IDC4	IDC3	IDC2	IDC1	IDC0

IDC7..0 IDCODE refer to **Table 16**

Time-Slot Value / Configuration RegisterRD Address: 1E**H**

Reset value: XXXX**H**

	15	14	13	12	11	10	9	8
TSVC	TSVC15	TSVC14	TSVC13	TSVC12	TSVC11	TSVC10	TSVC9	TSVC8
	7	6	5	4	3	2	1	0
	TSVC7	TSVC6	TSVC5	TSVC4	TSVC3	TSVC2	TSVC1	TSVC0

TSVC15..8 Configuration and Connection Data Memory (refer to page **89**)

TSVC7..0 Time-Slot Value (refer to page **85**)

6 Programming the Device

The register set consists of parameter registers (**SPA**, **ITSA**, **SCA**, **DPA**, **OTSA**, **GI1**..), command registers (**CCMD**, **CMD1**, **CMD2**) and status registers (**ISTA1**, **IESTA1**, **IESTA2**). Please note that some bits contained in the register **ISTA1** (Interrupt Status Register 1) do not generate any interrupt, for more details see the paragraph **Chapter 6.2**.

Before issuing a command the parameter registers have to be written accordingly. A connection command can only be issued if the connection command register is ready to be written to (see **Figure 25**). The connection command register status is shown with the RDY bit in the **ISTA1** register. A detailed description for the read and write access to the command registers can be found in **Chapter 6.1**.

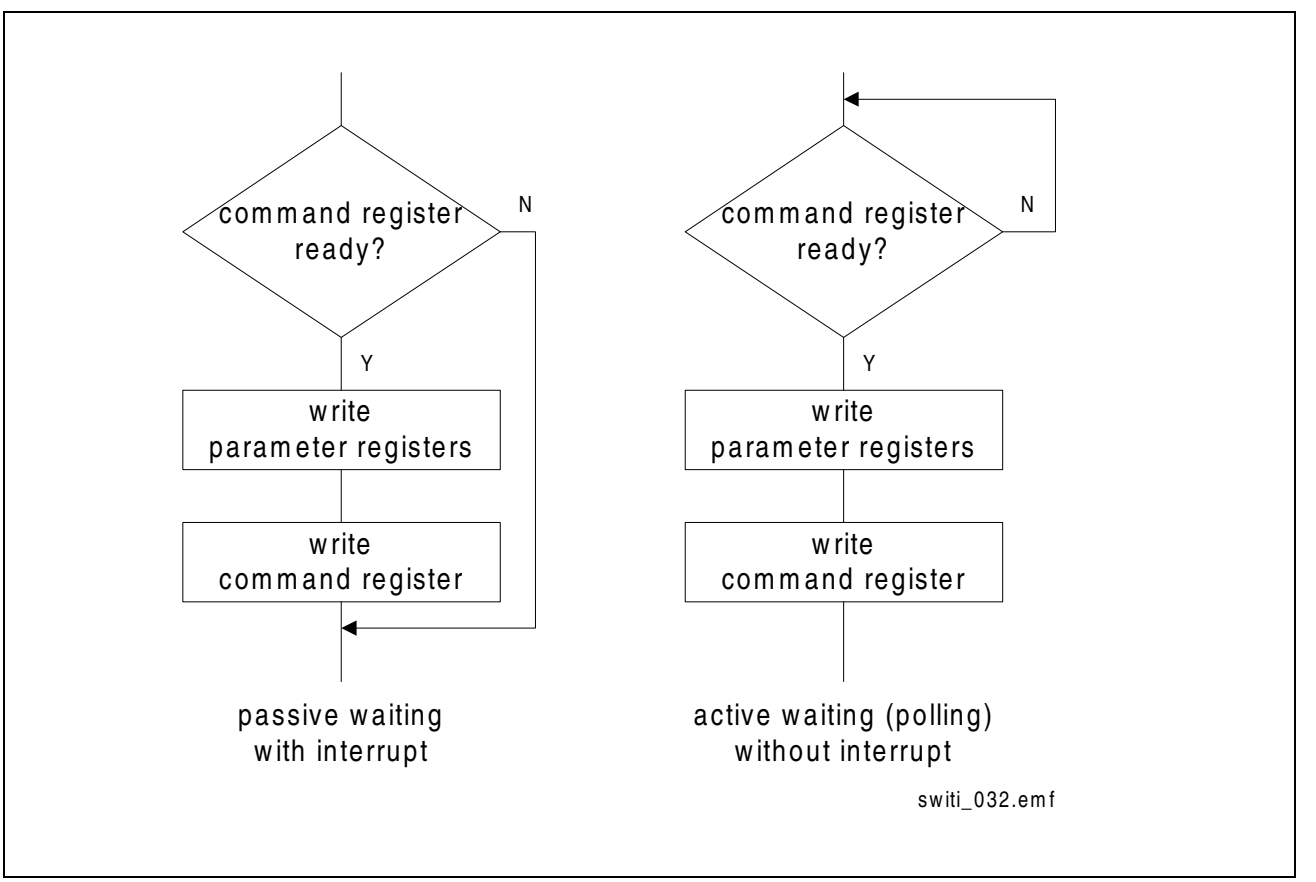


Figure 25 Order of Register Access

6.1 Read and Write Access

For the read and write access it is necessary to distinguish between a connection and configuration command. The connection command register is used to establish a connection (described in **Chapter 6.11**) and the configuration registers are used to configure the device, i.e. set the clock frequency.

If the **ISTA1**:RDY bit is set the connection command register is ready to receive data from the µP interface. If the parameter register and the connection command register are written the RDY bit will be reset from the internal controller. If the connection is established the internal controller will set the RDY bit and the connection command register is ready for the next write or read access. The **ISTA1**:RDY can be enabled to generate an interrupt to indicate that the device is ready to receive the data, otherwise the µP must poll the **ISTA1**:RDY bit.

The configuration command register works independent from the RDY bit.

Note: There must be a recovery time period of 120 ns after every configuration command write access to the next write access (command or parameter register).

6.2 Interrupt Handling

The SWITI interrupt concept consists of four interrupt status register with their corresponding mask register. The five interrupt status register can be divided in one main register, and two error interrupt register, one general purpose interrupt register and one time-slot value register. Every secondary status register and the time-slot value register has a bit in the main register to indicate the set of an interrupt in the assigned error or general purpose register or to indicate a new value in the time-slot value register.

The interrupt status register can be read via the microprocessor interface. The NFC and RDY will be set and reset from the internal controller.

When an interrupt occurs one or more of the bit GPIO, TSA, ER2, or ER1 is set, then the assigned secondary interrupt status register or time-slot value register must be read first in order to check for the cause of the interrupt. After a secondary status register read access, the error status register and the corresponding bit in the Interrupt Status Register 1 (ISTA1) will be reset.

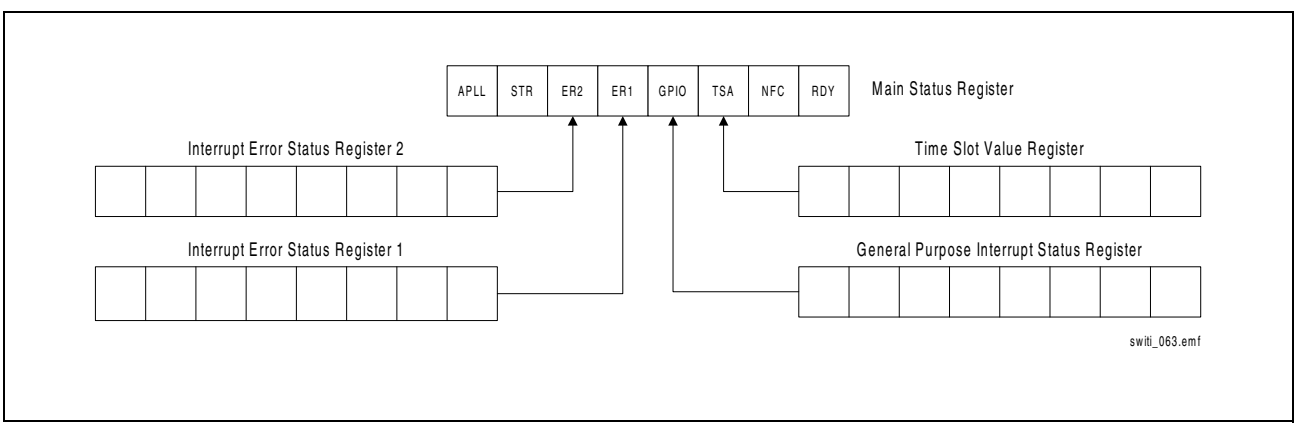


Figure 26 8-bit µP Access Interrupt Structure

The IREQ output is level active. It stays active until all interrupt sources have been serviced. If a new status bit is set while an interrupt is being serviced (µP read access), the IREQ pin stays active. For the duration of a write access to the **INTM1** register the IREQ line is deactivated. When using an edge-triggered interrupt controller, it is thus recommended to rewrite the **INTM1** register at the end of any interrupt service routine.

APLL, STR, RDY and NFC Bits

If the internal controller does set the RDY bit for the first time and the bit is not masked an interrupt will be generated. If the µP reads the **ISTA1** register the interrupt will be deactivated. The RDY bit is still active and can be reset from the internal controller.

The NFC, STR and APLL bits are not set by any interrupt and therefore can not be masked. Setting these bit does not generate any interrupt. The NFC bit is set from the internal controller if no further connections can be established. The STR bit is set from the internal stream to stream controller if a stream to stream connection is configured. The APLL bit is set from the internal analog PLL controller if the PLL is locked.

Masking Interrupts

If an interrupt is not masked (enabled) the IREQ pin will be active if one of the status bits in the interrupt status register is set. The mask bit prevents that the IREQ pin will be active if the status bit is set. The mask bits for the error status registers or general purpose interrupt register disables the interrupt indication for the interrupt status register. Only the interrupt status register can set the IREQ pin if the bit is not masked.

Interrupt Structure for a 16-bit Microprocessor Access

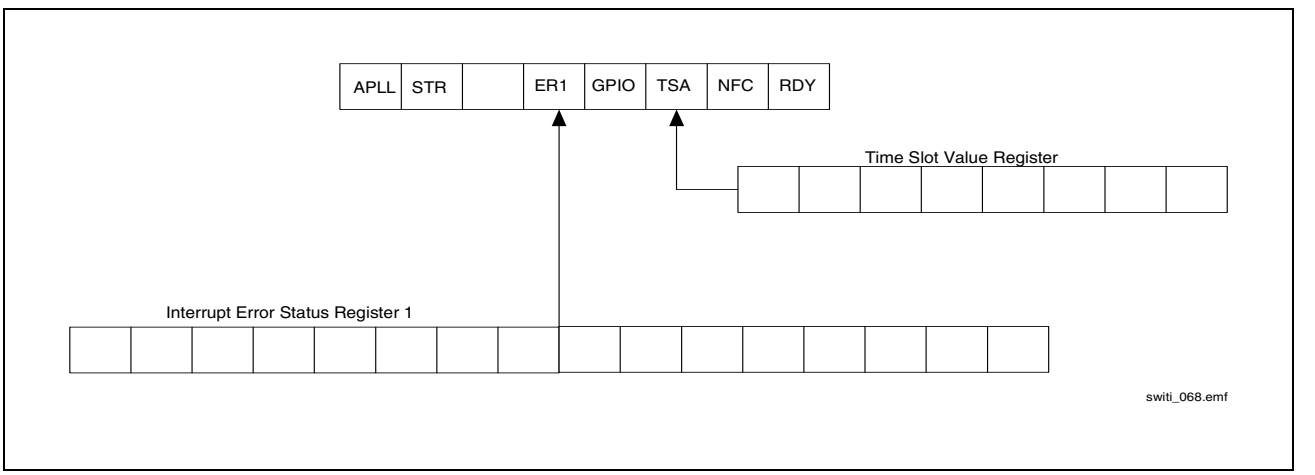


Figure 27 16-bit µP Access Interrupt Structure

In opposite to the 8-bit µP access there is only one bit (ER1) to indicate a change in the 16-bit Interrupt Error Status Register 1.

6.3 Command and Register Overview

The following table (Table 22) shows which parameter registers are considered by issuing an appropriate connection command.

Table 22 Affected Registers for Connection Commands

Command	Registers								
	SPA	ITSA	SCA	DPA	OTSA	MV	GI1	GI2	CON
Connect/Disconnect (without subchannels)	x	x		x	x				
Connect (with subchannels)	x	x	x	x	x				
Disconnect (with subchannels)	x	x		x	x				
Send Message				x	x	x			
Stop Message				x	x				
Disconnect Part of Broadcast (without subchannels)	x	x		x	x				
Disconnect Part of Broadcast (with subchannels)	x	x	x	x	x				
Multipoint Connect/ Disconnect	x	x		x	x				
Bidirectional Connection	x	x		x	x				
Disconnect All									
Memory Dump (Connection and Data Memory)									x

The following table (Table 23) shows which parameter registers are considered by issuing an appropriate configuration command.

Table 23 Affected Registers for Configuration Commands

Command	Registers									
	CMD1	CMD2	SPA	ITSA	SCA	DPA	OTSA	GI1	GI2	TSV
Set H.1x0 Master/ Slave	x									
PLL Primary Master Ref.	x							x		
PLL Secondary Master Ref.	x							x		
PLL Source Selection	x									
H.100/H.110 Clock Output	x									
PCM Clock Output	x									
Comp. Clock Output	x									
CT_NETREF_1(2) Output	x									
H.100/H.110 Fallback	x									
Set Bit Rate Local Bus	x		x			x				
Set Bit Rate H.100/H.110	x		x							
Read Time-Slot	x		x	x		x	x			
Stream to Stream Switch	x		x			x				
Clock Shift	x		x					x		
External Input Frequency		x								
Set Parallel Mode		x								
Set IREQ Pin		x								

Table 23 Affected Registers for Configuration Commands (cont'd)

Command	Registers									
	CMD1	CMD2	SPA	ITSA	SCA	DPA	OTSA	GI1	GI2	TSV
PCM and H.1x0 Standby		x								
Set Loop		x								
Frame Signal		x						x	x	
GPCLK Clock		x						x		
Set Range of Data Rate		x								
Read Configuration		x								x
Read GPCLK Configuration		x								x
Read PCM Line Configuration		x								x
Read H.1x0 Line Configuration		x								x
Read Bit Shift Configuration		x								x
Software Reset		x								

The command registers have the following structure:

7	6	5	4	3	2	1	0
I3	I2	I1	I0	CC3	CC2	CC1	CC0

CC3..0 is the command code and I3..0 is the parameter code.

The following tables (**Table 24** to **Table 25**) show all valid values of command and parameter codes and the related function.

Table 24 Connection Command and Parameter Codes

Command[1)]	Command Code (low nibble)	Parameter Code (high nibble)	Note
Constant Delay Connect Disconnect	1_H 5_H	0_H 1_H 2_H 3_H	address 8-bit connections address 4-bit connections address 2-bit connections address 1-bit connections
Minimum Delay Connect	2_H	x_H	
Send Message	3_H	x_H	
Stop Message	4_H	x_H	
Disconnect Part of Broadcast	6_H	0_H 1_H 2_H 3_H	address 8-bit connections address 4-bit connections address 2-bit connections address 1-bit connections
Multipoint Connect	7_H	0_H 1_H	OR connection of time-slots AND connection of time-slots
Disconnect All	8_H	x_H	
Bidirectional Connect	9_H	0_H 1_H	minimum delay constant delay
Memory Dump	A_H	0_H 1_H	disable enable

1) The input port is determined in SPA Bit4..0 and the output port in DPA Bit4..0. The input time-slot is determined in ITSA and the output time-slot in OTSA.

Table 25 Configuration Command 1 and Parameter Codes

Command	Command Code (low nibble)	Parameter Code (high nibble)	Note
Set Bit Rate Local Bus[1]	B_H	$0\text{-}3_H$ $4\text{-}7_H$ $8\text{-}B_H$ $C\text{-}F_H$	no effect set bit rate of local input port (2/4/8/16 Mbit/s) set bit rate of local output port (2/4/8/16 Mbit/s) set for both input and output (2/4/8/16 Mbit/s)
Set Bit Rate H.100/H.110 Bus[2]	C_H	0_H 1_H 2_H 3_H	set bit rate of port# to 2 Mbit/s set bit rate of port# to 4 Mbit/s set bit rate of port# to 8 Mbit/s set bit rate for all ports to 8 Mbit/s
Read Time-Slot[3]	D_H	0_H 1_H	read time-slot of input port read time-slot of output port
Stream-to-Stream[4]	E_H	0_H 4_H 1_H 5_H 2_H 6_H 3_H 7_H $8_H\text{-}FF_H$	Release Connection w. Mode 0[5] Establish Connection w. Mode 0 Release Connection w. Mode 1 Establish Connection w. Mode 1 Release Connection w. Mode 2 Establish Connection w. Mode 2 Release Connection w. Mode 3 Establish Connection w. Mode 3 Release all programmed stream to stream connections
Bit Shift[6]	F_H	0_H 1_H 2_H 3_H	set bit shift of input line set bit shift of all input lines set bit shift of all output lines set bit shift of all input and output lines

1) the input and output port is determined in **SPA**, **DPA**

2) the port is determined in **SPA**

3) the time-slot is determined in **SPA** and **ITSA** or **DPA** and **OTSA**

4) source and destination are determined in **SPA**, **DPA**

5) see **“Stream-to-Stream Connection Mapping” on page 28**

6) the input line is determined in **SPA**, the shift information in **GI1**

Table 26 Configuration Command 2 and Parameter Code

Command	Command Code (low nibble)	Parameter Code (high nibble)	Note
External Frequency	1_H	0_H 1_H	set frequency to 32.768 MHz set frequency to 16.384 MHz
Parallel Mode	2_H	0_H 1_H	disable enable = first 8 local input bus lines are parallel and first 8 local output lines are parallel
Set IREQ Pin	3_H	0_H 1_H 2_H 4_H 5_H 6_H	IREQ is active low, timer = 20 ns IREQ is active high, timer = 20 ns IREQ as open-drain, timer = 20 ns IREQ is active low, timer = 300 ns IREQ is active high, timer = 300 ns IREQ as open-drain, timer = 300 ns
PCM - H.1x0 Standby	4_H	0_H 1_H 2_H 3_H	disable PCM and H-Bus enable PCM and disable H-Bus disable PCM and enable H-Bus enable PCM and H-Bus
Loop	5_H	0_H 1_H 2_H 3_H	no loop at all enable PCM and disable H-Bus loop disable PCM and enable H-Bus loop enable PCM and H-Bus loop
Frame Signal[1)]	6_H	$0XXX_b$ $1XXX_b$	signal is high active signal is low active XXX is the line address
GPCLK as Clock[2)]	7_H	0_H-7_H	parameter code is line address
Range of Data Rate	8_H	0_H-6_H 8_H-A_H	logical OR connection from min. and max. codes

Table 26 Configuration Command 2 and Parameter Code (cont'd)

Command	Command Code (low nibble)	Parameter Code (high nibble)	Note
Read Configuration[3)]	9_H	0_H	Master/Slave configuration
		1_H	PLL Primary Reference - Master
		2_H	PLL Secondary Ref. - Master
		3_H	PLL Source - Slave
		4_H	Clock Output Selection - H.1x0
		5_H	Clock Output Selection - PCM
		6_H	Clock Ouput Selection for Interoperability Signals
		7_H	Output Selection - CT_NETREF_1
		8_H	Output Selection - CT_NETREF_2
		9_H	H.1x0 Fallback - Phase Alignment
		A_H	External Input Frequency
		B_H	Parallel Mode
		C_H	IREQ Pin
		D_H	H.1x0/PCM Standby
		E_H	Loop
		F_H	Range of Data Rate
Read GPCLK Configuration[4)]	A_H	0_H-7_H	parameter code is line address
Read PCM Line Configuration[5)]	B_H	0_H	Data Rate of Input Line[6)]
		1_H	Data Rate of Output Line[7)]
Read H.1x0 Line Configuration[8)]	C_H	-	Data Rate of H.1x0 Line[9)]
Read Bit Shift Configuration[10)]	D_H	0_H	Shift Value for Input Line[9)]
		1_H	Shift Value for all Output Lines

1) offset and width are determined in **GI1** and **GI2**

2) frequency is determined in **GI1**

3) The result can be read from the **TSV** register

4) The result can be read from the **TSV** and **CON** register

5) The result can be read from the **TSV** register

6) **SPA** must be used for line number

7) **DPA** must be used for line number

8) The result can be read from the **TSV** register

9) **SPA** must be used for line number

10) The result can be read from the **TSV** register

6.4 Indirect Configuration Register Access

It is possible to read the current SWITI configuration with an indirect register access for analyze and test purpose. There are five commands in the **CMD2** register which can be used to read the configuration. The clock generator output signal and external configuration for the SWITI can be read with the 'Read Configuration Command'. The four instruction bits select one possible configuration command. The current configuration is determined by the command written in the **TSV** register. The configuration information for every command can be found on **page 58**.

The line configuration can be read with two commands 'Read PCM Line configuration' and 'Read H.1x0 Line configuration'. Before one of these commands will be issued the **SPA** or **DPA** register must be written with the port number. The configuration for the selected line is written in the **TSV** register by the internal controller. The interrupt handling is described in **Chapter 6.2**. The bit shift configuration can be read with the command 'Read Bit Shift Configuration' and the dataflow is the same as described above.

With the command 'Read GPCLK Configuration' it is possible to read the configuration for every GPCLK line. If this command was written the configuration can be read from the **TSV** and **CON** register. The **CON** register is not interrupt controlled and will keep the last data after a microprocessor read access.

To read the correct configuration data from the **TSV** register it is not allowed to use the command "Read Time-Slot Value" before the **TSV** register was read.

6.5 Initialization Procedure

After the reset process the PLL, H.1x0 interface, PCM interface, and some other signals need to be initialized.

Since the SWITI offers the possibility to use two different external crystal/oscillator frequencies the command 'Set external frequency' must be used first to set the correct frequency and to set the correct value of the input frequency for the APLL. After approximately 750 µs the APLL is locked and the APLL status bit is set and the next commands can be written.

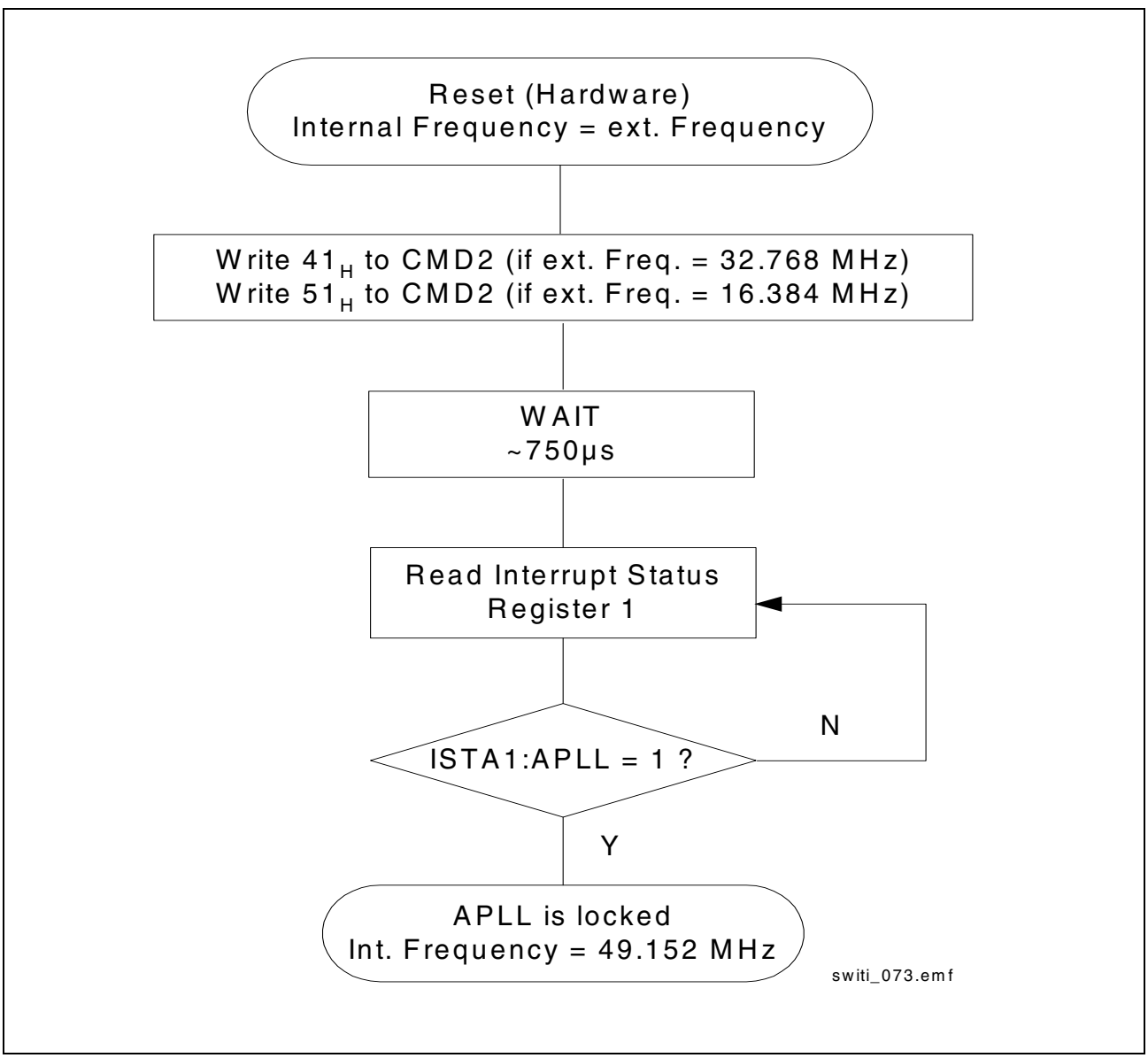


Figure 28 Initialization Procedure after Reset

After this initialization procedure the different functional blocks of the SWITI can be programmed.

– H.1x0 Interface
– PCM Interface
– Interrupt's and IREQ Pin
– GPCLK's and Frame Signals
– General Purpose Interface

6.6 H.1x0 Clocking Unit

If the HTSI in H-mode is used the the clock generator (PLL) for the H.1x0 interface must be programmed first. This chapter can be skipped for the M-mode.

For the PLL synchronization please refer to **Chapter 3.4.5** on **page 36**.

They are three program sequences for the H.1x0 interface:

– Program the H.1x0 fallback mechanism and PLL inputs for H.1x0 master or slave
– Program all output clock signals for the master configuration
– Program the frame signals for the slave configuration

Program the PLL Source and H.1x0 Clock Fallback

The program sequence for the PLL source programming and/or H.1x0 clock fallback must be finished with the command 'H.1x0 Master/Slave Selection' in the **CMD1** register.

Whenever the PLL source or the H.1x0 clock fallback was changed the H.1x0 Master/ Slave Selection' command must be programmed after this changes

Example:

A typical H.100 master or slave configuration is shown in **Figure 29**.

Slave Configuration:

– CT_C8_A as PLL input reference
– Enable clock monitoring (CT_C8_A, CT_C8_B)
– Enable automatic clock fallback from CT_C8_A to CT_C8_B

H.100 Primary Master Configuration:

– NTWK_1 = 8 KHz as primary PLL reference
– CT_NETREF = 1.544 MHz as fallback PLL reference
– Enable automatic clock fallback for the primary master
– Enable automatic switch back to NTWK_1 if NTWK_1 returns

H.100 Secondary Master Configuration

– CT_C8_A as primary PLL reference
– NTWK_1 = 8 KHz as fallback PLL reference
– Enable automatic clock fallback for the secondary master to NTWK_1

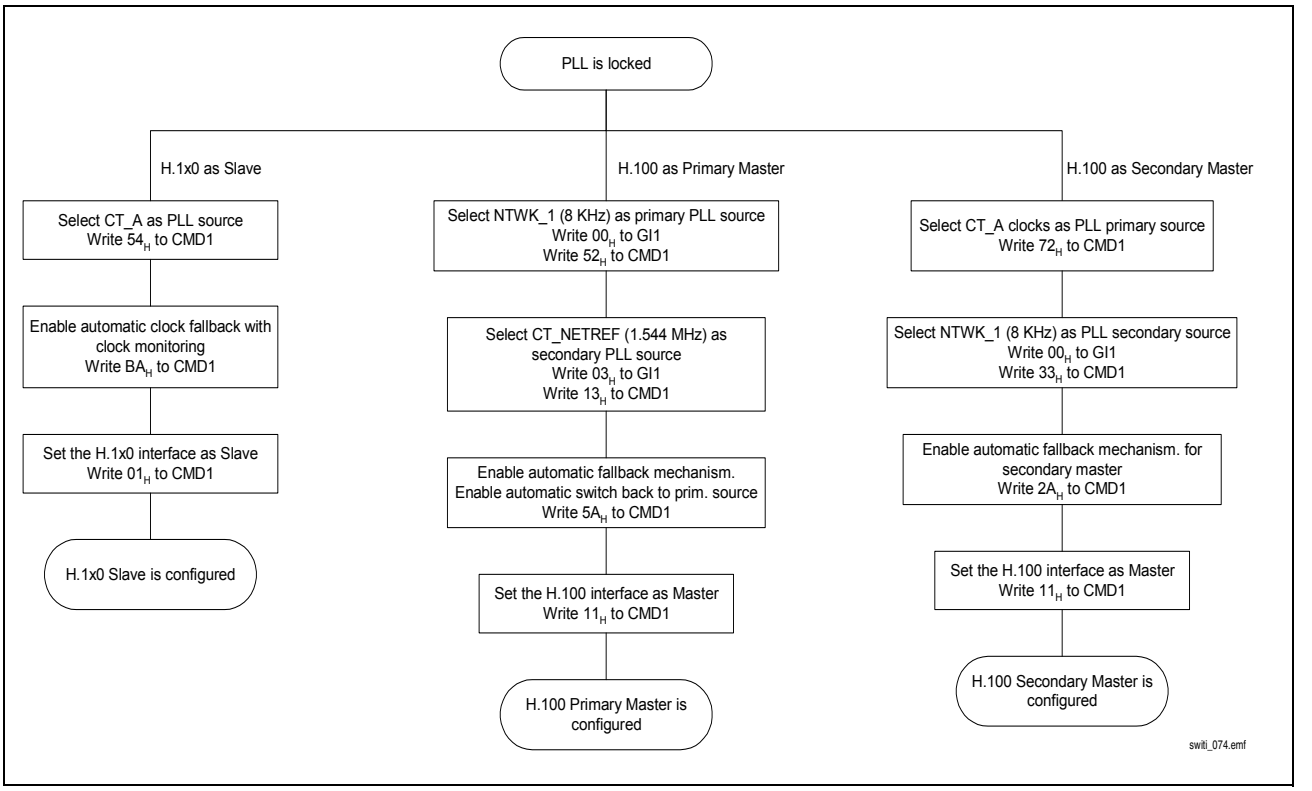


Figure 29 H.100 Master and Slave Configuration Process

Program the Output Clocks

Example:

HTSI in H-Mode is configured as H.100 primary master and CT_C8_A with / CT_FRAME_A shall be driven and the MVIP-90 clock signals shall be driven.

If H.100 primary master is configured then

– Write 15_H to **CMD1**
– Write 17_H to **CMD1**

Example:

HTSI in H-Mode is configured as H.100 secondary master and the CT_B clocks shall be driven.

If H.100 secondary master is configured then

– Write 25_H to **CMD1**

Example:

HTSI in H-Mode is configured as H.100 slave and the CT_NETREF_1 signal shall be provided. The signal is inverted and the source signal is NTWK_1.

If H.100 slave is configured then

– Write 38_H to **CMD1**

6.7 PCM Clocking Unit

If the HTSI in H-mode is used the H.1x0 clock generator must be programmed first. The PCM clock signals for the line interface will be provided from external PCM devices if the SWITI is used as PCM clock slave or will be provided from the internal PLL if the SWITI is used as PCM clock master. This PCM clock configuration can be programmed with the special command 'PCM Input/Output Selection' in the **Figure CMD1** register.

For the PLL synchronization please refer to **Chapter 3.4.5** on **page 36**.

Example:

HTSI in M-Mode as PCM clock master, PLL reference is NTWK_1 with 8 KHz and PDC is driven with 8.192 MHz and PFS is driven.

– Write 00_H to **GI1**
– Write 52_H to **CMD1**
– Write $B6_H$ to **CMD1**

Example

HTSI in M-Mode as PCM clock slave, PLL reference is PDC with 4.096 MHz.

– Write 05_H to **GI1**
– Write 22_H to **CMD1**
– Write 26_H to **CMD1** (PDC = 4.096 MHz and PFS as input)

6.8 H.1x0/PCM Line Interface

6.8.1 Standby Command

All H.1x0 and PCM lines are in a high impedance state after the reset process. If they are configured (data rate, bit shift) they can be enabled with the standby command. During the normal operation the PCM and H.1x0 lines can be enabled or disabled with the standby command. If the lines are disabled the device works internally like an active device.

Example:

Set all output PCM lines to high impedance.

– Write 24_H to **CMD1** (I1 must be set to '1' because only PCM shall be tristated)

6.8.2 Determining Clock Rates

The data rate range command is necessary to optimize the minimum delay feature. After the reset process the device assumes a bit rate of 2.048 Mbit/s for all PCM and H.1x0 lines. The command must be issued if other data rates are used.

Example (8-bit µP interface):

1. Specify that only 2.048 Mbit/s and 4.096 Mbit/s are used for following Set Bit Rate Command.
   – Write 38_H to **CMD2**

2. Set bit rate of 4.096 Mbit/s on local bus input line 8 and local bus output line 1
   – Write 08_H to **SPA**
   – Write 01_H to **DPA**
   – Write DB_H to **CMD1**

3. Set bit rate of 2.048 Mbit/s on H-bus line 8
   – Write 88_H to **SPA**
   – Write $0C_H$ to **CMD1**

Example (16-bit µP interface):

1.
   – Write 38_H to **CMD2**
2.
   – Write 0008_H to **SA**
   – Write 0001_H to **DA**
   – Write DB_H to **CMD1**

3.
   – Write 0008_H to **SA**
   – Write $0C_H$ to **CMD1**

6.8.3 Performing Bit Shifting

The bit shift is performed on half-bit steps, not on a clock basis. It is a true bit shift, it means that with a data rate equals to the data clock frequency (e.g. 4.096 Mbit/s with 4.096 MHz data clock) programming a bit shift of 1-bit results on a shift of 1 clock period, and programming a shift of half-bit the result is a shift of half clock period. Running in double data clock rate (e.g. 4.096 Mbit/s with 8.192 MHz data clock), a bit shift of 1-bit results on a shift of 2 clock periods and a shift of half-bit will result on a shift of 1 clock period.

6.8.3.1 Input Bit Shifting

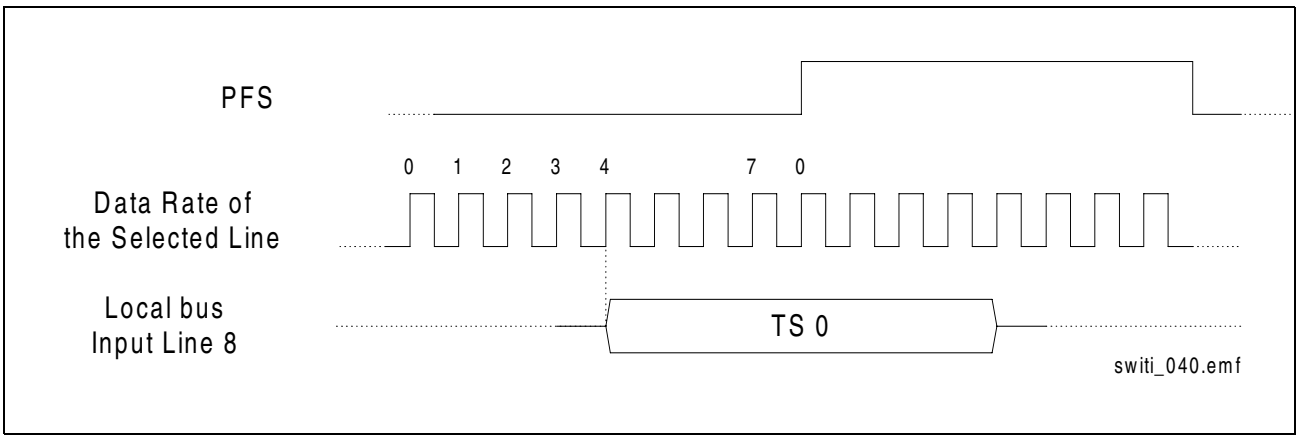


Figure 30 Example: Input Bit Shifting

Example (8-bit µP interface):

Begin time-slot 0 of local input line 8 with the 4th rising edge relative to one byte before the PFS rising edge. The bits are internally sampled with the falling edge.

- Write 08_H to **SPA**
- Write 08_H to **GI1**
- Write $0F_H$ to **CMD1**

Example (16-bit µP interface):

- Write 0008_H to **SA**
- Write 0008_H to **GI**
- Write $0F_H$ to **CMD1**

6.8.3.2 Output Bit Shifting

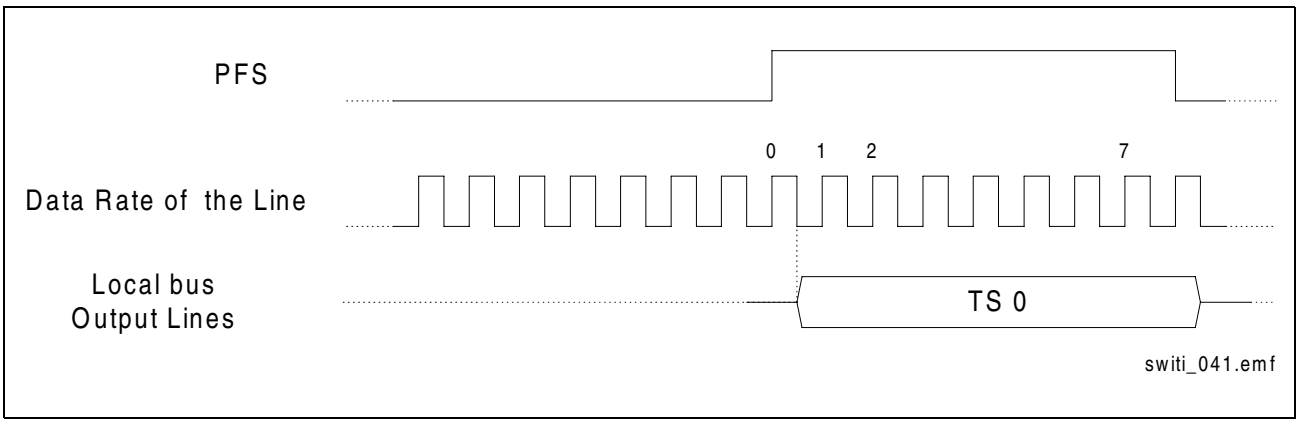


Figure 31 Example: Output Bit Shifting

Example (8-bit µP interface):

Output time-slot 0 of all output lines begins with the first falling edge relative to the first byte after PFS rising edge. The bits are internally sampled with the rising edge.

- Write 01_H to **GI1**
- Write $2F_H$ to **CMD1**

Example (16-bit µP interface):

- Write 0001_H to **GI**
- Write $2F_H$ to **CMD1**

6.9 Global Clock Signals

6.9.1 Framing Groups

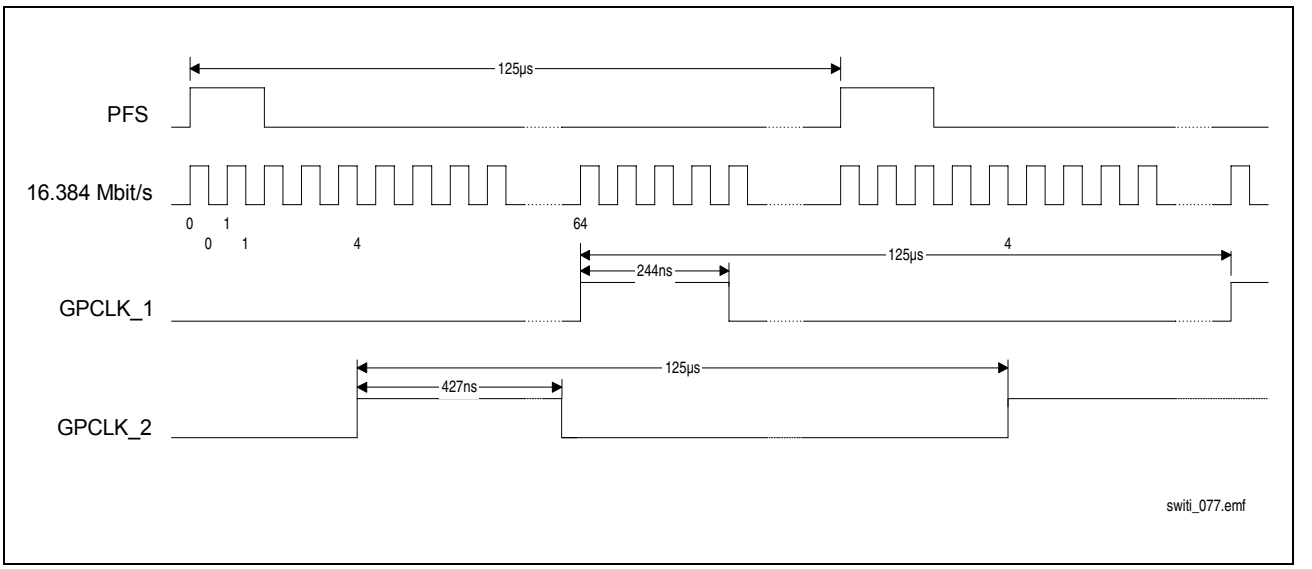


Figure 32 Example Framing Groups

Example (8-bit µP interface):

Frame signal on GPCLK_1 starts with the rising edge of 64th clock cycle and the length is set to 244 ns (4 x 61 ns).

- Write 00_H to **GI1**
- Write 61_H to **GI2**
- Write 16_H to **CMD2**

Frame signal on GPCLK_2 starts with the falling edge of the 4th clock cycle and the length is set to 427 ns (7 x 61 ns).

- Write 12_H to **GI1**
- Write $C0_H$ to **GI2**
- Write 26_H to **CMD2**

Example (16-bit µP interface):

- Write 6100_H to **GI2**
- Write 0016_H to **CMD2**

- Write $C012_H$ to **GI2**
- Write 0026_H to **CMD2**

6.10 Read Time-Slot Value

By issuing this command the time-slot value appears in the register **TSV** after arriving and an interrupt will be caused and a new read time-slot value will be accepted. The command has to be issued for every read request. The current TSV data will be overwritten if the read time-slot command is issued.

Example (8-bit µP interface):

Read time-slot 10 of local bus input line 3

- Write 03_H to **SPA**
- Write $0A_H$ to **ITSA**
- Write $0D_H$ to **CMD1**

Example (16-bit µP interface):

- Write $0A03_H$ to **SA**
- Write $0D_H$ to **CMD1**

Wrong Time-Slot and Time-Out

In some case it could be happen that the µP tries to read a wrong time-slot. A wrong time-slot is defined as a invalid time-slot number for the selected data rate, i.e. data rate = 2 MBit/s and selected time-slot is 58. If the µP tries to read a wrong time-slot no interrupt would be generated and the controller doesn't accept any further commands. The SWITI has a integrated time-out counter to allow a new read time-slot command after the maximum of three frames.

6.11 Establish Connections

The following chapter describes the programming of several kinds of connections. The programming interface allows to program or re-program a connection during the normal switching mode.

Before a new connection for a specific output time-slot and line will be programmed the specific connection has to be released.

6.11.1 Establish 8-bit Connections

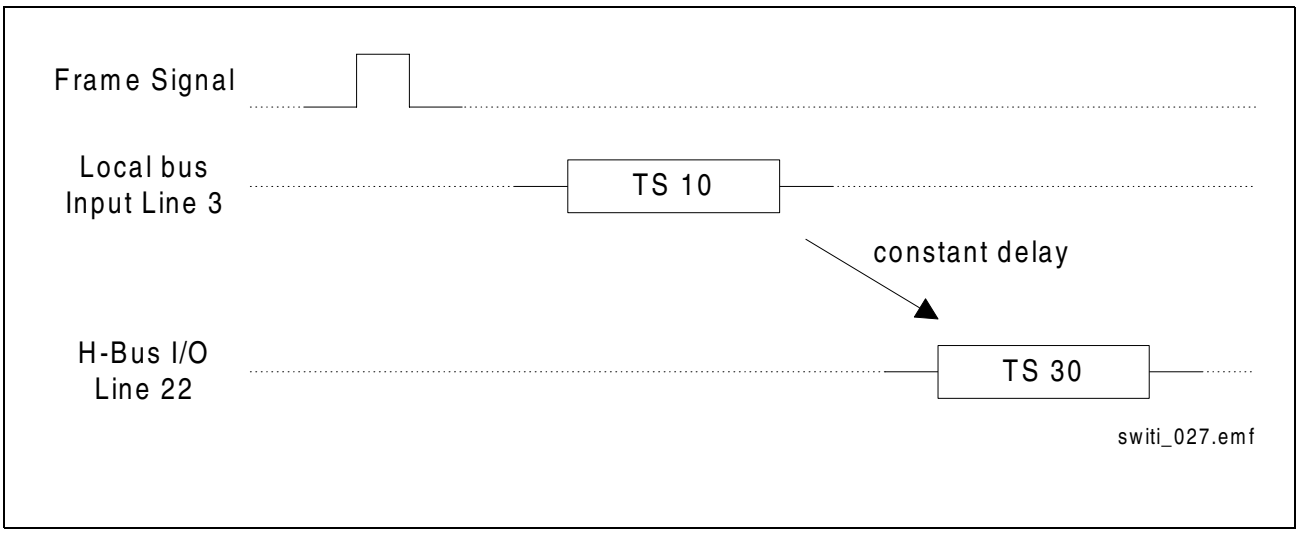


Figure 33 Example: 8-bit Connection

Example (8-bit µP interface):

Connect time-slot 10 of local bus line 3 with output time-slot 30 of H-Bus line 22 as a constant delay connection

- Write $0A_H$ to **ITSA**
- Write 03_H to **SPA**
- Write $1E_H$ to **OTSA**
- Write 96_H to **DPA**
- Write 01_H to **CCMD**

Example (16-bit µP interface):

- Write $0A03_H$ to **SA**
- Write $1E96_H$ to **DA**
- Write 0001_H to **CC16**

6.11.2 Subchannel Switching

With the subchannel address register (**SCA**) and the constant delay command it is possible to program 1,2, and 4 connections. The following figure explains the relation between the subchannel address and the corresponding bits in one time-slot.

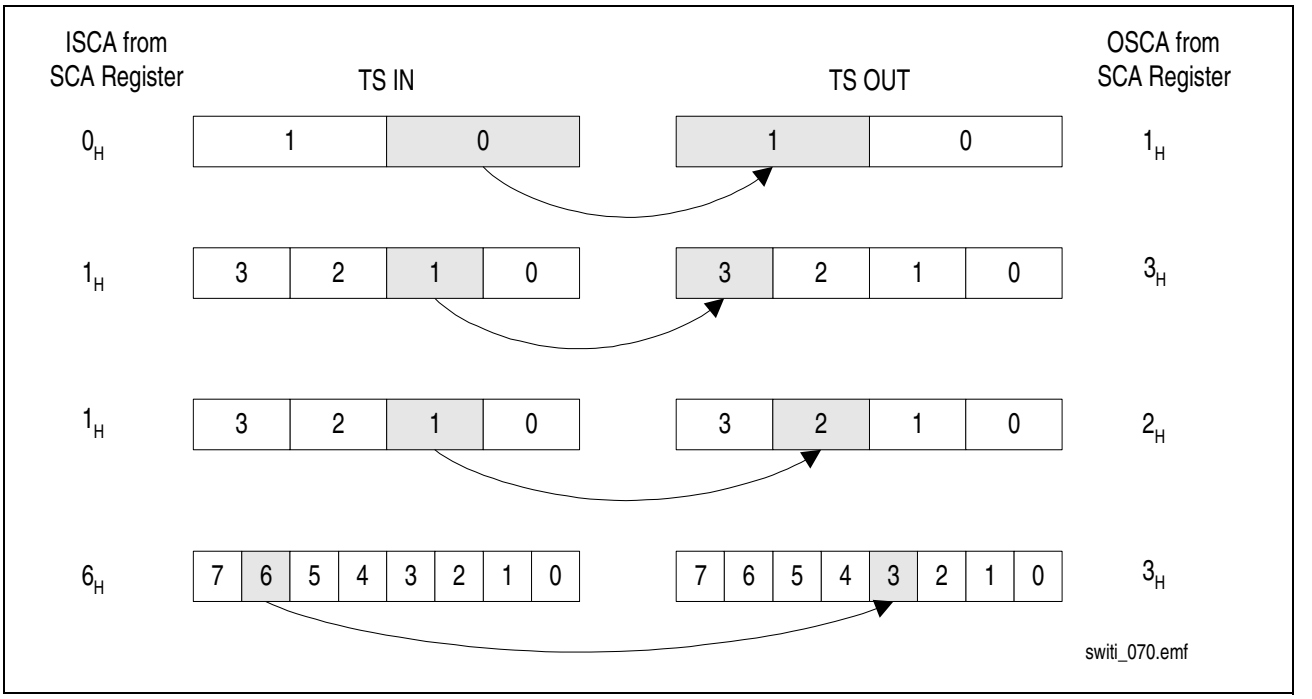


Figure 34 Subchannel Address in Time-Slot

6.11.2.1 Establish 4-bit Connections

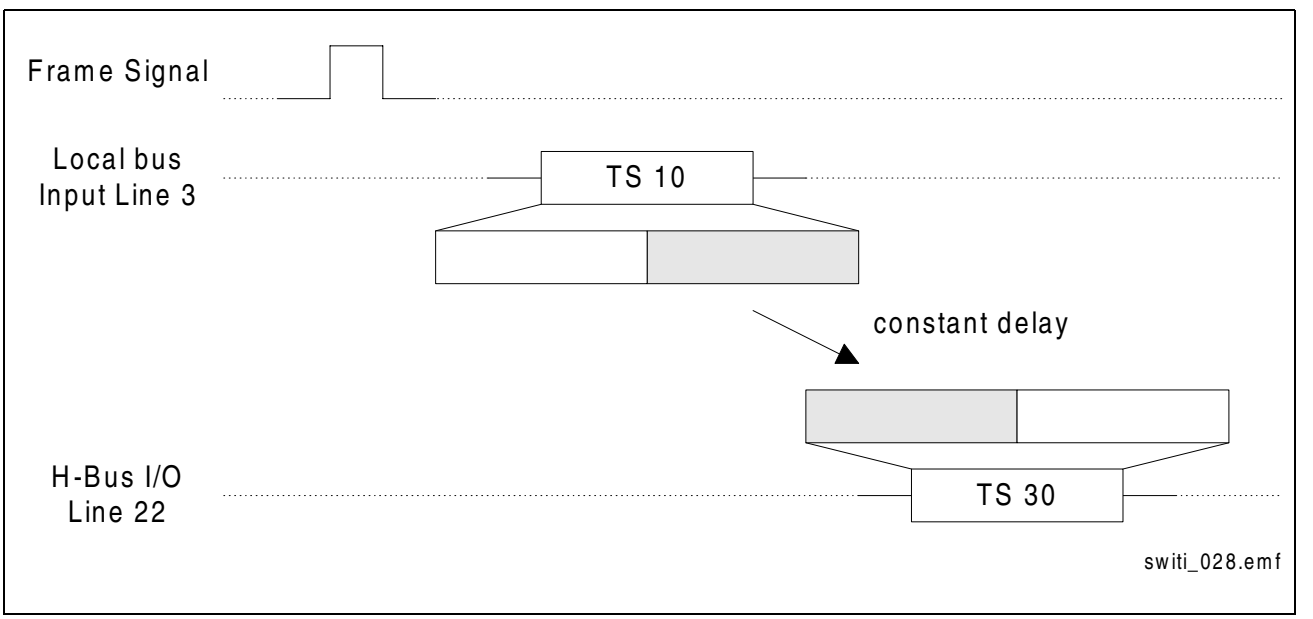


Figure 35 Example: 4-bit Connection

Example (8-bit µP interface):

Connect low nibble of time-slot 10 of local bus line 3 with high nibble of output time-slot 30 of H-Bus line 22 as a constant delay connection

- Write 08_H to **SCA**
- Write $0A_H$ to **ITSA**
- Write 03_H to **SPA**
- Write $1E_H$ to **OTSA**
- Write 96_H to **DPA**
- Write 11_H to **CCMD**

Example (16-bit µP interface):

- Write $0A03_H$ to **SA**
- Write $1E96_H$ to **DA**
- Write 0811_H to **CC16**

6.11.2.2 Establish 2-bit Connections

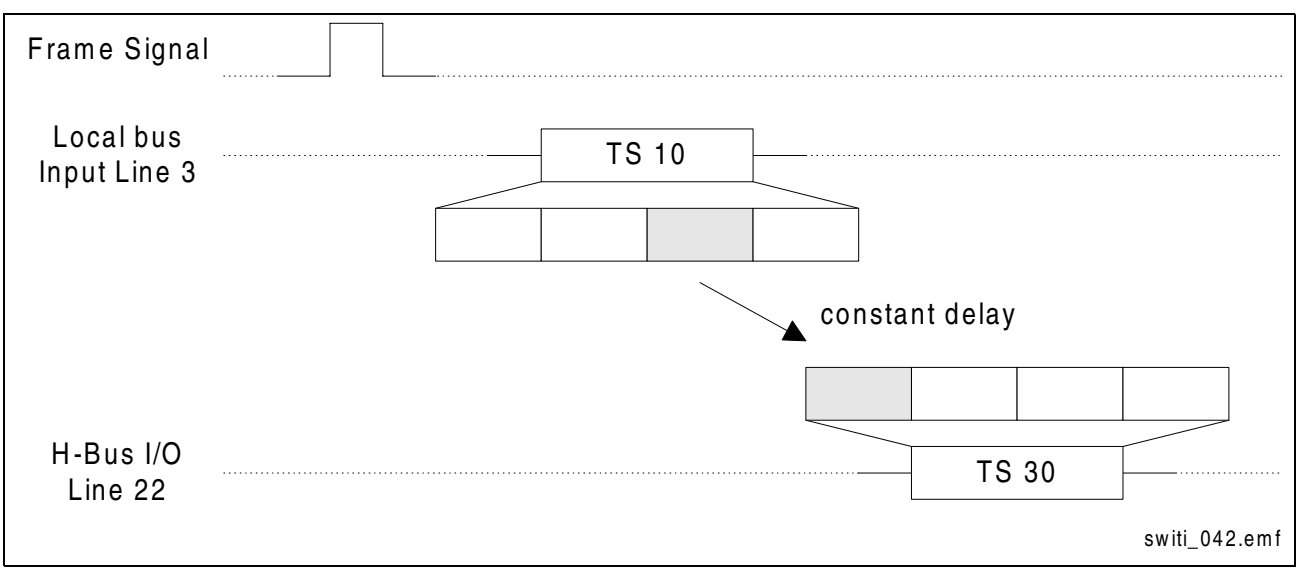


Figure 36 Example: 2-bit Connection

Example (8-bit µP interface):

Connect 2nd 2-bit subchannel of time-slot 10 of local bus line 3 with 4th 2-bit subchannel of output time-slot 30 of H-Bus line 22 as a constant delay connection

- Write 19_H to **SCA**
- Write $0A_H$ to **ITSA**
- Write 03_H to **SPA**
- Write $1E_H$ to **OTSA**
- Write 96_H to **DPA**
- Write 21_H to **CCMD**

Example (16-bit µP interface):

- Write $0A03_H$ to **SA**
- Write $1E96_H$ to **DA**
- Write 1921_H to **CC16**

6.11.2.3 Establish 1-bit Connections

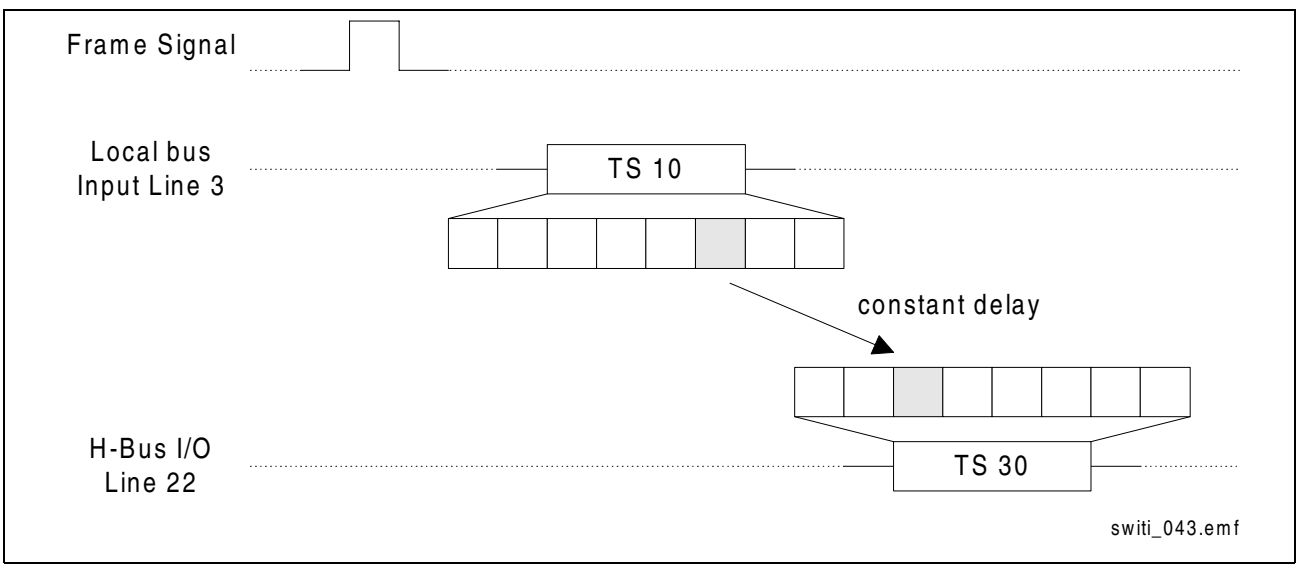


Figure 37 Example: 1-bit Connection

Example (8-bit µP interface):

Connect 3rd 1-bit subchannel of time-slot 10 of local bus line 3 with 6th 1-bit subchannel of output time-slot 30 of H-Bus line 22 as a constant delay connection

- Write $2A_H$ to **SCA**
- Write $0A_H$ to **ITSA**
- Write 03_H to **SPA**
- Write $1E_H$ to **OTSA**
- Write 96_H to **DPA**
- Write 31_H to **CCMD**

Example (16-bit µP interface):

- Write $0A03_H$ to **SA**
- Write $1E96_H$ to **DA**
- Write $2A31_H$ to **CC16**

6.11.3 Establish Broadcast Connections

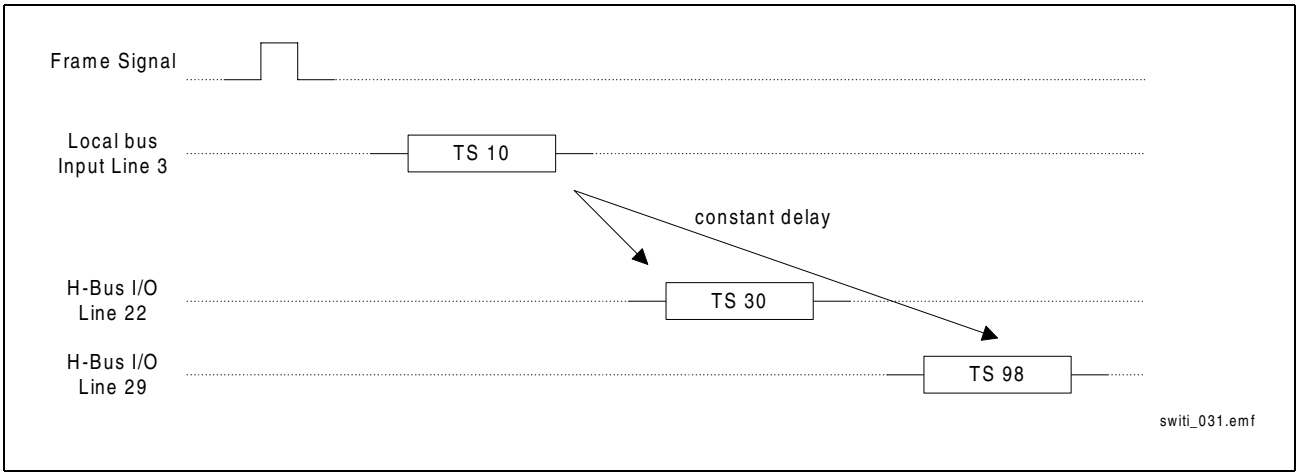


Figure 38 Example: Broadcast Connection

Example (8-bit µP interface):

Connect time-slot 10 of local bus line 3 with output time-slot 30 of H-Bus line 22 and output time-slot 98 of H-Bus line 29 in constant delay mode. If the connections are established consecutively it is not necessary to rewrite the source determining registers **ITSA** and **SPA** because they keep their values.

- Write $0A_H$ to **ITSA**
- Write 03_H to **SPA**
- Write $1E_H$ to **OTSA**
- Write 96_H to **DPA**
- Write 01_H to **CCMD**
- Write 62_H to **OTSA**
- Write $9D_H$ to **DPA**
- Write 01_H to **CCMD**

Example (16-bit µP interface):

- Write $0A03_H$ to **SA**
- Write $1E96_H$ to **DA**
- Write 0001_H to **CC16**
- Write $629D_H$ to **DA**
- Write 0001_H to **CC16**

6.11.4 Establish Subchannel Broadcast Connection

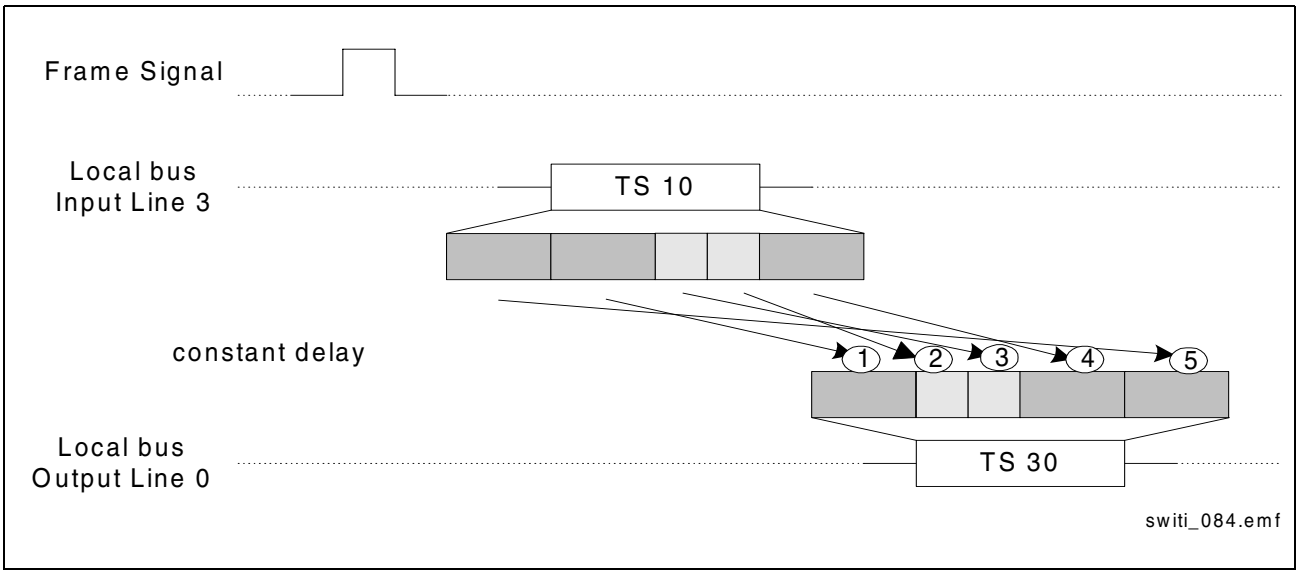


Figure 39 Example: Subchannel Broadcast Connection

- First Connection
  - Write 03_H to **SCA**
  - Write $0A_H$ to **ITSA**
  - Write 03_H to **SPA**
  - Write $1E_H$ to **OTSA**
  - Write 00_H to **DPA**
  - Write 21_H to **CCMD**
- Second Connection
  - Write $1A_H$ to **SCA**
  - Write $0A_H$ to **ITSA**
  - Write 03_H to **SPA**
  - Write $1E_H$ to **OTSA**
  - Write 00_H to **DPA**
  - Write 21_H to **CCMD**
- Third Connection
  - Write 23_H to **SCA**
  - Write $0A_H$ to **ITSA**
  - Write 03_H to **SPA**
  - Write $1E_H$ to **OTSA**
  - Write 00_H to **DPA**
  - Write 31_H to **CCMD**
- Fourth Connection
  - Write $2A_H$ to **SCA**
  - Write $0A_H$ to **ITSA**
  - Write 03_H to **SPA**

- Write $1E_H$ to **OTSA**
- Write 00_H to **DPA**
- Write 31_H to **CCMD**

– Fifth Connection
- Write 08_H to **SCA**
- Write $0A_H$ to **ITSA**
- Write 03_H to **SPA**
- Write $1E_H$ to **OTSA**
- Write 00_H to **DPA**
- Write 21_H to **CCMD**

6.11.5 Establish Multipoint Connection

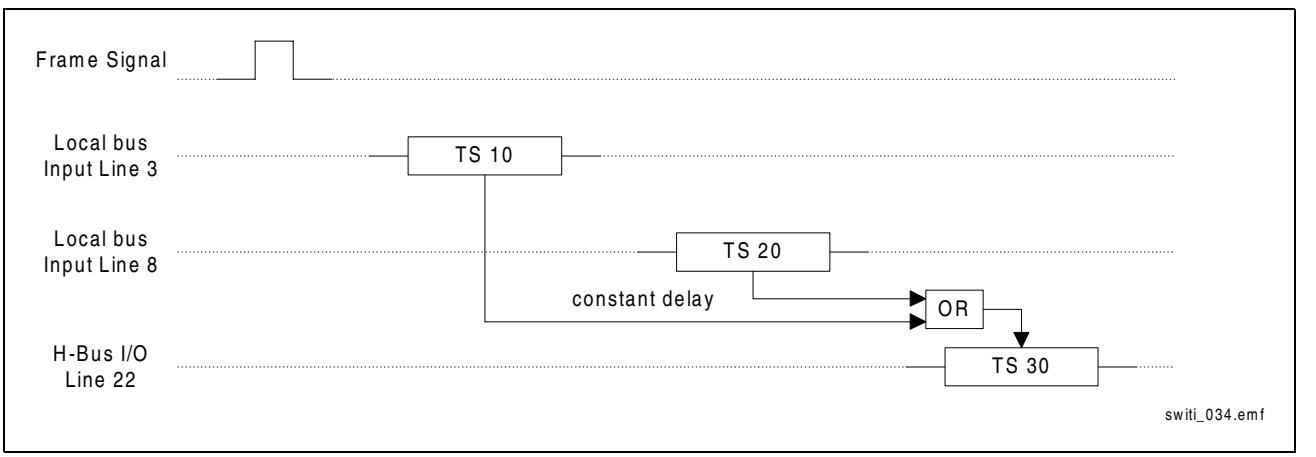


Figure 40 Example: Multipoint Connection

Example (8-bit µP interface):

Connect time-slot 10 of local bus line 3 and time-slot 20 of local bus line 8 logical OR with output time-slot 30 of H-Bus line 22 in constant delay mode. If the connections are established consecutively it is not necessary to rewrite the destination determining registers **OTSA** and **DPA** because they keep their values.

- Write $0A_H$ to **ITSA**
- Write 03_H to **SPA**
- Write $1E_H$ to **OTSA**
- Write 96_H to **DPA**
- Write 07_H to **CCMD**
- Write 14_H to **ITSA**
- Write 08_H to **SPA**
- Write 07_H to **CCMD**

Example (16-bit µP interface):

- Write $0A03_H$ to **SA**
- Write $1E96_H$ to **DA**
- Write 0007_H to **CC16**
- Write 1408_H to **SA**
- Write 0007_H to **CC16**

6.12 Send Messages

Sending messages means to transmit a constant value on any time-slot or subchannel after the message is programmed within three frames. That means a message has always a minimum delay and is sent until the sending is stopped by the stop message command.

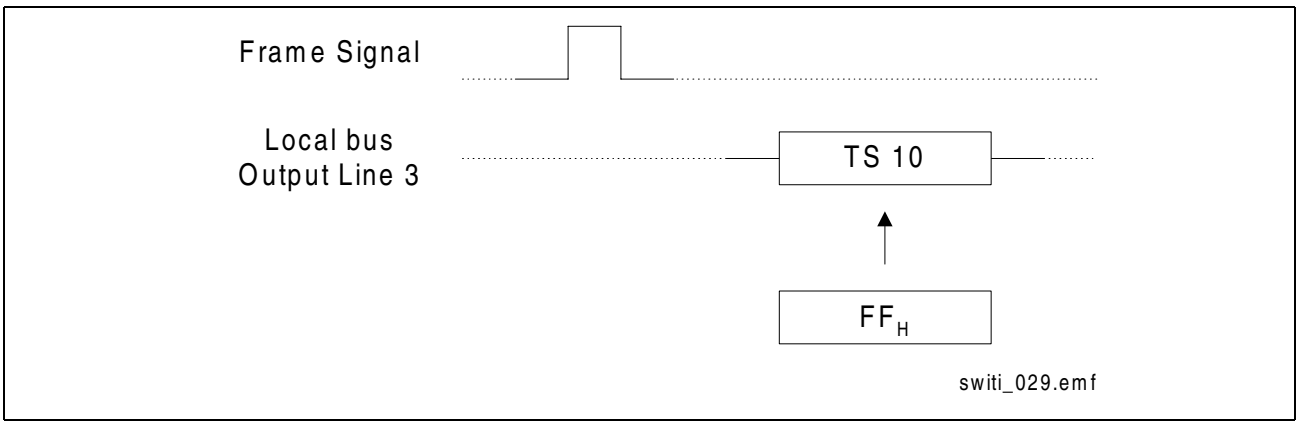


Figure 41 Example: Send Message

Example (8-bit µP interface):

Send constant value of FF_H on time-slot 10 of local bus line 3

- Write FF_H to **MV**
- Write $0A_H$ to **OTSA**
- Write 03_H to **DPA**
- Write 03_H to **CCMD**

Example (16-bit µP interface):

- Write FF_H to **MV**
- Write $0A03_H$ to **DA**
- Write 0003_H to **CC16**

6.13 Release Connections

6.13.1 Release 8-bit Connections

Example (8-bit µP interface):

Release connection established in **Figure 33**

- Write $0A_H$ to **ITSA**
- Write 03_H to **SPA**
- Write $1E_H$ to **OTSA**
- Write 96_H to **DPA**
- Write 05_H to **CCMD**

Example (16-bit µP interface):

- Write $0A03_H$ to **SA**
- Write $1E96_H$ to **DA**
- Write 0005_H to **CC16**

6.13.2 Release 4-bit Connections

Example (8-bit µP interface):

Release connection established in **Figure 35**

- Write 08_H to **SCA**
- Write $0A_H$ to **ITSA**
- Write 03_H to **SPA**
- Write $1E_H$ to **OTSA**
- Write 96_H to **DPA**
- Write 15_H to **CCMD**

Example (16-bit µP interface):

- Write $0A03_H$ to **SA**
- Write $1E96_H$ to **DA**
- Write 0815_H to **CC16**

6.13.3 Release 2-bit Connections

Example (8-bit µP interface):

Release connection established in **Figure 36**

- Write 19_H to **SCA**
- Write $0A_H$ to **ITSA**
- Write 03_H to **SPA**

– Write $1E_H$ to **OTSA**
– Write 96_H to **DPA**
– Write 25_H to **CCMD**

Example (16-bit µP interface):

– Write $0A03_H$ to **SA**
– Write $1E96_H$ to **DA**
– Write 1925_H to **CC16**

6.13.4 Release 1-bit Connections

Example (8-bit µP interface):

Release connection established in **Figure 37**

– Write $2A_H$ to **SCA**
– Write $0A_H$ to **ITSA**
– Write 03_H to **SPA**
– Write $1E_H$ to **OTSA**
– Write 96_H to **DPA**
– Write 35_H to **CCMD**

Example (16-bit µP interface):

– Write $0A03_H$ to **SA**
– Write $1E96_H$ to **DA**
– Write $2A35_H$ to **CC16**

6.13.5 Release Broadcast Connection

Example (8-bit µP interface):

Release connection established in **Figure 38**. All but the last connection participating on a broadcast connection have to be released by the **Disconnect Part of Broadcast** Command. The last connection has to be released by the **Constant Delay Connect Disconnect** Command.

- Write $0A_H$ to **ITSA**
- Write 03_H to **SPA**
- Write 62_H to **OTSA**
- Write $9D_H$ to **DPA**
- Write 06_H to **CCMD**
- Write $0A_H$ to **ITSA**
- Write 03_H to **SPA**
- Write $1E_H$ to **OTSA**
- Write 96_H to **DPA**
- Write 05_H to **CCMD**

Example (16-bit µP interface):

- Write $0A03_H$ to **SA**
- Write $629D_H$ to **DA**
- Write 0006_H to **CC16**
- Write $0A03_H$ to **SA**
- Write $1E96_H$ to **DA**
- Write 0005_H to **CC16**

6.13.6 Release Subchannel Broadcast Connection

The order can be different as the establish order. The last release must be a normal release command.

- First Connection
  - Write 03_H to **SCA**
  - Write $0A_H$ to **ITSA**
  - Write 03_H to **SPA**
  - Write $1E_H$ to **OTSA**
  - Write 00_H to **DPA**
  - Write 26_H to **CCMD**
- Second Connection
  - Write $1A_H$ to **SCA**
  - Write $0A_H$ to **ITSA**
  - Write 03_H to **SPA**
  - Write $1E_H$ to **OTSA**

  - Write 00_H to **DPA**
  - Write 26_H to **CCMD**
- Third Connection
  - Write 23_H to **SCA**
  - Write $0A_H$ to **ITSA**
  - Write 03_H to **SPA**
  - Write $1E_H$ to **OTSA**
  - Write 00_H to **DPA**
  - Write 36_H to **CCMD**
- Fourth Connection
  - Write $2A_H$ to **SCA**
  - Write $0A_H$ to **ITSA**
  - Write 03_H to **SPA**
  - Write $1E_H$ to **OTSA**
  - Write 00_H to **DPA**
  - Write 36_H to **CCMD**
- Fifth Connection
  - Write 08_H to **SCA**
  - Write $0A_H$ to **ITSA**
  - Write 03_H to **SPA**
  - Write $1E_H$ to **OTSA**
  - Write 00_H to **DPA**
  - Write 25_H to **CCMD**

6.13.7 Release Multipoint Connection

This type of connections is released with normal disconnect commands. (See “Release 8-bit Connections” on **page 124.**)

6.14 Stop Sending Messages

Example (8-bit µP interface):

Stop sending message invoked in **Figure 41**

- Write $0A_H$ to **OTSA**
- Write 03_H to **DPA**
- Write 04_H to **CCMD**

Example (16-bit µP interface):

- Write $0A03_H$ to **DA**
- Write 0004_H to **CC16**

7 Timing Diagrams

7.1 PCM Interface Timing

The following tables and figures give the PCM timing with a capacitive load of 50 pF. PDC and PFS are configured as inputs. The timing is also valid if PDC and PFS are configured as outputs.The PFS output high time is fixed to 488 ns for all data rates and clock rates.The PFS input minimum high time depends on the PDC input frequency (see table **Table 27**)

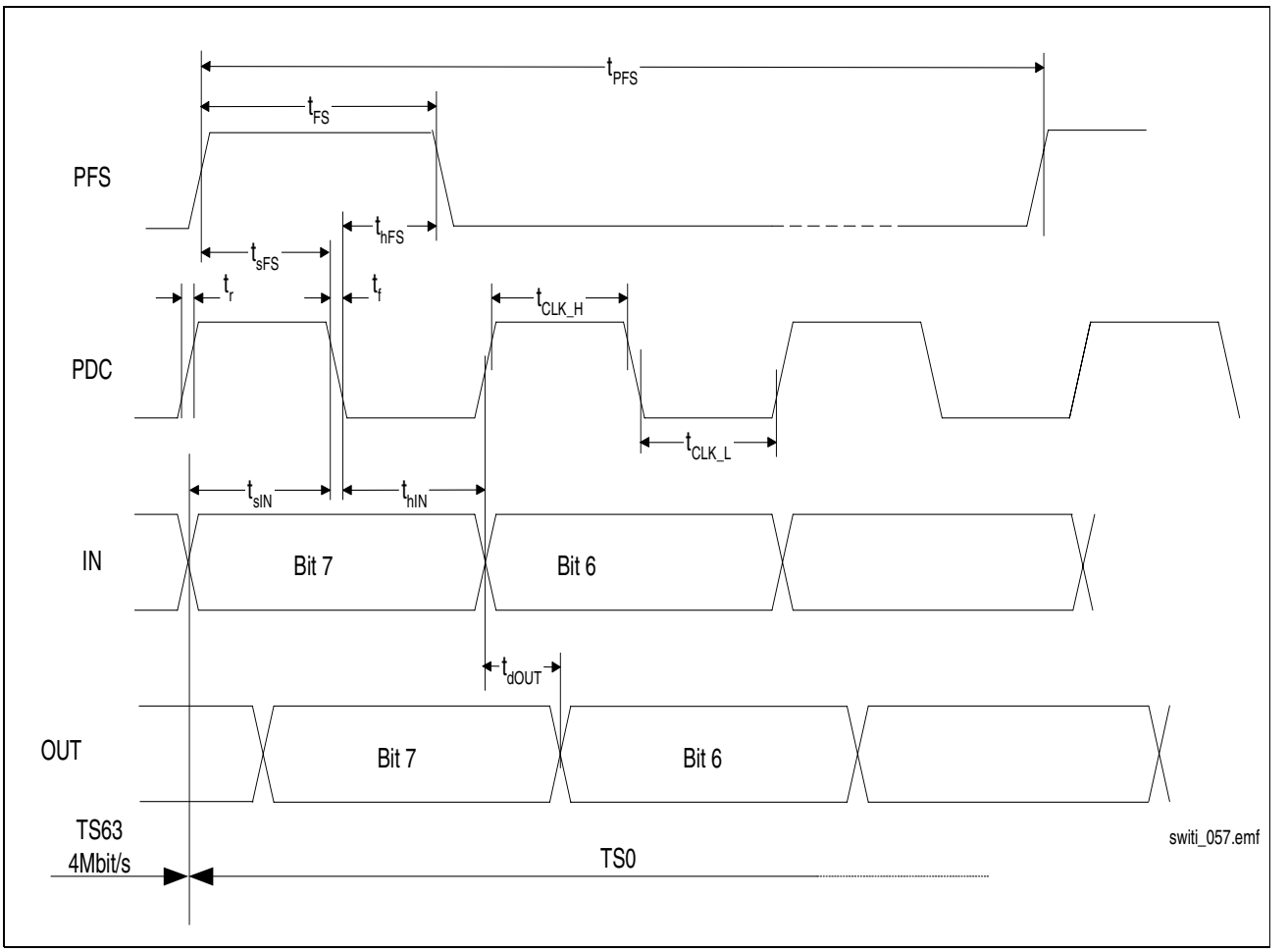


Figure 42 PCM Timing

Table 27 PCM Timing

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Period PFS	t_{PFS}		125	µs	
PFS high time	t_{FS}	480		ns	PDC = 2.048 MHz
PFS set up time to clock	t_{sFS}	15		ns	
PFS hold time from clock	t_{hFS}	20		ns	
PFS high time	t_{FS}	240		ns	PDC = 4.096 MHz
PFS set up time to clock	t_{sFS}	15		ns	
PFS hold time from clock	t_{hFS}	20		ns	
PFS high time	t_{FS}	120		ns	PDC = 8.192 MHz
PFS set up time to clock	t_{sFS}	10		ns	
PFS hold time from clock	t_{hFS}	20		ns	
PFS high time	t_{FS}	60		ns	PDC = 16.384 MHz
PFS set up time to clock	t_{sFS}	10		ns	
PFS hold time from clock	t_{hFS}	20		ns	
PDC clock period	t_{CLK}	480		ns	PDC = 2.048 MHz
PDC clock period low	t_{CLK_L}	232	251	ns	
PDC clock period high	t_{CLK_H}	233	252	ns	
PDC clock period	t_{CLK}	240		ns	PDC = 4.096 MHz
PDC clock period low	t_{CLK_L}	112	131	ns	
PDC clock period high	t_{CLK_H}	113	132	ns	
PDC clock period	t_{CLK}	120		ns	PDC = 8.192 MHz
PDC clock period low	t_{CLK_L}	51	70	ns	
PDC clock period high	t_{CLK_H}	52	71	ns	
PDC clock period	t_{CLK}	60		ns	PDC = 16.384 MHz
PDC clock period low	t_{CLK_L}	26	34	ns	
PDC clock period high	t_{CLK_H}	27	35	ns	
PDC rise time	t_r		10	ns	
PDC fall time	t_f		10	ns	

Table 27 PCM Timing (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Serial data input set up time	t_{sIN}	20		ns	PDC = 2.048 MHz
Serial data input hold time	t_{hIN}	30		ns	
Serial data input set up time	t_{sIN}	20		ns	PDC = 4.096 MHz
Serial data input hold time	t_{hIN}	30		ns	
Serial data input set up time	t_{sIN}	20		ns	PDC = 8.192 MHz
Serial data input hold time	t_{hIN}	30		ns	
Serial data input set up time	t_{sIN}	20		ns	PDC = 16.384 MHz
Serial data input hold time	t_{hIN}	30		ns	
Serial data output delay	t_{dOUT}	0	30 [1)]	ns	PDC = 2.048 MHz
Serial data output delay	t_{dOUT}	0	30 [1)]	ns	PDC = 4.096 MHz
Serial data output delay	t_{dOUT}	0	30 [1)]	ns	PDC = 8.192 MHz
Serial data output delay	t_{dOUT}	0	30 [1)]	ns	PDC = 16.384 MHz

[1)] for PCM master, the maximum delay is 15 ns

7.2 PCM Parallel Mode Timing

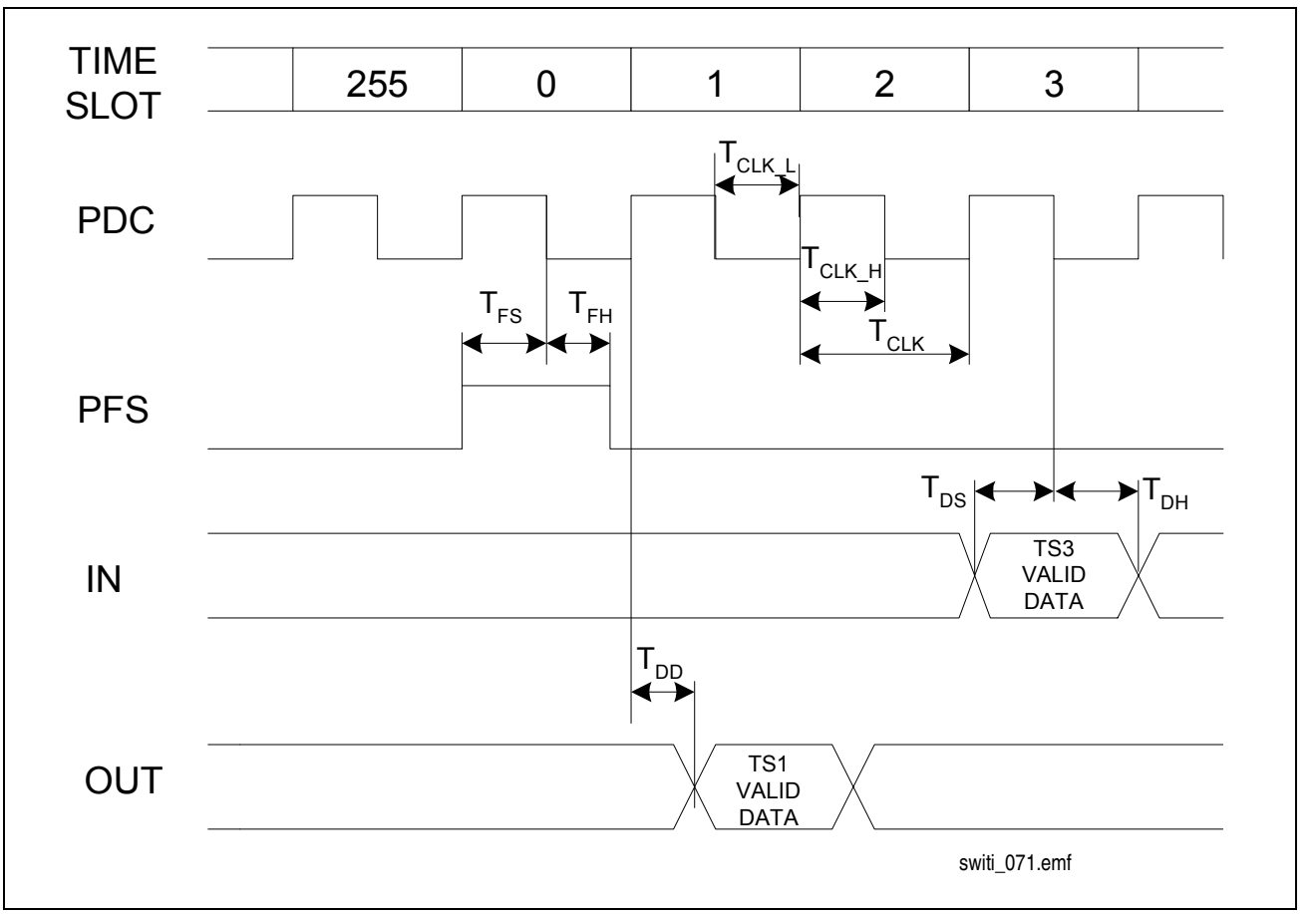


Figure 43 Parallel Mode Timing

Table 28 PCM Parallel Mode Timing

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Frame setup time to clock	T_{FS}	125		ns	
Frame hold time to clock	T_{FH}	125		ns	
Input data setup time	T_{DS}	50		ns	
Input data hold time	T_{DH}	15		ns	
Output data delay	T_{DD}		35	ns	
PDC clock period	T_{CLK}	483	493	ns	PDC = 2.048 MHz
PDC clock period high	T_{CLK_H}	231	257	ns	
PDC clock period low	T_{CLK_L}	231	257	ns	

7.3 H-Bus and PCM (Local Bus) Frame Structure

Figure 44 shows the H-Bus clock alignment together with the PCM (local bus) clock alignment.

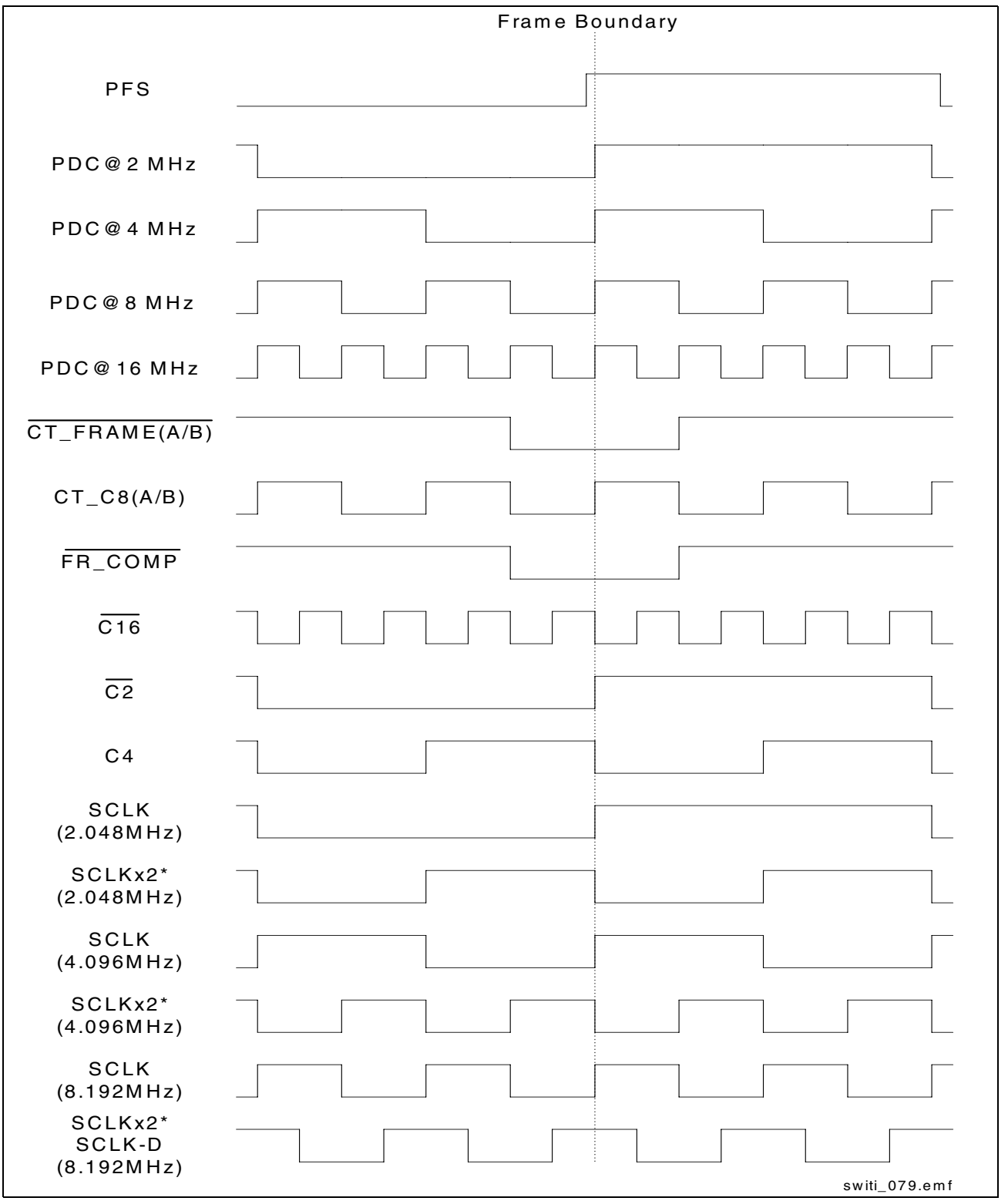


Figure 44 H-Bus and PCM (Local Bus) Clock Alignment

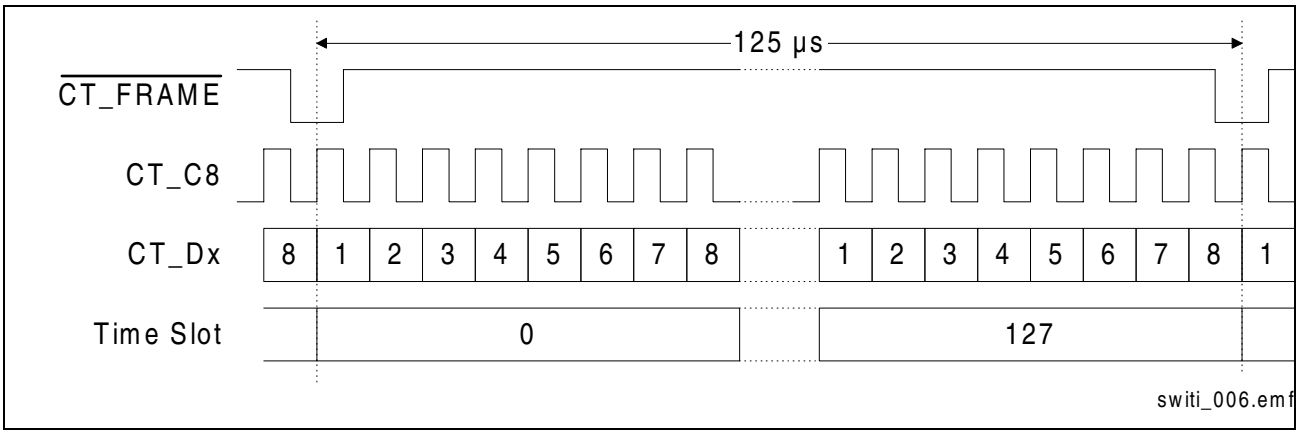


Figure 45 H-Bus Frame Structure

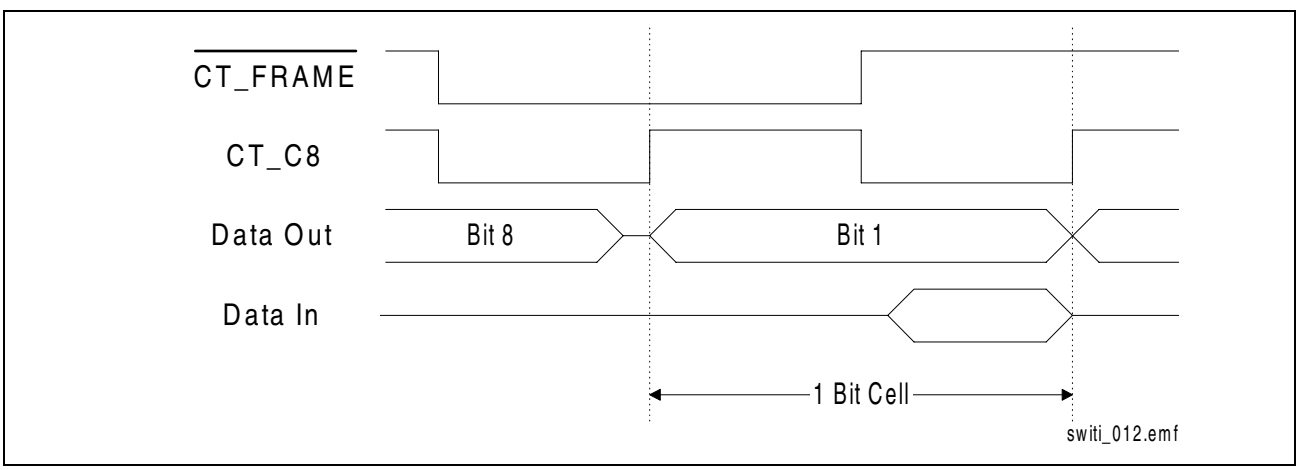


Figure 46 H.1x0 Detailed Functional Timing

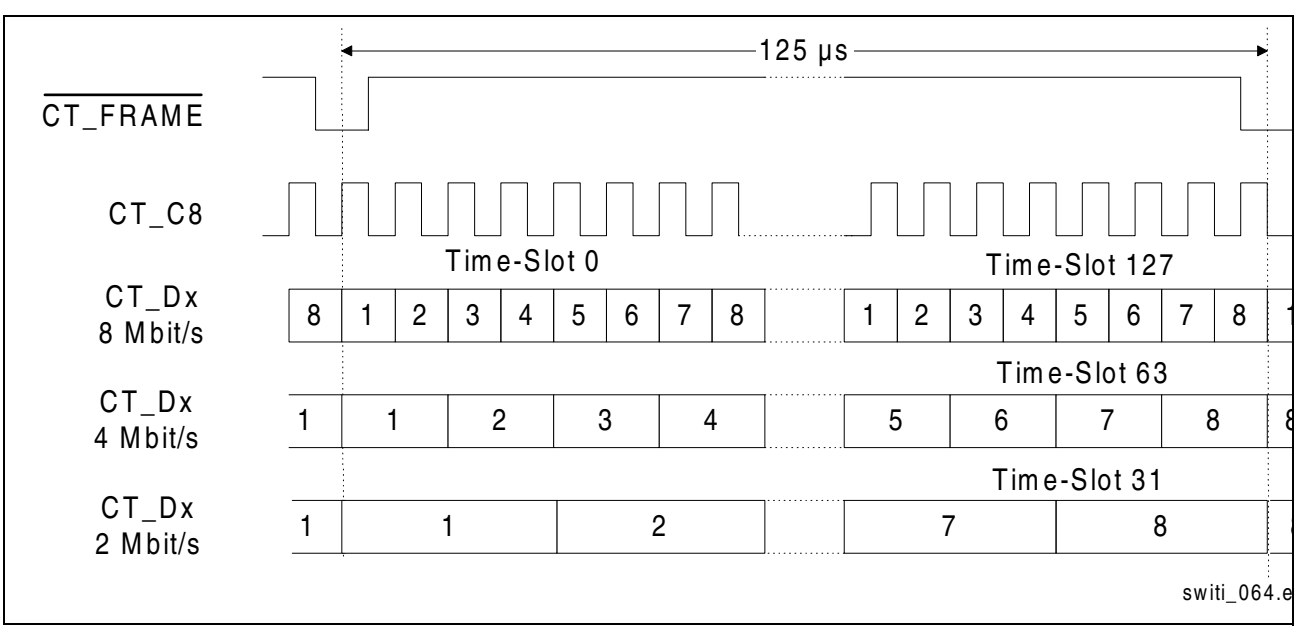


Figure 47 H.1x0 Functional Timing for 8, 4 and 2 MBit/s Data Streams

Note: The MSB (PCM sign bit) must be at the beginning (first bit) of the time-slot for PCM data. For other data types (e.g. HDLC) the MSB may be first or last depending on the format. The SWITI doesn't convert the data format between the PCM and H.1x0 interface.

7.4 H-Bus Timing

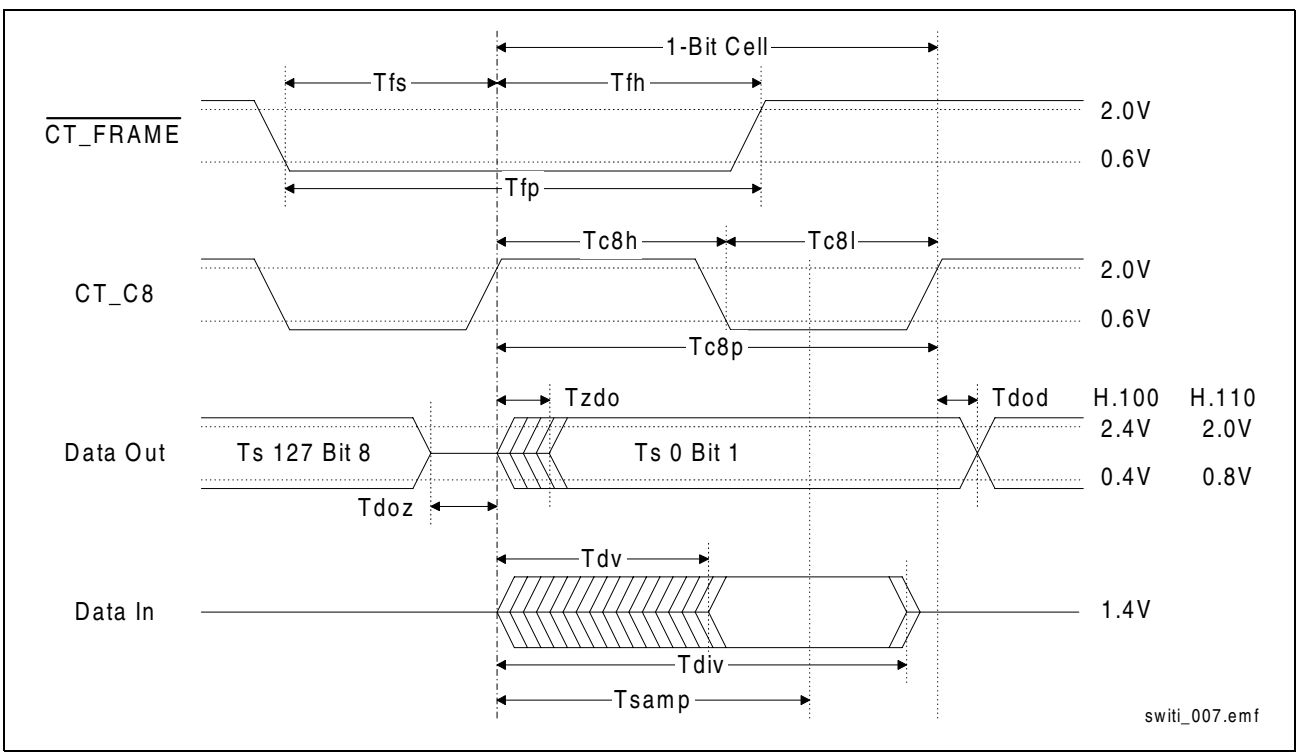


Figure 48 Detailed Data Bus Timing

Measuring conditions, data lines

- Vth (threshold voltage) = 1.4 V
- Vhi (test high voltage) = 2.0 V
- Vlo (test low voltage) = 0.8 V
- Input signal edge rate = 1 V/ns

Measuring conditions, clock and frame lines

- Vt+ (test high voltage) = 2.0 V
- Vt- (test low voltage) = 0.6 V
- Input signal edge rate = 1 V/ns

Table 29 Component Timing Specification

Symbol	Parameter	Min	Typ	Max	Unit	Notes
	Clock edge rate (All Clocks except CT_NETREF)	0.25		2	V/ns	1
	CT_NETREF edge rate			0.3	V/ns	16
Tc8p	Clock CT_C8 Period	122.066-Φ		122.074+Φ	ns	5
Tc8h	Clock CT_C8 High Time	49-Φ		73+Φ	ns	6, 12
Tc8l	Clock CT_C8 Low Time	49-Φ		73+Φ	ns	6, 12
Tsamp	Data Sample Point		90		ns	9
Tdoz	Data Output to HiZ Time	- 10		0	ns	3, 7, 10
Tzdo	Data HiZ to Output Time	0		23	ns	3, 7, 10
Tdod	Data Output Delay Time	0		23	ns	3, 7
Tdv	Data Valid Time	0		83	ns	8, 15,17
Tdiv	Data Invalid Time	102		112	ns	13, 14
Tfp	$\overline{\text{CT\_FRAME}}$ Width	90	122	180	ns	
Tfs	$\overline{\text{CT\_FRAME}}$ Setup Time	45		90	ns	
Tfh	$\overline{\text{CT\_FRAME}}$ Hold Time	45		90	ns	
Φ	Phase Correction	0		10	ns	11

Note:

1. The rise and fall times are determined by the edge rate in V/ns. A "Max" edge rate is the fastest rate at which a clock transitions.
2. Test Load: 200 pF
3. Test Load: 70 pF
4. When RESET is active, every output driver is tristated.
5. Tc8p Min and Max are under free-run conditions assuming ±32ppm clock accuracy.
6. Non-cumulative, Tc8p requirements still need to be met.
7. Measured at the transmitter.
8. Measured at the receiver.
9. For reference only.
10. Tdoz and Tzdo apply at every time-slot boundary.
11. Φ (Phase Correction) results from PLL timing corrections.
12. Duty Cycle measured at transmitter under no load conditions.
13. This range accounts for Φ (Phase Correction)
14. H.110: Tcell = Max. clock backplane delay + Max. data backplane delay + Max. Tzdo + (Min. Tdiv - Max. Tdv) + Max. Tdoz + Φ = 26 ns + 46 ns + 11 ns + (102 ns - 83 ns) + 10 ns + 10 ns = 122 ns. Max. clock delay and max. data delay are worst case numbers based on electrical simulation.
15. Based on worst case electrical simulation.
16. H.110: 10%-90%. Test Load = 150 pF.
17. Tdv = Max. clock backplane delay + Max. data backplane delay + Max. data HiZ to output time = 26 ns + 46 ns + 11 ns = 83 ns. Max. clock delay and max. data delay are worst case numbers based on electrical simulation.

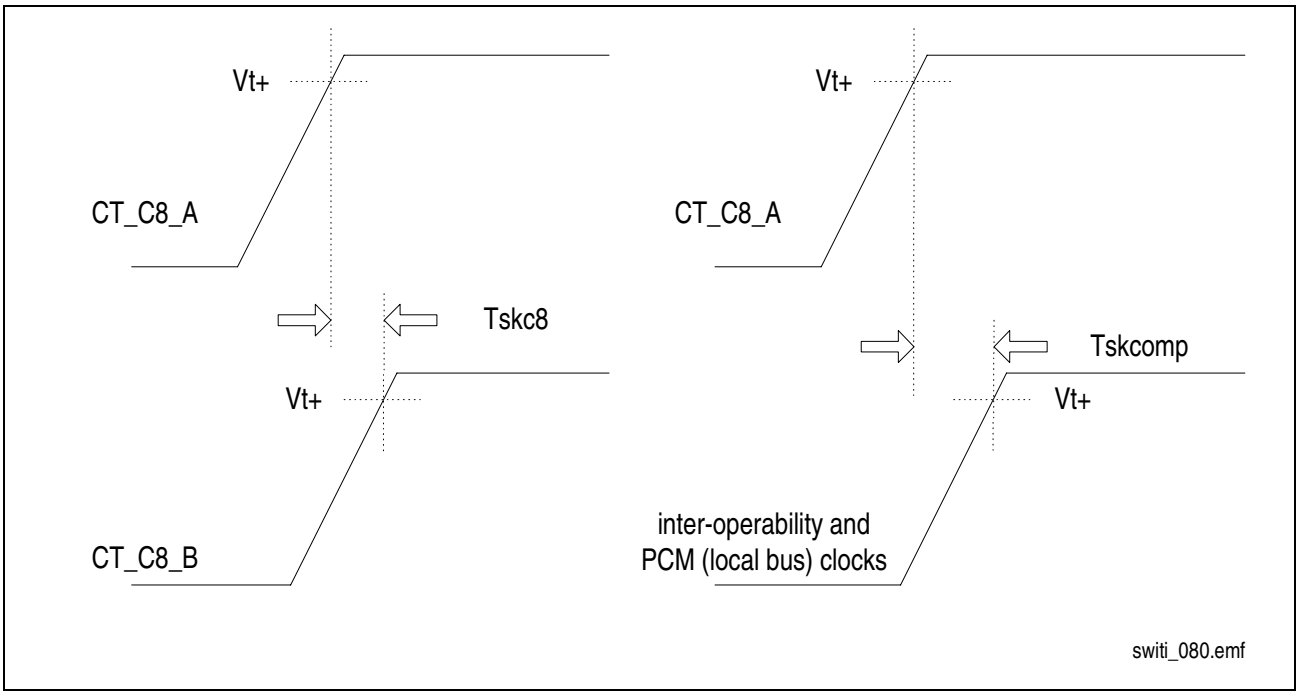


Figure 49 Clock Skew Timing

Table 30 Clock Skew Timing

Symbol	Parameter	Min	Max	Unit	Notes
Tskc8	Max Skew between CT_C8 "A" and "B"		16	ns	1,2,3,4
Tskcomp	Max Skew between CT_C8_A and any generated compatibility clock		17	ns	1
Tskout	Max Skew between all SWITI output clocks		±5	ns	
Vt+	Positive-going Threshold	1.2	2	V	5
Vt-	Negative-going Threshold	0.6	1.6	V	5
Vhys	Hysteresis (Vt+, Vt-)	0.4		V	5
Cin	Input pin capacitance		10	pF	5

Note:

1. Test Load: 50 pF
2. Assumes "A" and "B" masters in adjacent slots.
3. When static skew is 10 ns and, in the same clock cycle, each clock performs a 10 ns phase correction in opposite directions, a maximum skew of 30 ns will occur during that clock cycle.
4. Meeting the skew requirements in **Table 30** and the clock accuracy requirements could require the PLLs generating CT_C8 to have different time constants when acting as primary and secondary clock masters.
5. Requirements for CT_C8 and $\overline{\text{CT\_FRAME}}$ receivers.

7.5 Clock Interoperability

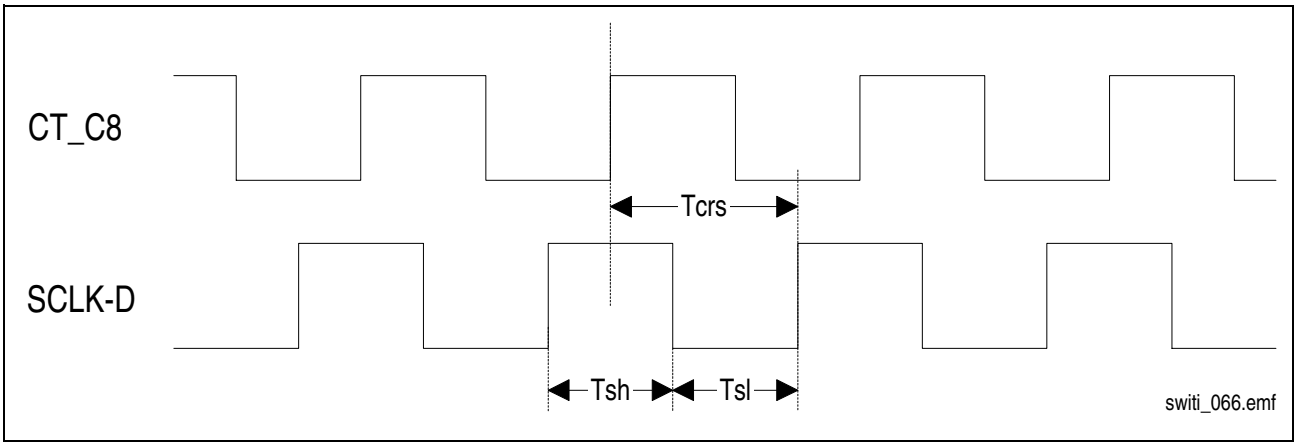


Figure 50 SCLK-D Timing for SCbus Operating at 8.192 Mbit/s

Table 31 SCLK-D Timing at 8.192 Mbit/s

Symbols	Parameter	Min.	Typ.	Max.	Unit
Tcrs	Rising Edge of CT_C8_*n* to Rising Edge of SCLK-D	100		110	ns
Tsh	SCLK-D High Time	51	61	71	ns
Tsl	SCLK-D Low Time	51	61	71	ns

Note:

1. Rising edge of Ct_C8_*n* to rising edge of SCLK-D includes ±5 ns of skew as with other compatibility signals (*n* = current primary CT Bus clock signal identifier)
2. SCLK-D high and low times include nominal ±Φ
3. This timing is valid under conditions specified in the PCI Local Bus Specification, rev. 2.1, Table 4-2, note 4
4. CT_C8 is configured as output and SCLK-D is configured as output.

7.6 Microprocessor Interface Timing

Microprocessor accesses of the SWITI are performed by an activation of the address and $\overline{CS}$.

– By driving the MODE16 pin 'low' the user selects the 8-bit microprocessor interface, by driving it 'high' - the 16-bit microprocessor interface.
– By driving the ALE pin 'high' the user selects Intel/Infineon mode, by driving it 'low' - Motorola mode. The pin is sampled during the hardware reset process.
– In Intel/Infineon mode, a distinction is needed between working in multiplexed address/data bus mode and de-multiplexed address and data bus mode. In Motorola mode, only de-multiplexed busses are used. By driving the ALE pin 'high' during the normal operation the user selects the de-multiplexed mode, a falling or rising edge during the normal operation selects the multiplexed mode.

7.6.1 Infineon/Intel Timing in De-Multiplexed Mode

In this mode driving $\overline{RD}$ 'low' causes a read access, driving $\overline{WR}$ 'low' causes a write access.

In de-multiplexed bus configuration, ALE must be driven 'high'.

Table 32 Infineon/Intel Timing in De-Multiplexed Mode

Parameter	Symbol	Limit Values (C_{LOAD}= 50pF)	
		min	max
Address setup time to $\overline{WR}$ or $\overline{RD}$	t_{AS}	15 ns	
$\overline{RD}$ pulse width	t_{RR}	60 ns	
$\overline{RD}$ recovery time	t_{RI}	120 ns	
Data output delay from $\overline{RD}$ active	t_{RD}		60 ns
Data float delay from $\overline{RD}$ inactive	t_{DF}		15 ns
$\overline{WR}$ pulse width	t_{WW}	40 ns	
$\overline{WR}$ recovery time	t_{WI}	120 ns	
Data setup time to $\overline{WR}$ x $\overline{CS}$	t_{DW}	20 ns	
Data hold time from $\overline{WR}$ x $\overline{CS}$	t_{WD}	10 ns	

Note: The read/write recovery time (t_{RI} and t_{WI}) are required only for consecutive accesses to the microprocessor interface.

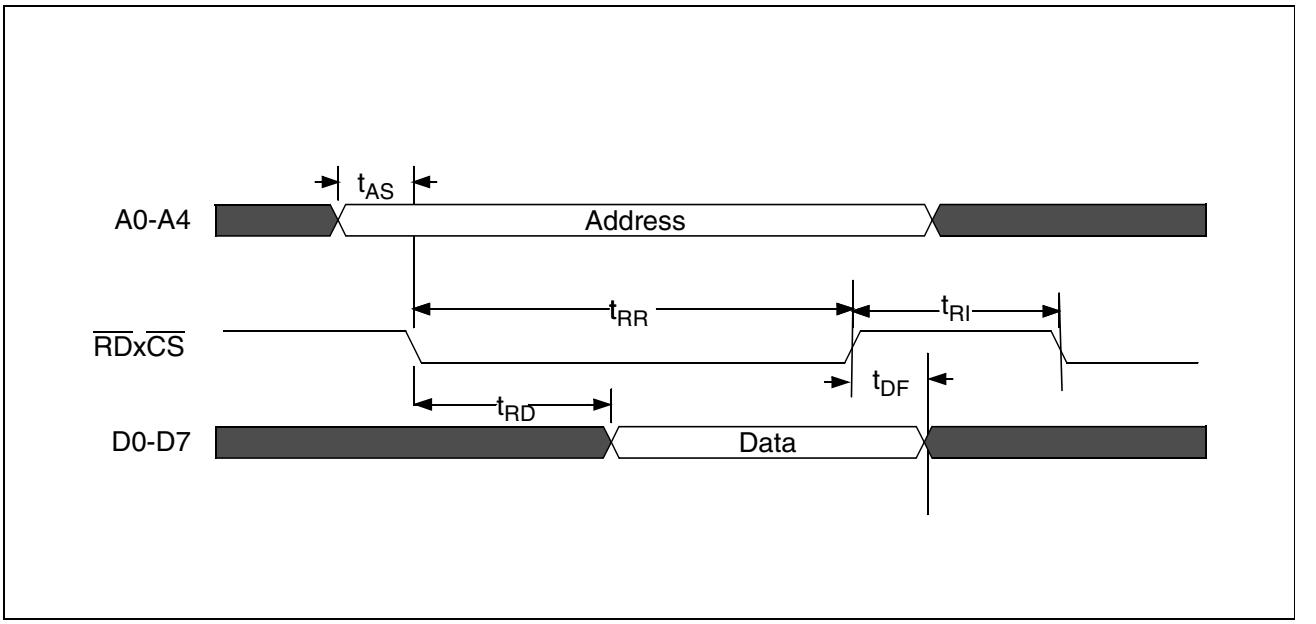


Figure 51 Infineon/Intel Read Cycle in De-Multiplexed Mode

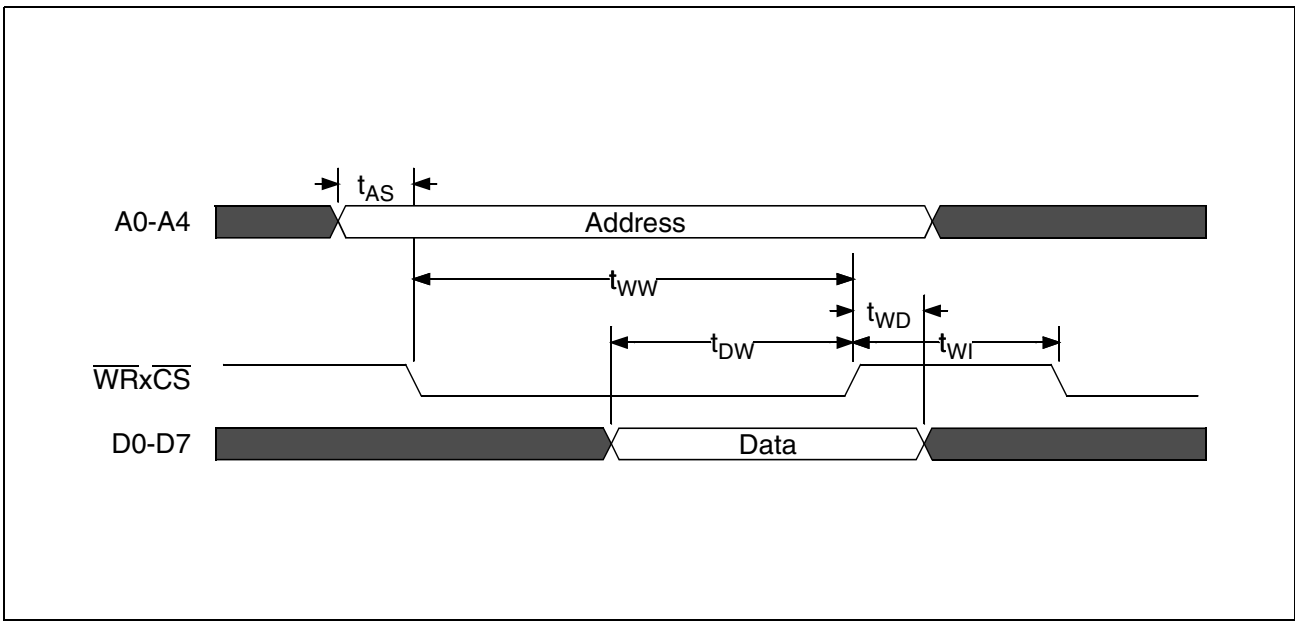


Figure 52 Infineon/Intel Write Cycle in De-Multiplexed Mode

Addresses will be latched with the falling $\overline{WR}$ edge during the write cycle internally.

7.6.2 Infineon/Intel Timing in Multiplexed Mode

In this mode the ALE pin is used to lock the address send via the multiplexed A/D bus.

Table 33 Infineon/Intel Timing in Multiplexed Mode

Parameter	Symbol	Limit Values (C_{LOAD}= 50pF)	
		min	max
ALE pulse width	t_{AA}	15 ns	
Address setup time to ALE falling edge	t_{AL}	15 ns	
Address hold time from ALE falling edge	t_{LA}	5 ns	
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	5 ns	
$\overline{RD}$ pulse width	t_{RR}	60 ns	
$\overline{RD}$ recovery time	t_{RI}	120 ns	
Data output delay from $\overline{RD}$ active	t_{RD}		60 ns
Data float delay from $\overline{RD}$ inactive	t_{DF}		15 ns
$\overline{WR}$ pulse width	t_{WW}	40 ns	
$\overline{WR}$ recovery time	t_{WI}	120 ns	
Data setup time to $\overline{WR}$ x $\overline{CS}$	t_{DW}	20 ns	
Data hold time from $\overline{WR}$ x $\overline{CS}$	t_{WD}	10 ns	

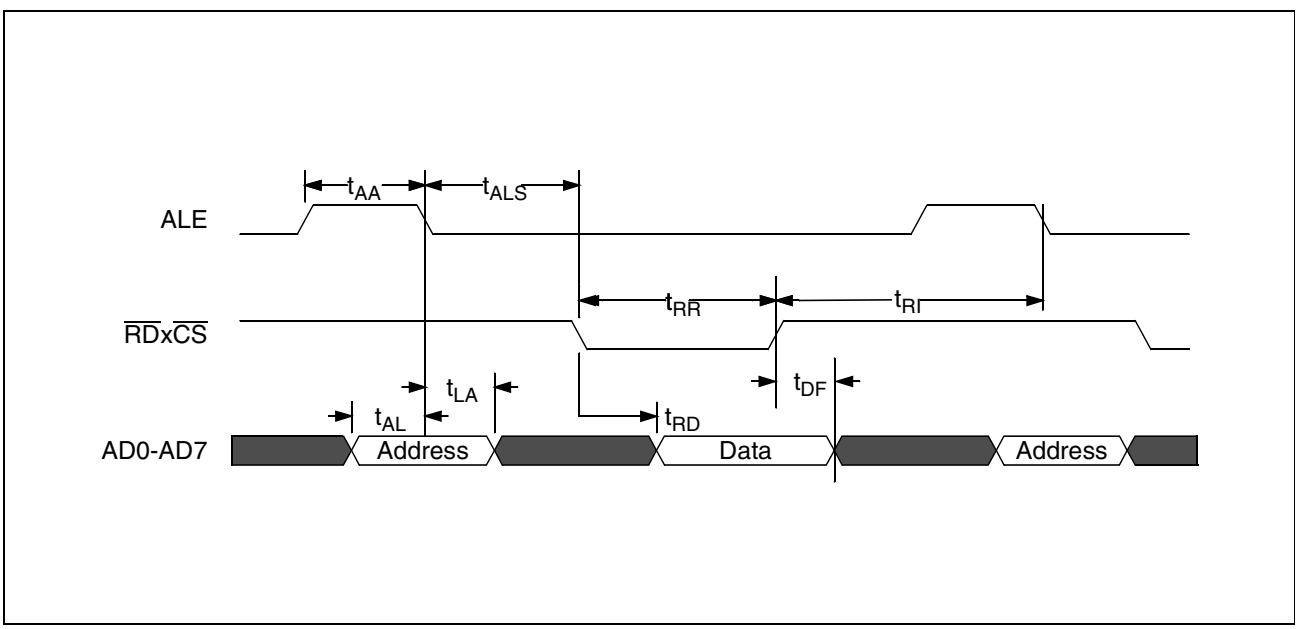


Figure 53 Infineon/Intel Read Cycle in Multiplexed Mode

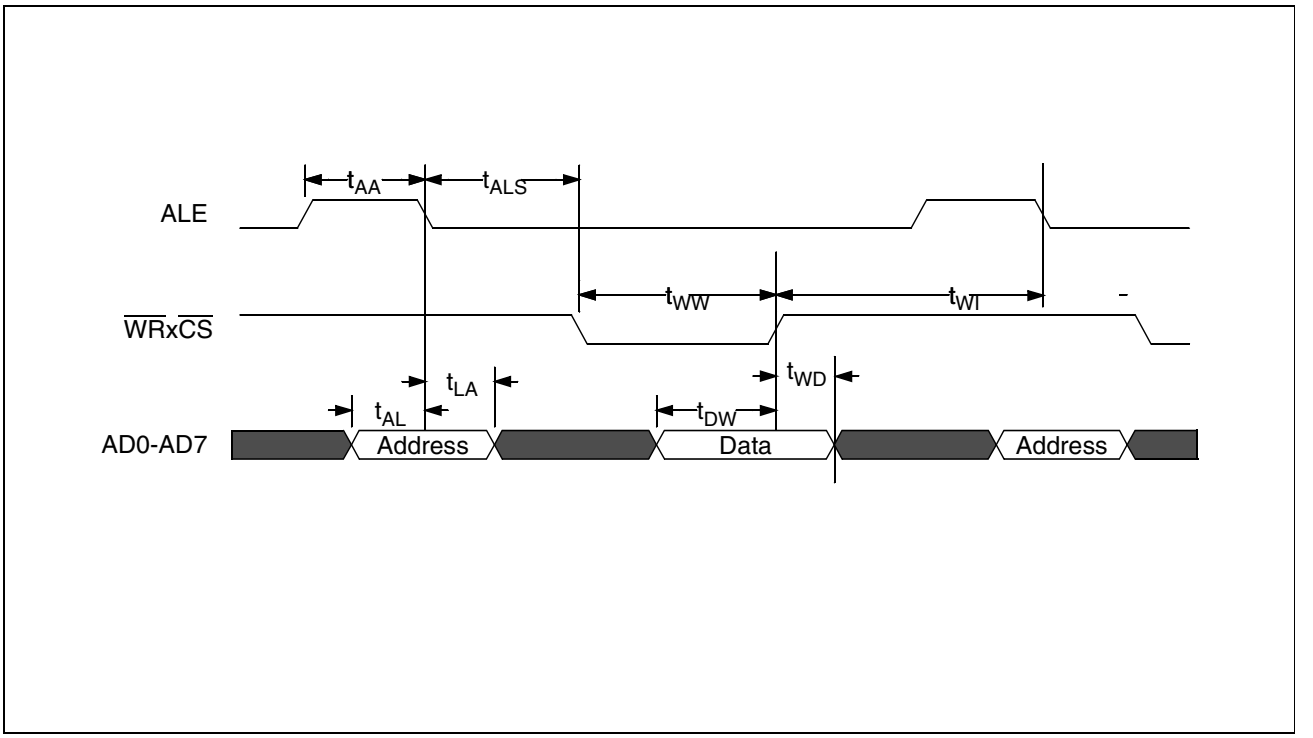


Figure 54 Infineon/Intel Write Cycle in Multiplexed Mode

7.6.3 Motorola Microprocessor Timing

In this mode R/$\overline{W}$ distinguishes between Read and Write interactions, and $\overline{DS}$ is used for timing. $\overline{DS}$ X $\overline{CS}$ is active (low) when both, $\overline{DS}$ and $\overline{CS}$, are active (low).

The ALE pin must be driven 'low'.

Table 34 Motorola Timing

Parameter	Symbol	Limit Values (C_{LOAD}= 50pF)	
		min	max
Address setup time to $\overline{CS}$x$\overline{DS}$	t_{AS}	15 ns	
R or $\overline{W}$ setup to $\overline{DS}$	t_{DSD}	0	
R/$\overline{W}$ hold from $\overline{CS}$x$\overline{DS}$ inactive	t_{RWD}	0	
R pulse width	t_{RR}	60 ns	
R recovery time	t_{RI}	120 ns	
Data output delay from R	t_{RD}		60 ns
Data float delay from R	t_{DF}		15 ns
$\overline{W}$ pulse width	t_{WW}	40 ns	
$\overline{W}$ recovery time	t_{WI}	120 ns	
Data setup time to $\overline{W}$ and $\overline{CS}$, $\overline{DS}$ and $\overline{CS}$	t_{DW}	10 ns	
Data hold time from $\overline{W}$ and $\overline{CS}$, $\overline{DS}$ and $\overline{CS}$	t_{WD}	10 ns	

Note: $\overline{DS}$ X $\overline{CS}$ is active (low) when, both, $\overline{DS}$ and $\overline{CS}$ are active (low)

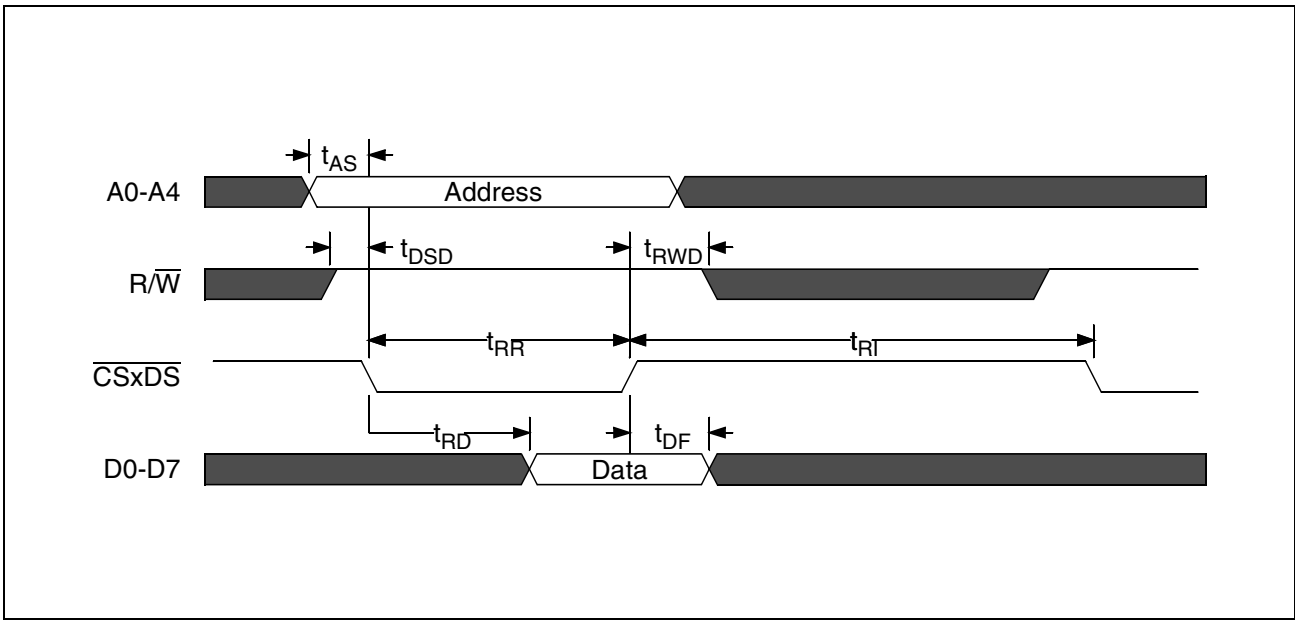


Figure 55 Motorola Read Cycle

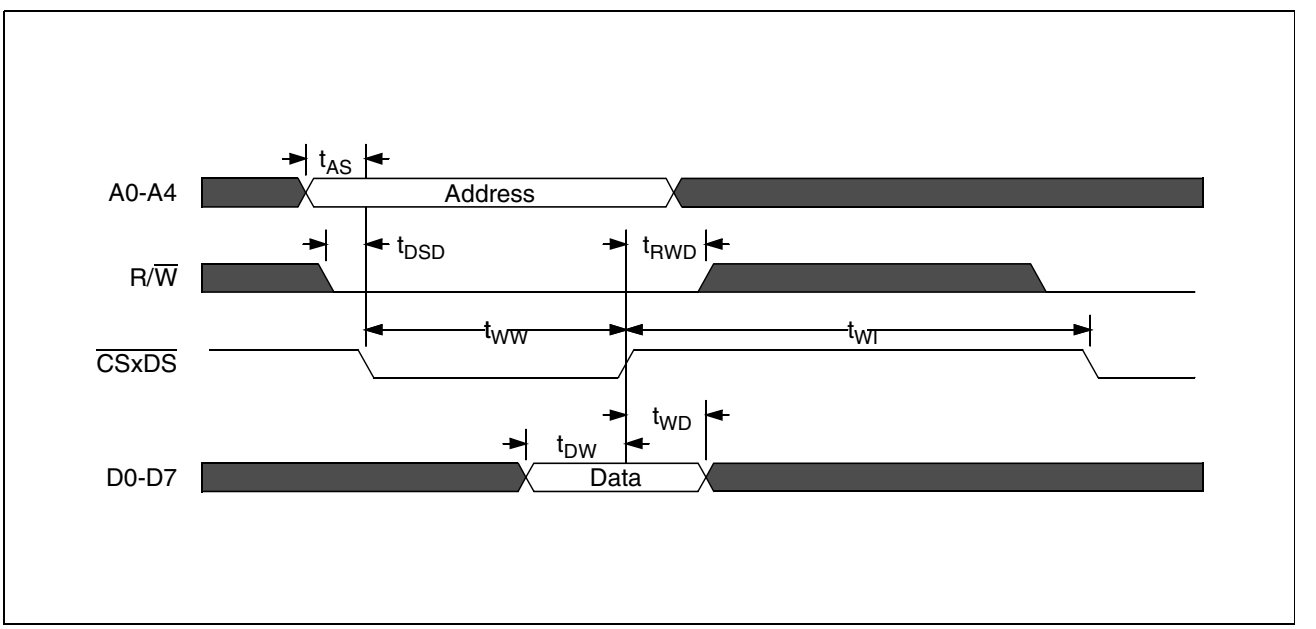


Figure 56 Motorola Write Cycle

7.7 JTAG Interface Timing

Table 35 JTAG Interface Timing

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Test Clock (TCK) Period	t_{TCJ}	100			ns	
Test Clock (TCK) Period Low	t_{CJL}	40			ns	
Test Clock (TCK) Period High	t_{CJH}	40			ns	
TMS Set-up time before TCK Rising Edge	t_{SUJ}	5			ns	
TMS Hold time after TCK Rising Edge	t_{HJR}	5			ns	
TDI Set-up time before TCK Rising Edge	t_{DSE}	5			ns	
TDI Hold time after TCK Rising Edge	t_{DHE}	5			ns	
Input Data Set-up time	t_{IPJ}	10			ns	
Input Data Hold time	t_{IAJ}	10			ns	
TDO Delay after TCK Falling Edge	t_{ODF}			20	ns	
Any output pin Delay after TCK Falling Edge	t_{OPD}			25	ns	In Update-DR TAP Controller State
Test Reset	t_{TRST}	1			µs	

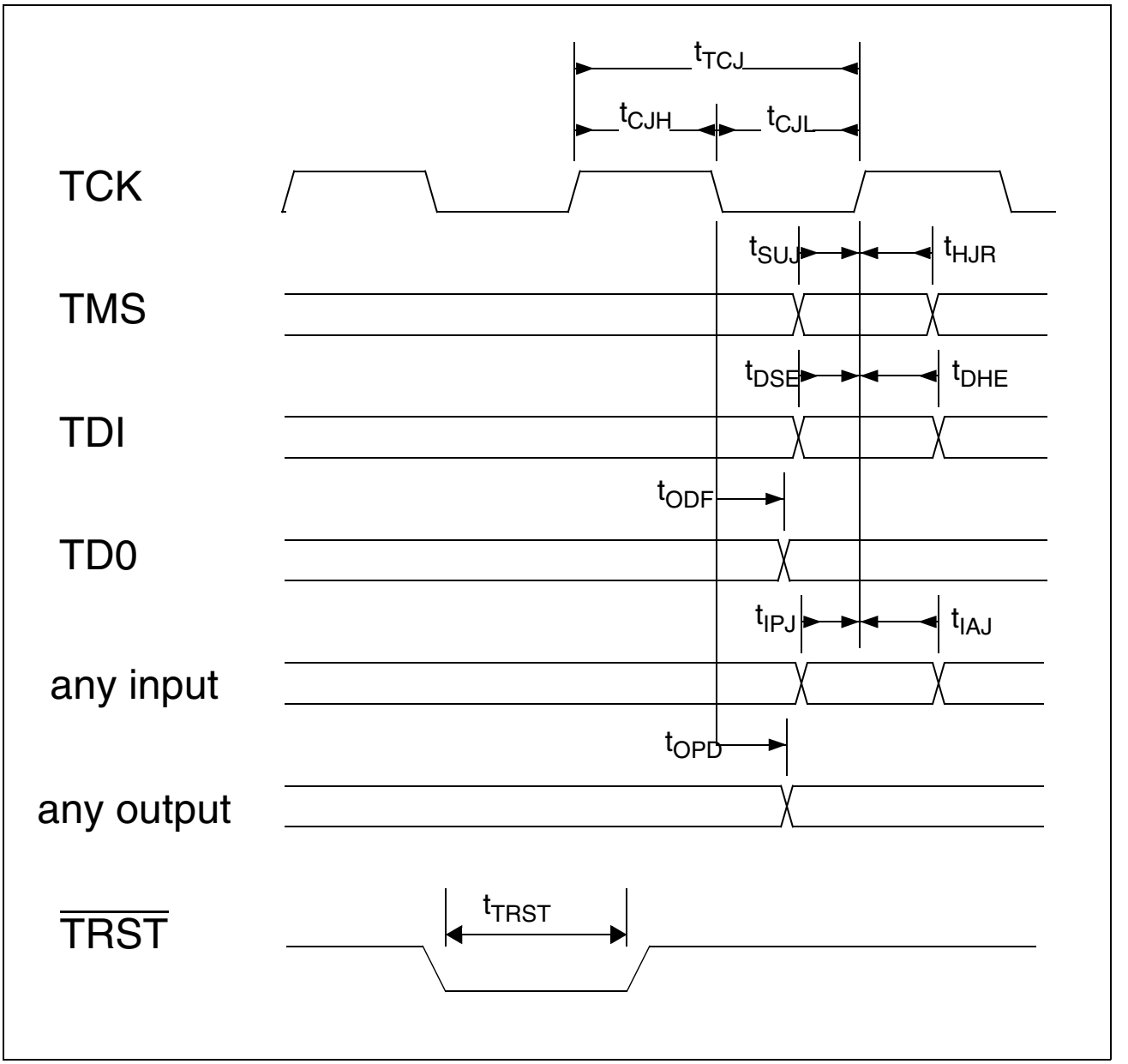


Figure 57 Boundary Scan Timing

7.8 Hardware Reset Timing

Table 36 Hardware Reset Timing

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Hardware Reset time	$t_{\overline{RESET}}$	1			µs	

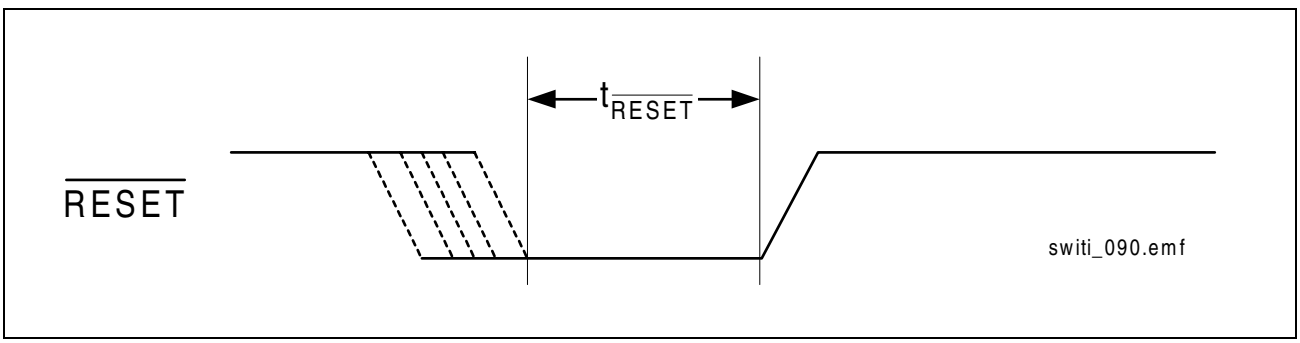


Figure 58 Hardware Reset Timing

*Note: In H.110 mode **Table 36** and **Figure 58** are also valid for the $\overline{CT\_RESET}$ signal.*

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Table 37 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias PEF	T_A	– 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 150	°C
Supply voltage	V_{DD}	– 0.5 to 4.6	V
I/O Supply voltage	V_{DD5}	– 0.5 to 7	V
Voltage on any input or output pin (referenced to ground)	V_S	– 0.5 to V_{DD} + 0.5 – 0.5 to V_{DD5} + 0.5	V
ESD robustness[1)] (HBM: 1.5 kΩ, 100 pF)	$V_{ESD,HBM}$	1500	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

8.2 Operating Range

Table 38 Operating Range

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Operating temperature	T_A	– 40	85	°C
Supply voltage	V_{DD}	3.13	3.47	V
I/O Supply voltage	V_{DD5}	4.75	5.25	V
Ground	V_{SS}	0	0	V
Voltage applied to input pins[1)]	V_{IN}	0	5.5	V
Voltage applied to output or I/O pins[2)]				
outputs enabled	V_{OUT}	0	V_{DD}	V
outputs high-Z	V_{OUT}	0	5.5	V
Voltage applied to H.1x0 I/O pins in 3,3V signal environment[3)]				
outputs enabled	V_{OUT}	0	V_{DD}	V
outputs high-Z	V_{OUT}	0	V_{DD} +0.3	V

1) If one of the H.1x0 input signals from the HTSI are used a 5 V signal environment the special V_{DD5} pins must be connected to 5 V as reference voltage to fulfill the operating range.

2) If one of the H.1x0 data ports and I/O signals or PCM16..31(IN/OUT) ports from the HTSI are used in a 5 V signal environment the special V_{DD5} pins must be connected to 5 V as reference voltage to fulfill the operating range.

3) V_{DD5} are connected to 3.3 V

Note: In the operating range, the functions given in the circuit description are fulfilled.

8.3 Crystal Oscillator

The SWITI requires a 16.384 MHz or 32.768 MHz clock source. To supply this a 16.384 MHz or 32.768 MHz crystal can be connected between the ECLKI and ECLKO pins. **Figure 59** shows a possible configuration of crystal with the external capacitors.

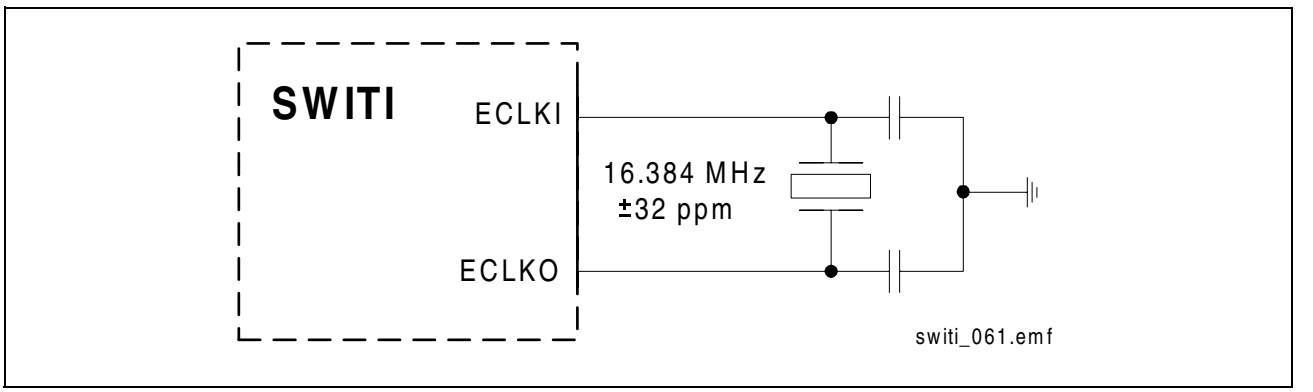


Figure 59 External Crystal

If a crystal is not used, a 16.384 MHz (±32 ppm or less) or a 32.768 MHz (±32 ppm) signal must be provided to the ECLKI pin and ECLKO should be left unconnected.

Table 39 External Capacitances for Crystal (Recommendation)

Parameter	Symbol	Rec. Values	Unit	Notes
Clock external input capacitance	C_{ECLKI}	6.8	pF	
Clock external output capacitance	C_{ECLKO}	8.2	pF	

8.4 DC Characteristics

Table 40 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{IL}	– 0.3	0.8	V	
Input high voltage	V_{IH}	2.0	V_{DD}+0.3	V	
Output low voltage	V_{OL}		0.4	V	I_{OL} = 6 mA I_{OL} = 24 mA[1)]
Output high voltage	V_{OH}	2.4		V	I_{OH} = – 2.0 mA I_{OH} = – 24.0 mA[2)]
Typical power supply current HTSI	I_{CC}		250	mA	V_{DD} = 3.3 V, T_A = 25 °C: PDC = 16.384 MHz
Input leakage current	I_{IL}		1	µA	V_{DD} = 3.3 V, GND = 0 V; all other pins are floating; V_{IN} = 0 V
Output leakage current	I_{OZ}		1	µA	V_{DD} = 3.3 V, GND = 0 V; V_{OUT} = 0 V
Positive Threshold	V_{t+}	1.2	2.0	V	
Negative Threshold	V_{t-}	0.6	1.6	V	
Hysterisis (V_{t+} - V_{t-})	V_{hys}	0.4		V	

1) only for CT_C8, $\overline{\text{CT\_FRAME}}$, $\overline{\text{FR\_COMP}}$, C2, $\overline{\text{C4}}$, $\overline{\text{C16+}}$, $\overline{\text{C16-}}$, SCLK, SCLK-D pins

2) only for CT_C8, $\overline{\text{CT\_FRAME}}$, $\overline{\text{FR\_COMP}}$, C2, $\overline{\text{C4}}$, $\overline{\text{C16+}}$, $\overline{\text{C16-}}$, SCLK, SCLK-D pins

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A= 25 °C and the given supply voltage.

8.5 Capacitances

Table 41 Input/Output Capacitances

Parameter	Symbol	Limit Values	Unit	Notes
		Typ.		
ECLKI input capacitance	C_{ECLKI}	7	pF	f_C = 1 MHz The pins, which are not under test, are connected to GND
ECLKO output capacitance	C_{ECLKO}	7	pF	
Input capacitance	C_{IN}	5	pF	
Output capacitance	C_{OUT}	5	pF	

8.6 AC Characteristics

Ambient temperature under bias range, VDD = 3.3 V ± 5 %.

Inputs are driven to 2.4 V for a logical ’1’ and to 0.4 V for a logical ’0’.

Timing measurements for the H.1x0 clock and frame lines are made at 2.0 V for a logical ’1’ and at 0.6 V for a logical ’0’.

Timing measurements for all other signals are made at 2.0 V for a logical ’1’ and at 0.8 V for a logical ’0’.

The AC-testing input/output wave forms are shown below.

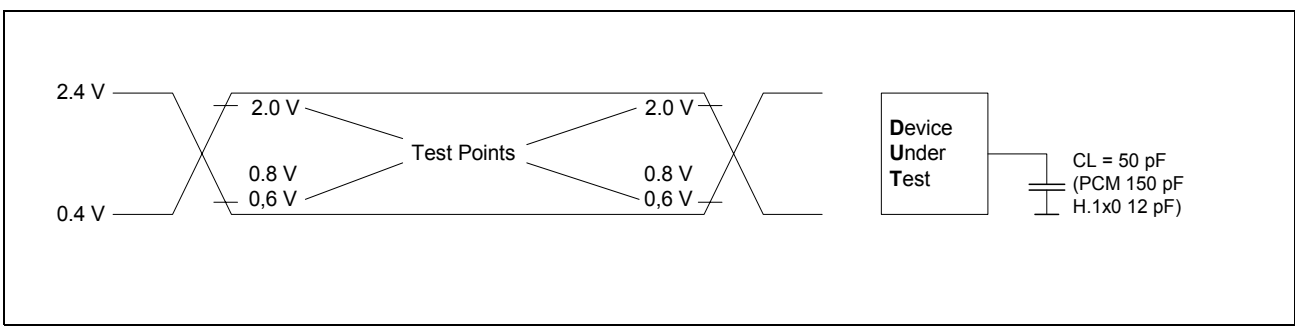


Figure 60 I/O Wave Form for AC-Test

9 Package Outlines

P-BGA-217-1
(Plastic Ball Grid Array Package)

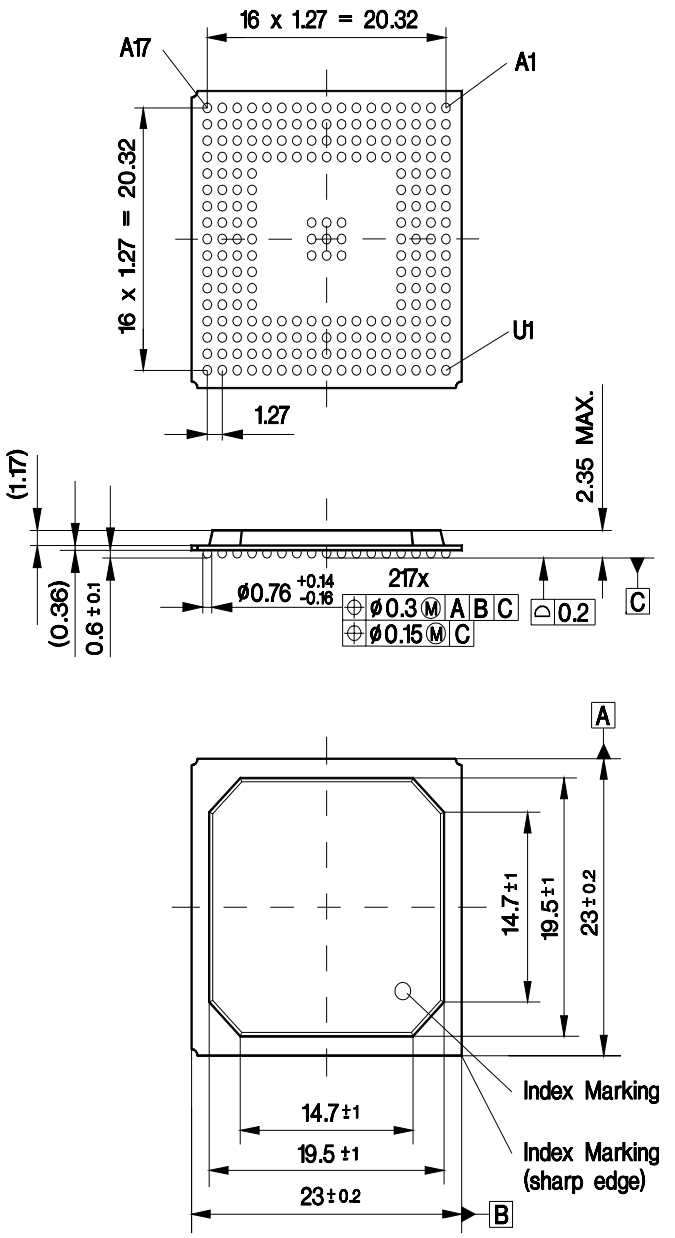


Figure 61 Outlines of P-BGA-217-1

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

PRELIMINARY

A

B

C

D

E

F

G

I

L

M

P

R

S

W

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
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Dr. Ulrich Schumacher

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