

HPND-0002

Small Signal RF PIN Diode Chips for Hybrid Integrated Circuits



Data Sheet

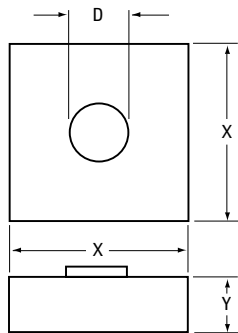
Description

These PIN/NIP diode chips are specifically designed for hybrid applications requiring thermosonic or thermocompression bonding techniques. The top metallization is a layer of gold for a tarnish free surface that allows either thermosonic or thermocompression bonding techniques. The bottom metallization is also gold, suitable for epoxy or eutectic die attach method.

Applications

These small signal, general purpose PIN/NIP diode chips are optimized for various analog and digital applications such as switches, digital phase shifters, pulse and amplitude modulators, limiters, leveling, and attenuating.

HPND-0002 Chip Dimensions



DIMENSIONS	FOR EPOXY OR EUTECTIC DIE ATTACH PART NO. HPND-0002
D (0.03) (1)	0.20 (8)
X (0.05) (2)	0.38 (15)
Y (0.03) (1)	0.20 (8)
TOP CONTACT	CATHODE
BOTTOM CONTACT	ANODE

DIMENSIONS IN MILLIMETERS
(1/1000 INCH).

Features

- Thermocompression/Thermosonically Bondable
- Ideal for Hybrid Integrated Circuits
- Gold Metallization
- Silicon Nitride Passivation
- Uniform Electrical Characteristics
- Batch Matched Versions Available
- Planar Construction

Maximum Ratings

Junction Operating and Storage Temperature Range:

-65°C to +150°C

T_A = 25°C

PD Power Dissipation: 250 mW

(Measured in an infinite heat sink derated linearly to zero at 150°C.)

Operation in excess of any one of these conditions may result in permanent damage to this device.

Electrical Specifications at $T_A = 25^\circ\text{C}$

Chip for Epoxy or Eutectic Die Attach HPND-	Nearest Equivalent Surface Mount Part No. HSMP-	Nearest Equivalent Axial Lead Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Capacitance C_j (pF)	Typical Parameters		
					Series Resistance R_S (Ω)	Typical Carrier Lifetime τ (ns)	Typical Reverse Recovery Time τ_{rr} (ns)
0002	3810	3081	100	0.20	3.5	1500	300
Test Conditions			$V_R = V_{BR}$ Measure $I_R \leq 10 \mu\text{A}$	$V_R = 50 \text{ V}$ $f = 1.0 \text{ MHz}$	$I_F = 100 \text{ mA}$ $f = 100\text{MHz}$	$I_F = 50 \text{ mA}$ $I_R = 250 \text{ mA}$	$I_F = 20 \text{ mA}$ $V_R = 10 \text{ V}$ 90% Recovery

Assembly and Handling

Procedures for PIN Chips:

1. Storage

Devices should be stored in a dry nitrogen purged desiccator or equivalent.

2. Cleaning

If required, surface contamination may be removed with electronic grade solvents. Typical solvents, such as freon (T.F. or T.M.C.), acetone, deionized water, and methanol, or their locally approved equivalents, can be used singularly or in combinations. Typical cleaning times per solvent are one to three minutes. DI water and methanol should be used (in that order) in the final cleans. Final drying can be accomplished by placing the cleaned dice on clean filter paper and drying with an infrared lamp for 5-10 minutes. Acids such as hydrofluoric (HF), nitric (HNO_3), and hydrochloric (HCl) should not be used.

The effects of cleaning methods/ solutions should be verified on small samples prior to submitting the entire lot. Following cleaning, dice should be either used in assembly (typically within a few hours) or stored in clean containers in a reducing atmosphere or a vacuum chamber.

3. Die Attach

a. Eutectic

Eutectic die attach can be accomplished by “scrubbing” the die with/without a preform on the header to combine with the silicon in the die. Temperature is approximately 400°C , with heating times of 5-10 seconds. (Note—times and temperature utilized may vary depending on the type, composition, and heat capacity of the header or substrate used.) This method is recommended for HPND-0002.

b. Epoxy

For epoxy die-attach, conductive silver-filled epoxies are recommended. This method can be used for all Avago Technologies’ PIN chips.

4. Wire Bonding

Either ultrasonic, thermosonic or thermocompression bonding techniques can be employed. Suggested wire is pure gold, 0.7 to 1.5 mil diameter.

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies, Limited in the United States and other countries. Data subject to change. Copyright © 2006 Avago Technologies Limited. All rights reserved. Obsoletes 5965-9143E
AV01-0640EN - November 28, 2006

Avago
TECHNOLOGIES