

HCD65R600T / HCU65R600T

650V N-Channel Super Junction MOSFET

Features

- Very Low FOM ($R_{DS(on)} \times Q_g$)
- Extremely low switching loss
- Excellent stability and uniformity
- 100% Avalanche Tested

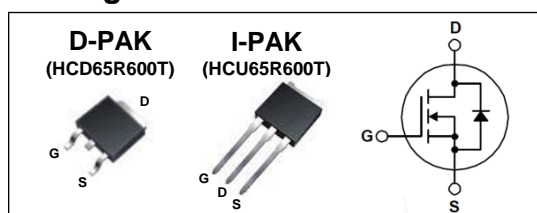
Application

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- TV power & LED Lighting Power

Key Parameters

Parameter	Value	Unit
$BV_{DSS} @ T_{j,max}$	700	V
I_D	7.5	A
$R_{DS(on), max}$	0.6	Ω
Q_g, Typ	14	nC

Package & Internal Circuit



Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	± 30	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$)	7.5	A
	Drain Current – Continuous ($T_C = 100^\circ\text{C}$)	4.7	A
I_{DM}	Drain Current – Pulsed (Note 1)	22	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	160	mJ
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	57	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	2.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient *	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_J=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.5	--	4.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 2.5\ \text{A}$	--	0.54	0.6	Ω

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\ \text{V}, I_D = 250\ \mu\text{A}$	650	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650\ \text{V}, V_{GS} = 0\ \text{V}$	--	--	10	μA
		$V_{DS} = 520\ \text{V}, T_J = 125\text{ }^\circ\text{C}$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 30\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	± 100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1.0\ \text{MHz}$	--	590	770	pF
C_{oss}	Output Capacitance		--	41	54	pF
C_{rss}	Reverse Transfer Capacitance		--	6.5	8.5	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 325\ \text{V}, I_D = 7.5\ \text{A},$ $R_G = 25\ \Omega$	--	18	46	ns
t_r	Turn-On Rise Time		--	20	50	ns
$t_{d(off)}$	Turn-Off Delay Time		--	60	130	ns
t_f	Turn-Off Fall Time		--	22	54	ns
Q_g	Total Gate Charge	$V_{DS} = 520\ \text{V}, I_D = 7.5\ \text{A}$ $V_{GS} = 10\ \text{V}$	--	14.0	18.5	nC
Q_{gs}	Gate-Source Charge		--	3.2	--	nC
Q_{gd}	Gate-Drain Charge		--	4.2	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I_S	Continuous Source-Drain Diode Forward Current	--	--	7.5	A	
I_{SM}	Pulsed Source-Drain Diode Forward Current	--	--	22		
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 7.5\ \text{A}, V_{GS} = 0\ \text{V}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$I_S = 7.5\ \text{A}, V_{GS} = 0\ \text{V}$ $di_F/dt = 100\ \text{A}/\mu\text{s}$	--	300	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.4	--	μC

Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{AS}=3.0\text{A}, V_{DD}=50\text{V}, R_G=25\Omega,$ Starting $T_J=25\text{ }^\circ\text{C}$
3. Pulse Test : Pulse Width $\leq 300\mu\text{s},$ Duty Cycle $\leq 2\%$

Typical Characteristics

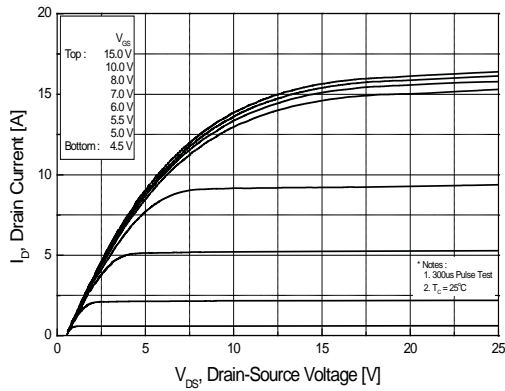


Figure 1. On Region Characteristics

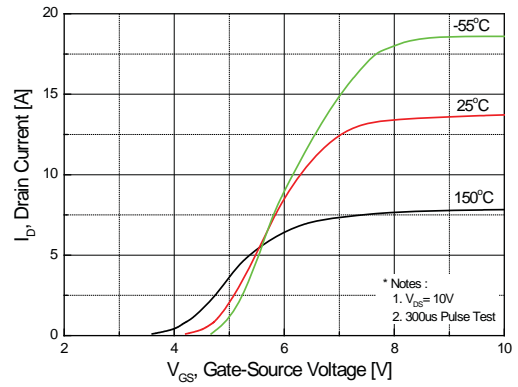


Figure 2. Transfer Characteristics

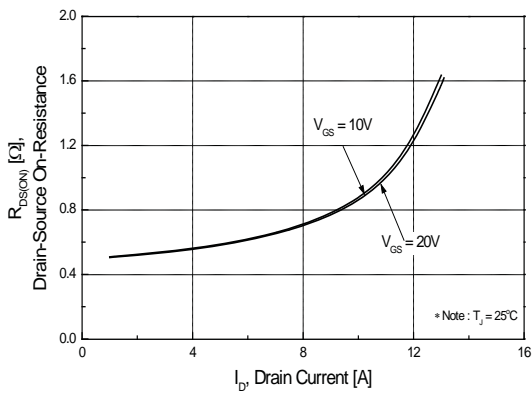


Figure 3. On Resistance Variation vs. Drain Current and Gate Voltage

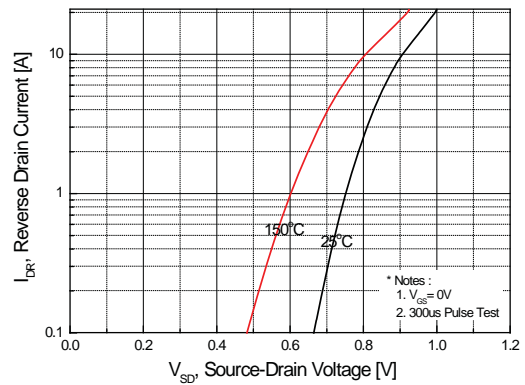


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

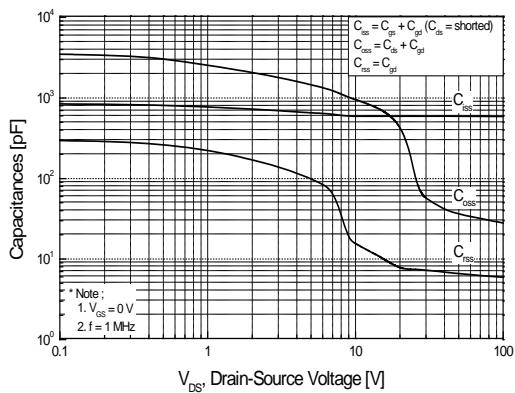


Figure 5. Capacitance Characteristics

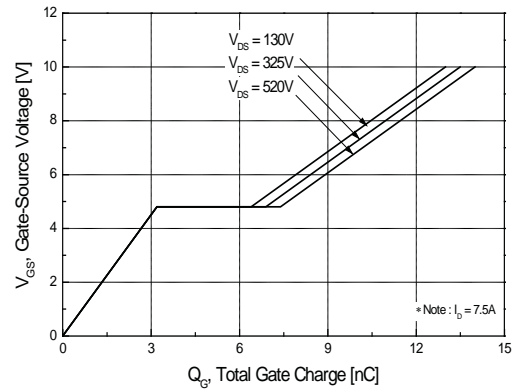


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

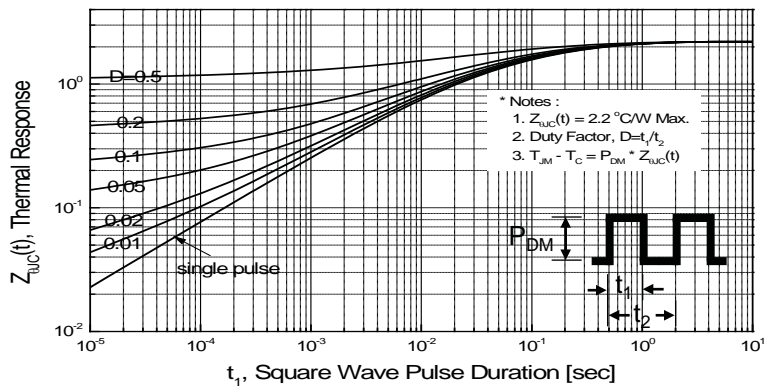
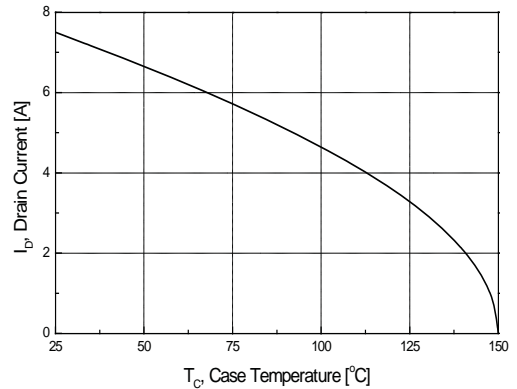
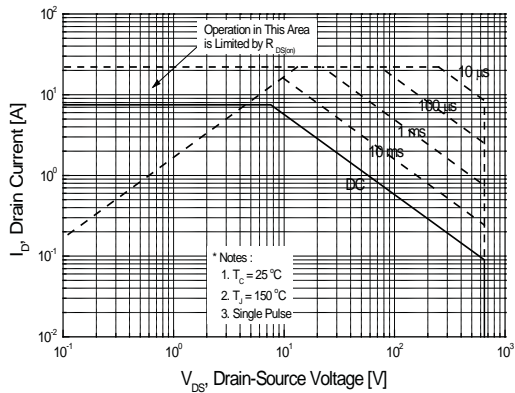
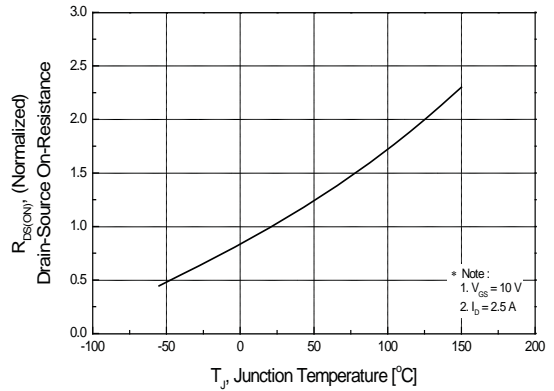
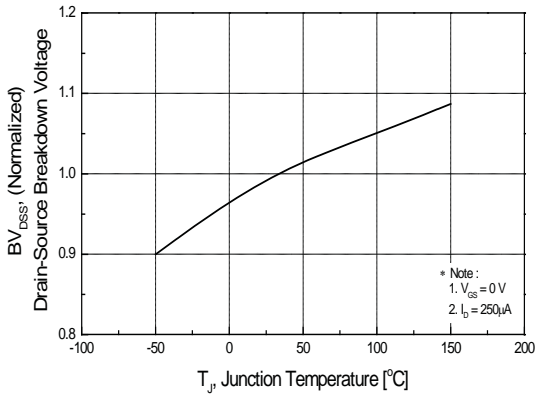


Fig 12. Gate Charge Test Circuit & Waveform

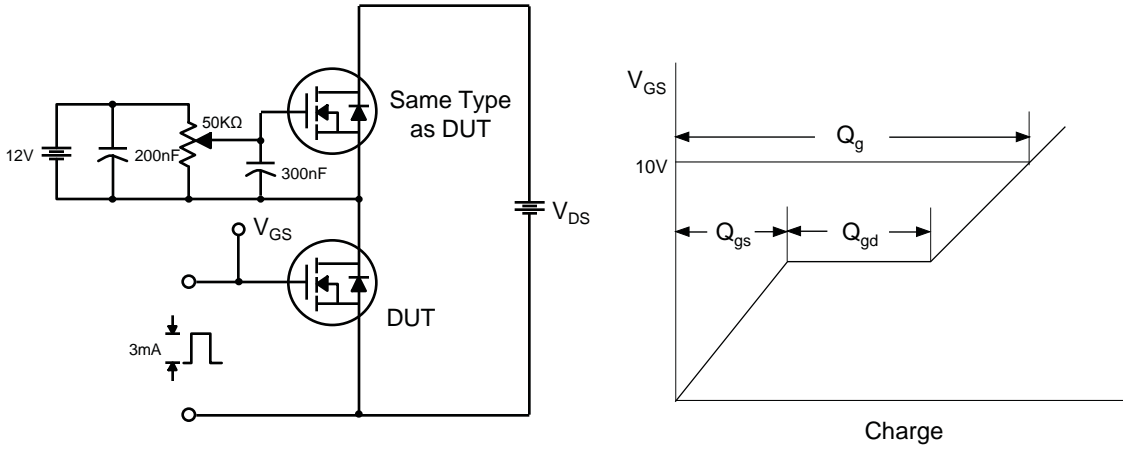


Fig 13. Resistive Switching Test Circuit & Waveforms

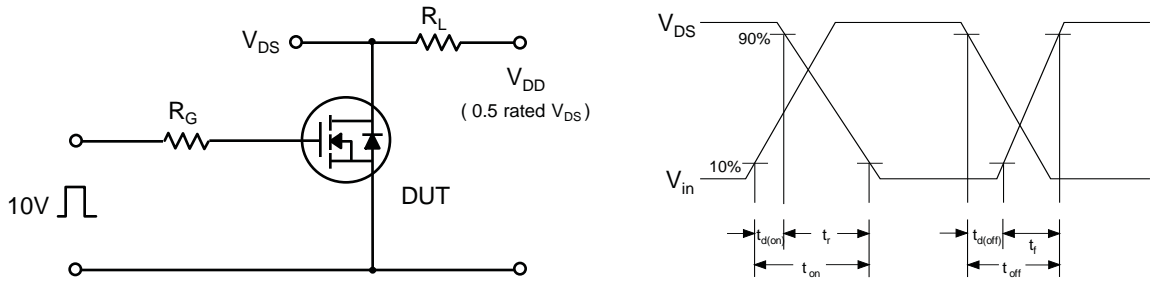


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

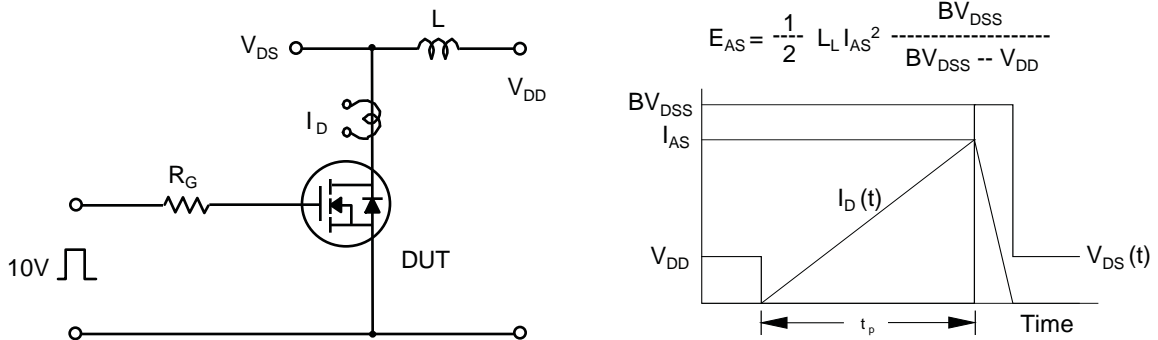
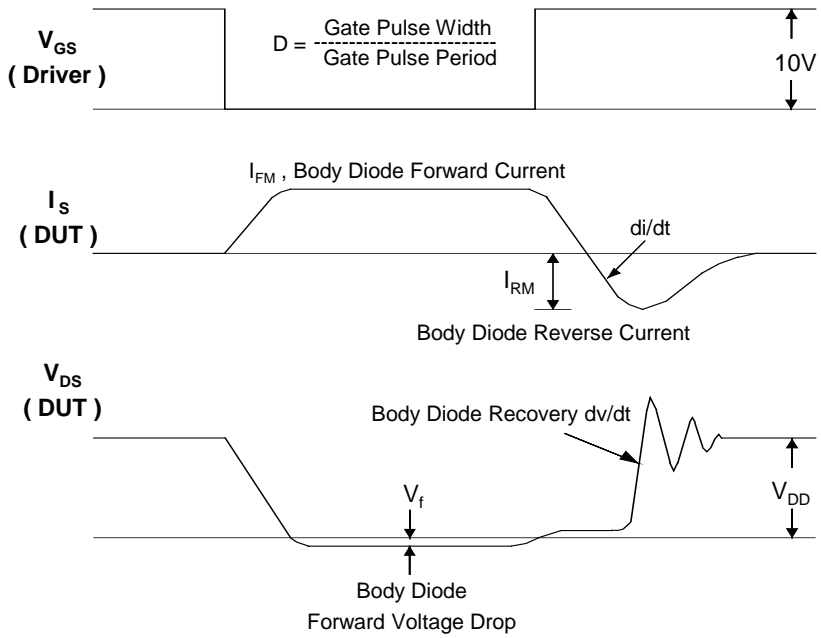
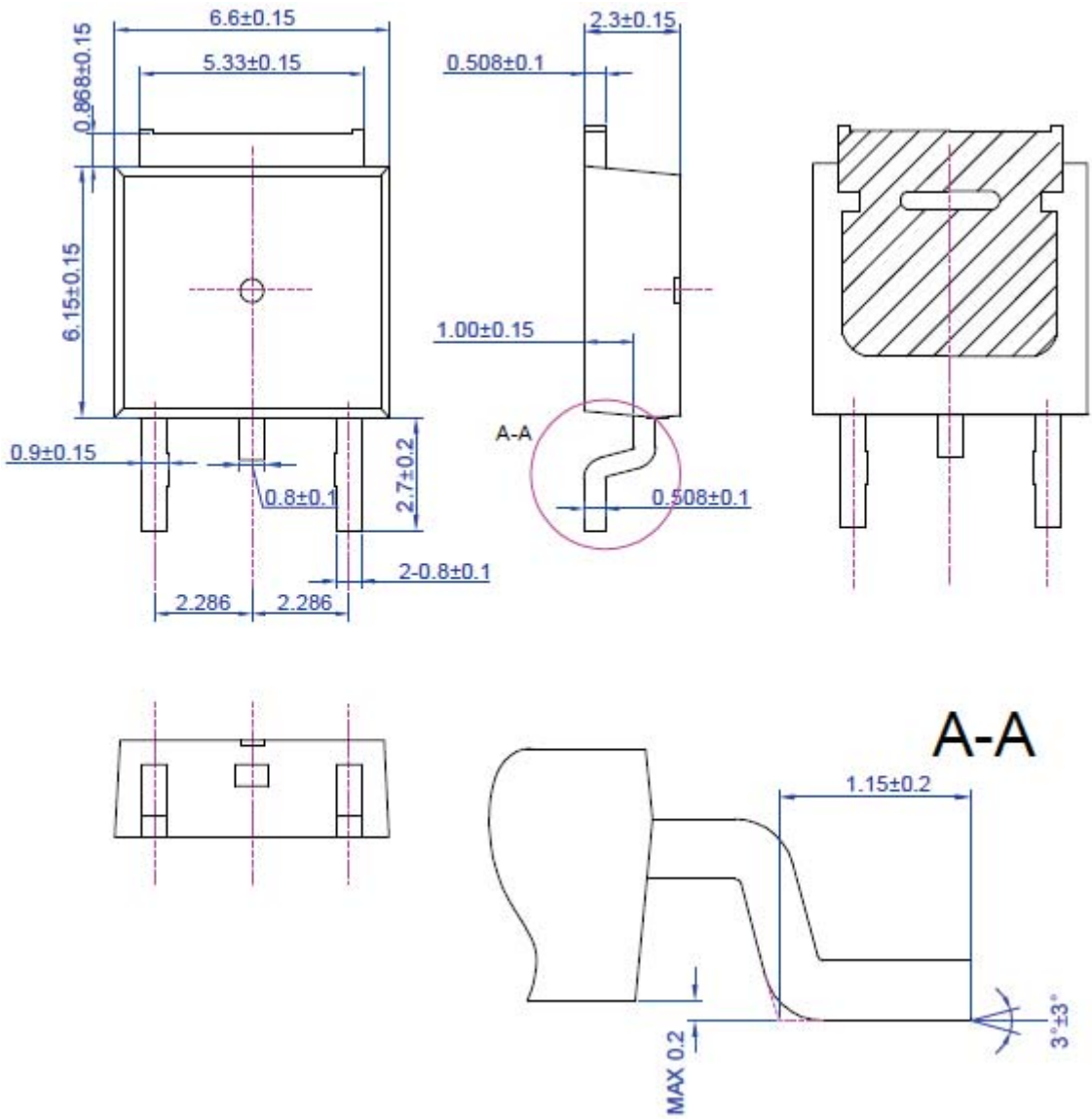


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

D-PAK
(TO-252A)



Package Dimension

I-PAK
(TO-251A)

