

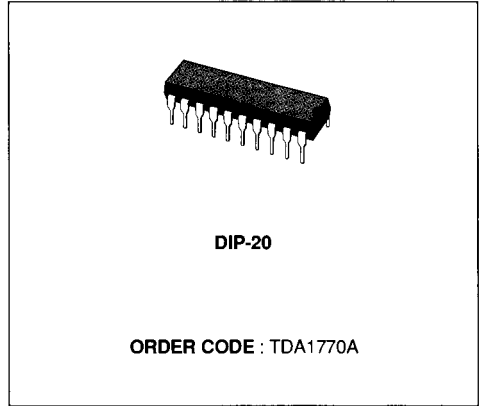
VERTICAL DEFLECTION CIRCUIT

ADVANCE DATA

The functions incorporated are :

- SYNCHRONIZATION CIRCUIT
- PRECISION OSCILLATOR AND RAMP GENERATOR
- POWER OUTPUT AMPLIFIER
- FLYBACK GENERATOR
- VOLTAGE REGULATOR
- PRECISION BLANKING PULSE GENERATOR
- THERMAL SHUT DOWN PROTECTION
- CRT SCREEN PROTECTION CIRCUIT WHICH BLANKS THE BEAM CURRENT IN THE EVENT OF LOSS OF VERTICAL DEFLECTION CURRENT.

The TDA 1770 A is assembled in a new 20-lead plastic package which has 4 centre pins connected together and used for heatsinking.

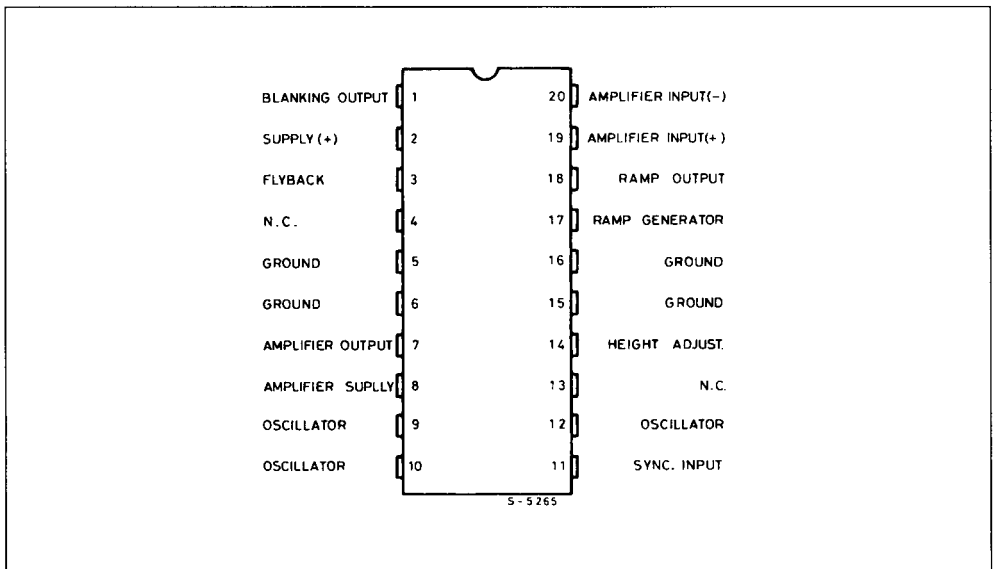


DESCRIPTION

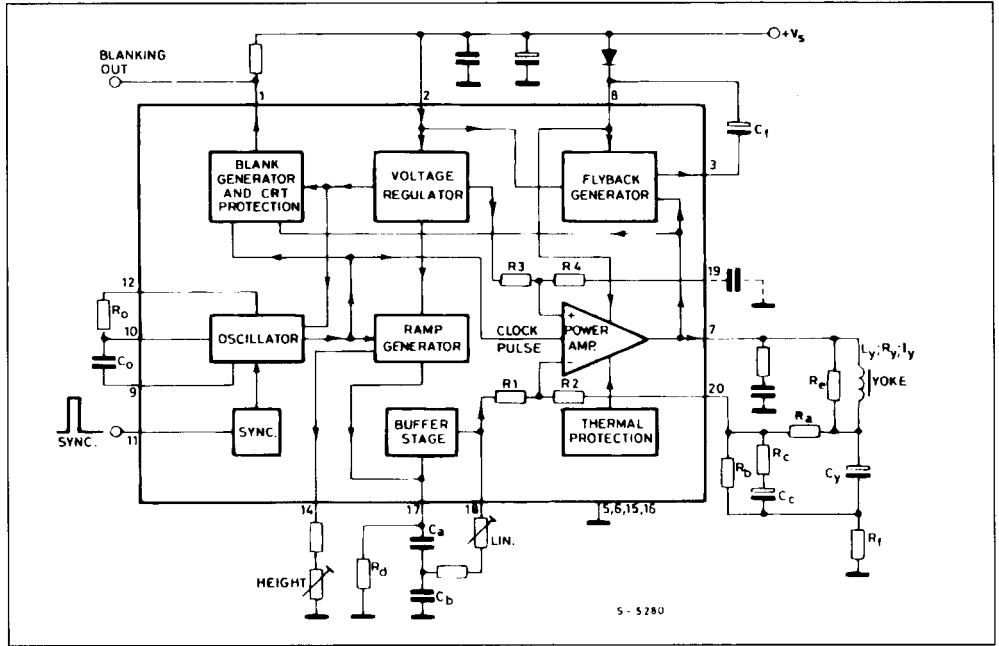
The TDA 1770A is a monolithic integrated circuit in 20-lead plastic package. It is a full performance and very efficient vertical deflection circuit intended for direct drive of the yoke.

It offers a wide range of applications in portable CTVs, BW TVs, monitors and displays.

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 2	35	V
V_7, V_8	Flyback Peak Voltage	60	V
V_{11}	Sync. Input Voltage	20	V
V_{19}, V_{20}	Power Amplifier Input Voltage	V_S - 10	V
V_1	Voltage at Pin 1	V_S	
I_o	Output Current (non repetitive) at $t = 2$ msec	2	A
I_o	Output Peak Current at $f = 50$ Hz $t > 10$ μ sec	1.2	A
I_o	Output Peak Current at $f = 50$ Hz $t \leq 10$ μ sec	2.2	A
I_3	Pin 3 Peak to Peak Flyback Current at $f = 50$ Hz, $t_{fly} \leq 1.5$ msec	2	A
I_3	Pin 3 DC Current at $V_7 < V_2$	50	mA
P_{Tot}	Maximum Power Dissipation : at $T_{pins} \leq 90$ °C at $T_{amb} = 70$ °C	4.3 1	W W
T_{stg}, T_J	Storage and Junction Temperature	- 40 to 150	°C

THERMAL DATA

$R_{th j-pins}$	Thermal Resistance Junction-pins	Max	14	°C/W
$R_{th j-amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS ($V_s = 35\text{ V}$, $T_{\text{amb}} = 25\text{ }^\circ\text{C}$, unless otherwise specified)**DC CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current			25	45	mA	1b
I_8	Pin 8 Quiescent Current	$I_7 = 0$		16	36	mA	1b
$-I_{17}$	Ramp Generator Bias Current	$V_{17} = 0$		0.02	1	μA	1a
$-I_{17}$	Ramp Generator Current	$V_{17} = 0$; $-I_{14} = 20\text{ }\mu\text{A}$	18.5	20	21.5	μA	1b
$\frac{ \Delta I_{17} }{I_{17}}$	Ramp Generator Non-linearity	$\Delta V_{17} = 0$ to 15 V $I_{14} = 20\text{ }\mu\text{A}$		0.2	1	%	1b
V_1	Blanking Output Saturation Voltage	$I_1 = 10\text{ mA}$		0.35	0.5	V	1b
V_3	Pin 3 Saturation Voltage to Ground	$I_3 = 20\text{ mA}$		1	1.5	V	1a
V_7	Quiescent Output Voltage	$V_s = 35\text{ V}$; $R_a = 2.2\text{ K}\Omega$ $R_b = 1\text{ K}\Omega$	16.4	17.8	19.5	V	1a
		$V_s = 15\text{ V}$; $R_a = 390\text{ }\Omega$ $R_b = 1\text{ K}\Omega$	6.9	7.5	8.1	V	
V_{7L}	Output Saturation Voltage to Ground	$I_7 = 0.7\text{ A}$		0.7	1	V	1c
V_{7H}	Output Saturation Voltage to Supply	$-I_7 = 0.7\text{ A}$		1.3	1.8	V	1d
V_{10}	Oscillator Virtual Ground			0.45		V	1a
V_{14}	Regulated Voltage at Pin 14	$-I_{14} = 20\text{ }\mu\text{A}$	6.3	6.6	7	V	1b
$\frac{\Delta V_{14}}{\Delta V_s}$	Regulated Voltage Drift with Supply Voltage	$\Delta V_s = 15$ to 35 V		1	2	mV/V	1b
V_{19}	Amplifier Input (+) Reference Voltage		4.1	4.4	4.7	V	1b

Figure 1 : DC Test Circuit.
Figure 1a.

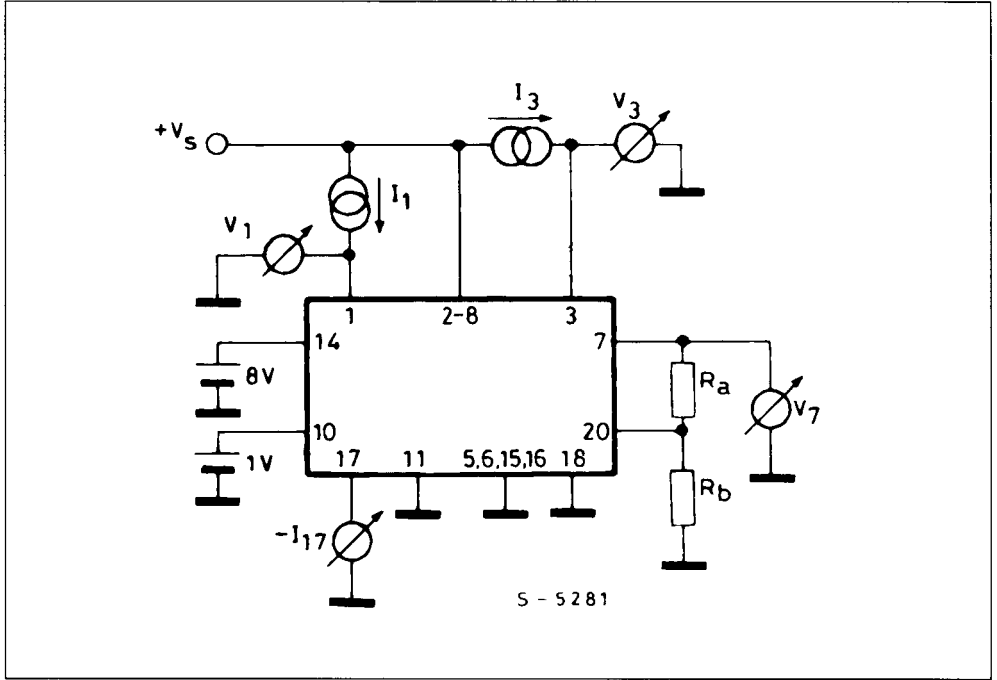


Figure 1b.

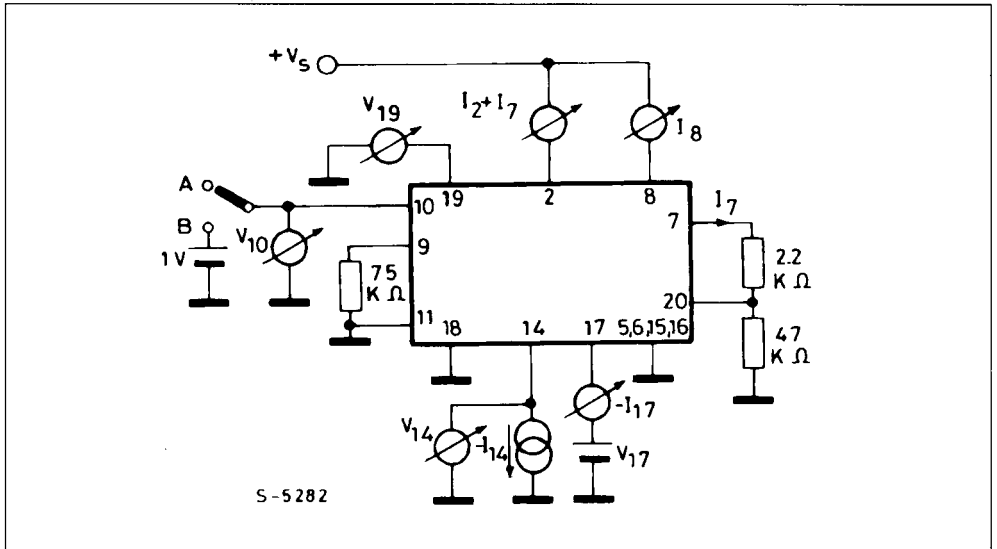


Figure 1c.

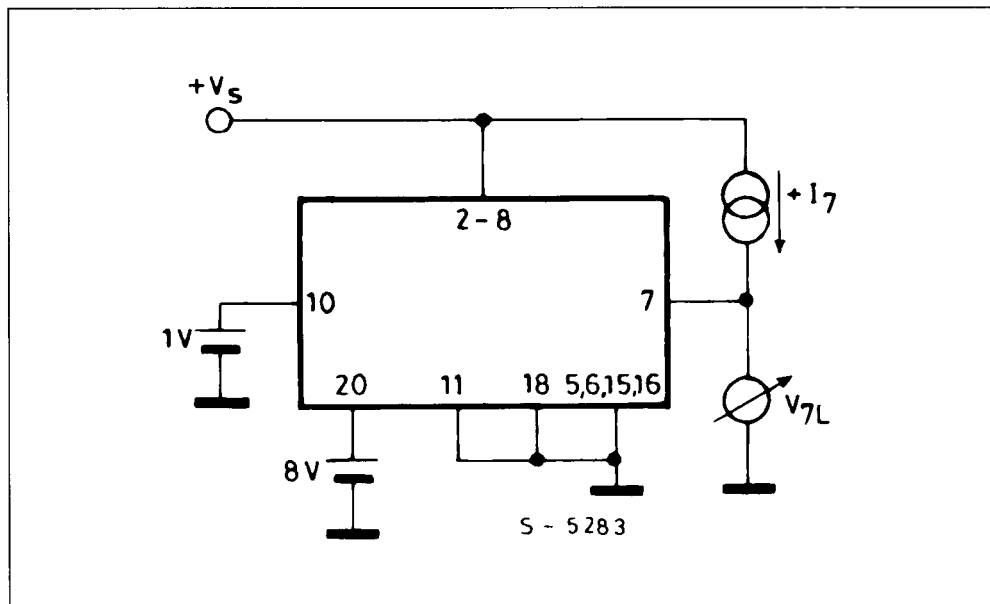
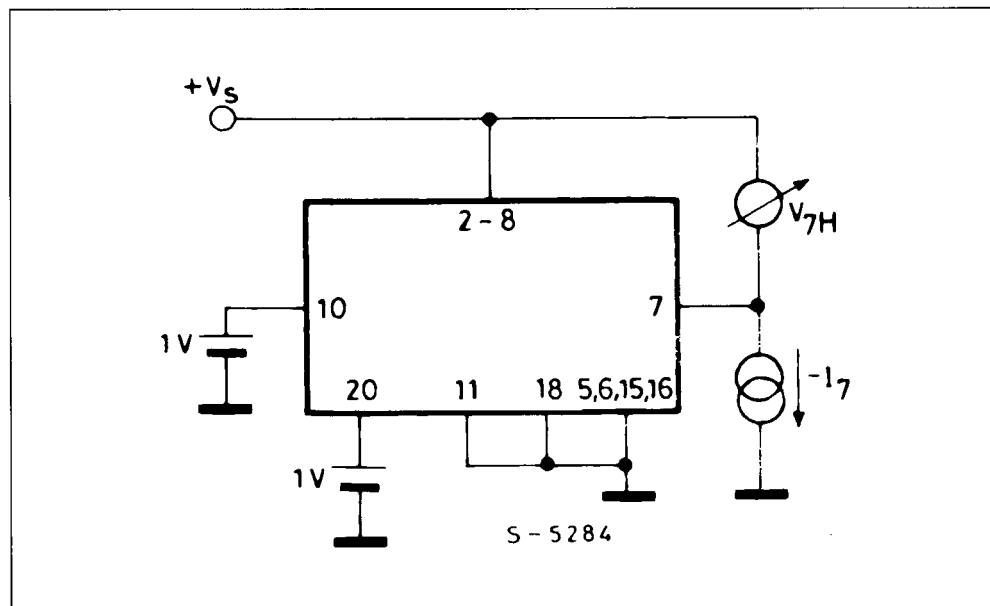


Figure 1d.



ELECTRICAL CHARACTERISTICS

(refer to the AC test circuit, $V_s = 22\text{ V}$, $f = 50\text{ Hz}$; $T_{amb} = 25\text{ }^\circ\text{C}$, unless otherwise specified)

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_s	Supply Current	$I_y = 1\text{ App}$		160		mA
I_{11}	Sync. Input Current		100			μA
V_7	Flyback Voltage	$I_y = 1\text{ App}$		42		V
V_9	Peak to Peak Oscillator Sawtooth Voltage	$I_{11} = 0$		3.6		V
		$I_{11} = 100\text{ }\mu\text{A}$		3.4		V
V_{18thL}	Starts Scan Level of the input Ramp			1.7		V
t_{fly}	Flyback Time	$I_y = 1\text{ App}$		0.75		msec
t_{blank}	Blanking Pulse Duration	$f_o = 50\text{ Hz}$ $T_j = 75\text{ }^\circ\text{C}$	1.33	1.4	1.47	ms
		$f_o = 60\text{ Hz}$ $T_j = 75\text{ }^\circ\text{C}$		1.17		ms
f_o	Free Running Frequency	$R_o = 7.5\text{ K}\Omega$ $T_j = 75\text{ }^\circ\text{C}$ $C_o = 330\text{ nF}$	42	43.5	46	Hz
		$R_o = 6.2\text{ K}\Omega$ $T_j = 75\text{ }^\circ\text{C}$ $C_o = 330\text{ nF}$		52.5		Hz
Δf	Synchronization Range	$I_{11} = 100\text{ }\mu\text{A}$ $T_j = 75\text{ }^\circ\text{C}$	14	16		Hz
T_j	Junction Temperature for Thermal Shut-down			145		$^\circ\text{C}$

Figure 2 : AC Test Circuit.

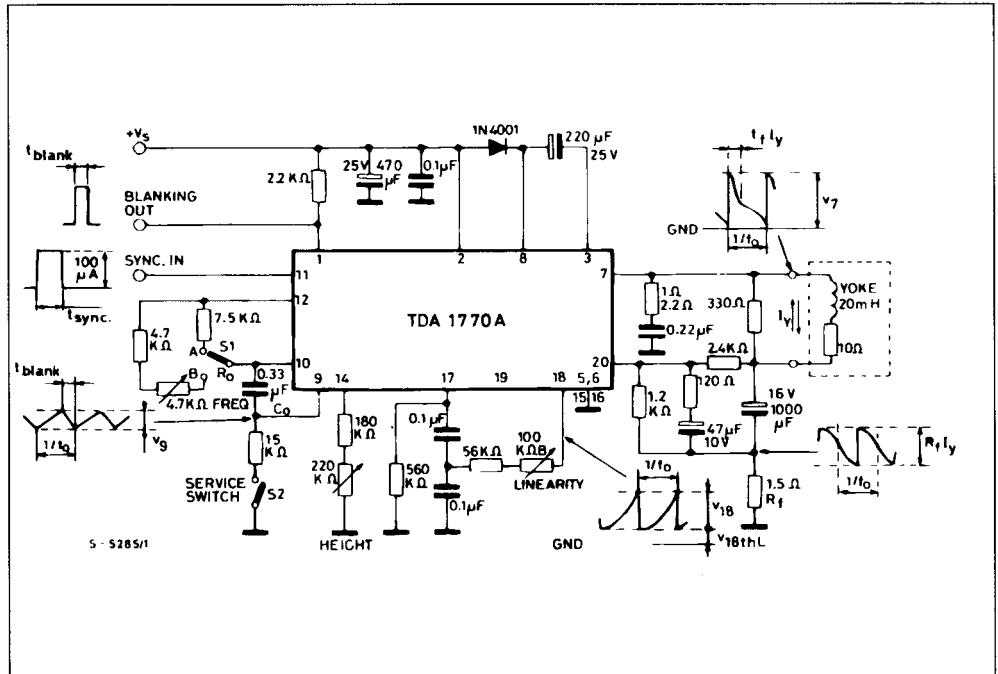
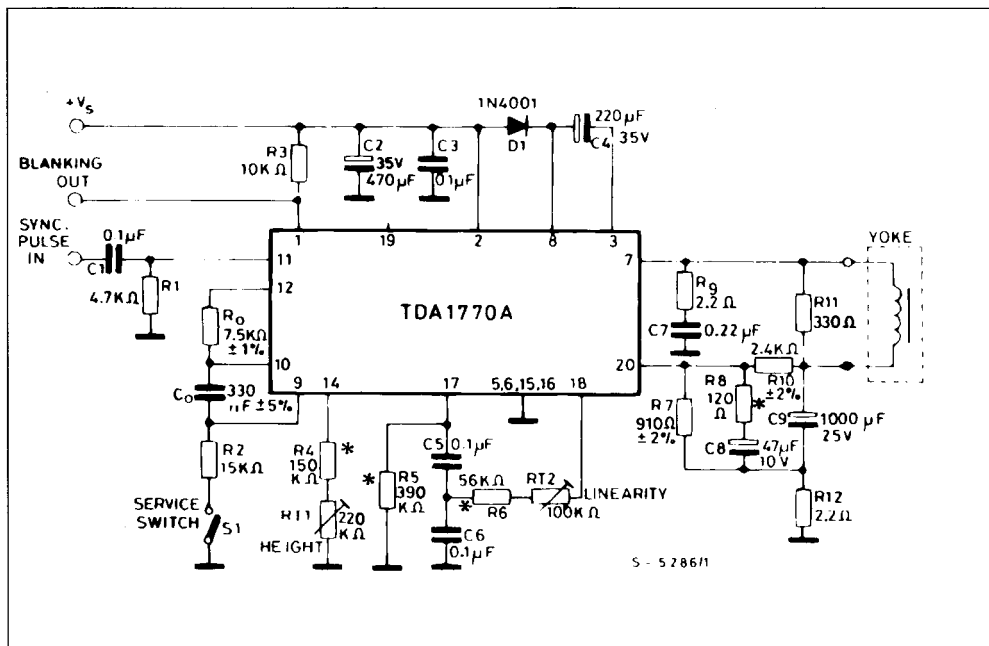


Figure 3 : Typical Application Circuit for SmaI Screen 90 ° TVC Set ($R_y = 15 \Omega$, $L_y = 30 \text{ mH}$, $I_y = 0.82 \text{ App}$).



* The value depends on the characteristics of the CRT. The value shown is indicative only.

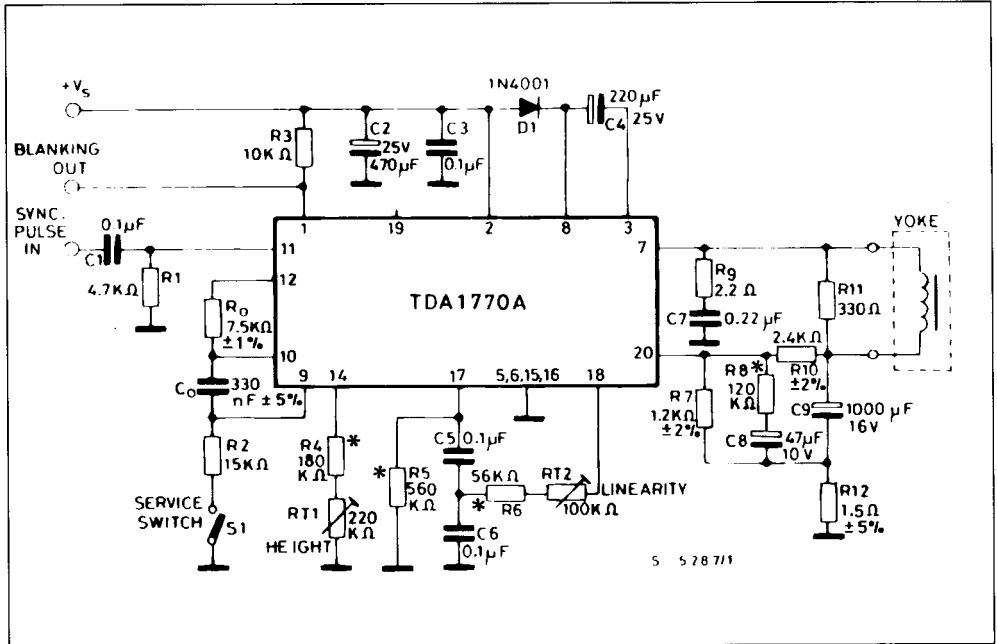
TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_s	Minimum Supply Voltage	25	V
I_s	Supply Current	140	mA
t_{fly}	Flyback Time	0.7	msec
t_{blk}	Blanking Time	1.4	msec
f_o	Free Running Frequency	43.5	Hz
* P_{tot}	Total Dissipation	2.4	W
* $R_{th \text{ heatsink}}$ **	Thermal Resistance of the Heatsink for $T_{amb} = 60 \text{ }^\circ\text{C}$ and $T_{j \text{ max}} = 130 \text{ }^\circ\text{C}$	8	$^\circ\text{C/W}$

* Worst case condition.

** See "Thermal considerations".

Figure 4 : Typical Application Circuit for B/W TV set ($R_y = 10 \Omega$; $L_y = 20 \text{ mH}$; $l_y = 1 \text{ App}$).



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* The value depends on the characteristics of the CRT. The value shown is indicative only.

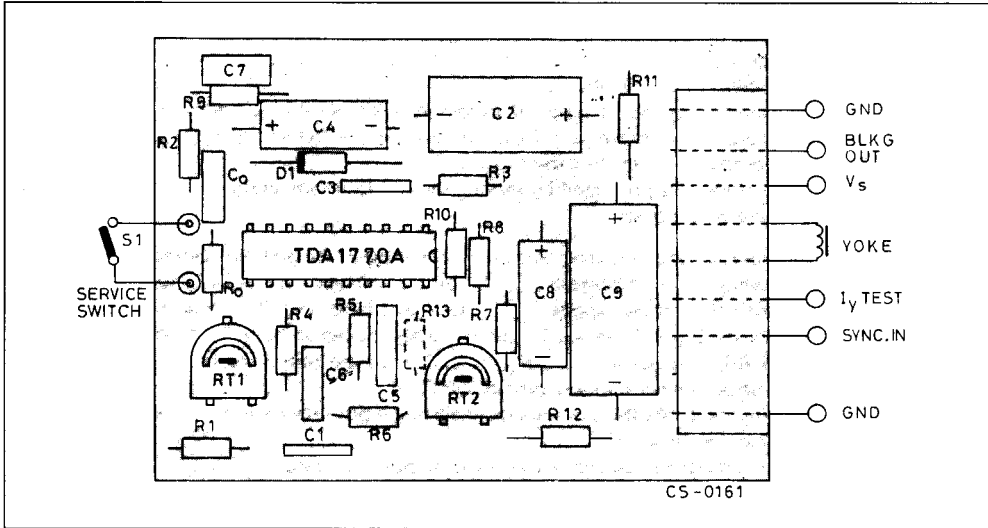
TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_s	Minimum Supply Voltage	20	V
I_s	Supply Current	160	mA
t_{fly}	Flyback Time	0.75	msec
t_{blkg}	Blanking Time	1.4	msec
f_o	Free Running Frequency	43.5	Hz
* P_{tot}	Power Dissipation	2.1	W
** $R_{th \text{ heatsink}}$ **	Thermal Resistance of the Heatsink for $T_{amb} = 60 \text{ }^\circ\text{C}$ and $T_{j \text{ max}} = 130 \text{ }^\circ\text{C}$	11	$^\circ\text{C/W}$

* Worst case condition.

** See "Thermal considerations".

Figure 6 : P.C. Board and Components Layout for the Application Circuits of fig. 3, 4 and 5 (1 : 1 scale).



APPLICATION INFORMATION (refer to the block diagram)

OSCILLATOR AND SYNC GATE (clock generation)

The oscillator is obtained by means of an integrator driven by a two threshold circuit that switches R_o high or low so allowing the charge or the discharge of C_o under constant current conditions.

The sync input pulse at the Sync gate lowers the level of the upper threshold and then it controls the period duration. A clock pulse is generated.

Pin 10 is the inverting input of the amplifier used as integrator.

Pin 12 is the output of the switch driven by the internal clock pulse generated by the threshold circuits.

Pin 9 is the output of the amplifier.

Pin 11 is the input for sync pulses (positive).

RAMP GENERATOR AND BUFFER STAGE

A current mirror, the current intensity of which can be externally adjusted, charges one capacitor producing a linear voltage ramp.

The internal clock pulse stops the increasing ramp by a very fast discharge of the capacitor, a new voltage ramp is immediately allowed.

The required value of the capacitance is obtained

by means of the series of two capacitors, C_a and C_b , which allow the linearity control by applying a feedback between the output of the buffer and the tapping from C_a and C_b .

Pin 14 The resistance between pin 14 and ground defines the current mirror current and then the height of the scanning.

Pin 17 is the output of the current mirror that charges the series of C_a and C_b . This pin is also the input of the buffer stage.

Pin 18 is the output of the buffer stage and it is internally coupled to the inverting input of the power amplifier through R_1 .

POWER AMPLIFIER

This amplifier is a voltage-to-current power converter, the transconductance of which is externally defined by means of a negative current feedback.

The output stage of the power amplifier is supplied by the main supply during the trace period, and by the flyback generator circuit during the most of the duration of the flyback time. The internal clock turns off the lower power output stage to start the flyback.

The power output stage is thermally protected by sensing the junction temperature and then by putting off the current sources of the power stage.

Pin 20 is the inverting input of the amplifier. An external network, R_a and R_b , defines the DC level across C_y so allowing a correct centering of the output voltage. The series network R_c and C_c , in conjunction with R_a and R_b , applies at the feedback input pin 20 a small part of the parabola, available across C_y , and the AC feedback voltage, taken across R_f . The external components R_c , R_a and R_d , produce the linearity correction on the output scanning current I_y and their values must be optimized for each type of CRT.

Pin 19 is the non-inverting input. At this pin the non-inverting input reference voltage supplied by the voltage regulator can be measured.

This pin is used on a quasi-bridge configuration or on portable TVS.

Pin 7 is the output of the power amplifier and it drives the yoke by a negative slope current ramp I_y . R_e and the Boucherot cell are used to stabilize the power amplifier.

Pin 8 the supply voltage of the power output stage is forced at this pin. During the trace time the supply voltage is obtained from the main supply voltage V_s by a diode, while during the retrace time this pin is supplied from the flyback generator.

FLYBACK GENERATOR

This circuit supplies both the power amplifier output stage and the yoke during the most of the duration of the flyback time (retrace).

The internal clock opens the loop of the amplifier and lets pin 1 floating so allowing the rising of the flyback. Crossing the main supply voltage at pin 2, the flyback pulse front end drives the flyback generator in such a way allowing its output to reach and overcome the main supply voltage, starting from a low condition forced during the trace period.

An integrated diode stops the rising of this output increase and voltage jump is transferred by means of capacitor C_f at the supply voltage pin of the power stage (pin 8).

THERMAL CONSIDERATIONS (a note referred to fig. 3, 4 and 5)

The shown value of case to ambient thermal resistance is the equivalent to three thermal resistances that are :

R_1 – Thermal resistance junction to ambient of the device.

R_2 – Thermal resistance of the p.c. copper side.

When the current across the yoke changes its direction, the output of the flyback generation falls down to the main supply voltage and it is stopped by means of the saturated output darlington at a high level. At this time the flyback generator starts to supply the power amplifier output stage by a diode inside the device. The flyback generator supplies the yoke too.

Later, the increasing flyback current reaches the peak value and then the flyback time is completed : the trace period restarts. The output of the power amplifier (pin 7) falls under the main supply voltage and the output of the flyback generator is driven for a low state so allowing the flyback capacitor C_f to restore the energy lost during the retrace.

Pin 3 is the output of the flyback generator that, when driven, jumps from low to high condition. An external capacitor C_f transfers the jump to pin 8 (see pin 8).

BLANKING GENERATOR AND CRT PROTECTION

This circuit is a pulse shaper and its output goes high during the blanking period or for CRT protection. The input is internally driven by the clock pulse that defines the width of the blanking time when a flyback pulse has been generated. If the flyback pulse is absent (short circuit or open circuit of the yoke), the blanking output remains high so allowing the CRT protection.

Pin 1 is an open collector output where the blanking pulse is available.

VOLTAGE REGULATOR

The main supply voltage V_s is lowered and regulated internally to allow the required reference voltages for all the above described blocks.

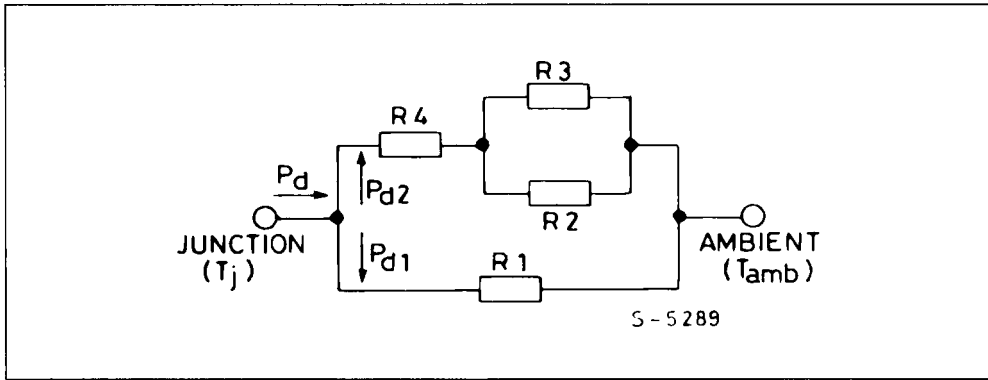
Pin 2 is the main supply voltage input V_s (positive).

Pin 5, 6, 15, 16 are the GND pins or the negative input of V_s .

R_3 – Thermal resistance of the auxiliary heatsink.

The circuit that contains these thermal resistances is shown on fig. 7 where R_3 is the thermal resistance junction to pins of the device and P_d is the maximum dissipated power.

Figure 7 : Semiconductor Heatsink Thermal Circuit.



Since the thermal resistance R3 of the heatsink is defined from its physical and mechanical characteristics, it is necessary to define the required copper side on the p.c. board for the necessary R2 value. For instance, let's consider the application for the 90° yoke.

It is known :

$T_{jmax} = 130\text{ }^{\circ}\text{C}$; $T_{ambmax} = 60\text{ }^{\circ}\text{C}$; $R_{thc-amb} = 8\text{ }^{\circ}\text{C/W}$;
 $R_{thj-pins}$ (or R4) = $14\text{ }^{\circ}\text{C/W}$; $R_{thj-amb} = 80\text{ }^{\circ}\text{C/W}$.

It can be calculated :

$$Pd = \frac{T_{jmax} - T_{ambmax}}{R_{thc-amb} + R_{thj-pins}} = \frac{130 - 60}{8 + 14} = 3.18\text{ W}$$

Using an auxiliary heatsink of a thermal resistance R3 = 20 °C/W (including some losses), it can be easily calculated (see fig. 7) : R2 = 94 °C/W.

From fig. 9, it can be found : $l \geq 21\text{ mm}$.

MOUNTING INSTRUCTIONS

The $R_{thj-amb}$ of the TDA 1770 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (fig. 8) or to an external heatsink.

The diagram of figure 9 shows the R_{th} as a function of the side "l" of two equal square copper areas

having a thickness of 35 μ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 8 : Example of P.C. Board Copper Area which is Used as Heatsink.

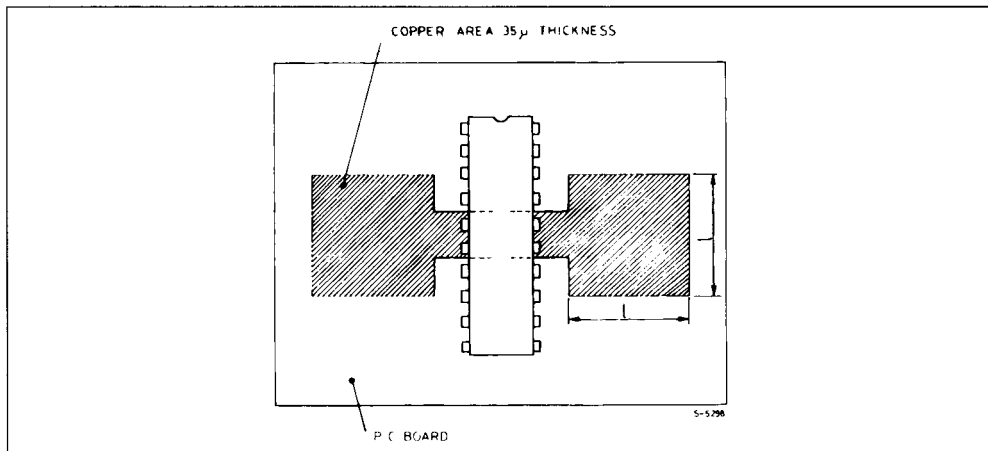


Figure 9 : Thermal Resistance of the P.C. Copper Side vs. Side "I".

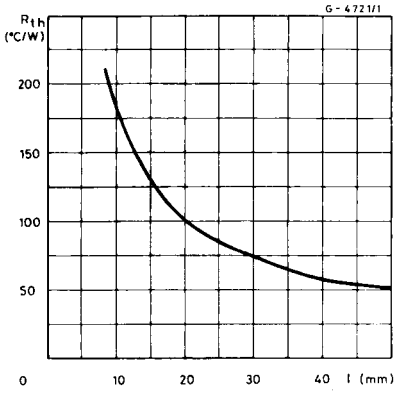


Figure 10 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

