FAIRCHILD
SEMICONDUCTOR®

April 2004

FDT461N

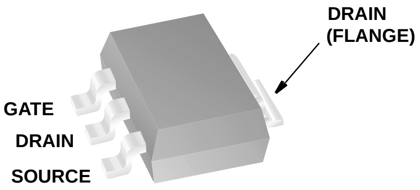
N-Channel Logic Level PowerTrench® MOSFET
100V, 0.4A, 2.5Ω

Features

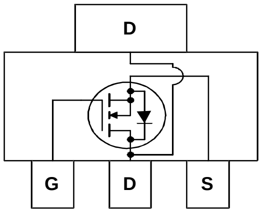
- $r_{DS(ON)}$ = 1.45Ω (Typ.), V_{GS} = 4.5V, I_D = 0.4A
- Q_g(tot) = 2.36nC (Typ.), V_{GS} = 10V
- Low Miller Charge
- Low Q_{RR} Body Diode

Applications

- Servo Motor Load Control
- DC-DC converters



SOT-223



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_A = 25^{o}C, V_{GS} = 10V, $R_{\theta JA}$= 110^{o}C/W)	0.54	A
	Continuous (T_A = 25^{o}C, V_{GS} = 4.5V, $R_{\theta JA}$= 110^{o}C/W)	0.4	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	6.3	mJ
P_D	Power dissipation	1.13	W
	Derate above 25^{o}C	9	mW/^{o}C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	^{o}C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance Junction to Ambient SOT-223, Pad area = 0.171 in^2	110	^{o}C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient SOT-223, Pad area = 0.068 in^2	128	^{o}C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient SOT-223, Pad area = 0.026 in^2	147	^{o}C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
461	FDT461N	SOT-223	13”	12mm	2500 units

Electrical Characteristics T_A = 25°C unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80V V_{GS} = 0V	-	-	1	μA
		T_C = 125°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	0.8	-	2	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 0.54A, V_{GS} = 10V	-	1.40	2.0	Ω
		I_D = 0.4A, V_{GS} = 4.5V	-	1.45	2.5	
		I_D = 0.54A, V_{GS} = 10V, T_J = 150°C	-	2.80	4.0	

Dynamic Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
C_{ISS}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	74	-	pF
C_{OSS}	Output Capacitance			-	11	-	pF
C_{RSS}	Reverse Transfer Capacitance			-	2.5	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V	V_{DD} = 50V I_D = 0.54A I_g = 1.0mA	-	2.36	4.0	nC
$Q_{g(4.5)}$	Total Gate Charge at 4.5V	V_{GS} = 0V to 4.5V			1.27	2.0	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 1V			0.1	0.15	nC
Q_{gs}	Gate to Source Gate Charge			-	0.37	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau			-	0.27	-	nC
Q_{gd}	Gate to Drain “Miller” Charge			-	0.25	-	nC

Switching Characteristics (V_{GS} = 10V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{ON}	Turn-On Time	V_{DD} = 50V, I_D = 0.54A V_{GS} = 10V, R_{GS} = 120Ω	-	-	6.5	ns
$t_{d(ON)}$	Turn-On Delay Time		-	3	-	ns
t_r	Rise Time		-	1.3	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	63	-	ns
t_f	Fall Time		-	12	-	ns
t_{OFF}	Turn-Off Time		-	-	113	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 0.54A	-	-	1.25	V
		I_{SD} = 0.3A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 0.54A, dI_{SD}/dt = 100A/μs	-	-	22	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 0.54A, dI_{SD}/dt = 100A/μs	-	-	18	nC

Notes:

1: Starting T_J = 25°C, L = 67mH, I_{AS} = 0.43A.

Typical Characteristics T_A = 25°C unless otherwise noted

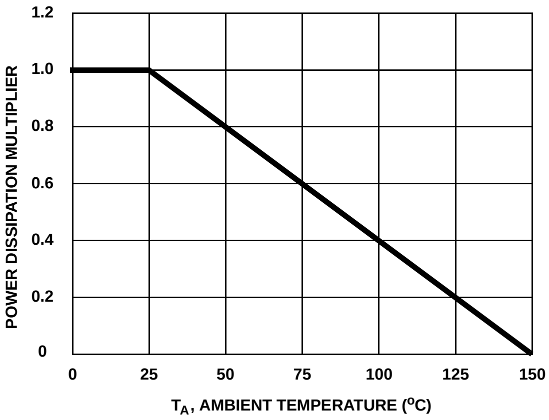


Figure 1. Normalized Power Dissipation vs Ambient Temperature

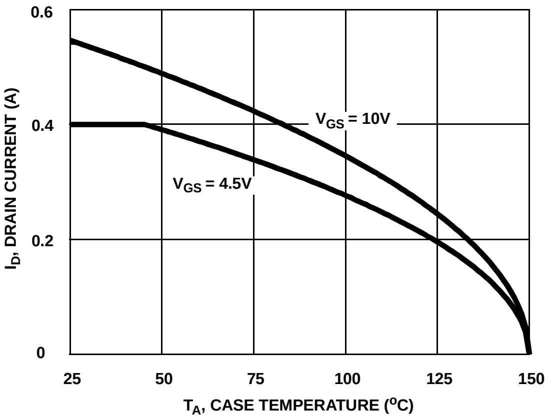


Figure 2. Maximum Continuous Drain Current vs Case Temperature

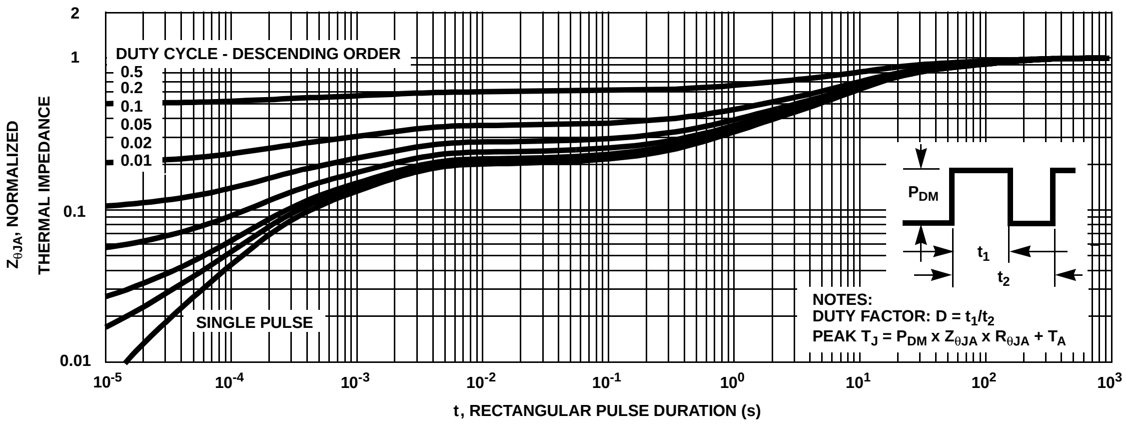


Figure 3. Normalized Maximum Transient Thermal Impedance

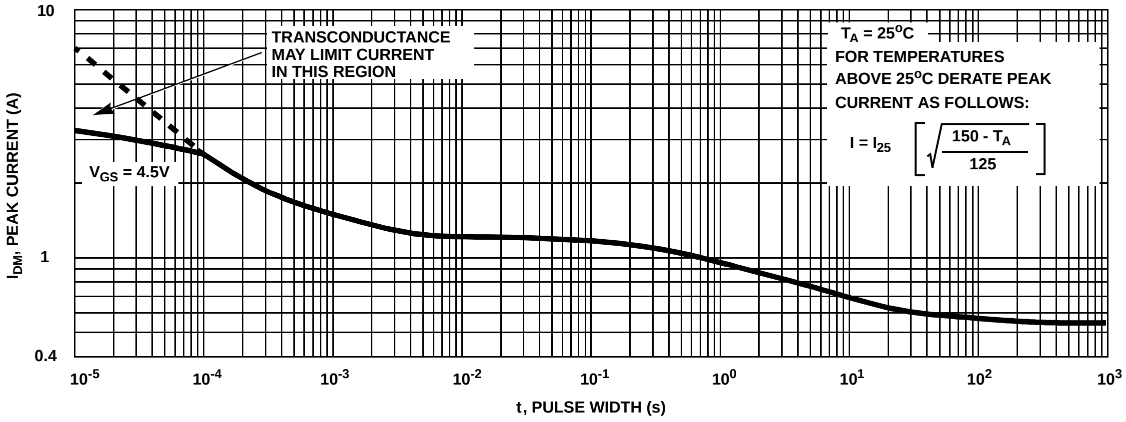


Figure 4. Peak Current Capability

Typical Characteristics T_A = 25°C unless otherwise noted

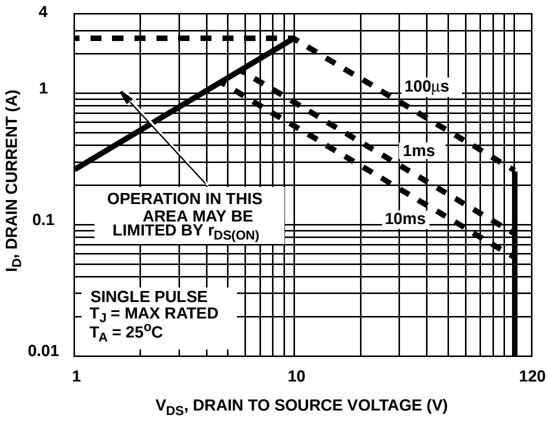


Figure 5. Forward Bias Safe Operating Area

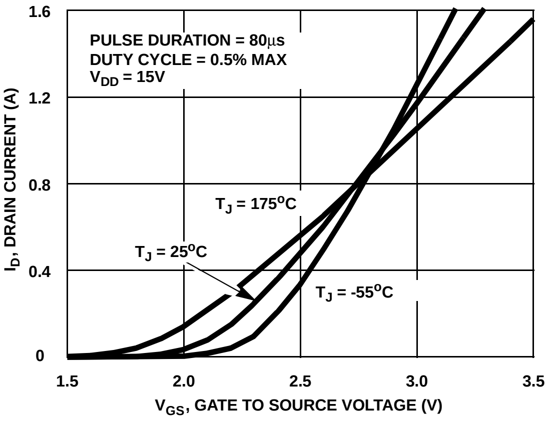


Figure 6. Transfer Characteristics

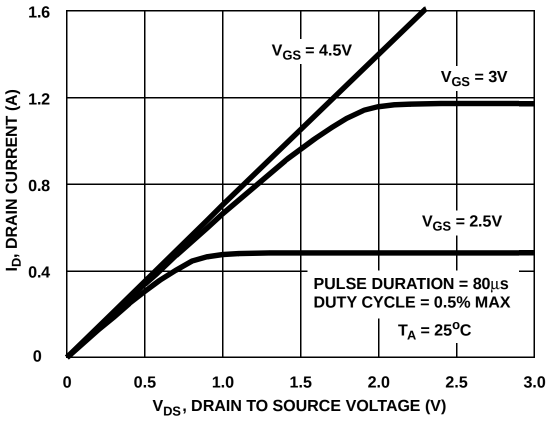


Figure 7. Saturation Characteristics

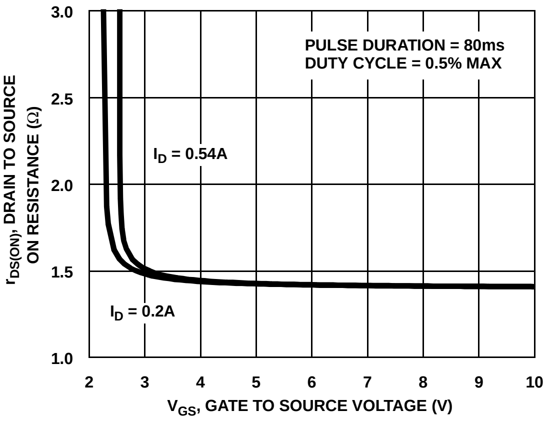


Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current

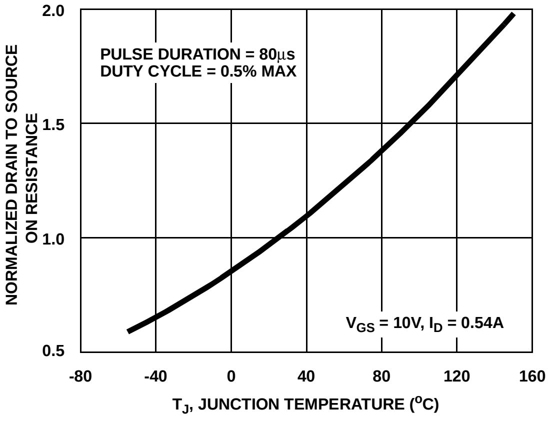


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

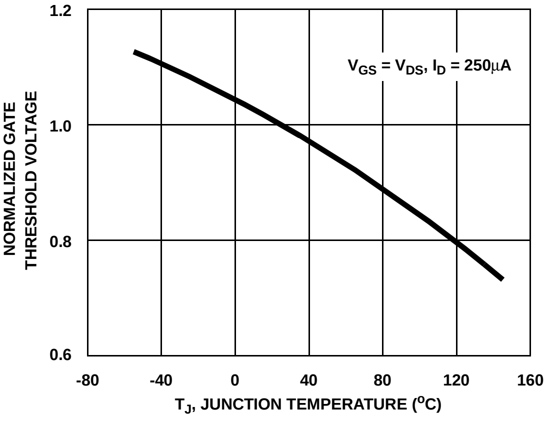


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristics T_A = 25°C unless otherwise noted

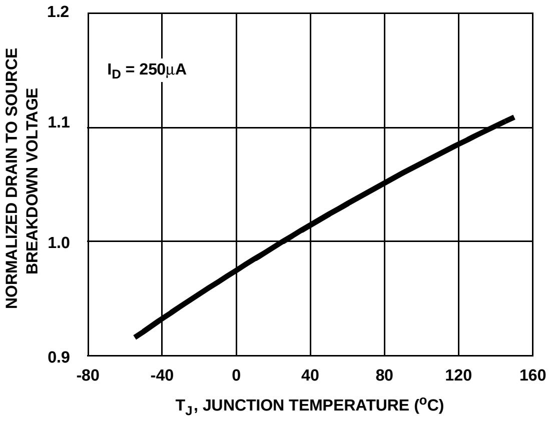


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

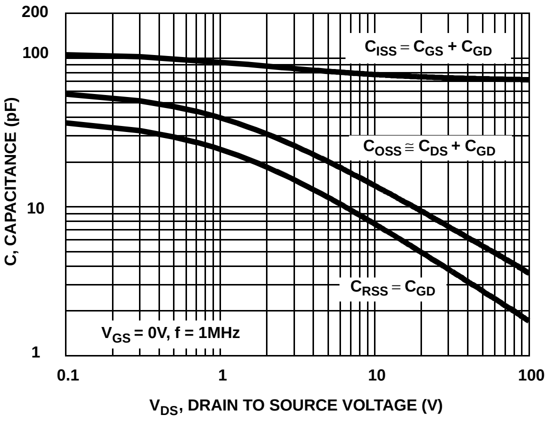


Figure 12. Capacitance vs Drain to Source Voltage

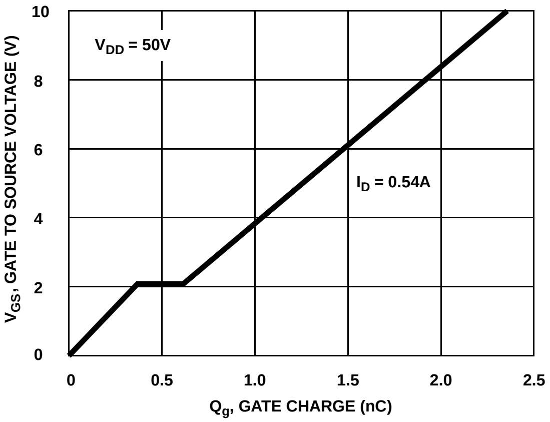


Figure 13. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms

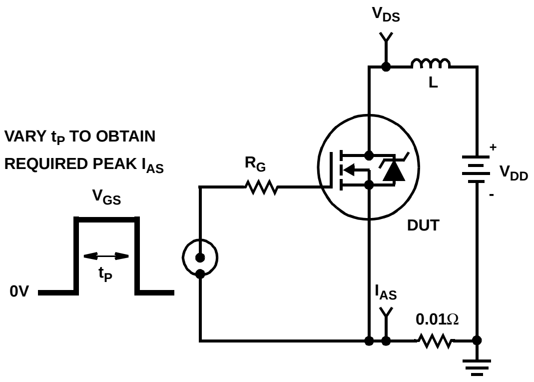


Figure 14. Unclamped Energy Test Circuit

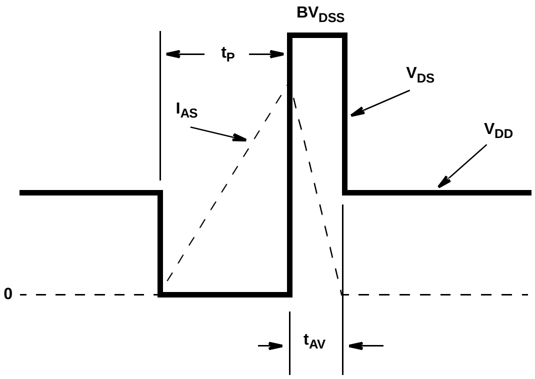


Figure 15. Unclamped Energy Waveforms

Test Circuits and Waveforms (Continued)

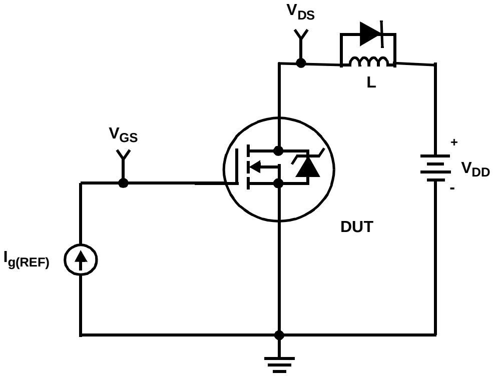


Figure 16. Gate Charge Test Circuit

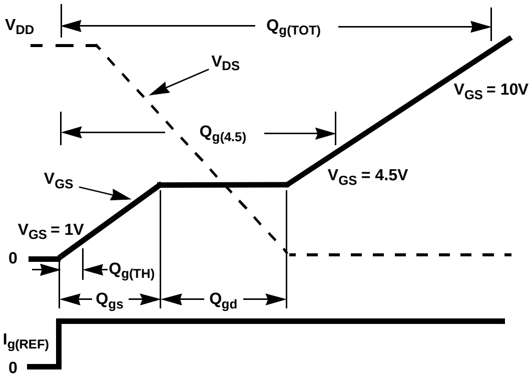


Figure 17. Gate Charge Waveforms

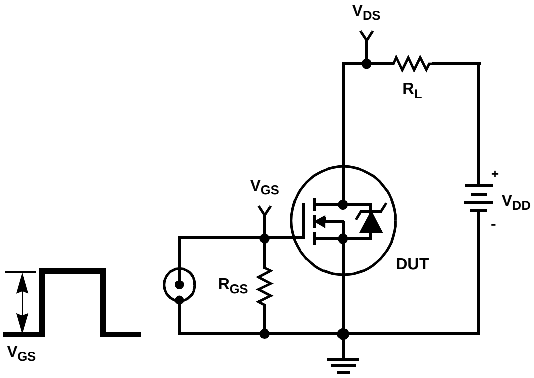


Figure 18. Switching Time Test Circuit

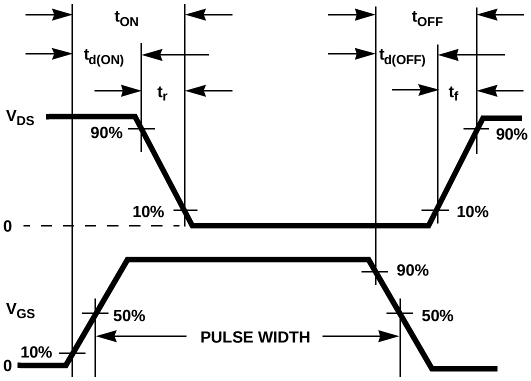
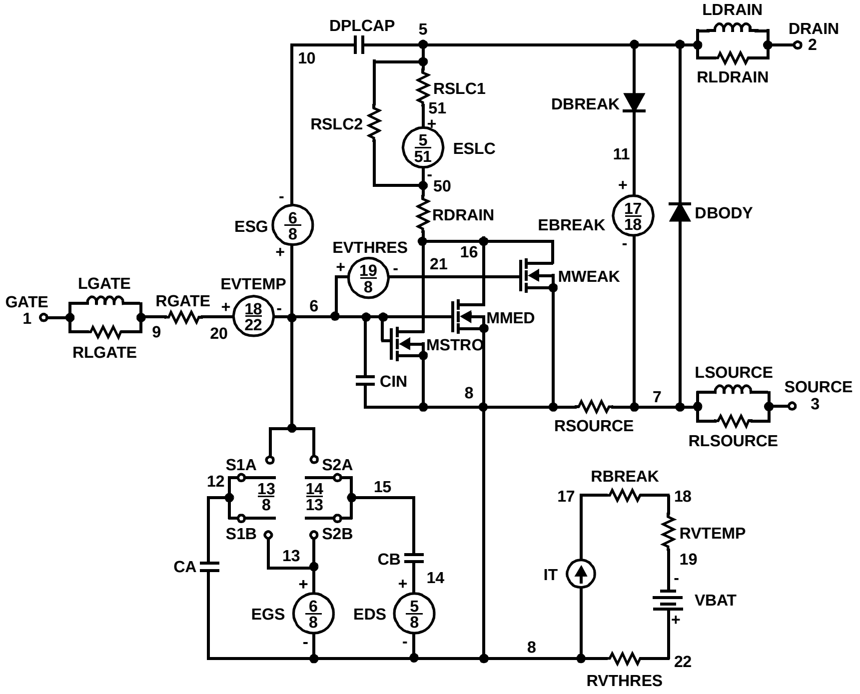


Figure 19. Switching Time Waveforms

PSPICE Electrical Model

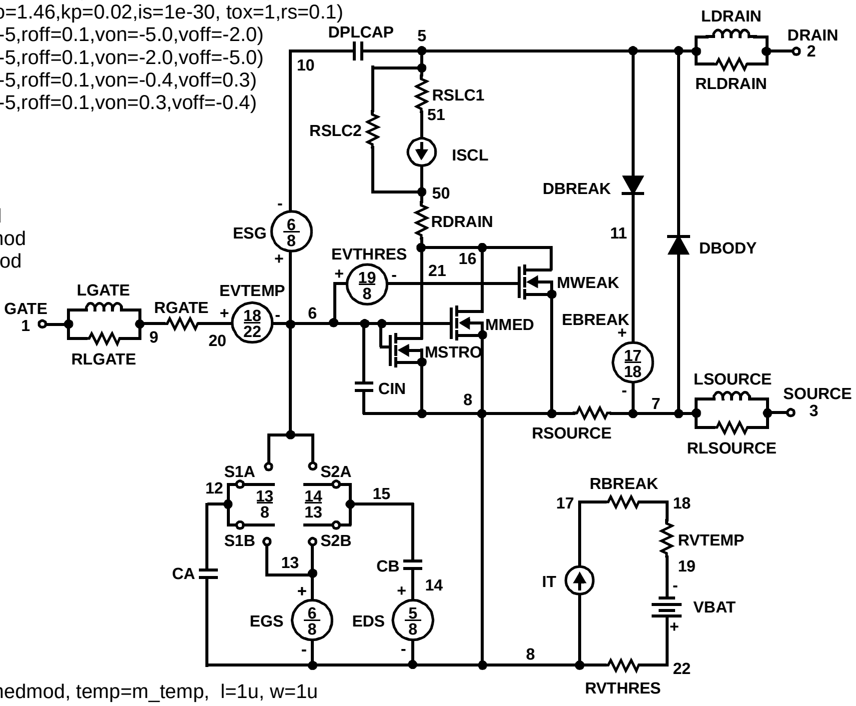


```
.SUBCKT FDT461N  2 1 3 ; rev January 2004
Ca 12 8 1.5e-10
Cb 15 14 1.1e-10
Cin 6 8 7.0e-11

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 109.7
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5.29e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 5.71e-9

RLgate 1 9 52.9
RLdrain 2 5 10
RLsource 3 7 57.1

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 0.9
Rgate 9 20 3.94
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 0.5
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*15),2.5))}

.MODEL DbodyMOD D (IS=6.4E-11  RS=8.0e-3 IKF=0.9 TRS1=2.5e-3 TRS2=9.5e-6
+ CJO=2.2e-11 M=0.52 TT=2.9e-8 XTI=0.1)
.MODEL DbreakMOD D (RS=0.6 TRS1=1.4e-3 TRS2=-5.0e-5)
.MODEL DplcapMOD D (CJO=3.9e-11 IS=1e-30 N=10 M=0.67)

.MODEL MmedMOD NMOS (VTO=1.75 KP=1.2 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=3.94 T_ABS=25)
.MODEL MstroMOD NMOS (VTO=2.03 KP=12 IS=1e-30 N=10 TOX=1 L=1u W=1u T_ABS=25)
.MODEL MweakMOD NMOS (VTO=1.46 KP=0.02 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=39.4 RS=0.1 T_ABS=25)

.MODEL RbreakMOD RES (TC1=1.0e-3 TC2=-8.8e-7)
.MODEL RdrainMOD RES (TC1=7.0e-3 TC2=2.0e-5)
.MODEL RSLCMOD RES (TC1=1.0e-3 TC2=9.0e-6)
.MODEL RsourceMOD RES (TC1=4.8e-3 TC2=1.0e-6)
.MODEL RvthresMOD RES (TC1=-9.0e-4 TC2=-7.0e-6)
.MODEL RvtempMOD RES (TC1=-2.1e-3 TC2=1.8e-6)
 MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5.0 VOFF=-2.0)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.0 VOFF=-5.0)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.4 VOFF=0.3)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.3 VOFF=-0.4)

.ENDS
```

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

```
rev January 2004
template FDT461N  n2,n1,n3 = m_temp
number m_temp=25
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod =  (isl=6.4e-11,rs=8.0e-3,ikf=0.9,trs1=2.5e-3,trs2=9.5e-6,cjo=2.2e-11,m=0.52,tt=2.9e-8,xti=0.1)
dp..model dbreakmod = (rs=0.6,trs1=1.4e-3,trs2=-5e-5)
dp..model dplcapmod =  (cjo=3.9e-11,isl=10e-30,nl=10,m=0.67)
m..model mmedmod = (type=_n,vto=1.75,kp=1.2,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=2.03,kp=12,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=1.46,kp=0.02,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod =  (ron=1e-5,roff=0.1,von=-5.0,voff=-2.0)
sw_vcsp..model s1bmod =  (ron=1e-5,roff=0.1,von=-2.0,voff=-5.0)
sw_vcsp..model s2amod =  (ron=1e-5,roff=0.1,von=-0.4,voff=0.3)
sw_vcsp..model s2bmod =  (ron=1e-5,roff=0.1,von=0.3,voff=-0.4)
c.ca n12 n8 = 1.5e-10
c.cb n15 n14 = 1.1e-10
c.cin n6 n8 = 7.0e-11

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 109.7
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 5.29e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 5.71e-9

res.rlgate n1 n9 = 52.9
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 57.1

m.mmed n16 n6 n8 n8 = model=mmedmod, temp=m_temp,  l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, temp=m_temp,  l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, temp=m_temp,  l=1u, w=1u

res.rbreak n17 n18  = 1, tc1=1.0e-3,tc2=-8.8e-7
res.rdrain n50 n16  = 0.9, tc1=7.0e-3,tc2=2.0e-5
res.rgate n9 n20 = 3.94
res.rslc1 n5 n51  = 1e-6, tc1=1.0e-3,tc2=9.0e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 0.5, tc1=4.8e-3,tc2=1e-6
res.rvthres n22 n8  = 1, tc1=-9.0e-4,tc2=-7.0e-6
res.rvtemp n18 n19  = 1, tc1=-2.1e-3,tc2=1.8e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/15))** 2.5))
}
}
```

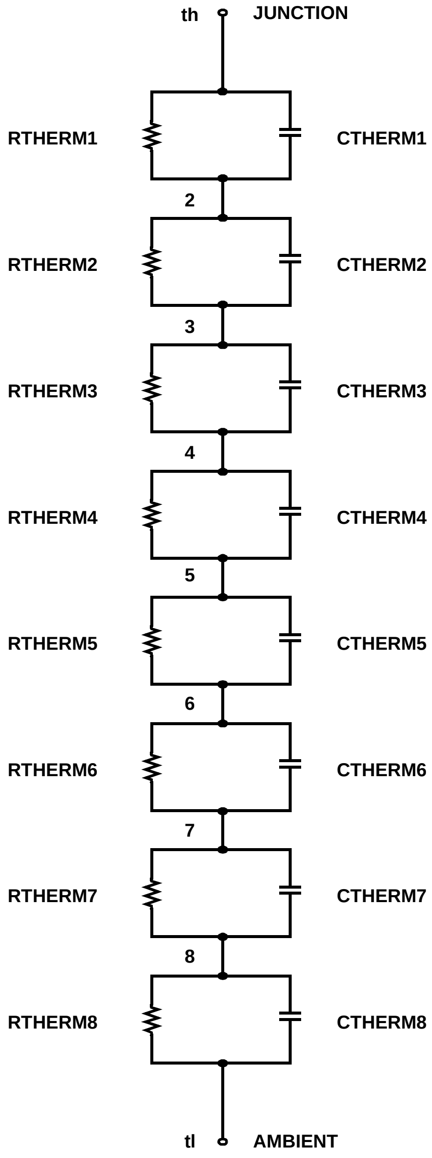


PSPICE Thermal Model

```
REV  January 2004
FDT461N_JA Junction Ambient
Copper Area= 1sq.in

CTHERM1 Junction c2 3.0e-5
CTHERM2 c2 c3 3.2e-5
CTHERM3 c3 c4 2.0e-4
CTHERM4 c4 c5 9.6e-2
CTHERM5 c5 c6 8.9e-1
CTHERM6 c6 c7 9.1e-1
CTHERM7 c7 c8 9.3e-1
CTHERM8 c8 Ambient 7

RTHERM1 Junction c2 0.5
RTHERM2 c2 c3 6
RTHERM3 c3 c4 9
RTHERM4 c4 c5 10
RTHERM5 c5 c6 11
RTHERM6 c6 c7 12
RTHERM7 c7 c8 13
RTHERM8 c8 Ambient 16
```

SABER Thermal Model

```
SABER thermal model FDT461N
Copper Area= 1sq.in
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th c2 = 3.0e-5
ctherm.ctherm2 c2 c3 = 3.2e-5
ctherm.ctherm3 c3 c4 = 2.0e-4
ctherm.ctherm4 c4 c5 = 9.6e-2
ctherm.ctherm5 c5 c6 = 8.9e-1
ctherm.ctherm6 c6 c7 = 9.1e-1
ctherm.ctherm7 c7 c8 = 9.3e-1
ctherm.ctherm8 c8 tl = 7

rtherm.rtherm1 th c2 = 0.5
rtherm.rtherm2 c2 c3 = 6
rtherm.rtherm3 c3 c4 = 9
rtherm.rtherm4 c4 c5 = 10
rtherm.rtherm5 c5 c6 = 11
rtherm.rtherm6 c6 c7 = 12
rtherm.rtherm7 c7 c8 = 13
rtherm.rtherm8 c8 tl = 16
}
```



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FRFET™
GlobalOptoisolator™
GTO™
HiSeC™
I^{2}C™
i-Lo™
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Programmable Active Droop™
ImpliedDisconnect™
ISOPLANAR™
LittleFET™
MICROCOUPLER™
MicroFET™
MicroPak™
MICROWIRE™
MSX™
MSXPro™
OCX™
OCXPro™
OPTOLOGIC®
OPTOPLANAR™
PACMAN™
POP™
Power247™
PowerSaver™
PowerTrench®
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
SILENT SWITCHER®
SMART START™
SPM™
Stealth™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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