![ANALOG DEVICES]

32 Gbps Dual Channel Advanced Linear Equalizer

Data Sheet **HMC6545**

FEATURES

- Supports data rates from dc up to 32 Gbps
- Protocol and data rate agnostic
- Low latency (<170 ps)
- Integrated AGC with differential sensitivity of <50 mV
- Up to 20 dB programmable multiple unit interval input equalization
- Extended chromatic and polarization mode dispersion tolerance
- Programmable differential output amplitude control of up to 600 mV
- Single 3.3 V supply eliminating external regulators
- Wide temperature range from −40°C to +95°C
- 5 mm × 5 mm, 32-lead LFCSP package

APPLICATIONS

- 40 Gbps/100 Gbps DQPSK direct detection receivers
- Short and long reach CFP2 and QSFP+ modules
- CEI-28G MR and CEI-25G LR 100 GE line cards
- 16 Gbps and 32 Gbps Fibre Channel
- Infiniband 14 Gbps FDR and 28 Gbps EDR rates
- Signal conditioning for backplane and line cards
- Broadband test and measurement equipment

FUNCTIONAL BLOCK DIAGRAM

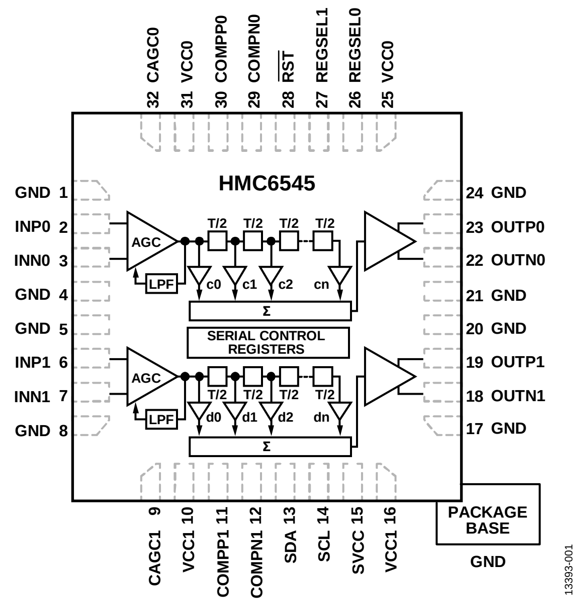

Figure 1.

GENERAL DESCRIPTION

The HMC6545 is a low power, high performance, fully programmable, dual-channel, asynchronous advanced linear equalizer that operates at data rates of up to 32 Gbps. The HMC6545 is protocol and data rate agnostic, and it can operate on the transmit path to predistort a transmitted signal to invert channel distortion or on the receiver path to equalize the distorted and attenuated received signal. The HMC6545 is effective in dealing with chromatic and polarization mode dispersion and intersymbol interference (ISI) caused by a wide variety of transmission media (backplane or fiber) and channel lengths.

The HMC6545 consists of an automatic gain control (AGC); dc offset correction circuitry; a 9-tap, 18 ps spaced feedforward equalizer (FFE); a summing node; and a linear programmable output driver. The input AGC linearly attenuates or amplifies the distorted input signal to generate a constant voltage at the input of the FFE. The 9-tap FFE is programmed via 2-wire interface to generate wide range frequency responses that are precursor or postcursor in nature for compensating signal impairments. After FFE tap coefficients are summed at the summing node, the signal is received by a linear output driver. DC offset correction circuitry is controlled either automatically or manually via Forward Error Correction (FEC).

All high speed differential inputs and outputs of the HMC6545 are current mode logic (CML) and terminated on chip with 50 Ω to the positive supply, 3.3 V, and can be dc-coupled or ac-coupled. The inputs and outputs of the HMC6545 can be operated either differentially or single-ended. The low power, high performance, and feature rich HMC6545 is packaged in a 5 mm × 5 mm, 32-lead LFCSP package. The device uses a single 3.3 V supply, eliminating external regulators. The HMC6545 operates over a −40°C to +95°C temperature range.

Rev. A Document Feedback

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REVISION HISTORY

10/15—Revision A: Initial Version

SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, typical values at V_{CC} = 3.3 V, T_A = 25°C.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER CONSUMPTION						
Supply Voltage	V_{CC}		3.00	3.30	3.45	V
Supply Current	I_{CCMAX}	Single channel; all tap amplifiers active		130	150	mA
	I_{CCMIN}	Single channel; single-tap amplifier active		93		mA
Power-Down Supply Current				17		mA
DC Offset Correction		At maximum AGC gain				
Automatic			−60		+60	mV
Manual			−60		+60	mV
CML INPUT PORT (INP0, INN0, INP1, INN1)						
Input Termination	R_{IN}	Differential input resistance	80	100	120	Ω
CML OUTPUT PORT (OUTP0, OUTN0, OUTP1, OUTN1)						
Output Termination	R_{OUT}	Single-ended output resistance	45	55	65	Ω
Output Level						
High	V_{OH}		V_{CC}			V
Output	V_{OL}				V_{CC} − 0.5	V
CMOS INPUT (SDA, SCL, $\overline{RST}$, REGSEL0, REGSEL1)						
Input Voltage Level						
High	V_{IH}		V_{CC} − 1.3			V
Input	V_{IL}				0.8	V
Input Current	I_{IL}, I_{IH}	V_{IL} = 0 V or V_{IH} = V_{CC}	−100		+100	µA

AC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, typical values at V_{CC} = 3.3 V, T_A = 25°C.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT					
Data Rate		DC		32	Gbps
Range	Differential input range for linear AGC operation, THD < 5%	40		880	mV p-p
Input Equalization			20		dB
DIFFERENTIAL AMPLITUDE					
Input		40		1600	mV p-p
Output	Input signal: PRBS 2^{31} − 1 at 100 mV p-p				
Linear AGC Operation	THD < 5%; AGC = 2; all taps enabled, Tap 4 gain = 63, gain of all other taps = 0, predriver gain = 63		410		mV p-p
	AGC = 7		600		mV p-p
Saturated AGC Operation	All taps are enabled with maximum gain, predriver gain = 63, AGC = 7		960		mV p-p
AGC SETTLING TIME	No external capacitor		0.5		µs
FFE					
Tap Delay			18		ps
Delay Depth			145		ps

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE CHARACTERISTICS					
Channel to Channel Isolation	Up to 32 GHz		30		dB
Total Harmonic Distortion	AGC = 2, for differential input voltage ≤ 250 mV p-p			5	%
Output Driver Rise/Fall Time	20% to 80%		16		ps
Additive RMS Jitter[1]	Input signal: 28 Gbps, 1010 pattern; all taps enabled, Tap 4 gain = 63, gain of all other taps = 0, predriver gain = 63; AGC = 2			0.4	ps
LATENCY				170	ps
DIFFERENTIAL RETURN LOSS	Up to 20 GHz				
Input		−9			dB
Output		−8			dB
NUMBER OF TAPS			9		

[1] Additive rms jitter is calculated by $J_{RMS,DUT} = \sqrt{((J_{TESTED})^2 - (J_{SOURCE})^2)}$.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VCC to GND	−0.6 V to +3.6 V
All Pins to GND	−0.3 V to V_{CC} + 0.3 V
Operating Ambient Temperature Range	−40°C to +95°C
Differential Peak-to-Peak Input Voltage Swing	1.6 V p-p
Maximum Input Voltage at CML Inputs	V_{CC} + 0.6 V
Maximum Input Voltage at Digital Inputs (SDA, SCL, REGSEL1, REGSEL0, $\overline{RST}$)	V_{CC} + 0.6 V
Maximum Peak Reflow Temperature	260°C
Maximum Junction Temperature	125°C
Continuous Power Dissipation (T_A = 85°C, Derate 46.59 mW/°C Above 85°C)	1.86 W
Thermal Resistance (Junction to EPAD)	21.46°C/W
ESD Sensitivity, Human Body Model (HBM)	Class 1C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

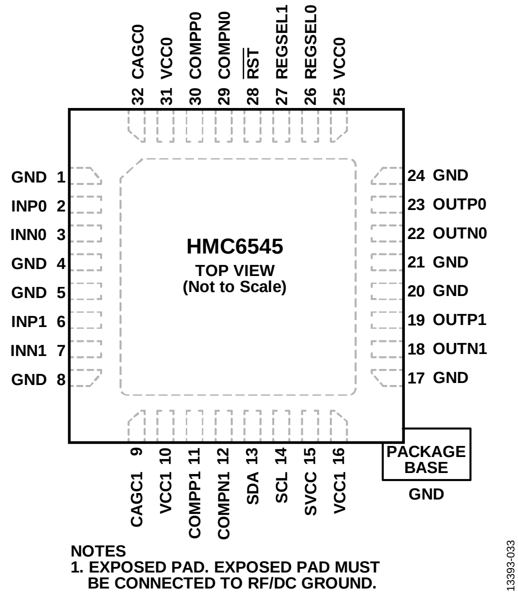


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin Number	Mnemonic	Description
1, 4, 5, 8, 17, 20, 21, 24	GND	Ground. This pin and the package base must be connected to RF and dc ground.
2, 3	INP0, INN0	Differential CML Inputs, Channel 0.
6, 7	INP1, INN1	Differential CML Inputs, Channel 1.
9, 32	CAGC1, CAGC0	External Capacitor for AGC Bandwidth.
10, 16	VCC1	Power Supplies for Channel 1.
11, 12	COMPP1, COMPN1	External Capacitors to Cancel DC Offset, Channel 1.
13	SDA	2-Wire Digital Data.
14	SCL	2-Wire Digital Clock.
15	SVCC	Power Supply for Digital Circuitry and Bias.
18, 19	OUTN1, OUTP1	Differential CML Data Outputs, Channel 1.
22, 23	OUTN0, OUTP0	Differential CML Data Outputs, Channel 0.
25, 31	VCC0	Power Supplies for Channel 0.
29, 30	COMPN0, COMPP0	External Capacitors to Cancel DC Offset, Channel 0.
26, 27	REGSEL0, REGSEL1	Default Coefficient Selection for Channel and 2-Wire Interface Device Address.
28	$\overline{\text{RST}}$	Reset for 2-Wire Interface.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

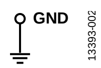


Figure 3. GND Interface Schematic

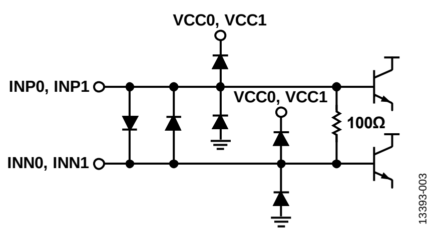


Figure 4. INPx, INNx Interface Schematic

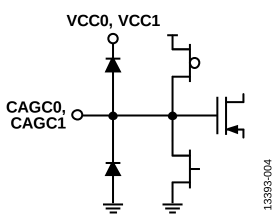


Figure 5. CAGCx Interface Schematic

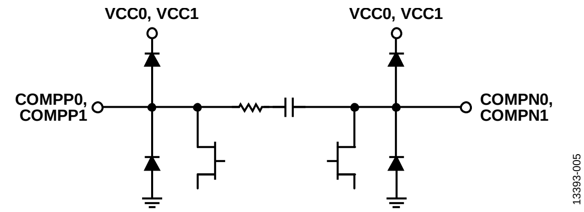


Figure 6. COMPPx, COMPNx Interface Schematic

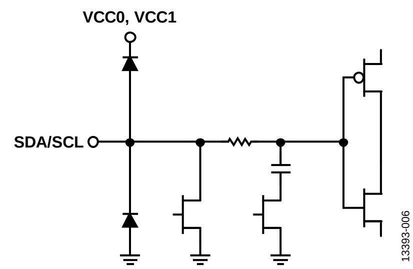


Figure 7. SDA, SCL Interface Schematic

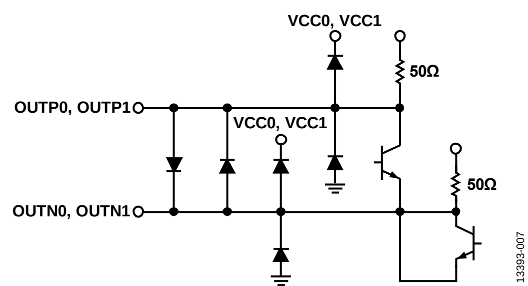


Figure 8. OUTPx, OUTNx Interface Schematic

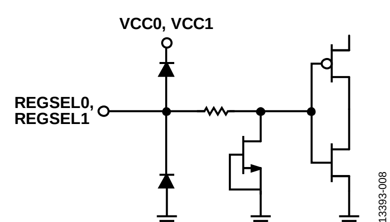


Figure 9. REGSELx Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

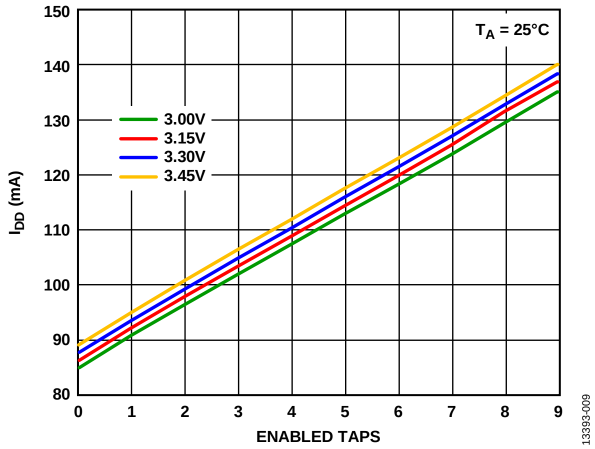


Figure 10. Supply Current (I_{DD}) vs. Enabled Taps Over Supply Voltage

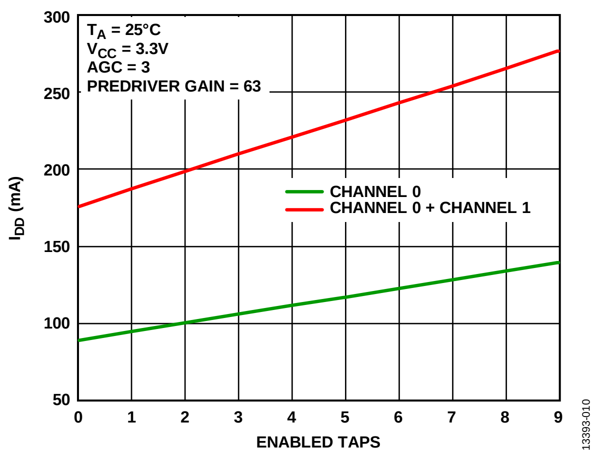


Figure 11. Supply Current (I_{DD}) vs. Enabled Taps Over Enabled Channels

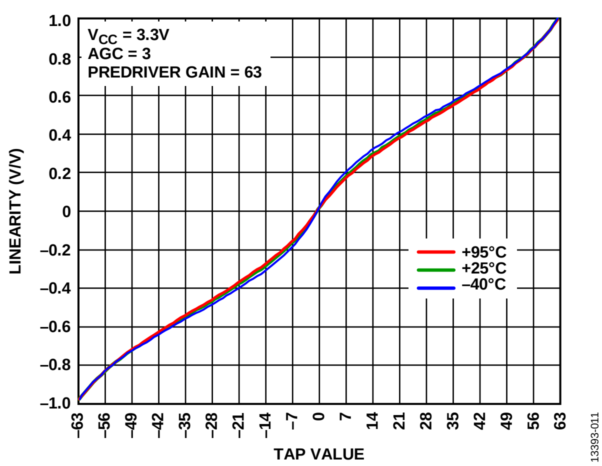


Figure 12. Normalized Linearity vs. Tap Value Over Temperature, Tap 4 Value Is Varied, While Others Are Enabled with No Gain

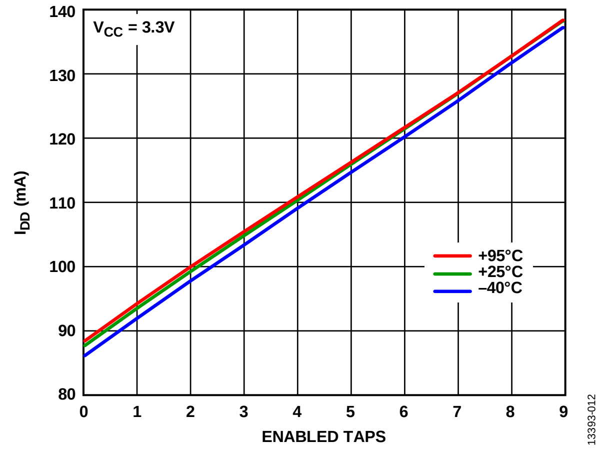


Figure 13. Supply Current vs. Enabled Taps Over Temperature

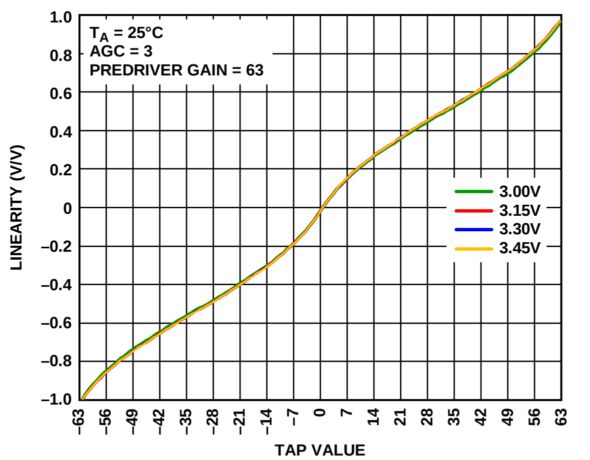


Figure 14. Normalized Linearity vs. Tap Value Over Supply Voltage, Tap 4 Value Is Varied, While Others Are Enabled with No Gain

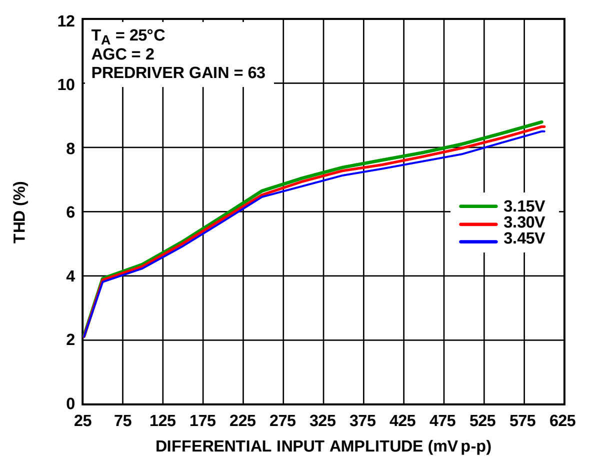


Figure 15. THD vs. Differential Input Amplitude Over Supply Voltage, Tap 4 Gain Is Set to +63, While Others are Enabled with No Gain

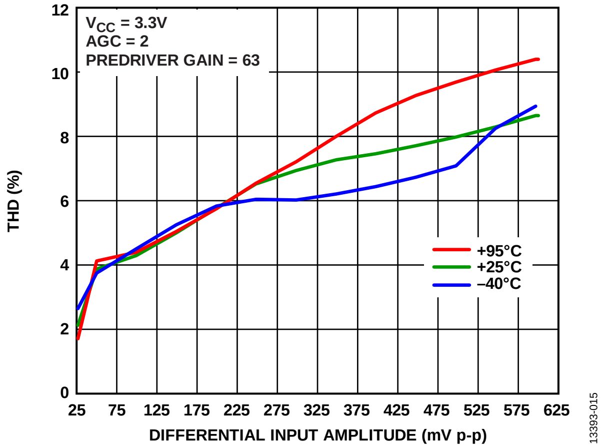


Figure 16. THD vs. Differential Input Amplitude Over Temperature, Tap 4 Gain Is Set to Maximum Gain, While Others Are Enabled with No Gain

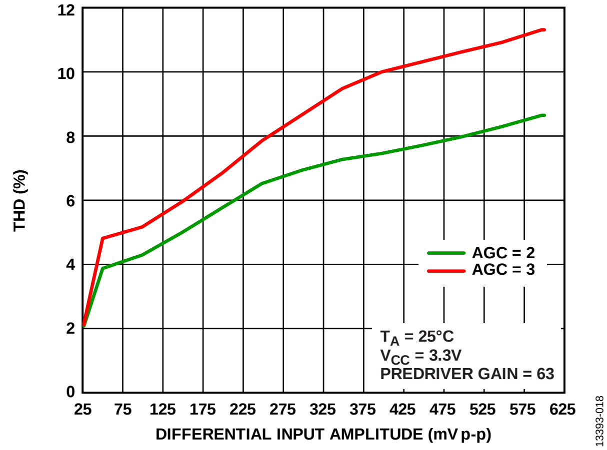


Figure 19. THD vs. Differential Input Amplitude Over AGC Value, Tap 4 Gain Is Set to Maximum Gain, While Others Are Enabled with No Gain

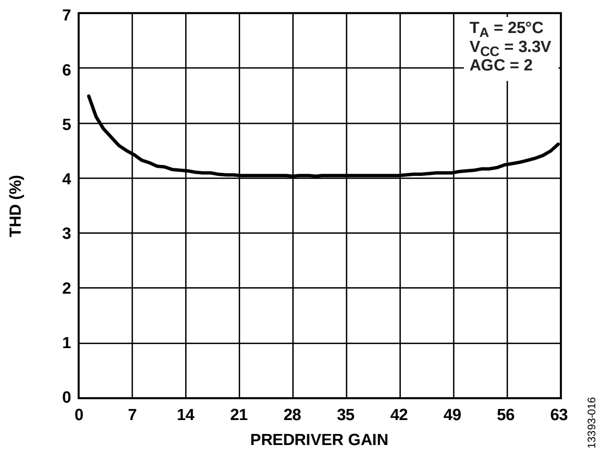


Figure 17. THD vs. Predriver Gain, Tap 4 Gain Is Set to Maximum Gain, While Others Are Enabled with No Gain

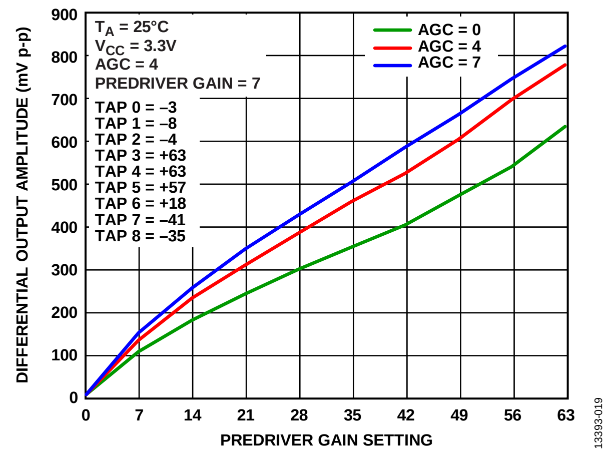


Figure 20. Differential Output Amplitude vs. Predriver Gain Over AGC, Input Signal: Differential PRBS $2^{31} - 1$, 10 Gbps at 500 mV p-p

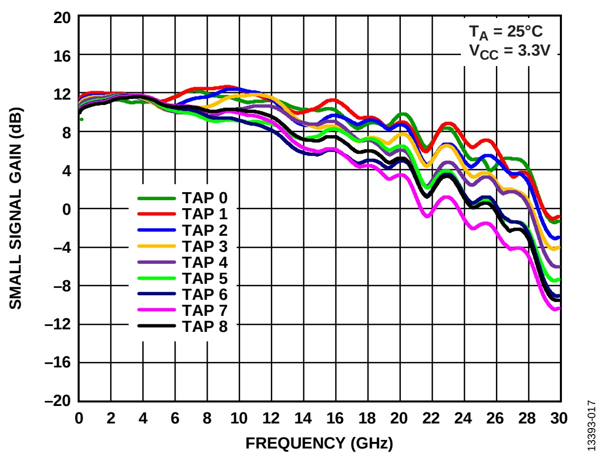


Figure 18. Small Signal Gain Over Taps, for S21 Line of Each Tap, Relevant Tap Is Set to Maximum Gain While Remaining Taps Are Enabled with No Gain

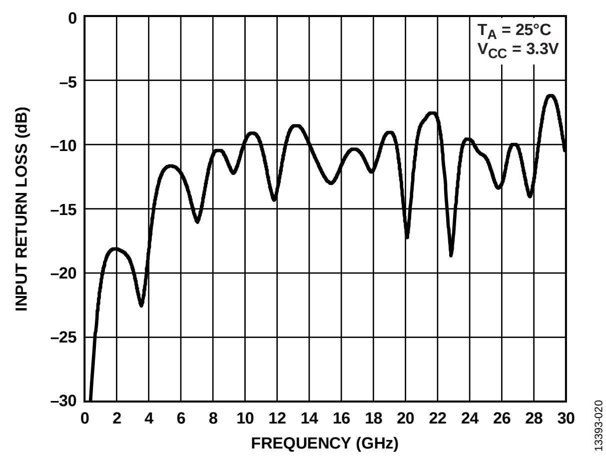


Figure 21. Input Return Loss

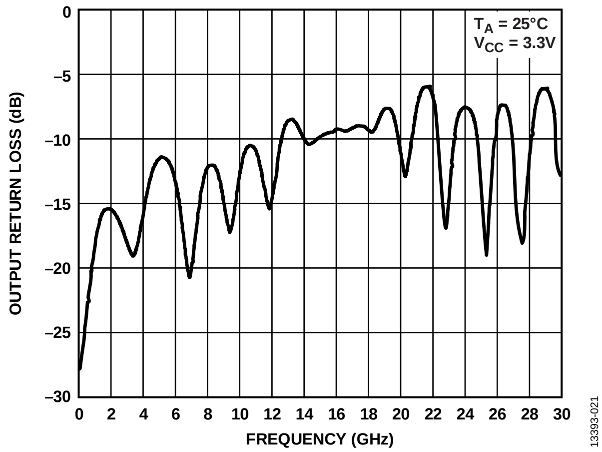


Figure 22. Output Return Loss

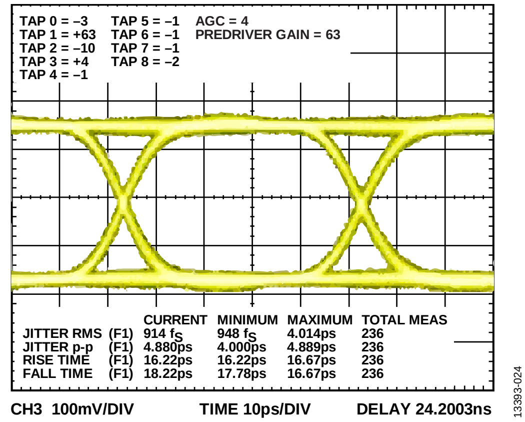


Figure 25. Typical Output Waveform at 10 Gbps PRBS 2^{31} – 1 Input Data

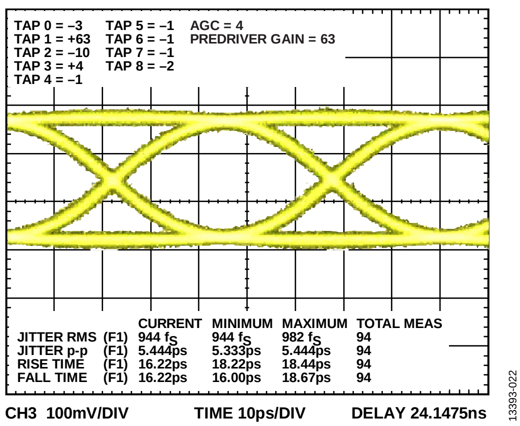


Figure 23. Typical Output Waveform at 22 Gbps, PRBS 2^{31} – 1 Input Data, Input Signal = 300 mV p-p Differential

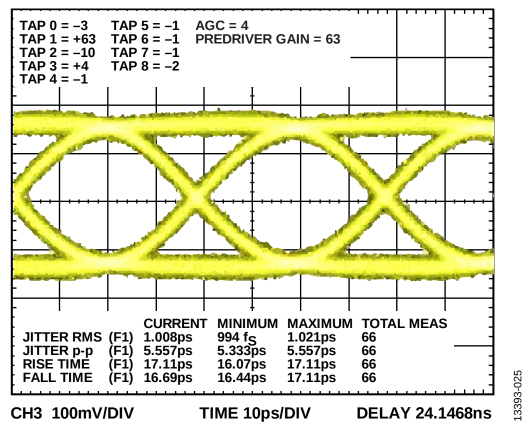


Figure 26. Typical Output Waveform at 25.8 Gbps, PRBS 2^{31} – 1 Input Data

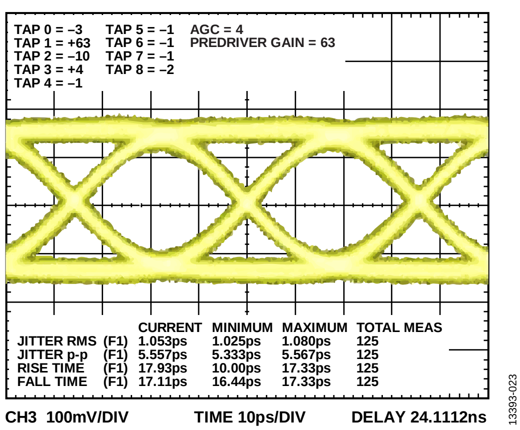


Figure 24. Typical Output Waveform t 28 Gbps, PRBS 2^{31} – 1 Input Data

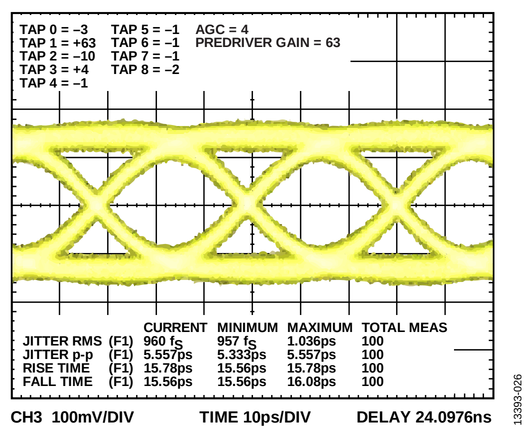


Figure 27. Typical Output Waveform at 32 Gbps, PRBS 2^{31} – 1 Input Data

THEORY OF OPERATION

The HMC6545 advanced linear equalizer has two symmetrical channels, each containing an input AGC, a 9-tap delay chain with each delay tap connected to a variable tap amplifier, a summation node combining the outputs of the tap amplifiers, and an output driver.

INPUT RECEIVER

AGC

The HMC6545 has an integrated AGC that linearly amplifies/ attenuates the input signal, generating a fixed voltage swing level for further processing in the FFE delay line. An input AGC is required both to supply a well defined voltage swing level to the FFE delay line and to control the internal and external (output) voltage swings because the signal path is linear. The AGC has a sensitivity level of 40 mV p-p differential. The HMC6545 processes the input signal linearly at up to a 600 mV p-p differential input voltage level.

The AGC loop bandwidth and settling time can be changed using an external capacitor connected to the CAGC0/GND and CAGC1/GND nodes. An internal 2.5 pF capacitor at these nodes sets the default AGC settling time to 0.5 µs. The evaluation board includes 1 nF capacitors for both channels.

Internal and External Offset Correction Circuitry

The input receiver has two modes of offset correction that can be configured by changing the offset settings register via the 2-wire interface: automatic offset correction and manual offset correction (all registers in Table 5 are identical to each other).

Table 5. Offset Settings Registers

Register	Description
Register 0x0A	Channel 0 Offset Settings, Array A register
Register 0x2A	Channel 0 Offset Settings, Array B register
Register 0x4A	Channel 1 Offset Settings, Array A register
Register 0x6A	Channel 1 Offset Settings, Array B register

By default, the input receiver is configured in the automatic offset correction mode, which can correct up to ±60 mV of input referred dc offset at the worst case AGC gain (maximum AGC gain with a minimum input signal level). The input referred automatic offset correction range changes depending on the AGC gain and increases up to ±180 mV for minimum AGC gain with a maximum signal level at the input of the receiver.

Automatic offset correction loop bandwidth is externally set by a series RC network (for each channel, R1/C1 and R2/C2), and it is recommended to keep the component values as shown in the evaluation board schematic (see Figure 35).

For Channel 1, Array A, automatic offset correction loop can be disabled by setting Register 0x4A, Bit 6 to 0, which enables the manual offset correction (set Register 0x0A for Channel 0, Array A; Register 0x2A for Channel 0, Array B; and Register 0x6A for Channel 1, Array B; see Table 5). Manual offset correction amount can be adjusted by configuring Register 0x4A, Bits[5:0], where Register 0x4A, Bit 5 defines the sign and Bits[4:0] define the magnitude of gain (see Table 48). Similar to automatic offset correction mode, manual offset correction dynamic range changes with the AGC gain with the total correction being ±60 mV for maximum AGC gain, which corresponds to about 2 mV/step (5-bit control) adjustment resolution for maximum AGC gain. For minimum AGC gain, the correction dynamic range increases to ±180 mV, and the minimum step for adjustment increases to 6 mV/step.

FFE DELAY LINE

The FFE delay line receives an input signal from the AGC (with a controlled magnitude), and this signal propagates along a delay line composed of eight delay elements, where each delay element has 18 ps nominal propagation. The delayed signals are then multiplied by programmable coefficients by the tap amplifiers and summed together. One of the taps near the center can be selected as the main tap. The taps that follow are called postcursor taps, and the taps that precede are called precursor taps.

By combining different tap values, a wide variety of filter transfer functions can be created that can, for example, compensate for the gain or phase distortion of a lossy channel or the chromatic dispersion of an optical channel.

Tap amplifier gains are controlled using the 2-wire interface with five bits of magnitude resolution with positive or negative polarity. To disable a coefficient, set the gain of the particular tap amplifier to 0 (positive gain sign, and 0 gain setting). In addition, the tap amplifier can be powered down to save power, but this may have an impact on the delay and gain of the remaining taps in the delay chain. See Table 14 to Table 22 and Table 38 to Table 46 for Array A tap amplifier settings for Channel 0 and Channel 1, respectively. For Array B tap amplifier settings, see Table 26 to Table 34 and Table 50 to Table 58 for Channel 0 and Channel 1, respectively.

Each channel has two sets of tap coefficient register arrays (Channel 0, Array A; Channel 0, Array B; Channel 1, Array A; and Channel 1, Array B) that can be configured through the 2-wire interface. Register 0x00 to Register 0x08 set the tap coefficients of Channel 0, Array A. Register 0x20 to Register 0x28 set the tap coefficients of Channel 0, Array B. Register 0x40 to Register 0x48 set the tap coefficients of Channel 1, Array A. Register 0x60 to Register 0x68 set the tap coefficients of Channel 1, Array B. The REGSEL0 and REGSEL1 pins of the device set the default register array (A or B), determining the tap coefficients of a particular channel. For example, applying REGSEL0 = 0 activates Channel 0, Array A; and REGSEL1 = 0 activates Channel 1, Array A. Applying REGSEL0 = 1 activates Channel 0, Array B; and REGSEL1 = 1 activates Channel 1, Array B.

OUTPUT DRIVER

After the tap amplifier outputs are summed, the combined signal is received by a linear output driver. The output driver consists of two stages. The first stage is a predriver stage providing controllable signal amplification (6-bit resolution) using Register 0x09 (Channel 0, Array A), Register 0x29 (Channel 0, Array B), Register 0x49 (Channel 1, Array A), and Register 0x69 (Channel 1, Array B). Similar to the tap coefficient registers, each predriver has two registers that can be selected asynchronously by the REGSEL0 and REGSEL1 pins. The register values must be configured through the 2-wire interface prior to the register selection via the REGSEL0 and REGSEL1 pins.

See Table 7 to Table 10 for the predriver settings for Channel 0 and Channel 1.

The final stage of the output driver is a 50 Ω CML driver stage that provides the specified linearity (according to the THD specification) up to 600 mV p-p differential output swing. The linearity degrades at higher output swings.

2-WIRE SERIAL PORT

To access all of its internal registers, the HMC6545 uses a 2-wire interface, which consists of a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are implemented with open-drain input/output pins and are connected to a positive supply voltage via pull-up resistors.

Typically, a microcontroller, a microprocessor or a digital signal processor acts as a master, controls the bus, and has the responsibility to generate the clock signal and device addresses.

The HMC6545 functions as a slave device. The device address on the HMC6545 is 0x38 (default) and set by connecting the REGSEL0 and REGSEL1 pins to either V_{CC} (Logic 1) or GND (Logic 0) and by writing 1 to Register 0x80, Bit 6. If Register 0x80, Bit 6 = 0 (default), the REGSEL0 and REGSEL1 pins select Array A or Array B. If Register 0x80, Bit 6 = 1, the REGSEL0 and REGSEL1 pins also determine the 2-wire interface device address according to Table 6.

Table 6. 2-Wire Interface Device Address Setting

REGSEL1	REGSEL0	Address Setting (Register 0x80, Bit 6 = 1)
0	0	0x38 (default)
0	1	0x39
1	0	0x3A
1	1	0x3B

Table 7. Register 0x09—Channel 0 Predriver Settings, Array A Register

Bits	Type	Name	Default	Minimum	Maximum	Description
[5:0]	R/W	Predriver gain	0x30	000000	111111	Channel 0 predriver gain
[7:6]	R/W	Factory set	0b00			Not used

Table 8. Register 0x29—Channel 0 Predriver Settings, Array B Register

Bits	Type	Name	Default	Minimum	Maximum	Description
[5:0]	R/W	Predriver gain	0x3F	000000	111111	Channel 0 predriver gain
[7:6]	R/W	Factory set	0b00			Not used

Table 9. Register 0x49—Channel 1 Predriver Settings, Array A Register

Bits	Type	Name	Default	Minimum	Maximum	Description
[5:0]	R/W	Predriver gain	0x30	000000	111111	Channel 1 predriver gain
[7:6]	R/W	Factory set	0b00			Not used

Table 10. Register 0x69—Channel 1 Predriver Settings, Array B Register

Bits	Type	Name	Default	Minimum	Maximum	Description
[5:0]	R/W	Predriver gain	0x3F	000000	111111	Channel 1 predriver gain
[7:6]	R/W	Factory set	0b00			Not used

Protocol

Table 11 lists the definitions and conditions occurring in a 2-wire data transfer.

Figure 28 shows a representation of a complete communication cycle on the 2-wire interface.

The master generates a start condition to indicate the beginning of a new data transfer.

The master then starts generating clock pulses on SCL and transmits the first byte on SDA. This first byte always consists of a 7-bit slave address followed by one bit that indicates the read/write direction ($R/\overline{W}$). The device on the bus with a matching address generates an acknowledge.

The master continues generating more clock pulses on SCL and, depending on the value of the R/W bit, sends (write operation, $R/\overline{W}$ = 0) or receives (read operation, $R/\overline{W}$ = 1) data on SDA. In each case, the receiver must acknowledge the data sent by the transmitter. This sequence of 8-bit data followed by a 1-bit acknowledge can be repeated multiple times.

When all data communication is over for the current transfer cycle, the master indicates the end of data transfer by generating a stop condition.

Data Transfer Formats

Write Cycle

In a write cycle, the master transmitter sends data to the slave receiver. The transfer direction is from master to slave and does not change (see Figure 29). The master generates a start condition followed by a 7-bit slave address and by the $R/\overline{W}$ bit set to 0. The slave with a matching address replies with an acknowledge. The master then transmits the first byte to the slave device. This first byte is an address of the internal registers of the slave. The slave device replies with an acknowledge bit. For a subsequent read cycle, the master generates a stop bit; otherwise, the master then transmits the next byte, which is a data byte to be stored in the internal slave register previously addressed. This data byte is followed by an acknowledge bit from the slave. This process can continue for multiple bytes, and the slave device increments its internal register address count as it receives subsequent bytes from the master. When all data transfer is over, the master generates a stop condition to end the cycle.

Table 11. 2-Wire Data Transfer Terminology and Definitions

Term	Definition
Start	A start condition is always generated by the master and is defined as a high to low transition on the SDA line while SCL is high. The bus becomes busy after a start condition.
Stop	A stop condition is always generated by the master and is defined as a low to high transition on the SDA line while SCL is high. The bus becomes free after the stop condition occurs.
Byte Format	Every byte transmitted on SDA must be eight bits long and is transferred with the most significant bit (MSB) first. Each byte must be followed by an acknowledge bit.
Data Valid Condition	For data to be considered valid, the SDA line must be stable during the entire high period of its respective clock pulse.
Acknowledge	For each byte sent or received on the bus, the master generates an extra clock cycle that is used for acknowledgement, for a total of nine bits. The transmitter releases the SDA line, which is pulled high by the external resistor, and the receiver must pull down the SDA line and drive it low while SCL is high during this entire clock cycle to indicate acknowledgment. SDA is left high during this clock cycle to indicate a no acknowledge (NACK) situation, usually because the device addressed is unable to receive or transmit the data requested.

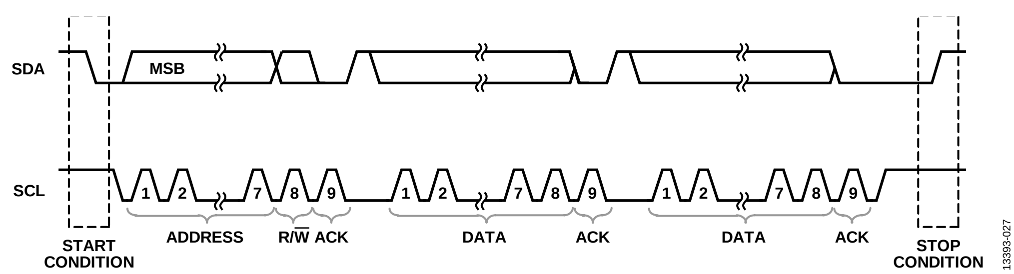


Figure 28. Complete Data Transfer

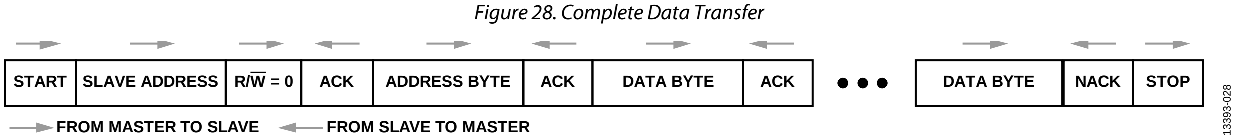


Figure 29. Write Cycle

Read Cycle

In a read cycle, the master reads from the slave immediately after the first byte. The direction of data transfer changes between master and slave (see Figure 32). In this case, the R/$\overline{W}$ bit is set to 1 to indicate that the master reads data from the slave device. The address of the internal register from which the data is to come has been previously set in a precedent write cycle; otherwise, the slave device defaults to Address 0x00. This time, the slave device transmits all the data bytes and the master replies with an acknowledge bit. For the last byte read, the master replies with a no acknowledge bit to indicate to the slave that it must stop transmitting data. The master then generates a stop condition, and the cycle ends.

2-Wire Interface Design Considerations

The HMC6545 2-wire interface slave interface responds to any register address or data matching its chip address even when there is no preceding start condition. A 2-wire interface communication is defined as shown in Figure 30.

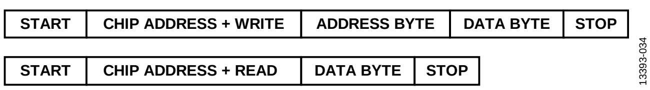


Figure 30. 2-Wire Interface Communication

Coincidentally, the data or register address can be the same as the chip address of another device on the same bus. However, that other device does not respond because there is no preceding start condition.

In the HMC6545, regardless of whether there is a start condition, if the HMC6545 sees a bit stream that corresponds to its chip address, it then responds and causes unwanted results.

There must be only one HMC6545 device on the 2-wire interface bus; otherwise, 2-wire interface bus multiplexers can be used to isolate the HMC6545 devices. See Figure 33 for an example design.

Reset

A low strobe signal must be sent to the $\overline{RST}$ pin to reset the registers to their default values. SDA and SCL must be high in the 2-wire interface bus before and after the rising edge.

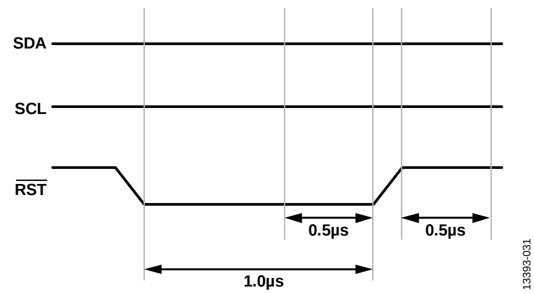


Figure 31. Reset Registers

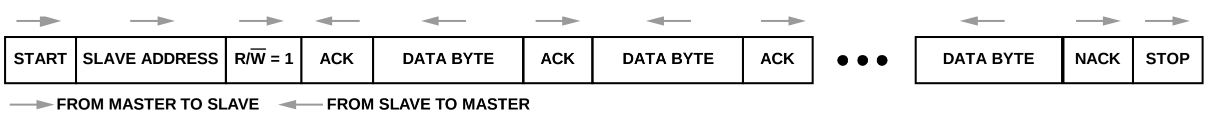


Figure 32. Read Cycle

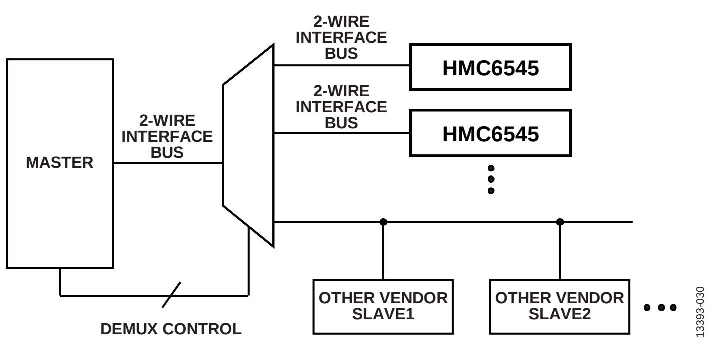


Figure 33. Multiple HMC6545 Devices on 2-Wire Interface Bus

REGISTER MAP

REGISTER LIST SUMMARY AND REGISTER DESCRIPTIONS

Global Register

Global register bit order is different for read and write operations.

Table 12. Register 0x80—Global Register, Write Operation

Bit	Type	Name	Default	Description
7	W	Factory set	0	Not used.
6	W	2-wire interface device address read	0	2-wire interface device address set. Writing 1 generates a 2-wire interface device address read command.
5	W	Channel 1 enable	1	Channel 1 enable. Writing 1 enables Channel 1.
4	W	Channel 0 enable	1	Channel 0 enable. Writing 1 enables Channel 0.
3	W	Factory set	1	Not used.
2	W	Channel 1 reset	1	Channel 1 soft reset. Writing 0 generates a soft reset, resetting all the registers in Channel 1 to their default states. Writing 1 resumes normal chip operation.
1	W	Channel 0 reset	1	Channel 0 soft reset. Writing 0 generates a soft reset, resetting all the registers in Channel 0 to their default states. Writing 1 resumes normal chip operation.
0	W	Global reset	1	Global soft reset. Writing 0 generates a soft reset, resetting all the registers to their default states. Writing 1 resumes normal chip operation.

Table 13. Register 0x80—Global Register, Read Operation

Bit	Type	Name	Default	Description
7	R	2-wire interface device address, Bit 1	0	Bit 1 of device address
6	R	2-wire interface device address, Bit 0	0	Least significant bit of device address
5	R	Factory set	Not applicable	Not used
4	R	Channel 1 enable	1	Channel 1 enable
3	R	Channel 0 enable	1	Channel 0 enable
2	R	Factory set	Not applicable	Not used
1	R	Channel 1 reset	1	Channel 1 reset
0	R	Factory set	0	Not used

Channel 0, Array A Register Set

Table 14. Register 0x00—Channel 0, Tap 0 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 0 enable	1	Channel 0 Tap 0 enable.
6	R/W	Tap 0 gain sign	1	Channel 0 Tap 0 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 0 gain	0x00	Channel 0 Tap 0 gain.

Table 15. Register 0x01—Channel 0, Tap 1 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 1 enable	1	Channel 0 Tap 1 enable.
6	R/W	Tap 1 gain sign	1	Channel 0 Tap 1 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 1 gain	0x00	Channel 0 Tap 1 gain.

Table 16. Register 0x02—Channel 0, Tap 2 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 2 enable	1	Channel 0 Tap 2 enable.
6	R/W	Tap 2 gain sign	1	Channel 0 Tap 2 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 2 gain	0x00	Channel 0 Tap 2 gain.

Table 17. Register 0x03—Channel 0, Tap 3 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 3 enable	1	Channel 0 Tap 3 enable.
6	R/W	Tap 3 gain sign	1	Channel 0 Tap 3 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 3 gain	0x00	Channel 0 Tap 3 gain.

Table 18. Register 0x04—Channel 0, Tap 4 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 4 enable	1	Channel 0 Tap 4 enable.
6	R/W	Tap 4 gain sign	1	Channel 0 Tap 4 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 4 gain	0x3F	Channel 0 Tap 4 gain.

Table 19. Register 0x05—Channel 0, Tap 5 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 5 enable	1	Channel 0 Tap 5 enable.
6	R/W	Tap 5 gain sign	1	Channel 0 Tap 5 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 5 gain	0x00	Channel 0 Tap 5 gain.

Table 20. Register 0x06—Channel 0, Tap 6 Settings, Array A Register

Bit	Type	Name	Default	Description
[5:0]	R/W	Tap 6 gain	0x00	Channel 0 Tap 6 gain.
6	R/W	Tap 6 gain sign	1	Channel 0 Tap 6 gain sign. 1 means positive, 0 means negative.
7	R/W	Tap 6 enable	1	Channel 0 Tap 6 enable.

Table 21. Register 0x07—Channel 0, Tap 7 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 7 enable	1	Channel 0 Tap 7 enable.
6	R/W	Tap 7 gain sign	1	Channel 0 Tap 7 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 7 gain	0x00	Channel 0 Tap 7 gain.

Table 22. Register 0x08—Channel 0, Tap 8 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 8 enable	1	Channel 0 Tap 8 enable.
6	R/W	Tap 8 gain sign	1	Channel 0 Tap 8 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 8 gain	0x00	Channel 0 Tap 8 gain.

Table 23. Register 0x09—Channel 0 Predriver Settings, Array A Register

Bit	Type	Name	Default	Description
[7:6]	R/W	Factory set	0b00	Not used
[5:0]	R/W	Predriver gain	0x30	Channel 0 predriver gain

Table 24. Register 0x0A—Channel 0 Offset Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Factory set	0	Not used
6	R/W	Automatic offset enable	1	Channel 0 automatic offset enable
5	R/W	Manual offset sign	0	Channel 0 manual offset sign
[4:0]	R/W	Manual offset gain	0x00	Channel 0 manual offset gain

Table 25. Register 0x0B—Channel 0 Internal AGC Amplitude, Array A Register

Bit	Type	Name	Default	Description
[7:3]	R/W	Factory set	0x00	Not used
[2:0]	R/W	Internal AGC amplitude	0b100	Internal AGC amplitude

Channel 0, Array B Register Set

Table 26. Register 0x20—Channel 0, Tap 0 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 0 enable	1	Channel 0 Tap 0 enable.
6	R/W	Tap 0 gain sign	1	Channel 0 Tap 0 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 0 gain	0x00	Channel 0 Tap 0 gain.

Table 27. Register 0x21—Channel 0, Tap 1 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 1 enable	1	Channel 0 Tap 1 enable.
6	R/W	Tap 1 gain sign	0	Channel 0 Tap 1 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 1 gain	0x04	Channel 0 Tap 1 gain.

Table 28. Register 0x22—Channel 0, Tap 2 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 2 enable	1	Channel 0 Tap 2 enable.
6	R/W	Tap 2 gain sign	1	Channel 0 Tap 2 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 2 gain	0x3F	Channel 0 Tap 2 gain.

Table 29. Register 0x23—Channel 0, Tap 3 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 3 enable	1	Channel 0 Tap 3 enable.
6	R/W	Tap 3 gain sign	0	Channel 0 Tap 3 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 3 gain	0x28	Channel 0 Tap 3 gain.

Table 30. Register 0x24—Channel 0, Tap 4 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 4 enable	1	Channel 0 Tap 4 enable.
6	R/W	Tap 4 gain sign	0	Channel 0 Tap 4 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 4 gain	0x04	Channel 0 Tap 4 gain.

Table 31. Register 0x25—Channel 0, Tap 5 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 5 enable	1	Channel 0 Tap 5 enable.
6	R/W	Tap 5 gain sign	1	Channel 0 Tap 5 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 5 gain	0x00	Channel 0 Tap 5 gain.

Table 32. Register 0x26, Channel 0, Tap 6 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 6 enable	1	Channel 0 Tap 6 enable.
6	R/W	Tap 6 gain sign	1	Channel 0 Tap 6 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 6 gain	0x00	Channel 0 Tap 6 gain.

Table 33. Register 0x27—Channel 0, Tap 7 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 7 enable	1	Channel 0 Tap 7 enable.
6	R/W	Tap 7 gain sign	1	Channel 0 Tap 7 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 7 gain	0x00	Channel 0 Tap 7 gain.

Table 34. Register 0x28—Channel 0, Tap 8 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 8 enable	1	Channel 0 Tap 8 enable.
6	R/W	Tap 8 gain sign	1	Channel 0 Tap 8 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 8 gain	0x00	Channel 0 Tap 8 gain.

Table 35. Register 0x29—Channel 0 Predriver Settings, Array B Register

Bit	Type	Name	Default	Description
[7:6]	R/W	Factory set	0b00	Not used
[5:0]	R/W	Predriver gain	0x3F	Channel 0 predriver gain

Table 36. Register 0x2A—Channel 0 Offset Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Factory set	0	Not used
6	R/W	Automatic offset enable	1	Channel 0 automatic offset enable
5	R/W	Manual offset sign	0	Channel 0 manual offset sign
[4:0]	R/W	Manual offset gain	0x00	Channel 0 manual offset gain

Table 37. Register 0x2B—Channel 0 Internal AGC Amplitude, Array B Register

Bit	Type	Name	Default	Description
[7:3]	R/W	Factory set	0x00	Not used
[2:0]	R/W	Internal AGC amplitude	0b100	Internal AGC amplitude

Channel 1, Array A Register Set

Table 38. Register 0x40—Channel 1, Tap 0 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 0 enable	1	Channel 1 Tap 0 enable.
6	R/W	Tap 0 gain sign	1	Channel 1 Tap 0 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 0 gain	0x00	Channel 1 Tap 0 gain.

Table 39. Register 0x41—Channel 1, Tap 1 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 1 enable	1	Channel 1 Tap 1 enable.
6	R/W	Tap 1 gain sign	1	Channel 1 Tap 1 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 1 gain	0x00	Channel 1 Tap 1 gain.

Table 40. Register 0x42—Channel 1, Tap 2 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 2 enable	1	Channel 1 Tap 2 enable.
6	R/W	Tap 2 gain sign	1	Channel 1 Tap 2 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 2 gain	0x00	Channel 1 Tap 2 gain.

Table 41. Register 0x43—Channel 1, Tap 3 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 3 enable	1	Channel 1 Tap 3 enable.
6	R/W	Tap 3 gain sign	1	Channel 1 Tap 3 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 3 gain	0x00	Channel 1 Tap 3 gain.

Table 42. Register 0x44—Channel 1, Tap 4 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 4 enable	1	Channel 1 Tap 4 enable.
6	R/W	Tap 4 gain sign	1	Channel 1 Tap 4 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 4 gain	0x1F	Channel 1 Tap 4 gain.

Table 43. Register 0x45—Channel 1, Tap 5 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 5 enable	1	Channel 1 Tap 5 enable.
6	R/W	Tap 5 gain sign	1	Channel 1 Tap 5 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 5 gain	0x00	Channel 1 Tap 5 gain.

Table 44. Register 0x46—Channel 1, Tap 6 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 6 enable	1	Channel 1 Tap 6 enable.
6	R/W	Tap 6 gain sign	1	Channel 1 Tap 6 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 6 gain	0x00	Channel 1 Tap 6 gain.

Table 45. Register 0x47—Channel 1, Tap 7 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 7 enable	1	Channel 1 Tap 7 enable.
6	R/W	Tap 7 gain sign	1	Channel 1 Tap 7 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 7 gain	0x00	Channel 1 Tap 7 gain.

Table 46. Register 0x48—Channel 1, Tap 8 Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Tap 8 enable	1	Channel 1 Tap 8 enable.
6	R/W	Tap 8 gain sign	1	Channel 1 Tap 8 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 8 gain	0x00	Channel 1 Tap 8 gain.

Table 47. Register 0x49—Channel 1 Predriver Settings, Array A Register

Bit	Type	Name	Default	Description
[7:6]	R/W	Factory set	0b00	Not used
[5:0]	R/W	Predriver gain	0x30	Channel 1 predriver gain

Table 48. Register 0x4A—Channel 1 Offset Settings, Array A Register

Bit	Type	Name	Default	Description
7	R/W	Factory set	0	Not used
6	R/W	Automatic offset enable	1	Channel 0 automatic offset enable
5	R/W	Manual offset sign	0	Channel 0 manual offset sign
[4:0]	R/W	Manual offset gain	0x00	Channel 0 manual offset gain

Table 49. Register 0x4B—Channel 1 Internal AGC Amplitude, Array A Register

Bit	Type	Name	Default	Description
[7:3]	R/W	Factory set	0x00	Not used
[2:0]	R/W	Internal AGC amplitude	0b100	Internal AGC amplitude

Channel 1, Array B Register Set

Table 50. Register 0x60—Channel 1, Tap 0 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 0 enable	1	Channel 1 Tap 0 enable.
6	R/W	Tap 0 gain sign	1	Channel 1 Tap 0 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 0 gain	0x00	Channel 1 Tap 0 gain.

Table 51. Register 0x61—Channel 1, Tap 1 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 1 enable	1	Channel 1 Tap 1 enable.
6	R/W	Tap 1 gain sign	0	Channel 1 Tap 1 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 1 gain	0x04	Channel 1 Tap 1 gain.

Table 52. Register 0x62—Channel 1, Tap 2 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 2 enable	1	Channel 1 Tap 2 enable.
6	R/W	Tap 2 gain sign	1	Channel 1 Tap 2 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 2 gain	0x3F	Channel 1 Tap 2 gain.

Table 53. Register 0x63—Channel 1, Tap 3 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 3 enable	1	Channel 1 Tap 3 enable.
6	R/W	Tap 3 gain sign	0	Channel 1 Tap 3 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 3 gain	0x28	Channel 1 Tap 3 gain.

Table 54. Register 0x64—Channel 1, Tap 4 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 4 enable	1	Channel 1 Tap 4 enable.
6	R/W	Tap 4 gain sign	0	Channel 1 Tap 4 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 4 gain	0x04	Channel 1 Tap 4 gain.

Table 55. Register 0x65—Channel 1, Tap 5 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 5 enable	1	Channel 1 Tap 5 enable.
6	R/W	Tap 5 gain sign	1	Channel 1 Tap 5 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 5 gain	0x00	Channel 1 Tap 5 gain.

Table 56. Register 0x66—Channel 1, Tap 6 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 6 enable	1	Channel 1 Tap 6 enable.
6	R/W	Tap 6 gain sign	1	Channel 1 Tap 6 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 6 gain	0x00	Channel 1 Tap 6 gain.

Table 57. Register 0x67—Channel 1, Tap 7 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 7 enable	1	Channel 1 Tap 7 enable.
6	R/W	Tap 7 gain sign	1	Channel 1 Tap 7 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 7 gain	0x00	Channel 1 Tap 7 gain.

Table 58. Register 0x68—Channel 1, Tap 8 Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Tap 8 Enable	1	Channel 1 Tap 8 enable.
6	R/W	Tap 8 Gain Sign	1	Channel 1 Tap 8 gain sign. 1 means positive, 0 means negative.
[5:0]	R/W	Tap 8 Gain	0x00	Channel 1 Tap 8 gain.

Table 59. Register 0x69—Channel 1 Predriver Settings, Array B Register

Bit	Type	Name	Default	Description
[7:6]	R/W	Factory set	0b00	Not used
[5:0]	R/W	Predriver gain	0x3F	Channel 1 predriver gain

Table 60. Register 0x6A—Channel 1 Offset Settings, Array B Register

Bit	Type	Name	Default	Description
7	R/W	Factory set	0	Not used
6	R/W	Automatic offset enable	1	Channel 1 automatic offset enable
5	R/W	Manual offset sign	0	Channel 1 manual offset sign
[4:0]	R/W	Manual offset gain	0x00	Channel 1 manual offset gain

Table 61. Register 0x6B—Channel 1 Internal AGC Amplitude, Array B Register

Bit	Type	Name	Default	Description
[7:3]	R/W	Factory set	0x00	Not used
[2:0]	R/W	Internal AGC amplitude	0b100	Internal AGC amplitude

EVALUATION PRINTED CIRCUIT BOARD (PCB)

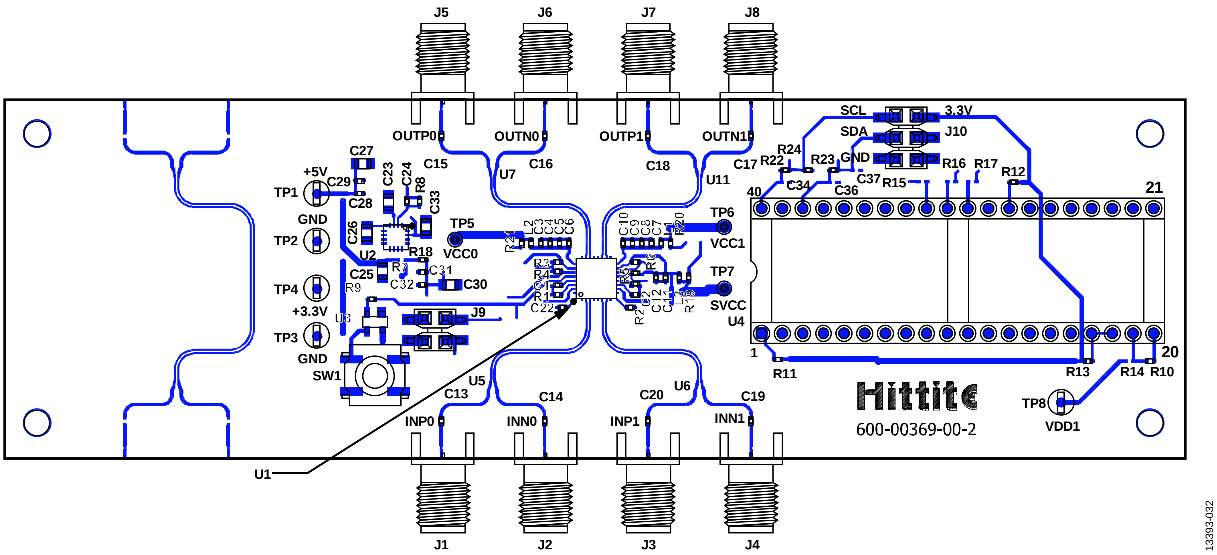


Figure 34. PCB

EVALUATION KIT CONTENTS

The HMC6545 evaluation PCB kit, EKIT01-HMC6545LP5, includes the following components:

- 6-foot USB 2.0, Type A male to Type B male cable
- User software CD-ROM

The CD-ROM contains user software, an evaluation PCB schematic, and a user manual.

To order the evaluation kit, see the Ordering Guide section.

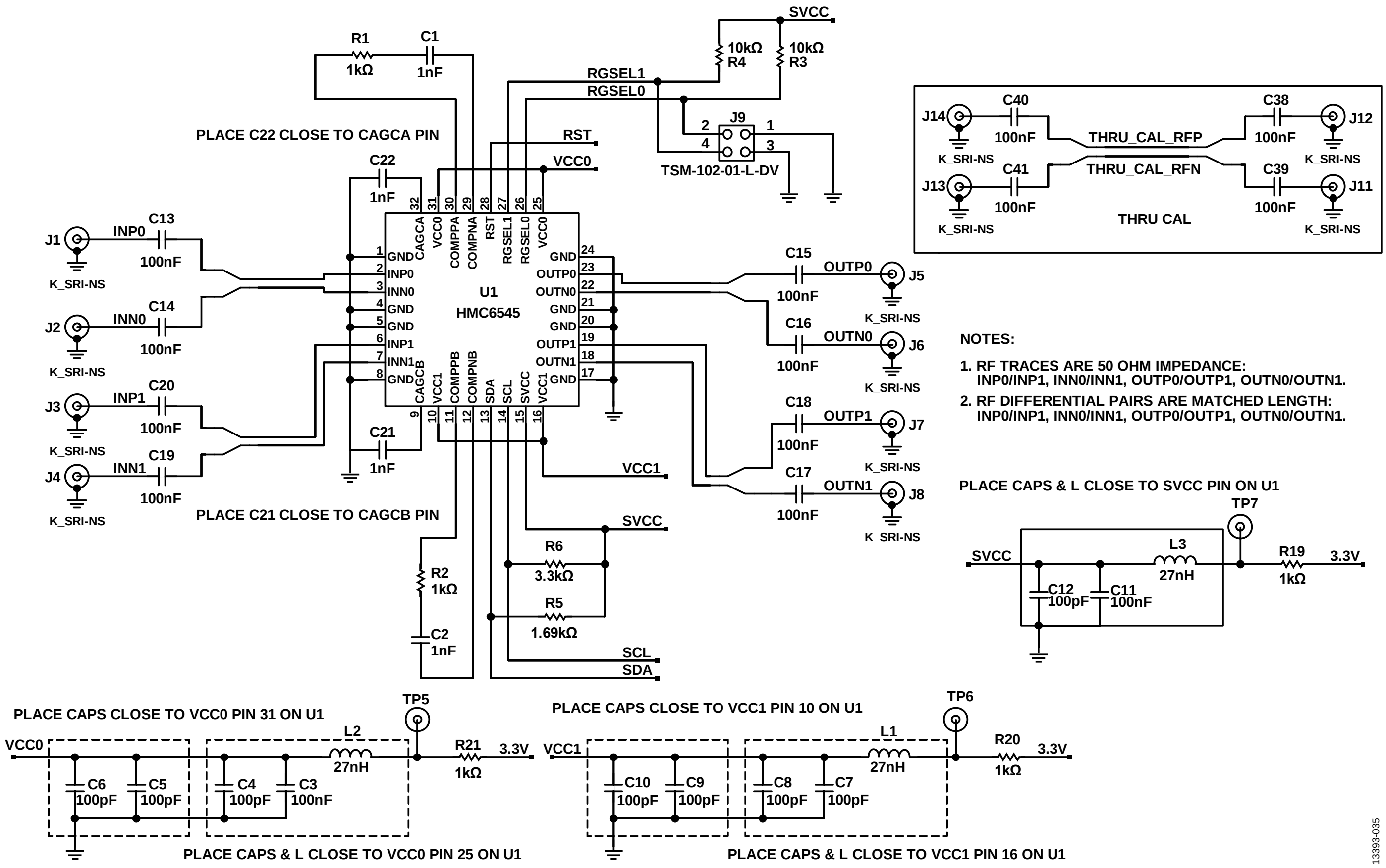
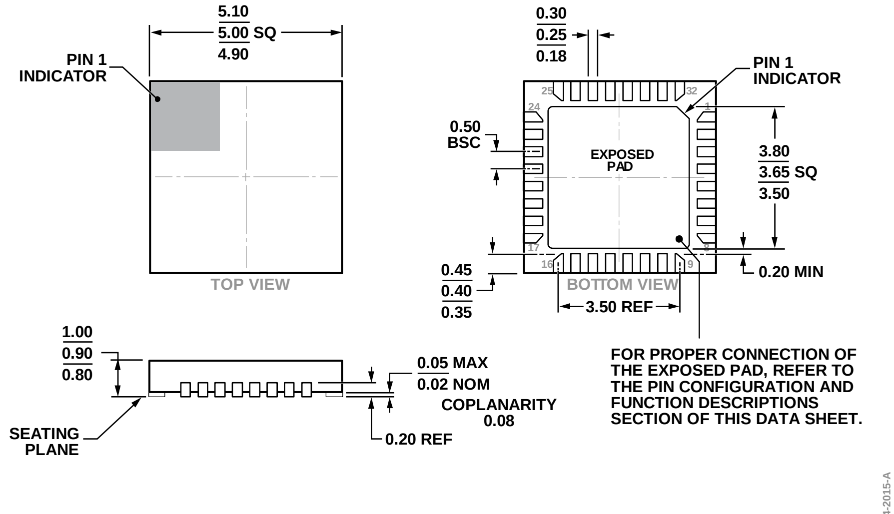


Figure 35. Evaluation Board Schematic

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-4.

Figure 36.32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.90 mm Package Height
(HCP-32-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Lead Finish	MSL Rating[1]	Package Marking[2]	Package Option
HMC6545LP5E	−40°C to +95°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	100% matte Sn	MSL1	H6545 / XXXX	HCP-32-1
HMC6545LP5ETR	−40°C to +95°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	100% matte Sn	MSL1	H6545 / XXXX	HCP-32-1
EKIT01-HMC6545LP5		Evaluation Kit				

[1] Maximum peak reflow temperature of 260°C.
[2] XXXX is the four-digit lot number.

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