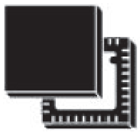
STW81200

Multi-band RF fractional/integer frequency synthesizer with integrated VCOs

Datasheet - preliminary data



VFQFPN36

Features

- Output frequency range: 46.875 to 6000 MHz
- Very Low Noise
  – Normalized in band phase noise floor: -227 dBc/Hz
  – VCO phase noise: -135 dBc/Hz @ 1 MHz offset, 4.0 GHz carrier
  – Noise floor: -160 dBc/Hz
- Dual architecture frequency synthesizer: Fractional-N and Integer-N
- Integrated VCOs with automatic center frequency calibration
- Programmable RF output dividers by 1/2/4/8/16/32/64
- Dual RF Output broadband matched with programmable power level and mute function
- External VCO option with 5 V charge pump
- Integrated low noise LDO voltage regulators
- Maximum phase detector frequency: 100 MHz
- Exact frequency mode
- Fast lock and cycle slip reduction
- Differential reference clock input (LVDS and LVECPL compliant) supporting up to 800 MHz
- 13-bit programmable reference frequency divider
- Programmable charge pump current
- Digital lock detector
- Integrated reference crystal oscillator core
- R/W SPI interface
- Logic compatibility/tolerance 1.8 V/3.3 V
- Low Power Functional mode
- Supply Voltage: 3.0 V to 5.4 V
- Small size exposed pad VFQFPN36 package
- 6 x 6 x 1.0 mm
- Process: BICMOS 0.25 µm SiGe

Applications

- Cellular/4G infrastructure equipment
- Instrumentation and test equipment
- Cable TV
- Other wireless communication systems

Table 1. Device summary

Order Code	Package	Packing
STW81200T	VFQFPN36	Tray
STW81200TR	VFQFPN36	Tape and reel

Description

The STW81200 is a dual architecture frequency synthesizer (Fractional-N and Integer- N), that features three low phase noise VCOs with a fundamental frequency range of 3.0 GHz to 6.0 GHz and a programmable dual RF output divider stage which allows to cover from 46.875 MHz to 6 GHz.

The STW81200 optimizes size and cost of the final application thanks to the integration of low noise LDO voltage regulators and internally broadband matched RF outputs.

The STW81200 is compatible with a wide range of supply voltage (from 3.0 V to 5.4 V) providing to the end user a very high level of flexibility which trades off excellent performance with power dissipation requirements. A low power functional mode (software-controlled) gives an extra power saving.

Additional features include crystal oscillator core, external VCO mode and output mute function.

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice

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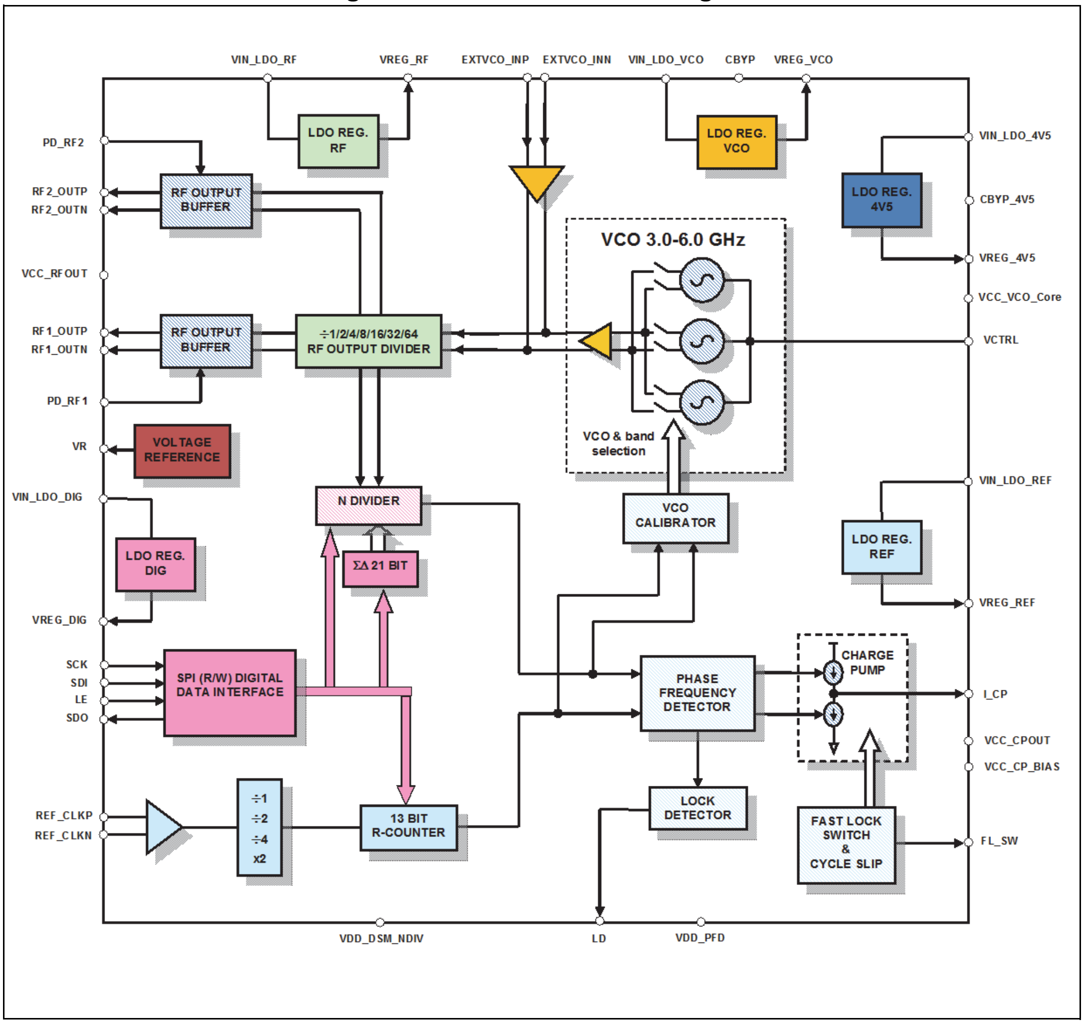
1 Functional block diagram

Figure 1. Functional block diagram



2 Pin definitions

Figure 2. Top view

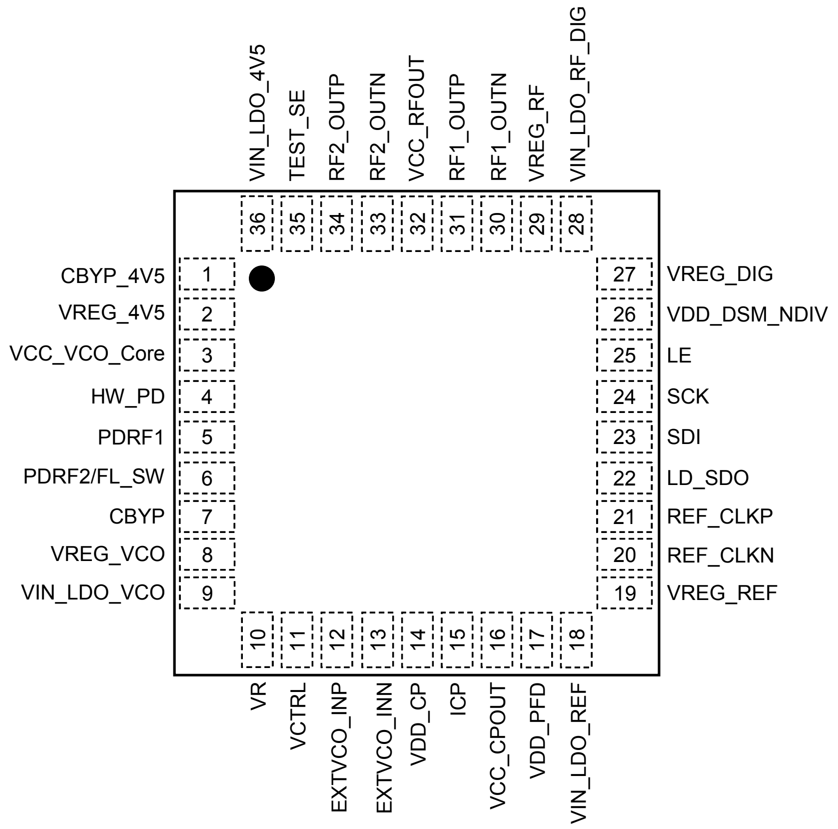


Table 2. Pin description

Pin No	Name	Description	Observation
1	CBYP_4V5	Connection for 4.5 V regulator bypass capacitor	-
2	VREG_4V5	Regulated output voltage for 4.5V regulator	Adjustable output voltage: 5.0 V, 4.5 V, 2.6 V, 3.3 V
3	VCC_VCO_Core	Supply voltage for VCO Core	It must be connected to VREG_4V5 or VREG_VCO
4	HW_PD	HW Power Down	CMOS Schmitt Triggered Input, 1.8 V compatible, 3.3 V tolerant
5	PD_RF1	RF1 output stage Power Down control	CMOS Schmitt Triggered Input, 1.8 V compatible, 3.3 V tolerant
6	PD_RF2/FL_SW	RF2 output stage Power Down Control / Fast Lock switch	CMOS Schmitt Triggered Input, 1.8 V compatible, 3.3V tolerant (with Fast lock feature disabled); High impedance/ GND shorted output (with Fast Lock feature enabled)
7	CBYP	Connection for VCO circuitry regulator bypass capacitor	-
8	VREG_VCO	Regulated output voltage for VCO circuitry regulator	-
9	VIN_LDO_VCO	Supply voltage for VCO circuitry regulator	-
10	VR	Connection for reference voltage filtering capacitor	-
11	VCTRL	VCO control voltage	-
12	EXTVCO_INP	External VCO positive input	It must be connected to ground if external VCO is not used
13	EXTVCO_INN	External VCO negative input	It must be connected to ground if external VCO is not used
14	VCC_CP_BIAS	Supply voltage for Charge Pump bias	It must be connected to VREG_VCO
15	ICP	PLL charge pump output	-
16	VCC_CPOUT	Supply voltage for Charge Pump output stage	It must be connected to VREG_4V5 or VREG_VCO
17	VDD_PFD	Supply voltage for PFD	It must be connected to VREG_REF
18	VIN_LDO_REF	Supply voltage for PLL regulator	-
19	VREG_REF	Regulated output voltage for Reference Clock regulator	-
20	REF_CLKN	Reference clock negative input	-
21	REF_CLKP	Reference clock positive input	-

Table 2. Pin description (continued)

Pin No	Name	Description	Observation
22	LD_SDO	Lock Detector/SPI Data output	CMOS push-pull Output 2.5V with slew rate control or open drain (1.8V to 3.3V tolerant)
23	SDI	SPI Data input	CMOS Schmitt triggered Input, 1.8 V compatible, 3.3 V tolerant
24	SCK	SPI clock	CMOS Schmitt triggered Input, 1.8 V compatible, 3.3 V tolerant
25	LE	SPI load enable	CMOS Schmitt triggered Input, 1.8 V compatible, 3.3 V tolerant
26	VDD_DSM_NDIV	Supply voltage for DSM and N divider	It must be connected to VREG_DIG
27	VREG_DIG	Regulated output voltage for digital circuitry regulator	-
28	VIN_LDO_RF_DIG	Supply voltage for RF Output divider stage and digital regulators	-
29	VREG_RF	Regulated output voltage for RF Output Divider stage regulator	-
30	RF1_OUTN	Main RF negative output	50 Ω output impedance
31	RF1_OUTP	Main RF positive output	50 Ω output impedance
32	VCC_RFOUT	Supply voltage for RF Output stages	Connected to VREG_DIV, VREG_4V5 or external 5V
33	RF2_OUTN	Auxiliary RF negative output	50 Ω output impedance
34	RF2_OUTP	Auxiliary RF positive output	50 Ω output impedance
35	TEST_SE	Test pin	It must be connected to ground
36	VIN_LDO_4V5	Supply voltage for 4.5 V regulator	-

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Supply voltage pins #14, #17, #26	-0.3 to 2.7	V
	Supply voltage LDOs pins #9, #18, #28, #36	-0.3 to 5.4	V
	Supply voltage pins #3	-0.3 to 5	V
	Supply voltage pins #16, #32	-0.3 to 5.4	V
Tstg	Storage temperature	+150	°C
ESD	Electrical Static Discharge HBM CDM-JEDEC Standard MM	 2 0.5 0.2	kV

4 Operating conditions

Table 4. Operating conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
VCC	Supply voltage pins #14, #17, #26	-	2.5	-	2.7	V
	Supply voltage (LDOs inputs) pins #9, #18, #28, #36	-	3.0	-	5.4	V
	Supply voltage pin #3, #16, #32	-	2.5	-	5	V
I_{CC}	Current Consumption Pin #3, #16 and #32 supplied at 4.5 V	DIV2 ON, Main Output only, 4 GHz VCO, max. performance	-	84	-	mA
	Current Consumption Pin #3, #16 and #32 supplied at 2.6 V		-	50	-	mA
	Current consumption other blocks an supplies at 2.6 V		-	110	-	mA
T_A	Operating ambient temperature	-	-40	-	85	°C
T_J	Maximum junction temperature	-	-	-	125	°C
Θ_{JA}	Junction to ambient package thermal resistance(1)	Multilayer JEDEC board	-	33	-	°C/W
Θ_{JB}	Junction to board package thermal resistance(1)	Multilayer JEDEC board	-	18	-	°C/W
Θ_{JC}	Junction to case package thermal resistance(1)	Multilayer JEDEC board	-	3	-	°C/W
Ψ_{JB}	Thermal characterization parameter junction to board(1)	Multilayer JEDEC board	-	17	-	°C/W
Ψ_{JT}	Thermal characterization parameter junction to top case(1)	Multilayer JEDEC board	-	0.3	-	°C/W

1. Refer to JEDEC standard JESD 51-12 for a detailed description of the thermal resistances and thermal parameters. Data here presented are referring to a Multilayer board according to JEDEC standard.
$T_J = T_A + \Theta J_A * P_{diss}$ (in order to estimate T_J if ambient temperature T_A and dissipated power P_{diss} are known)
$TJ = T_B + \Psi_{JB} * P_{diss}$ (in order to estimate T_J if ambient temperature T_B and dissipated power P_{diss} are known)
$T_J = T_T + \Psi_{JT} * P_{diss}$ (in order to estimate T_J if ambient temperature T_T and dissipated power P_{diss} are known)

Table 5. Digital logic levels

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Vdd	Internal Supply for digital circuits	-	-	2.6	-	V
Vil	Low level input voltage	Schmitt input	0	-	0.6	V
Vih	High level input voltage	Schmitt input	1.2	-	3.6	V
Vol	Low level output voltage	-	-	-	0.2	V
Voh	High level output voltage	-	Vdd-0.2	-	-	V

5 Electrical specifications

All electrical specifications are given at 25°C T_{AMB} and in a full-current mode, unless otherwise stated.

Table 6. Electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
Output frequency range						
F_{OUT}	Output Frequency	Direct output	3000	-	6000	MHz
		Divider by 2 output	1500	-	3000	MHz
		…	…	-	…	MHz
		Divider by 64 output	46.875	-	93.75	MHz
VCO dividers						
N	VCO Divider Ratio	Integer Mode	24	-	131071	-
		Fractional mode (DSM 1st Order)	24	-	510	-
		Fractional mode (DSM 2nd Order)	25	-	509	-
		Fractional mode (DSM 3rd Order)	27	-	507	-
		Fractional mode (DSM 4st Order)	31	-	503	-
Xtal oscillator						
F_{XTAL}	XTAL frequency range	-	10	-	50	MHz
ESR_{XTAL}	XTAL ESR	-	-	-	50	Ω
P_{XTAL}	XTAL Power Dissipation	-	-	-	5	mW
CIN_{XTAL}	XTAL Oscillator Input capacitance	Single ended	0.6	-	-	pF
PN_{XTAL}	XTAL Oscillator Phase Noise Floor	50 MHz XTAL	-	-162	-	dBc/Hz
TOL_{XTAL}	XTAL Oscillator accuracy	@12 MHz, 25 °C	-	-	10	ppm
Reference clock and phase frequency detector						
F_{ref}	Reference input frequency(1)	-	10	-	800	MHz
	Reference input sensitivity	Differential Mode	0.2	1	1.25	Vp
		Single Ended Mode	0.35	1	1.25	Vp
PN_{REFIN}	Reference Input Buffer Phase Noise Floor	Single Ended Mode @100 MHz, sinusoidal signal 1.25 Vp	-	-163	-	dBc/Hz
		LVDS signal @100 MHz 400 mVp	-	-159	-	dBc/Hz

Table 6. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{REF}	Current consumption(2)	Differential Mode	-	10	-	mA
		Single Ended Mode	-	3	-	
		XTAL oscillator Mode	-	5	-	
R	Reference Divider Ratio	-	1	-	8191	
F_{PFD}	PFD input frequency(3)	-	-	-	100	MHz
F_{STEP}	Frequency step(3)	LO direct output		47.5		Hz
		LO with divider by 2		23.75		Hz
		…		…		Hz
		LO with divider by 64		0.7422		Hz
Charge pump						
VCC_{CPOUT}	CP Supply	Pin # 16 (VCC_CPOUT)	2.5	-	5	V
I_{CP}	ICP sink/source	5-bit programmable	-	-	4.9	mA
V_{OCP}	Output voltage compliance range	-	0.4	-	VCC_{CPOUT} -0.4	V
	Comparison frequency Spurs (4)	-	-	-85		dBc
	In-Band Fractional Spurs (5)	-	-	-50		
VCOs						
$VCC_{VCOCore}$	VCO Core Supply	Pin # 3 (VCC_VCO_Core)	2.5	-	5	V
$I_{VCOCore}$	Oscillator Core current consumption	@ 4 GHz and 4.5 V supply	-	52	-	mA
		@ 4 GHz and 3.3 V supply	-	35	-	
		@ 4 GHz and 2.6 V supply	-	30	-	
I_{VCOBUF}	VCO buffer consumption	Pin # 3 (VCC_VCO_Core)	-	35	-	mA
K_{VCO}	VCO gain	VCO freq. range: 3.0 to 4.0 GHz	-	35-85	-	MHz/V
		VCO freq. range: 4.0 to 5.0 GHz	-	40-90	-	MHz/V
		VCO freq. range: 5.0 to 6.0 GHz	-	45-95	-	MHz/V
ΔT_{LK}	Maximum temperature variation for continuous lock(6)(7)	Pin #16 @4.5/5 V	-125		125	^{o}C
		Pin #16 @3.3 V	-125		125	^{o}C
		Pin #16 @2.6 V	-125		115	^{o}C
RF output stage						
VCC_{RFOUT}	RF Output supply	Pin # 35 (VCC_RFOUT)	2.5	-	5	V
P_{OUT}	Output level	Differential 3.3 V to 5 V supply	-1	-	+7	dBm
	-	Differential 2.6 V supply	-1	-	+1	

Table 6. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Z_{OUT}	Output impedance	Differential	-	100	-	Ω
		Single Ended	-	50	-	Ω
R_L	Return Loss	Matched to 50-ohm Single Ended	-	15	-	dB
H_2	LO 2nd Harmonic	Direct output (single/differential)	-	-30/-40	-	dBc
		Divided output (single/differential)	-	-30/-35	-	dBc
H_3	LO 3rd Harmonic	Direct output (single/differential)	-	-15/-15	-	dBc
		Divided output (single/differential)	-	-15/-15	-	dBc
P_{MUTE}	Level of Signal with RF Mute Enabled	Direct output @4 GHz (single/diff)	-	-45/-60	-	dBm
		Divided output @2 GHz (single/diff)	-	-45/-60	-	dBm
P_{ISO}	Main/aux port isolation	Direct output @4 GHz (single/diff)	-	-35/-40	-	dBc
		Divided output @2 GHz (single/diff)	-	-40/-45	-	dBc
I_{DIV}	RF Divider Current Consumption(8)	Direct output (1 differential output)	-	28	-	mA
		DIV2 buff (1 differential output)	-	47	-	
		DIV4 buff (1 differential output)	-	56	-	
		DIV8 buff (1 differential output)	-	65	-	
		DIV16 buff (1 differential output)	-	75	-	
		DIV32 buff (1 differential output)	-	83		
		DIV64 buff (1 differential output)	-	92	-	
		Auxiliary path enabled	-	19	-	
$I_{RFOUTBUF}$	RF Output Buffer Current Consumption(8)	3.3 V to 5 V supply (1 differential output; P_{OUT} = +7 dBm)	-	25	-	mA
		3.3 V to 5 V Auxiliary path enabled	-	25	-	
		2.6 V supply (1 differential output; P_{OUT} = +1 dBm)	-	12	-	
		2.6 V Auxiliary path enabled	-	12	-	

Table 6. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
PLL miscellaneous						
I_{PLL}	PLL current Consumption(8)	Prescaler, digital dividers, misc.	-	20	-	mA
I_{DSM}	ΔΣ Modulator current consumption(8)	-	-	3.5	-	mA

1. The maximum frequency of the Reference Divider is 200 MHz; when using higher reference clock frequency (up to the max. value of 800 MHz) the internal divider by 2 or divider by 4 must be enabled.
The fractional mode is allowed in the full frequency range only with reference clock frequency >11.93 MHz With reference clock frequency in the range 10 MHz to 11.93 MHz, due to the limits of N value in fractional mode, the full VCO frequencies would not be addressed in fractional mode; in this case the frequency doubler in the reference path can be enabled.
2. Reference clock signal @ 100 MHz, R=2
3. The minimum frequency step is obtained as F_{PFD} / (2^21); these typical values are obtained considering F_{PFD} = 100 MHz.
4. PFD frequency leakage.
5. This is the level inside the PLL loop bandwidth due to the contribution of the ΔΣ Modulator. In order to obtain the fractional spurs level for a specific frequency offset, the attenuation provided by the loop filter at such offset should be subtracted.
6. Once a VCO is programmed at the initial temperature T_0 inside the operating temperature range (-40 °C to +85 °C), the synthesizer is able to maintain the lock status only if the temperature drift (in either direction) is within the limit specified by ΔT_{LK}, provided that the final temperature T_f is still inside the nominal range.
7. In order to guarantee the performance of ΔT_{LK} the bit CAL_TEMP_COMP in register ST6 must be set to ‘1’.
8. Current consumption measured with PLL locked in following conditions: Reference clock signal @ 100 MHz; PFD @50 MHz (R=2); VCO @ 4005 MHz

Table 7. Phase noise specifications(1)

Parameter	Min	Typ	Max	Units
Normalized In Band Phase Noise Floor(2)	-	-227	-	dBc/Hz
VCO Open Loop Phase Noise at F_{OUT} @ 4 GHz – VIN=5.0 V, VREG=4.5 V				
Phase Noise @ 1 kHz	-	-64	-	dBc/Hz
Phase Noise @ 10 kHz	-	-91	-	dBc/Hz
Phase Noise @ 100 kHz	-	-114	-	dBc/Hz
Phase Noise @ 1 MHz	-	-135	-	dBc/Hz
Phase Noise @ 10 MHz	-	-154	-	dBc/Hz
Phase Noise @ 100 MHz	-	-160	-	dBc/Hz
VCO Open Loop Phase Noise at F_{OUT} @ 4 GHz/2 = 2GHz – VIN=5.0 V, VREG=4.5 V				
Phase Noise @ 1 kHz	-	-70	-	dBc/Hz
Phase Noise @ 10 kHz	-	-97	-	dBc/Hz
Phase Noise @ 100 kHz	-	-120	-	dBc/Hz
Phase Noise @ 1 MHz	-	-141	-	dBc/Hz
Phase Noise @ 10 MHz	-	-156	-	dBc/Hz
Phase Noise @ 40 MHz	-	-159	-	dBc/Hz
VCO Open Loop Phase Noise at F_{OUT} @ 4 GHz/4 = 1 GHz – VIN=5.0 V, VREG=4.5 V				
Phase Noise @ 1 kHz	-	-76	-	dBc/Hz
Phase Noise @ 10 kHz	-	-103	-	dBc/Hz
Phase Noise @ 100 kHz	-	-126	-	dBc/Hz
Phase Noise @ 1 MHz	-	-146	-	dBc/Hz
Phase Noise @ 10 MHz	-	-159	-	dBc/Hz
Phase Noise Floor	-	-160	-	dBc/Hz
VCO Open Loop Phase Noise at F_{OUT} @ 4 GHz/32 = 125 MHz – VIN=5.0 V, VREG=4.5 V				
Phase Noise @ 1 kHz	-	-92	-	dBc/Hz
Phase Noise @ 10 kHz	-	-121	-	dBc/Hz
Phase Noise @ 100 kHz	-	-144	-	dBc/Hz
Phase Noise @ 1 MHz	-	-161	-	dBc/Hz
Phase Noise @ 10 MHz	-	-163	-	dBc/Hz
Phase Noise Floor	-	-164	-	dBc/Hz
VCO Open Loop Phase Noise at F_{OUT} @ 4 GHz – VIN=3.6V , VREG=3.3 V				
Phase Noise @ 1 kHz	-	-62	-	dBc/Hz
Phase Noise @ 10 kHz	-	-89	-	dBc/Hz
Phase Noise @ 100 kHz	-	-113.2	-	dBc/Hz

Table 7. Phase noise specifications[1]

Parameter	Min	Typ	Max	Units
Phase Noise @ 1 MHz	-	-133.6	-	dBc/Hz
Phase Noise @ 10 MHz	-	-152.4	-	dBc/Hz
Phase Noise @ 100 MHz	-	-158.5	-	dBc/Hz
VCO Open Loop Phase Noise at F_{OUT} @ 4 GHz – VIN=3.0 V, VREG=2.6 V				
Phase Noise @ 1 kHz	-	-60.5	-	dBc/Hz
Phase Noise @ 10 kHz	-	-88	-	dBc/Hz
Phase Noise @ 100 kHz	-	-110.3	-	dBc/Hz
Phase Noise @ 1 MHz	-	-131	-	dBc/Hz
Phase Noise @ 10 MHz	-	-150	-	dBc/Hz
Phase Noise @ 100 MHz	-	-157	-	dBc/Hz

1. Phase Noise SSB unless otherwise specified. The VCO Open loop figures are specified at 4.5/5 V on VCC_VCO_Core (pin #3).
2. Normalized PN = Measured PN – 20log(N) – 10log(F_{PFD}) where N is the VCO divider ratio and F_{PFD} is the comparison frequency at the PFD input.

6 Typical Performance Characteristics

Figure 3. VCO open loop Phase Noise @ 5 V Supply

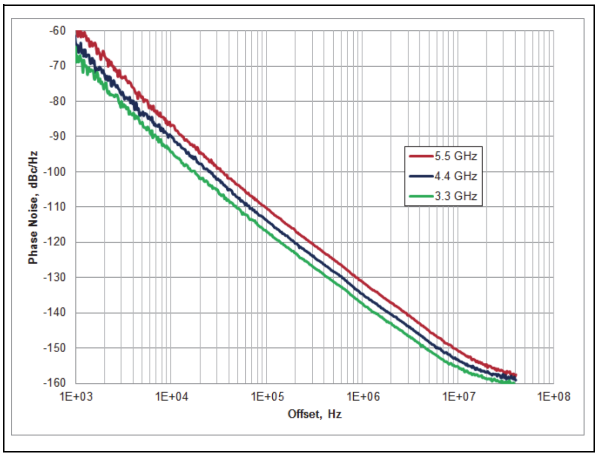


Figure 4. Closed Loop Phase Noise at 4.8 GHz, divided by 1 to 64 (5 V Supply)

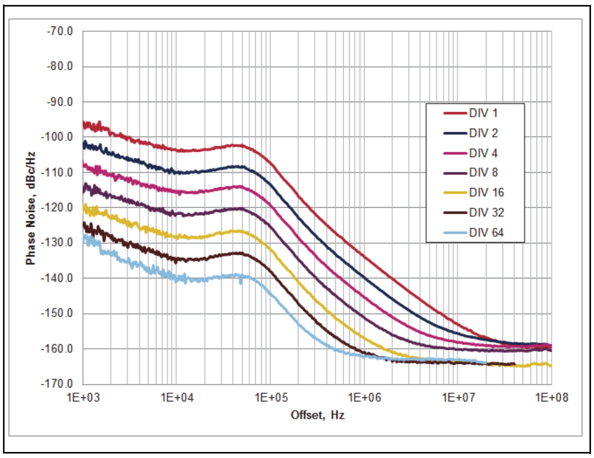


Figure 5. VCO Open Loop Phase Noise at 4.4 GHz vs. Supply setup

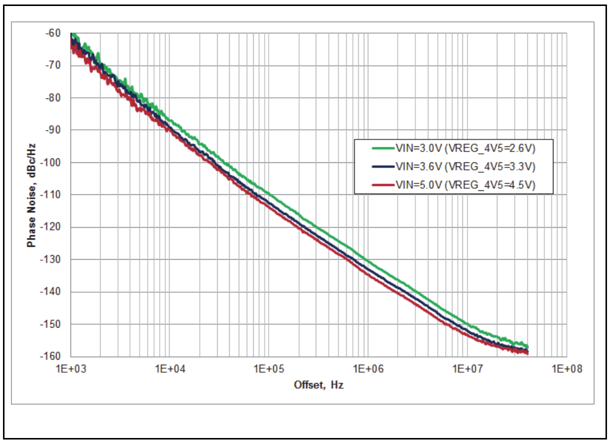


Figure 6. VCO Open Loop Phase Noise over Frequency GHz vs. Supply setup

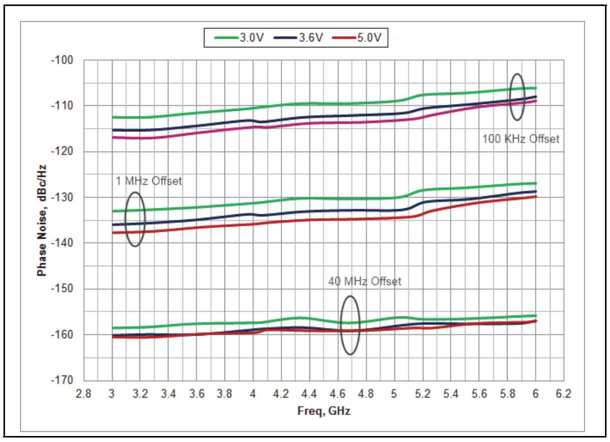


Figure 7. Single Sideband Integrated Phase Noise (5 V Supply; FPFD=50MHz)

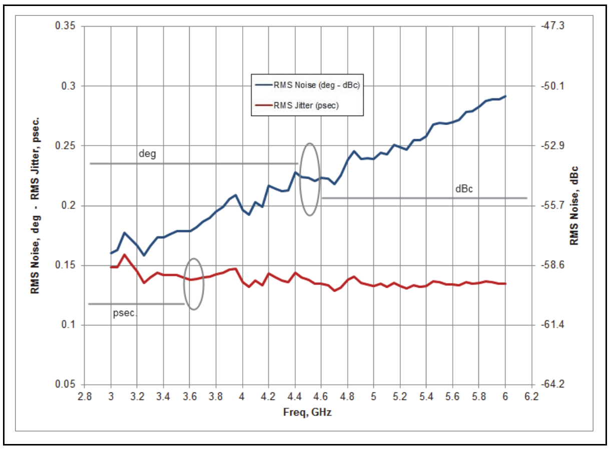


Figure 8. Output Power Level – Single ended (3 dB more for differential)

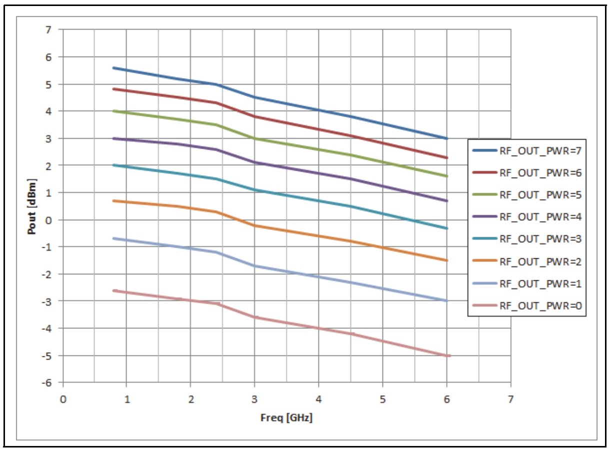


Figure 9. Phase Noise and Fractional spurs at 2646.96 MHz vs Supply setup (F_{PFD}=61.44 MHz)

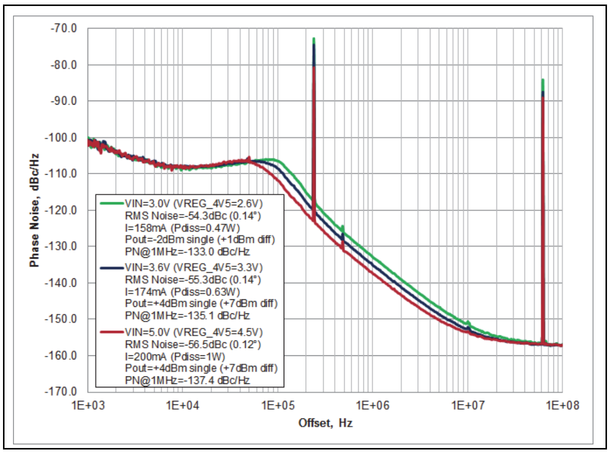


Figure 10. Phase Noise and Fractional spurs at 2118.24 MHz vs Supply setup (F_{PFD}=61.44 MHz)

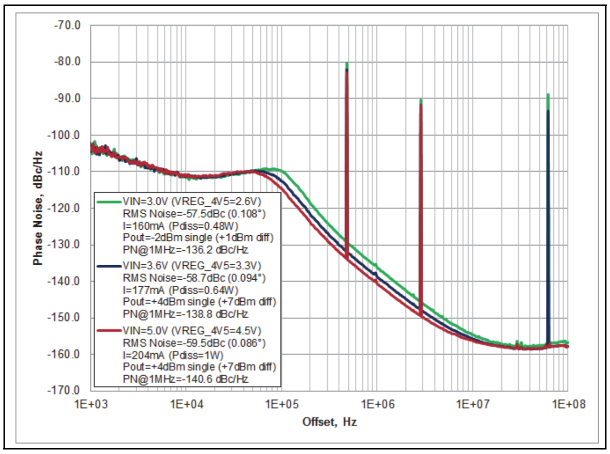


Figure 11. Phase Noise and Fractional spurs at 2118.24 MHz at 5.0 V Supply (F_{PFD}=61.44 MHz)

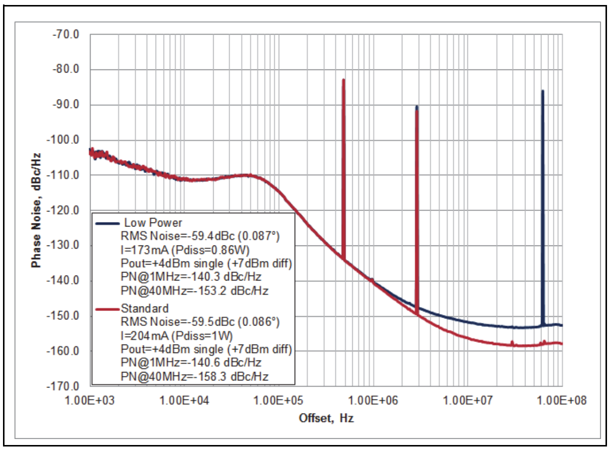


Figure 12. Phase Noise and Fractional spurs at 2118.24 MHz at 3.6 V Supply (F_{PFD}=61.44 MHz)

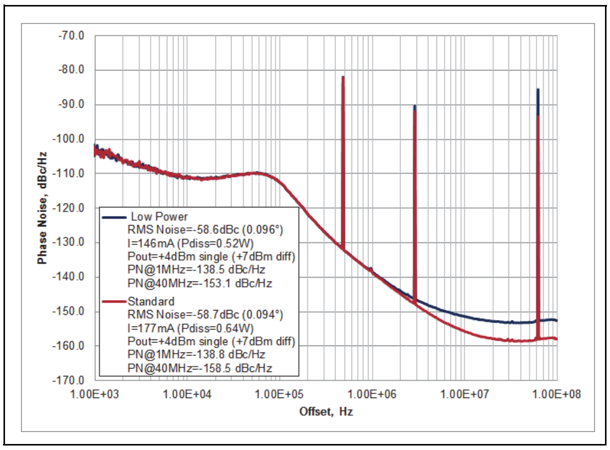


Figure 13. Phase Noise and Fractional spurs at 2118.24 MHz at 3.0 V Supply (F_{PFD}=61.44 MHz)

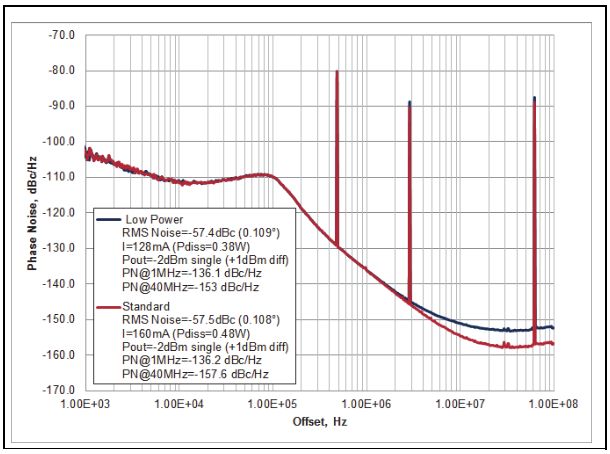


Figure 14. Phase Noise at 5.625 GHz and 4.6 GHz (F_{PFD}=50 MHz)

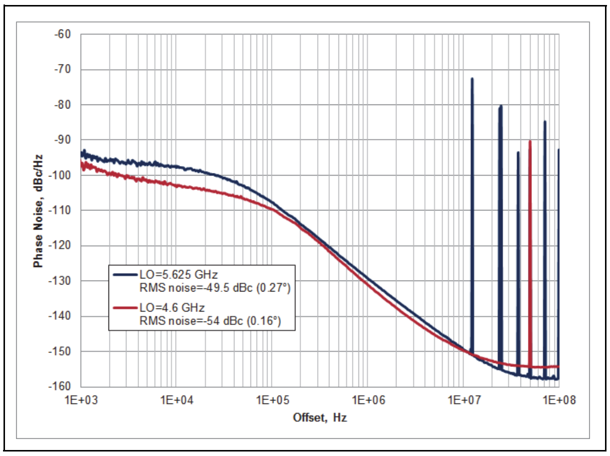


Figure 15. Typical VCO control voltage after VCO calibration @ 3.6 V Supply

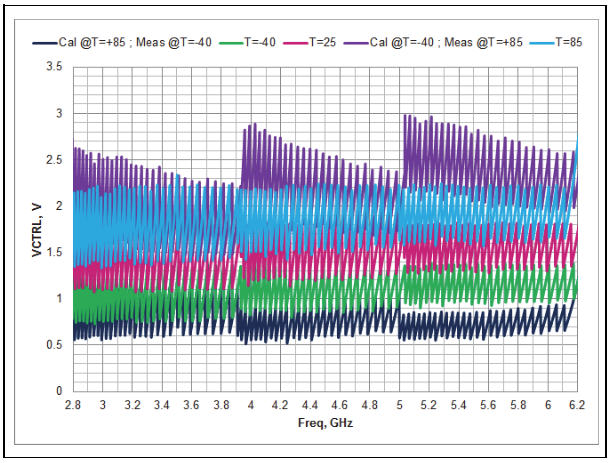
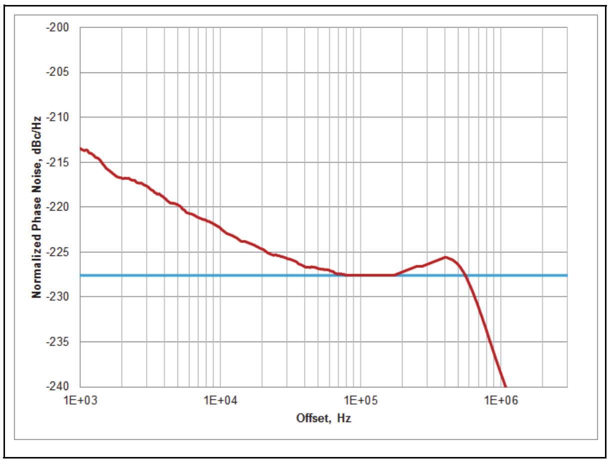


Figure 16. Figure of Merit



7 Circuit description

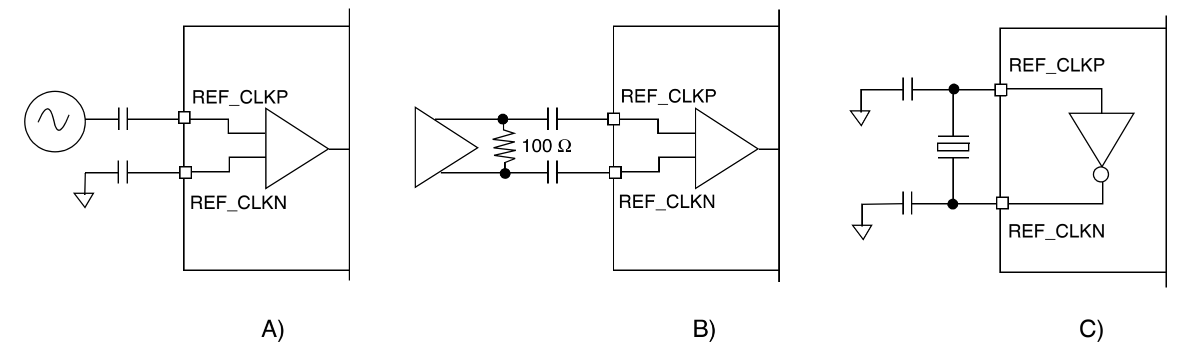
7.1 Reference input stage

The reference input stage provides different modes for the reference clock signal.

Both single-ended and differential modes (LVDS, LVECPL) are supported; a crystal mode is also provided in order to build a Pierce type crystal oscillator. *Figure 17* shows the connections required for the different configurations supported.

In single-ended and differential modes the inputs must be AC coupled as the REF_CLKP and REF_CLKN pins are internally biased to an optimal DC operating point. The input resistance is 100 ohms differential and the best performance for phase noise is obtained for signals with a higher slew rate, such as a square wave.

Figure 17. Reference clock buffer configurations: single-ended (A), differential (B), crystal mode (C)



7.2 Reference divider

The 13-bit programmable reference counter is used to divde the input reference frequency to the desired PFD frequency. The division ratio is programmable from 1 to 8191.

The maximum allowed input frequency of the R-Counter is 200 MHz.

The reference clock can be extended up to 400 MHz enabling the divide-by-2 stage or up to 800 MHz enabling the divide-by-4 stage.

A frequency doubler is provided in order to double low reference frequencies and increase the PFD operating frequency thus allowing an easier filtering of the out-of-band noise of the Delta-Sigma Modulator; the doubler is introducing a noise degradation in the in-band PLL noise thus this feature should be carefully used.

When the doubler is enabled, the maximum reference frequency is limited to 25 MHz.

7.3 PLL N divider

The N divider set the division ratio in the PLL feedback path.

Both Integer-N and Fractional-N PLL architectures are implemented in order to ensure the best overall performance of the synthesizer.

The Fractional-N division is achieved combining the integer divider section with a Delta-Sigma modulator (DSM) which sets the fractional part of the overall division ratio.

The DSM is implemented as a MASH structure with programmable order (2 bit; 1^{st}, 2^{nd}, 3^{rd} and 4^{th} order), programmable MODULUS (21 bit).

It includes also a DITHERING function (1 bit) which can be used to reduce fractional spur tones by spreading the DSM sequence and consequently the energy of the spurs over a wider bandwidth.

The overall divisio ratio N is given by:

$$N = N_{INT} + N_{FRAC}$$

The integer part N_{INT} is 17-bit programmable and can range from 24 to 131071 in Integer Mode. For $N_{INT} \geq 512$ the fractional mode is not allowed and the setting used for DSM does not have any effect.

Based upon the selected order of the Delta-Sigma Modulator the allowed range of N_{INT} values changes as follows:

- 24 to 510 - 1st Order DSM
- 25 to 509 - 2nd Order DSM
- 27 to 507 - 3rd Order DSM
- 31 to 503 - 4th Order DSM

The fractional part N_{FRAC} of the division ratio is controlled by setting the values FRAC and MOD (21 bits each) and it depends also on the value of DITHERING (1 bit):

$$N_{FRAC} = \frac{FRAC}{MOD} + \frac{DITHERING}{2 \cdot MOD}$$

The MOD value can range from 2 to 2097151, while the range of FRAC is from 0 to MOD-1. If the DITHERING function is not used (DITHERING=0) the fractional part of N is simply achieved as ratio of FRAC over MOD.

The resulting VCO frequency is:

$$F_{VCO} = \frac{F_{ref}}{R} \cdot N = \frac{F_{ref}}{R} \cdot \left(N_{INT} + \frac{FRAC}{MOD} + \frac{DITHERING}{2 \cdot MOD}\right)$$

where:

F_{VCO} is the output frequency of VCO

F_{ref} is the input reference frequency

R is the division ratio of reference chain

N is the overall division ratio of the PLL

The implementation with programmable modulus allows the user to select easily the desired fraction and the exact synthesized frequency whitout any approximation.

The MOD value can be set to very high values thus the frequency resolution of the synthesizer can reach very fine steps (down to a few hertz).

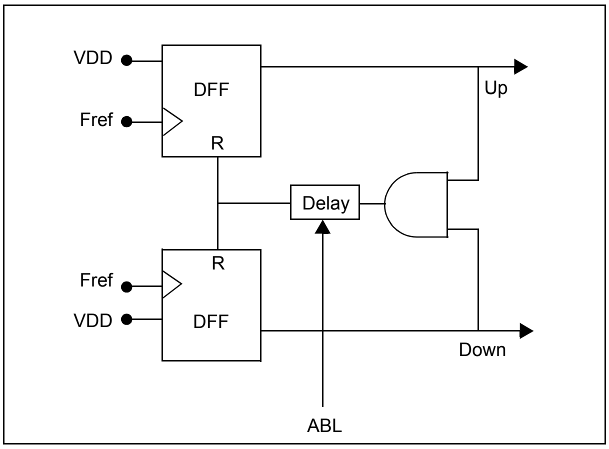
A ‘low spur mode’ could be configured by maximizing both FRAC and MOD values, keeping the same desired FRAC/MOD ratio, and setting the DITHERING bit to ‘1’. The drawback is a small frequency error, equal to F_{PFD}/(2*MOD), on the synthesized frequency which is in the range of a few hertz, usually tolerated by most applications.

7.4 Phase frequency detector (PFD)

The PFD takes inputs from the reference and the VCO dividers and produces an output proportional to the phase error. The PFD includes a delay gate that controls the width of the anti-backlash pulse (1.2 to 3 ns). This pulse ensures that there is no dead zone in the PFD transfer function.

The following figure is a simplified schematic of the PFD.

Figure 18. PFD diagram



7.5 Lock detect

The lock detector indicates the lock state for the PLL. The lock condition is detected by comparing the UP and DOWN outputs of the digital Phase Frequency Detector

A CMOS logic output signal indicates the lock state; the polarity of the output signal can be inverted using the LD_ACTIVELOW bit.

The lock condition occurs when the delay between the edges of UP and DOWN signals is lower than a specific value (3-bit programmable from 2 ns to 16 ns) and this condition is stable for a specific number of consecutive PFD cycles (3-bit programmable counter from 4 to 4096 cycles).

This flexibility is needed by the lock detector circuitry to work properly with all the possible different PLL setups (Integer-N, Fractional-N, different PFD frequencies and so on).

7.6 Charge pump

This Charge Pump consists of two matched current sources, Iup and Idown, which are controlled respectively by UP and DOWN PFD outputs. The nominal value of the output current (I_{CP}) is controlled by the selection among 32 different values by a 5-bit word.

The minimum value of the output current (I_{CP}) is 158 µA.

The charge pump also includes a compensation circuitry to take into account the K_{VCO} variation with the loop filter VCO control voltage. It adjusts the nominal I_{CP} value, minimizing the variation of the product of I_{CP} and K_{VCO} to keep the PLL bandwidth constant.

The charge pump output stage can be supplied from 2.5 V to 5.0 V.

Table 8. Current value vs. selection

CPSEL4	CPSEL3	CPSEL2	CPSEL1	CPSEL0	Current	Value
0	0	0	0	0	-	0
0	0	0	0	1	I_{MIN}	158 µA
0	0	0	1	0	$2*I_{MIN}$	316 µA
-	-	-	-	-	-	-
-	-	-	-	-	-	-
1	1	1	0	1	$29*I_{MIN}$	4.58 mA
1	1	1	1	0	$30*I_{MIN}$	4.74 mA
1	1	1	1	1	$31*I_{MIN}$	4.9 mA

7.7 Fast lock mode

The fast-lock feature can be enabled to trade fast settling time with spurs rejection, performances which are generally requiring different settings of PLL bandwidth (narrow for better spurs rejection and wide for fast settling time).

A narrow bandwidth for lower spurs can be designed for the lock state while a wider bandwidth can be designed for the PLL transients.

The wider bandwidth is achieved during the transient by increasing the charge pump current and reducing accordingly the dumping resistor value of the loop filter in order to keep the phase margin of the PLL constant. The duration of the PLL wide band mode, in terms of number of PFD cycles, is set by programming the fast lock 13 bit counter.

7.8 Cycle slip reduction

The use of high F_{PFD}/PLL_BW ratios may lead to an increased settling time due to cycle slips.

A cycle slip compensation circuit is provided which automatically increases the charge pump current for high frequency errors and restores the programmed value at the end of the locking phase.

7.9 Voltage controlled oscillators (VCOs)

The STW81200 VCO section consists of three separate low-noise VCOs with different LC Tanks structures to cover a wide band from 3000 MHz to 6000 MHz.

Each VCO is implemented using a structure with multiple sub-bands to keep low the VCO sensitivity (Kvco), thus resulting in low phase noise and spurs performances.

The correct VCO and sub-band selection is automatically performed by a dedicated digital circuitry (clocked by the PFD) at every new frequency programming.

During the selection procedure the VCTRL of the VCO is charged to a fixed reference voltage.

The procedure for the VCO and sub-band selection takes approximately 11 * CALDIV PFD cycles, where CALDIV is the division ratio of the programmable divider included in the path between the PFD and the selection circuitry. The maximum frequency allowed for the sub-band selection is 1MHz and the CALDIV value must be set accordingly if the PFD frequency is higher.

Once the correct VCO and sub-band are selected the normal PLL operations are resumed.

The VCO core could be supplied up to 5 V for maximum performance or to a minimum of 2.5 V trading off current consumption and performance.

7.10 RF output divider stage

The signal coming from the VCOs is fed to a flexible RF divider stage.

The divider ratio is programmable among different values (1, 2, 4, 8 ,16, 32 and 64) and allows the selection of the desired output frequency band:

- 3.0 to 6.0 GHz (divider ratio = 1)
- 1.5 to 3.0 GHz (divider ratio = 2)
- 0.75 to 1.5 GHz (divider ratio = 4)
- 375 to 750 MHz (divider ratio = 8)
- 187.5 to 375 MHz (divider ratio = 16)
- 93.75 to 187.5 MHz (divider ratio = 32)
- 46.875 to 93.75 MHz (divider ratio = 64)

The final output stage buffer (pins RF1_OUTP, RF1_OUTN) is internally broadband matched to 100-ohm differential (50-ohm single-ended) and it delivers up to +7 dBm of output power on a 100-ohm differential load (+4 dBm on 50-ohm from each single-ended output).

The final output stage buffer has a 3-bit programmable output level and can be powered down by software and/or hardware (pin PD_RF1) while the internal PLL is locked.

An auxiliary output stage buffer (pins RF2_OUTP and RF2_OUTN) is available with the same features of the main one.

The RF division ratio of this auxiliary output can be set independently from the main output in order to increase the flexibility. Furthermore it is possible to get on the auxiliary output a signal In-Phase or in Quadrature with the main one, if the same frequency is selected on both outputs.

The auxiliary output stage can also be powered down by software and/or hardware (pin PD_RF2).

The output stage can be muted until the PLL achieves the lock status; this function can be activated by software.

7.11 Low power functional mode

All the performance characteristics defined in the electrical specifications are achieved in full current mode. The STW81200 is able to provide a set of low power functional modes which allows control of the current consumption of the different blocks.

This feature can be helpful for those applications requiring low power consumption. The power saving modes trade the current consumption with the phase noise performance, and/or output level.

The current of the blocks defined in *Table 9* can be set by software, and the power saved on each block affect a specific performance as described in the same table.

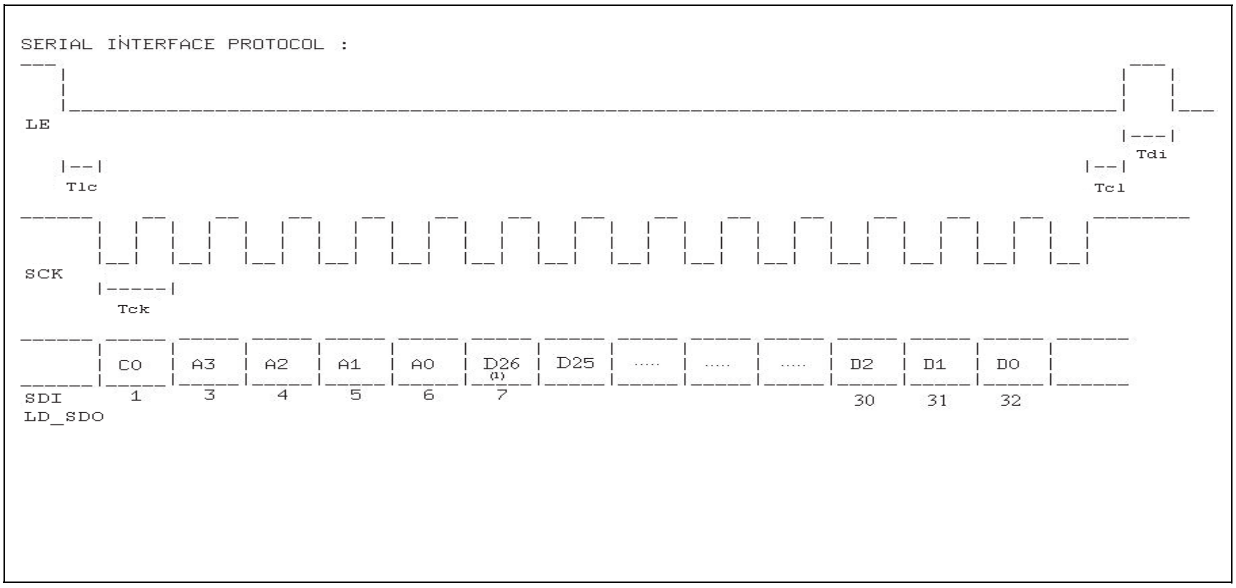
Table 9. Blocks with programmable current and related performance

Block	Current Control bits	Affected Performance
VCO Core	4 bit	VCO phase noise (offset >PLL_BW)
VCO Buffers	2 bit	Phase Noise Floor (offset > ~10 MHz)
RF Dividers Core	1 bit/each divider stage	Phase Noise Floor (offset > ~10 MHz)
RF output stage	3 bit	RF output level

7.12 STW81200 Register Programming

The STW81200 has 12 registers (10 R/W + 2 Read-Only) programmed through an SPI digital interface. The protocol uses 3 wires (SDI, SCK, LE) for write mode plus an additional pin (LD_SDO) for read operation. Each register has 32 bits, one for Read/Write mode selection, 4 address bits and 27 data bits.

Figure 19. SPI Protocol



1. Bit for double buffering used for some registers only

The Data bits are stored in the internal shift register on the rising edge of SCK.

The first bit ,CO is used for mode selection (0=Write Operation, 1=Read Operation). The bit A[3:0] represents the register address, and D[26:0] are the data bits.

In some registers, the first data bit D26 is used (when set to '1') for double-buffering purposes. In this case the register content is stored in a temporary buffer and is transferred to the internal register once a write operation is done on the master register ST0.

Figure 20. SPI timing diagram

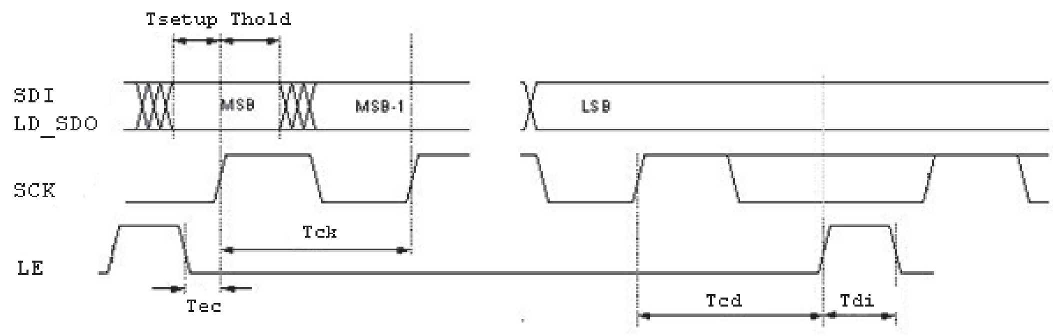


Table 10. SPI timings

Parameter	Comments	Min	Typ	Max	Unit
Tsetup	data to clock setup time	4	-	-	ns
Thold	data to clock hold time	1	-	-	ns
Tck	clock cycle period	20	-	-	ns
Tdi	disable pulse width	4	-	-	ns
Tcd	clock-to-disable time	1	-	-	ns
Tec	enable-to-clock time	3	-	-	ns

7.13 STW81200 Register Summary

Table 11. SPI Register map (address 12 to 15 not available)

Address	Register Name	Type	Description	Page
0x00	ST0_Register	Read/Write	Master register. N divider, CP current	on page 31
0x01	ST1_Register	Read/Write Double-Buffered	FRAC value, RF1 output control	on page 32
0x02	ST2_Register	Read/Write Double-Buffered	MOD value, RF2 output control	on page 33
0x03	ST3_Register	Read/Write Double-Buffered	R divider, CP leakage, CP down-split pulse, Ref. Path selection, Device power down	on page 34
0x04	ST4_Register	Read/Write	Lock det. control, Ref. Buffer, CP supply mode, VCO settings, Output power control	on page 36
0x05	ST5_Register	Read/Write	Low power mode control bit	on page 38
0x06	ST6_Register	Read/Write	VCO Calibrator, Manual VCO control, DSM settings	on page 39
0x07	ST7_Register	Read/Write	Fast Lock control, LD_SDO settings	on page 41
0x08	ST8_Register	Read/Write	LDO Voltage Regulator settings	on page 42
0x09	ST9_Register	Read/Write	Reserved (Test & Initialization bit)	on page 43
0x0A	ST10_Register	Read Only	VCO, Lock det. Status, LDO status	on page 44
0x0B	ST11_Register	Read Only	Device ID	on page 45

ST0 Register

26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	CP_SEL[4:0]					PFD_DEL[1:0]		RESERVED	RESERVED	N[16:0]																
RW	RW					RW		RW	RW	RW																

Address: STW81200BaseAddress + 0x00

Type: R/W

Description: Master register. N divider, CP current

[26] RESERVED: must be set to ‘0’

[25:21] CP_SEL: Set Charge Pump pulse current value (0 to 4.9 mA; step ~158 µA)
00000: (0) set ICP=0
00001: (1) set ICP=158 µA
00010: (2) set ICP=316 µA
…
11110: (30) set ICP=4.74 mA
11111: (31) set ICP=4.90 mA

[20:19] PFD_DEL: Set PFD anti-backlash delay
00: (0) 1.2 ns (default)
01: (1) 1.9 ns
10: (2) 2.5 ns
11: (3) 3.0 ns

[18] RESERVED: must be set to ‘0’

[17] RESERVED: must be set to ‘0’

[16:0] N: Set integer part of N divider ratio (N_{INT})
For $N_{INT} \geq 512$, fractional mode is not allowed (FRAC and MOD settings are ignored)

ST1 Register

26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBR	RESERVED	RF1_OUT_PD	RF1_DIV_SEL[2:0]			FRAC[20:0]																				
RW	RW	RW	RW			RW																				

Address: STW81200BaseAddress + 0x01

Type: R/W

Applicability: Double buffered (based upon DBR bit setting)

Description: FRAC value, RF1 output control

[26] DBR: Double buffering bit enable; at ‘1’ the register is buffered and transferred only once the master register ST0 is written

[25] RESERVED: must be set to ‘0’

[24] RF1_OUT_PD: RF1 output power down
0 = RF1 output enabled
1 = RF1 output disabled

[23:21] RF1_DIV_SEL: RF1 output divider selection
000: (0) VCO direct
001: (1) VCO divided by 2
010: (2) VCO divided by 4
011: (3) VCO divided by 8
100: (4) VCO divided by 16
101: (5) VCO divided by 32
110: (6) VCO divided by 64
111: (7) Reserved

[20:0] FRAC: Fractional value bit; set the numerator value of the fractional part of the overall division ratio ($N=N_{INT}+FRAC/MOD$)
Range: 0 to 2097151 (must be < MOD)

ST2 Register

26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBR	RESERVED	RF2_OUT_PD	RF2_DIV_SEL[2:0]			MOD[20:0]																				
RW	RW	RW	RW			RW																				

Address: STW81200BaseAddress + 0x02

Type: R/W

Applicability: Double buffered (based upon DBR bit setting)

Description: MOD value, RF2 output control

[26] DBR: Double buffering bit enable; at ‘1’ the register is buffered and transferred only once the master register ST0 is written

[25] RESERVED: must be set to ‘0’

[24] RF2_OUT_PD: RF2 output power down
0 = RF2 output enabled
1 = RF2 output disabled

[23:21] RF2_DIV_SEL: RF2 output divider selection
000: (0) VCO direct
001: (1) VCO divided by 2
010: (2) VCO divided by 4
011: (3) VCO divided by 8
100: (4) VCO divided by 16
101: (5) VCO divided by 32
110: (6) VCO divided by 64
111: (7) same divided output of RF1 (not valid if RF1_DIV_SEL=0)

[20:0] MOD: Modulus value bit; set the denominator value of the fractional part of the overall division ratio ($N=N_{INT}+FRAC/MOD$)
Range: 2 to 2097151

ST3 Register

26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBR	PD	CP_LEAK_x2	CP_LEAK[4:0]					CP_LEAK_DIR	DNSPLIT_EN	PFD_DEL_MODE[1:0]		REF_PATH_SEL[1:0]		R[12:0]												
RW	RW	RW	RW					RW	RW	RW		RW		RW												

Address: STW81200BaseAddress + 0x03

Type: R/W

Applicability: Double buffered (based upon DBR bit setting)

Description: R divider, CP leakage, CP down-split pulse, Ref. Path selection, Device power down

[26] DBR: Double buffering bit enable; at ‘1’ the register is buffered and transferred only once the master register ST0 is written

[25] PD: device power down; at ‘1’ put OFF all blocks (except LDOs)

[24] CP_LEAK_x2: double Charge Pump leakage current bit
0 = set standard leakage current
1 = set doubled leakage current

[23:19] CP_LEAK: Set Charge Pump leakage current value (0 to 620 µA; step 10 µA or 20 µA base upon CP_LEAK_x2 setting)
00000: (0) set I_{LEAK} = 0 (default)
00001: (1) set I_{LEAK} = 10 µA (I_{LEAK} = 20 µA if CP_LEAK_x2 = 1)
00010: (2) set I_{LEAK} = 20 µA (I_{LEAK} = 40 µA if CP_LEAK_x2 = 1)
…
11110: (30) set I_{LEAK} = 300 µA (I_{LEAK} = 600 µA if CP_LEAK_x2 = 1)
11111: (31) set I_{LEAK} = 310 µA (I_{LEAK} = 620 µA if CP_LEAK_x2 = 1)

[18] CP_LEAK_DIR: set direction of the leakage current
0: set down-leakage (current sink)
1: set up-leakage (current source)

[17] DNSPLIT_EN: at ‘1’ enables down-split pulse current

[16:15] PFD_DEL_MODE: set PFD delay mode; delay values set by PFD_DEL[1:0] in register ST0
00: (0) no delay (default)
01: (1) VCO_DIV delayed
10: (2) REF_DIV delayed
11: (3) Reserved

[14:13] REF_PATH_SEL: reference clock path selection
00: (0) Direct
01: (1) Doubled in single mode; Not Applicable in differential mode
10: (2) Divided by 2
11: (3) Divided by 4

[13:0] R: set Reference clock divider ratio (1 to 8191)

ST4 Register

26	25–23	22	21	20	19	18–15	14	13–12	11	10	9–8	7	6	5–3	2–0
RESERVED	RF_OUT_PWR[2:0]	VCO_2V5_MODE	RESERVED	RESERVED	EXT_VCO_EN	VCO_AMP[3:0]	PLL_MUX_DIV	CP_SUPPLY_MODE[1:0]	KVCO_COMP_DIS	PFD_POL	REF_BUFF_MODE[1:0]	MUTE_LOCK_EN	LD_ACTIVELOW	LD_PREC[2:0]	LD_COUNT[2:0]
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: STW81200BaseAddress + 0x04

Type: R/W

Description: Lock det. control, Ref. Buffer, CP supply mode, VCO settings, Output power control

[26] RESERVED: must be set to ‘0’

[25:23] RF_OUT_PWR: RF Output power control bit; set output power level of differential signal (valid for both RF1 and RF2 outputs; measured @ 4 GHz)
000: (0) -1.0 dBm (-4.0 dBm on each single-ended signal)
001: (1) +1.0 dBm (-2.0 dBm on each single-ended signal)
010: (2) +2.5 dBm (-0.5 dBm on each single-ended signal)
011: (3) +3.5 dBm (+0.5 dBm on each single-ended signal)
100: (4) +4.5 dBm (+1.5 dBm on each single-ended signal)
101: (5) +5.5 dBm (+2.5 dBm on each single-ended signal)
110: (6) +6.5 dBm (+3.5 dBm on each single-ended signal)
111: (7) +7.0 dBm (+4.0 dBm on each single-ended signal)

[22] VCO_2V5_MODE: to be set to ‘1’ when VCO core (pin #3) is supplied at 2.6 V

[21] RESERVED: must be set to ‘0’

[20] RESERVED: must be set to ‘0’

[19] EXT_VCO_EN: external VCO Buffer enable
0: external VCO buffer disabled; integrated VCOs are used
1: external VCO buffer enabled; external VCO required (internal VCOs are powered down)

[18:15] VCO_AMP: set VCO signal amplitude at the internal oscillator circuit nodes; higher signal level gives best phase noise performance while lower signal level gives low current consumption.
Different ranges of value are available, based upon the supply voltage provided to pin VCC_VCO_core (pin #3).
Allowed settings:
0000 to 0110: (0-6) when VCO core is supplied at 2.6 V
0000 to 1010: (0-10) when VCO core is supplied at 3.3 V
0000 to 1111: (0-15) when VCO core is supplied at 4.5/5 V

[14] PLL_MUX_DIV: PLL MUX setting; select the desired signal path from VCO to the N Divider (VCO divider in the PLL feedback path):
0: VCO direct to N Divider (default)
1: VCO divided to N Divider (division ratio set by RF1_DIV_SEL in register ST1)

[13:12] CP_SUPPLY_MODE: Charge Pump supply mode settings; value to be set according to the supply used for charge pump core circuit (pin #16)
00: (0) 4.5V to 5.0 V
01: (1) 3.3 V
10: (2) 2.6 V
11: (3) Reserved

[11] KVCO_COMP_DIS: disable KVCO compensation circuit
0: compensation enabled (default - CP current auto-adjusted to compensate K_{VCO} variation)
1: compensation disabled (CP current fixed by CP_SEL settings)

[10] PFD_POL: set PFD polarity
0: standard mode (default)
1: “inverted” mode (to be used only with active inverting loop filter or with VCO with negative tuning characteristics)

[9:8] REF_BUFF_MODE: set Reference Clock buffer mode
00: (0) Reserved
01: (1) Differential Mode (Ref. clock signal on pin #20 and #21)
10: (2) XTAL Mode (Xtal osc. enabled with Crystal connected on pin #20 and #21)
11: (3) Single Ended Mode (Ref. clock signal on pin #21)

[7] MUTE_LOCK_EN: enables mute function
0: “mute on unlock” function disabled
1: “mute on unlock” function enabled (RF output stages are put OFF when PLL is unlocked)

[6] LD_ACTIVELOW: set low state as lock indicator
0: set lock indicator active high (LD=0 means PLL unlocked; LD=1 means PLL locked)
1: set lock indicator active low (LD=0 means PLL locked; LD=1 means PLL unlocked)

[5:3] LD_PREC: set Lock Detector precision
000: (0) 2 ns (default for Integer Mode)
001: (1) 4 ns (default for Fractional Mode)
010: (2) 6 ns
011: (3) 8 ns
100: (4) 10 ns
101: (5) 12 ns
110: (6) 14 ns
111: (7) 16 ns

[2:0] LD_COUNT: set Lock Detector counter for lock condition
000: (0) 4
001: (1) 8 (default for F_{PFD} ~1MHz in Integer Mode)
010: (2) 16
011: (3) 64
100: (4) 256
101: (5) 1024 (default for F_{PFD} ~50MHz in both Fractional/Integer Mode)
110: (6) 2048
111: (7) 4096

ST5 Register

26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED												VCO_BUFF_LP	VCO_MUX_LP	RF_DIV2_LP	RF_DIV4_LP	RF_DIV8_LP	RF_DIV16_LP	RF_DIV32_LP	RF_DIV64_LP	RF_DIV_MUXOUT_LP	RESERVED	PLL_MUX_LP	RESERVED	REF_BUFF_LP
RW	RW	RW												RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: STW81200BaseAddress + 0x05

Type: R/W

Description: Low power mode control bit

[26] RESERVED: must be set to ‘0’

[25] RESERVED: must be set to ‘0’

[24:13] RESERVED: must be set to ‘0’

[12] VCO_BUFF_LP: VCO Buffer low power mode (0=full power; 1=low power)

[11] VCO_MUX_LP: VCO MUX low power mode (0=full power; 1=low power)

[10] RF_DIV2_LP: RF Div. by 2 low power mode (0=full power; 1=low power)

[9] RF_DIV4_LP: RF Div. by 4 low power mode (0=full power; 1=low power)

[8] RF_DIV8_LP: RF Div. by 8 low power mode (0=full power; 1=low power)

[7] RF_DIV16_LP: RF Div. by 16 low power mode (0=full power; 1=low power)

[6] RF_DIV32_LP: RF Div. by 32 low power mode (0=full power; 1=low power)

[5] RF_DIV64_LP: RF Div. by 64 low power mode (0=full power; 1=low power)

[4] RF_DIV_MUXOUT_LP: RF Div. MUX low power mode (0=full power; 1=low power)

[3] RESERVED: must be set to ‘0’

[2] PLL_MUX_LP: MUX PLL low power mode (0=full power; 1=low power)

[1] RESERVED: must be set to ‘0’

[0] REF_BUFF_LP: Ref. Buffer low power mode (0=full power; 1=low power)

ST6 Register

26	25	24	23 22	21	20	19 18	17 16 15 14 13	12	11 10	9	8 7 6 5 4 3 2 1 0
DITHERING	CP_UP_OFF	CP_DN_OFF	DSM_ORDER[1:0]	DSM_CLK_DISABLE	MAN_CALB_EN	VCO_SEL[1:0]	VCO_WORD[4:0]	CAL_TEMP_COMP	PRCHG_DEL[1:0]	CAL_ACC_EN	CAL_DIV[8:0]
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: STW81200BaseAddress + 0x06

Type: R/W

Description: VCO Calibrator, Manual VCO control, DSM settings

[26] DITHERING: at ‘1’ enables dithering of DSM output sequence

[25] CP_UP_OFF: for test purposes only; must be set to ‘0’

[24] CP_DN_OFF: for test purposes only; must be set to ‘0’

[23:22] DSM_ORDER: set the order of Delta-Sigma Modulator
00: (0) 3rd order DSM (recommended)
01: (1) 2nd order DSM
10: (2) 1st order DSM
11: (3) 4th order DSM

[21] DSM_CLK_DISABLE: for test purposes only ; must be set to ‘0’

[20] MAN_CALB_EN: enables manual VCO calibrator mode
0: automatic VCO calibration (VCO_SEL, VCO_WORD settings are ignored)
1: manual VCO calibration (VCO_SEL, VCO_WORD settings are used)

[19:18] VCO_SEL: VCO selection bit
00: (0) VCO_HIGH
01: (1) VCO_LOW
10: (2) VCO_MID
11: (3) VCO_LOW

[17:13] VCO_WORD: select specific VCO sub-band (range:0 to 31)

[12] CAL_TEMP_COMP: at ‘1’ enables temperature compensation for VCO calibration procedure (to be used when PLL Lock condition is required on extremes thermal cycles)

[11:10] PRCHG_DEL: set the number of calibration slots for pre-charge of VCTRL node at the Voltage reference value used during VCO calibration procedure
00: (0) 1 slot (default)
01: (1) 2 slots
10: (2) 3 slots
11: (3) 4 slots

[9] CAL_ACC_EN: at ‘1’ increase calibrator accuracy by removing residual error taking 2 additional calibration slots (default = ‘0’)

[8:0] CAL_DIV: Set Calibrator Clock divider ratio (Range:1 to 511); ‘0’ set the maximum ratio (‘511’)

ST7 Register

26	25	24	23	22-21	20	19	18	17-13	12-0
RESERVED	LD_SDO_tristate	LD_SDO_MODE	SPI_DATA_OUT_DISABLE	LD_SDO_SEL[1:0]	REGDIG_OCP_DIS	CYCLE_SLIP_EN	FSTLCK_EN	CP_SEL_FL[4:0]	FSTLCK_CNT[12:0]
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: STW81200BaseAddress + 0x07

Type: R/W

Description: Fast Lock control, LD_SDO settings

[26] RESERVED: must be set to '0'

[25] LD_SDO_tristate: at '1' put LD_SDO out pin in Tri-State mode

[24] LD_SDO_MODE: LD_SDO output interface mode selection
0: Open Drain mode (Level Range: 1.8V to 3.6V)
1: 2.5V CMOS output mode

[23] SPI_DATA_OUT_DISABLE: disable auto-switch of LD_SDO pin during SPI read mode
0: LD_SDO pin automatically switched to SPI data out line during SPI read mode
1: LD_SDO pin fixed to Lock detector indication (SPI read operation not possible)

[22:21] LD_SDO_SEL: LD_SDO Mux output selection bit
00: (0) Lock Detector (default)
01: (1) VCO Divider output (for test purposes only)
10: (2) Calibrator VCO Divider output (for test purposes only)
11: (3) Fast Lock clock output (for test purposes only)

[20] REGDIG_OCP_DIS: for test purposes only ; must be set to '0' (at '1' disable the over-current protection of Digital LDO Voltage Regulator)

[19] CYCLE_SLIP_EN: at '1' enables Cycle Slip feature

[18] FSTLCK_EN: at '1' enables Fast lock mode using pin #6 (PD_RF2/FL_SW)

[17:13] CP_SEL_FL: set the Charge Pump current during fast lock time slot (range:0 to 31)

[12:0] FSTLCK_CNT: Fast-Lock counter value (Range: 2 to 8191); set duration of fast-lock time slot as number of F_{PFD} cycles

ST8 Register

26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD_RF2_DISABLE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	REG_OCP_DIS	REG_DIG_PD	REG_DIG_VOUT[1:0]		RESERVED	REG_REF_PD	REG_REF_VOUT[1:0]		RESERVED	REG_RF_PD	REG_RF_VOUT[1:0]		RESERVED	REG_VCO_PD	REG_VCO_VOUT[1:0]		RESERVED	REG_VCO_4V5_PD	REG_VCO_4V5_VOUT[1:0]	
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW		RW	RW	RW		RW	RW	RW		RW	RW	RW	

Address: STW81200BaseAddress + 0x08

Type: R/W

Description: LDO Voltage Regulator settings

[26] PD_RF2_DISABLE: at ‘1’ disable the hardware power down function of the pin PD_RF2 (pin #6) thus allowing the pin PD_RF1 (pin #5) to control the power down status of both RF Output stages

[25] RESERVED: must be set to ‘0’

[24] RESERVED: must be set to ‘0’

[23] RESERVED: must be set to ‘0’

[22] RESERVED: must be set to ‘0’

[21] RESERVED: must be set to ‘0’

[20] RESERVED: must be set to ‘0’

[19] REG_OCP_DIS: for test purposes only ; must be set to ‘0’ (at ‘1’ disable the overcurrent protection of LDO Voltage Regulators except DIG regulator)

[18] REG_DIG_PD: DIGITAL Regulator power down; must be set to ‘0’

[17:16] REG_DIG_VOUT: DIGITAL Regulator output voltage set
00: (0) 2.6 V (Default)
01: (1) 2.3 V (for test purposes only)
10: (2) 2.4 V (for test purposes only)
11: (3) 2.5 V (for test purposes only)

[15] RESERVED: must be set to ‘0’

[14] REG_REF_PD: REFERENCE CLOCK Regulator power down; must be set to ‘0’

[13:12] REG_REF_VOUT: REFERENCE CLOCK Regulator output voltage set
00: (0) 2.6 V (default)
01: (1) 2.5 V (for test purposes only)
10: (2) 2.7 V (for test purposes only)
11: (3) 2.8 V (for test purposes only)

[11] RESERVED: must be set to ‘0’

[10] REG_RF_PD: RF Output section Regulator power down; must be set to ‘0’

[9:8] REG_RF_VOUT: RF Output section Regulator output voltage set
00: (0) 2.6 V (default)
01: (1) 2.5 V (for test purposes only)
10: (2) 2.7 V (for test purposes only)
11: (3) 2.8 V (for test purposes only)

[7] RESERVED: must be set to ‘0’

[6] REG_VCO_PD: VCO Bias&Control Regulator power down; must be set to ‘0’

[5:4] REG_VCO_VOUT: VCO Bias&Control Regulator output voltage set
00: (0) 2.6 V (default)
01: (1) 2.5 V (for test purposes only)
10: (2) 2.7 V (for test purposes only)
11: (3) 2.8 V (for test purposes only)

[3] RESERVED: must be set to ‘0’

[2] REG_VCO_4V5_PD: High Voltage Regulator power down(to be used to supply VCO core, RF output final stage and Charge Pump); must be set to ‘0’

[1:0] REG_VCO_4V5_VOUT: High Voltage Regulator output voltage set (to be used to supply VCO core, RF output final stage and Charge Pump output)
00: (0) 5.0 V (Require 5.4 V unregulated voltage line on pin# 36)
01: (1) 2.6 V (3.0-5.4 V unregulated voltage line Range allowed on pin#36)
10: (2) 3.3 V (3.6-5.4 V unregulated voltage line Range allowed on pin#36)
11: (3) 4.5 V (5.0-5.4 V unregulated voltage line Range allowed on pin#36)

ST9 Register

<table>
<tr><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="27">RESERVED</td></tr>
<tr><td colspan="27">RW</td></tr>
</table>

Address: STW81200BaseAddress + 0x09

Type: R/W

Description: Reserved (Test & Initialization bit)

[26:0] RESERVED: Test & Initialization bit; must be set to ‘0’

ST10 Register

26–18	17	16	15	14	13	12	11	10	9	8	7	6–5	4–0
RESERVED	REG_DIG_STARTUP	REG_REF_STARTUP	REG_RF_STARTUP	REG_VCO_STARTUP	REG_VCO_4V5_STARTUP	REG_DIG_OCP	REG_REF_OCP	REG_RF_OCP	REG_VCO_OCP	REG_VCO_4V5_OCP	LOCK_DET	VCO_SEL[1:0]	WORD[4:0]
R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: STW81200BaseAddress + 0x0A

Type: R

Description: VCO, Lock det. Status, LDO status

[26:18] RESERVED: fixed to ‘0’

[17] REG_DIG_STARTUP: DIGITAL regulator Ramp-Up indicator (‘1’ means correct start-up)

[16] REG_REF_STARTUP: REFERENCE CLOCK regulator Ramp-Up indicator (‘1’ means correct start-up)

[15] REG_RF_STARTUP: RF Output section regulator Ramp-Up indicator (‘1’ means correct start-up)

[14] REG_VCO_STARTUP: VCO Bias&Control regulator Ramp-Up indicator (‘1’ means correct start-up)

[13] REG_VCO_4V5_STARTUP: High Voltage regulator Ramp-Up indicator (‘1’ means correct start-up)

[12] REG_DIG_OCP: DIGITAL regulator over-current protection indicator (‘1’ means over-current detected)

[11] REG_REF_OCP: REFERENCE CLOCK regulator over-current protection indicator (‘1’ means over-current detected)

[10] REG_RF_OCP: RF Output section regulator over-current protection indicator (‘1’ means over-current detected)

[9] REG_VCO_OCP: VCO Bias&Control regulator over-current protection indicator (‘1’ means over-current detected)

[8] REG_VCO_4V5_OCP: High Voltage regulator over-current protection indicator (‘1’ means over-current detected)

[7] LOCK_DET: Lock detector status bit (‘1’ means PLL locked)

[6:5] VCO_SEL: VCO selected by Calibration algorithm
00: (0) VCO_HIGH
01: (1) VCO_LOW
10: (2) VCO_MID
11: (3) VCO_LOW

[4:0] WORD: specific VCO sub-band selected by Calibration algorithm (Range:0 to 31)

ST11 Register

26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device_ID																										
R																										

Address: STW81200BaseAddress + 0x0B

Type: R

Description: Device ID

[26:0] Device_ID: Device Identifier (0x000801C)

7.14 Power ON sequence

In order to guarantee the correct start-up of the internal circuitry after the power on, the following steps must be followed:

1. Power up the device (LDO supply pins: pin#9 #18, #28 and #36)
2. Once the voltages applied on the LDO supply pins are stable, wait 50 msec. (After this transient time, the LDOs are powered on with the regulated voltages available at pins #2, #8, #19, #27 and #29, while all other circuits are in power down mode)
3. Provide the reference clock signal
4. Implement the first programming sequence as follow:
   a) Program register ST9 (test & initialization) with all bit set to ‘0’
   b) Program all the remaining registers according to the desired configuration with following order: ST8, ST7, ST6, ST5, ST4, ST3, ST2, ST1, ST0
5. Check the PLL Lock status on pin LD_SDO (pin #26) and/or read all relevant information provided on registers ST10 and ST11

7.15 Example of Register programming

Setup conditions and requirements:

- Unregulated Supply voltage: 5.0 V
- Reference Clock: 122.88 MHz , single-ended, sine wave
- LO Frequency: 2646.96 MHz – exact freq. mode (VCO Frequency=5293.92 MHz)
- Output Power: +7 dBm (differential)
- Phase Noise requirements: full performance VCO; full performance Noise floor

Register configurations (Hex values including register address)

- ST9 = 0x48000000 (initialization; all bit set to ‘0’)
- ST8 = 0x40000003 (REG_4V5 = 4.5 V)
- ST7 = 0x39000000 (“fast lock” not used; LD_SDO pin configured as 2.5 V CMOS buffer)
- ST6 = 0x30001000 (DITHERING=0; DSM_ORDER=0 for 3rd order DSM; CAL_TEMP_COMP=1 to guarantee lock on extreme temperature drift)
- ST5 = 0x28000000 (low power modes not used)
- ST4 = 0x2387838D (lock detector setting for fractional mode and F_{PFD} =61.44 MHz; REF_BUF_MODE=3 for single-ended mode; VCO_AMP=15 for best VCO phase noise @4.5 V supply; RF_OUT_PWR=7 to have +7 dBm differential)
- ST3 = 0x18000002 (R=2 and REF_PATH_SEL=0 “direct” for F_{PFD}=61.44 MHz)
- ST2 = 0x13000080 (MOD=128; RF2_OUT_PD=1 for RF2 Output in power down)
- ST1 = 0x08200015 (FRAC=21; RF1_DIVSEL=1 set RF1 Output with VCO freq. Divided By 2)
- ST0 = 0x03E00056 (N_{INT}=86; CPSEL=31 for Icp=4.9 mA)

8 Application diagram

Figure 21. Application diagram

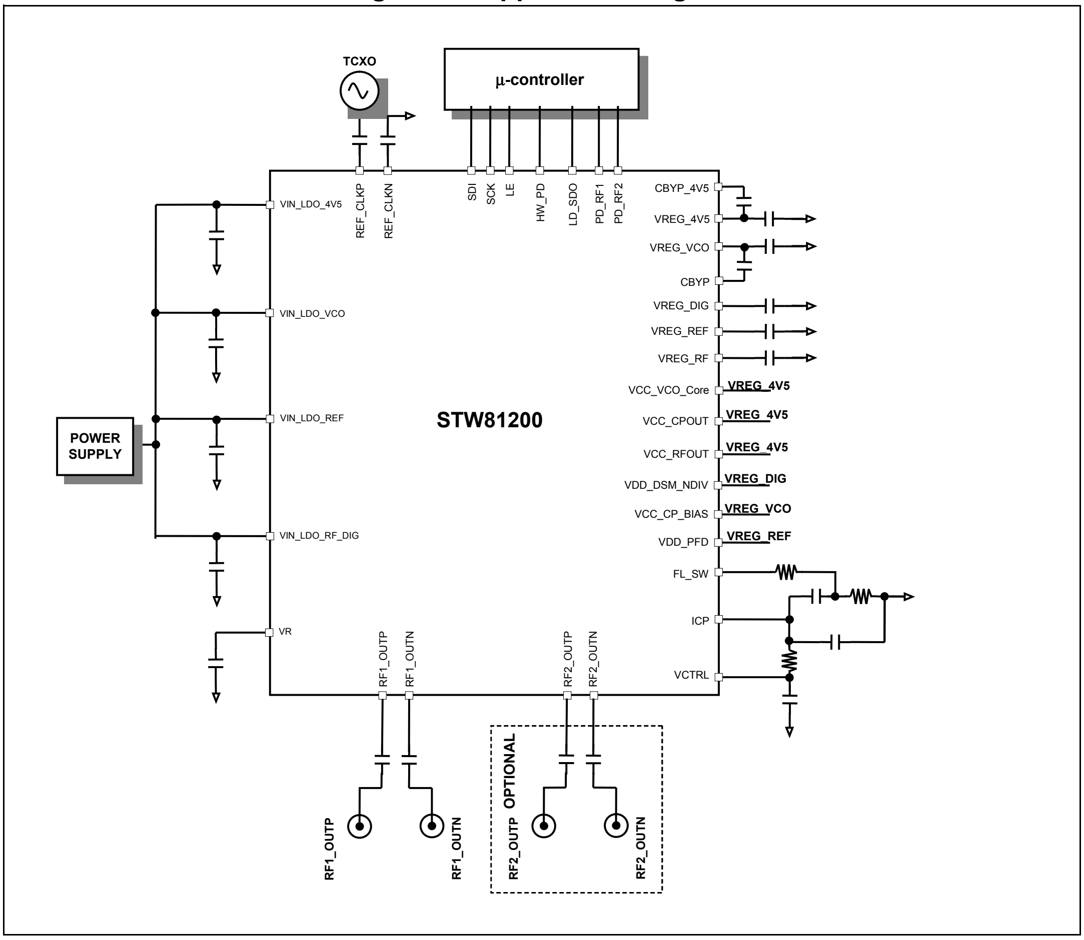
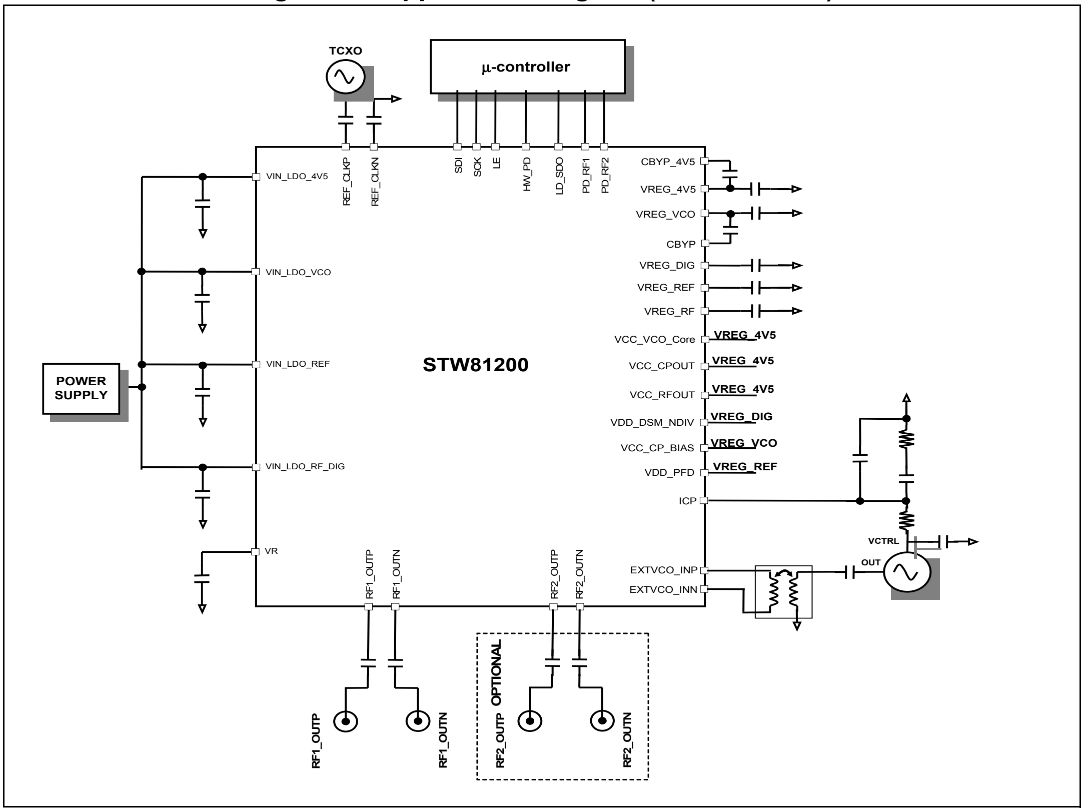


Figure 22. Application diagram (External VCO)



9 Package mechanical data

Figure 23. Package mechanical data

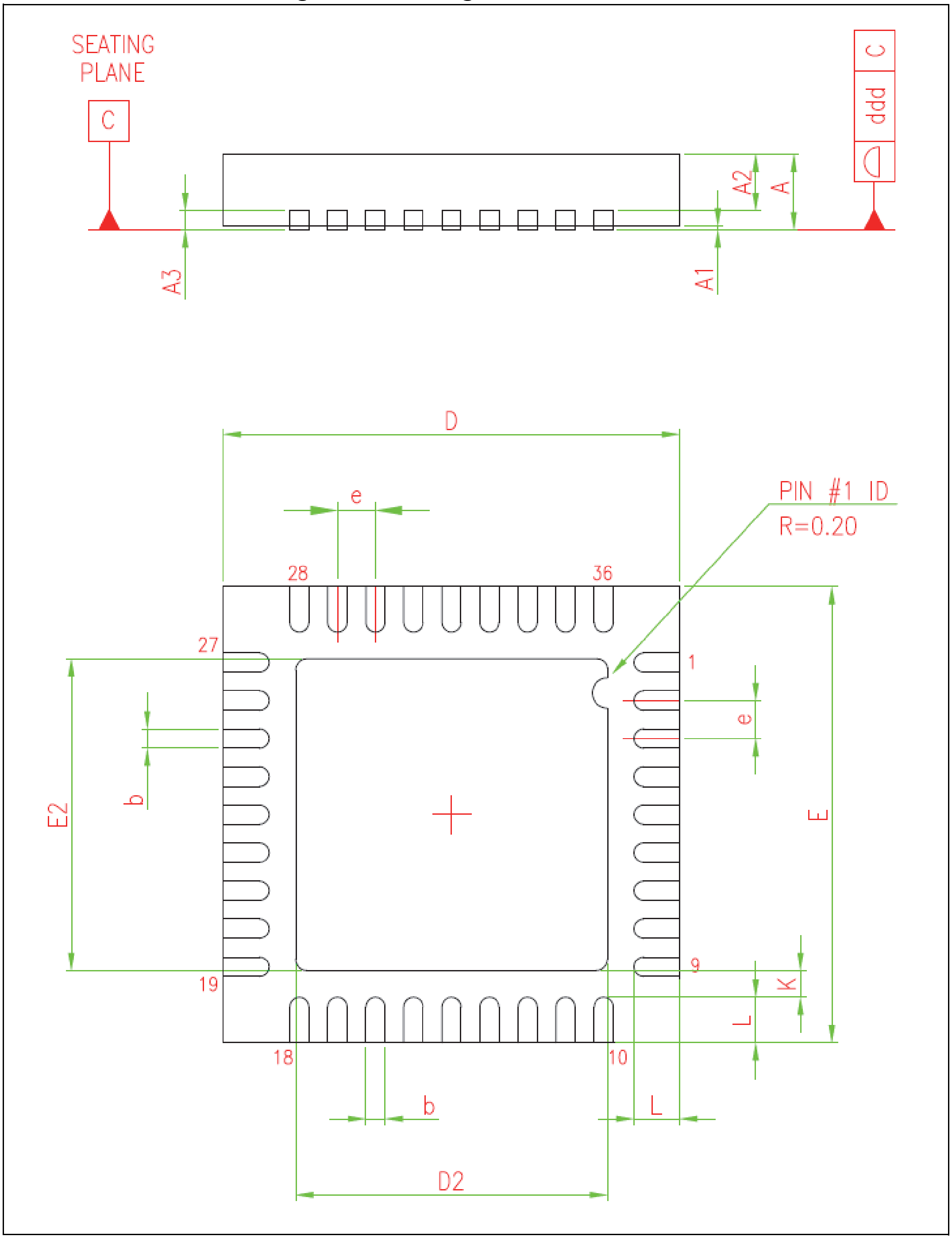


Table 12. Package dimensions

REF.	MIN.	TYP.	MAX.	NOTES
A	0.80	0.90	1.00	
A1		0.02	0.05	
A2		0.65	1.00	
A3		0.20		
b	0.18	0.23	0.30	
D	5.875	6.00	6.125	
D2	1.75	3.70	4.25	
E	5.875	6.00	6.125	
E2	1.75	3.70	4.25	
e	0.45	0.50	0.55	
L	0.35	0.55	0.75	
K	0.25			
ddd			0.08	

1. VFQFNP stands for Thermally Enhanced Very thin Fine pitch Quad Flat Package No lead. Very thin: A=1.00 Max.
2. Details of terminal 1 identifier are optional but must be located on the top surface of the package by using either a mold or marked features.

10 ECOPACK®

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Revision history

Table 13. Document revision history

Date	Revision	Changes
21-Feb-2014	1	Initial release.
07-Apr-2014	2	Removed ‘Confidential’ banners

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