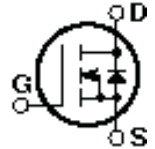


Super Junction MOSFET



- Ultra low $R_{DS(ON)}$
- Low Miller Capacitance
- Ultra Low Gate Charge, Q_g
- Avalanche Energy Rated
- TO-247 Package

MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT11N80BC3	UNIT
V_{DSS}	Drain-Source Voltage	800	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	11	Amps
I_{DM}	Pulsed Drain Current ^①	33	
V_{GS}	Gate-Source Voltage Continuous	± 20	Volts
V_{GSM}	Gate-Source Voltage Transient	± 30	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	156	Watts
	Linear Derating Factor	1.25	W/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	260	
$\frac{dv}{dt}$	Drain-Source Voltage slope ($V_{DS} = 640\text{V}$, $I_D = 11\text{A}$, $T_J = 125^\circ\text{C}$)	50	V/ns
I_{AR}	Repetitive Avalanche Current ^⑦	11	Amps
E_{AR}	Repetitive Avalanche Energy ^⑦	0.2	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	470	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$)	800			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10\text{V}$, $I_D = 7.1\text{A}$)		0.39	0.45	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}$, $V_{GS} = 0\text{V}$)		0.5	20	μA
	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}$, $V_{GS} = 0\text{V}$, $T_J = 150^\circ\text{C}$)			200	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 680\mu\text{A}$)	2.1	3	3.9	Volts

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DYNAMIC CHARACTERISTICS

APT11N80BC3

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = 25V f = 1 MHz		1585		pF
C _{oss}	Output Capacitance			770		
C _{rss}	Reverse Transfer Capacitance			18		
Q _g	Total Gate Charge ^④	V _{GS} = 10V V _{DD} = 400V I _D = 11A @ 25°C		60		nC
Q _{gs}	Gate-Source Charge			8		
Q _{gd}	Gate-Drain ("Miller") Charge			30		
t _{d(on)}	Turn-on Delay Time	RESISTIVE SWITCHING V _{GS} = 10V V _{DD} = 400V I _D = 11A @ 25°C R _G = 7.5Ω		25		ns
t _r	Rise Time			15		
t _{d(off)}	Turn-off Delay Time			70	80	
t _f	Fall Time			7	10	
E _{on}	Turn-on Switching Energy ^⑥	INDUCTIVE SWITCHING @ 25°C V _{DD} = 533V, V _{GS} = 15V I _D = 11A, R _G = 5Ω		165		μJ
E _{off}	Turn-off Switching Energy			50		
E _{on}	Turn-on Switching Energy ^⑥	INDUCTIVE SWITCHING @ 125°C V _{DD} = 533V, V _{GS} = 15V I _D = 11A, R _G = 5Ω		305		
E _{off}	Turn-off Switching Energy			65		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I _S	Continuous Source Current (Body Diode)			11	Amps
I _{SM}	Pulsed Source Current ^① (Body Diode)			33	
V _{SD}	Diode Forward Voltage ^② (V _{GS} = 0V, I _S = -11A)		1	1.2	Volts
t _{rr}	Reverse Recovery Time (I _S = 11A, di _S /dt = -100A/μs, V _R = 640V)		550		ns
Q _{rr}	Reverse Recovery Charge (I _S = 11A, di _S /dt = -100A/μs, V _R = 640V)		10		μC
dv _{dt}	Peak Diode Recovery dv _{dt} ^③			6	V/ns

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R _{θJC}	Junction to Case			0.80	°C/W
R _{θJA}	Junction to Ambient			62	

① Repetitive avalanche causes additional power losses that can be calculated as P_{AV} = E_{AR} * f

② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting T_J = +25°C, L = 194mH, R_G = 25Ω, Peak I_L = 2.2A

⑤ dv_{dt} numbers reflect the limitations of the test circuit rather than the device itself. I_S ≤ -I_D 11A di_S/dt ≤ 700A/μs V_R ≤ V_{DSS} T_J ≤ 150°C

⑥ Eon includes diode reverse recovery. See figures 18, 20.

⑦ Repetitive avalanche causes additional power losses that can be calculated as P_{AV} = E_{AR} * f

APT Reserves the right to change, without notice, the specifications and information contained herein.

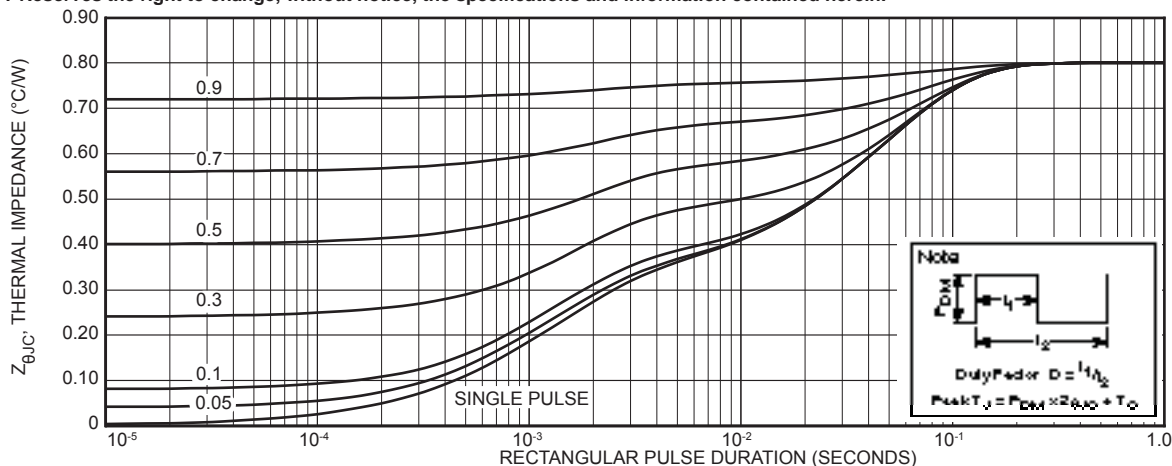


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

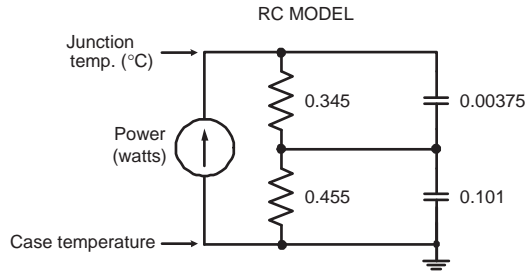


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

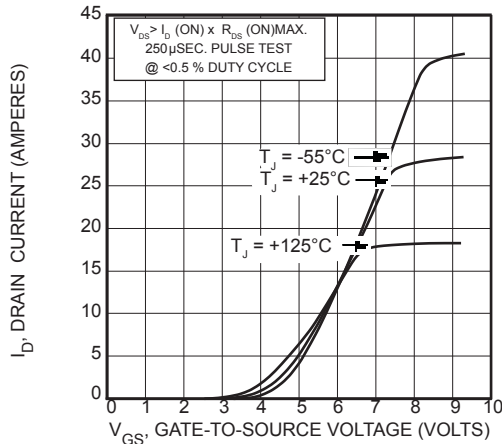


FIGURE 4, TRANSFER CHARACTERISTICS

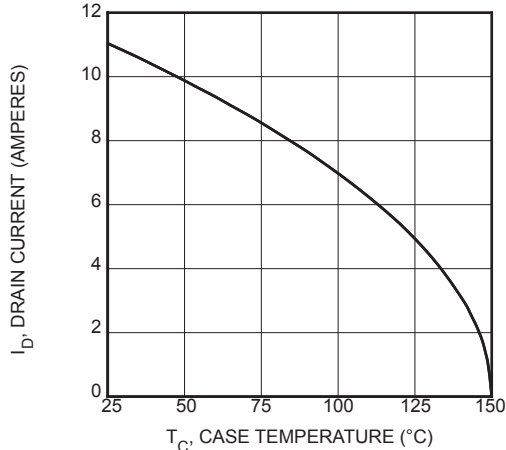


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

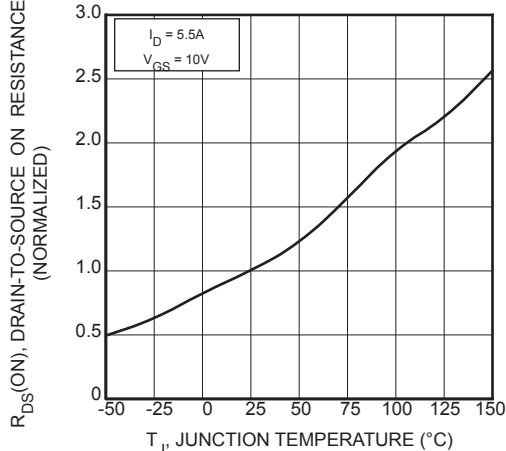


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

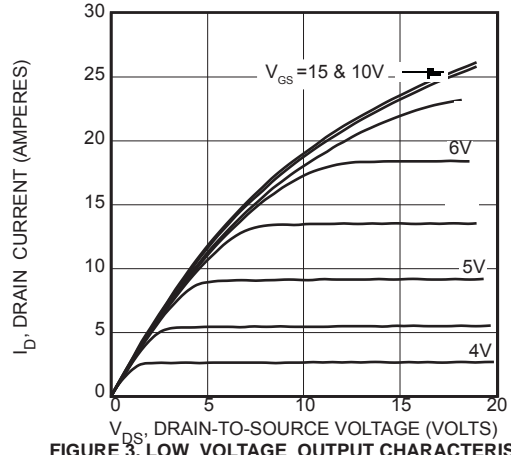


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

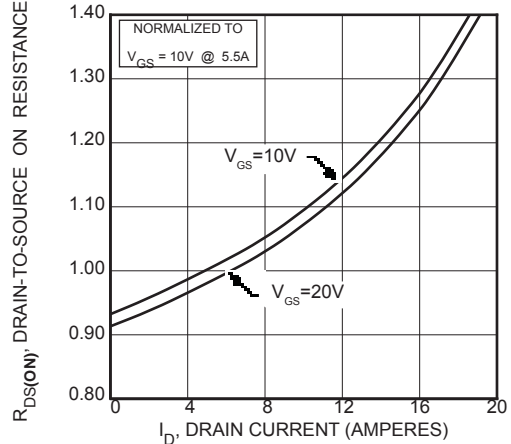


FIGURE 5, $R_{DS(\text{ON})}$ vs DRAIN CURRENT

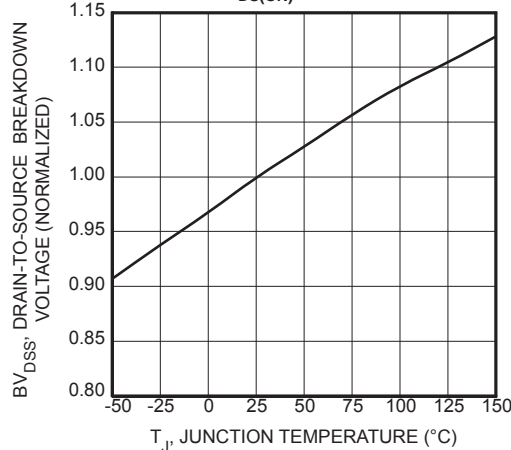


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

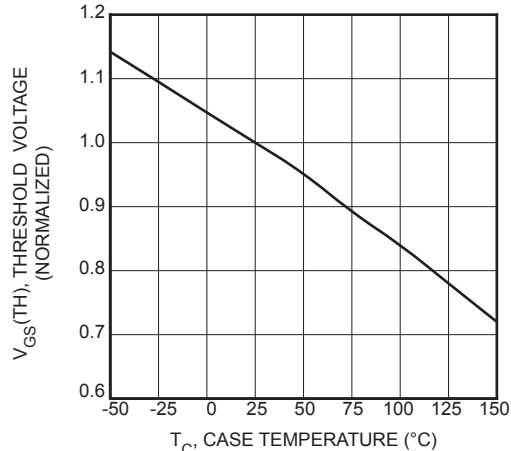


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

Typical Performance

APT11N80BC3

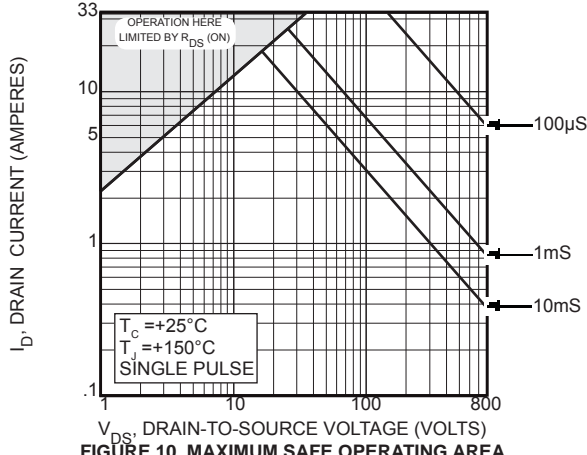


FIGURE 10, MAXIMUM SAFE OPERATING AREA

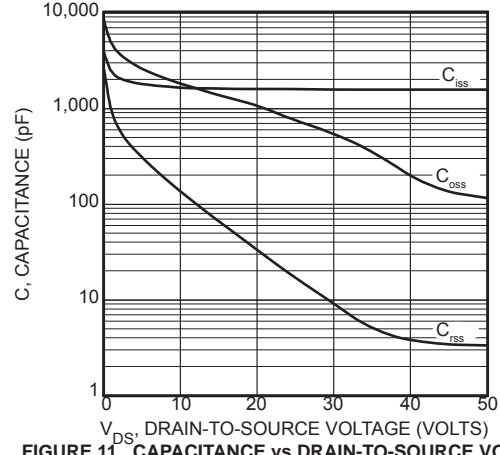


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

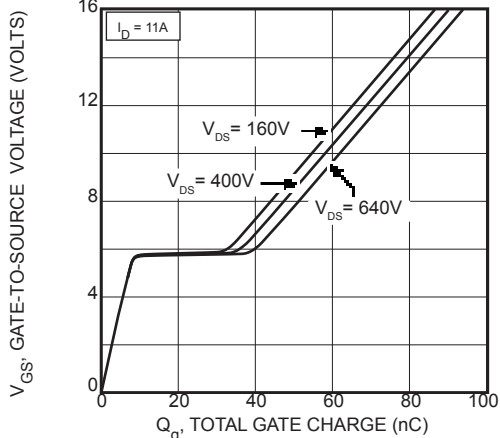


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

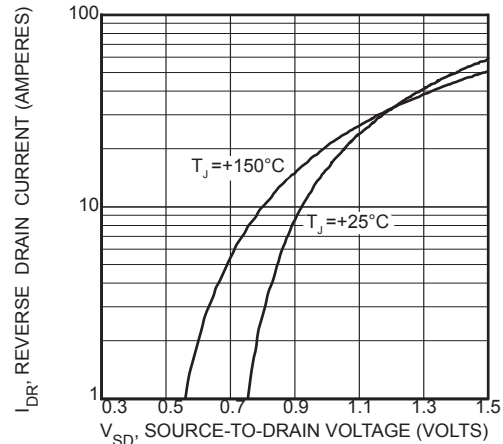


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

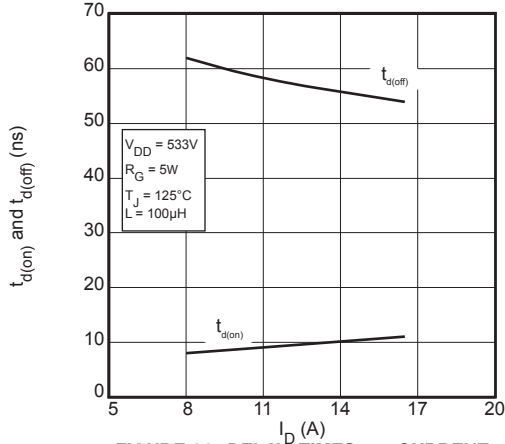


FIGURE 14, DELAY TIMES vs CURRENT

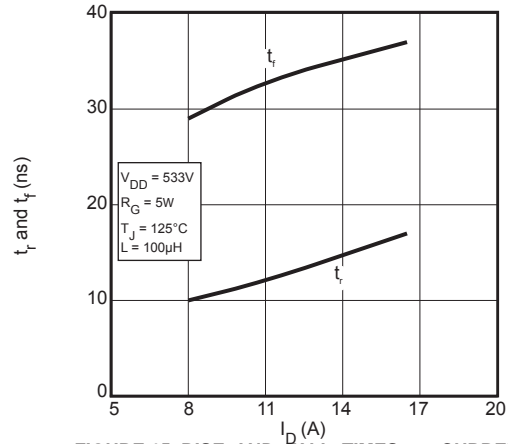


FIGURE 15, RISE AND FALL TIMES vs CURRENT

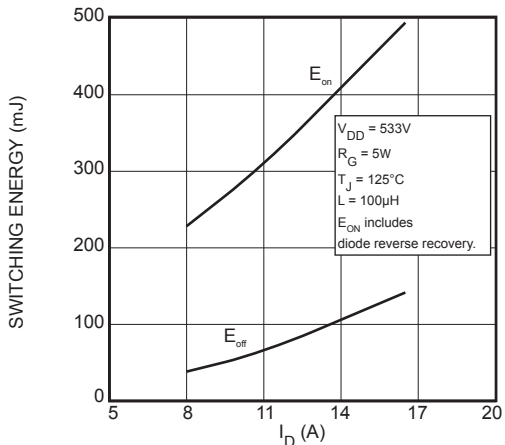


FIGURE 16, SWITCHING ENERGY vs CURRENT

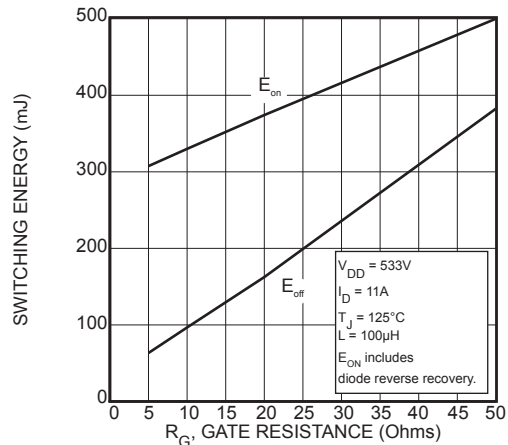


FIGURE 17, SWITCHING ENERGY vs. GATE RESISTANCE

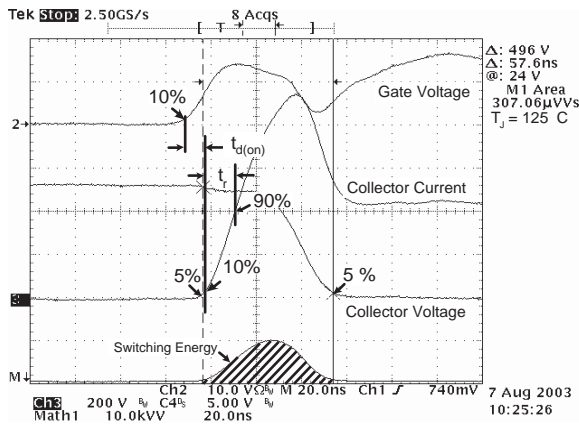


Figure 18, Turn-on Switching Waveforms and Definitions

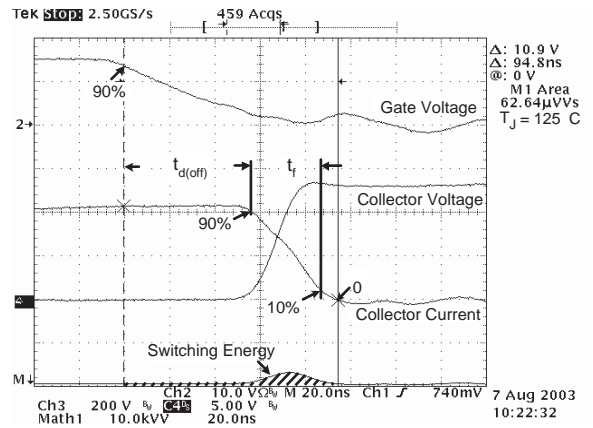


Figure 19, Turn-off Switching Waveforms and Definitions

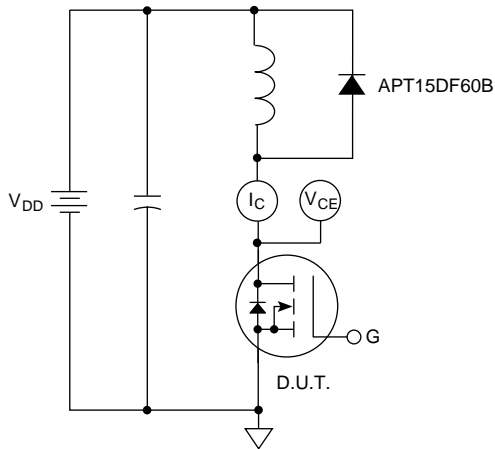


Figure 20, Inductive Switching Test Circuit

TO-247 Package Outline

