Elektronische Bauelemente

# SST2611B

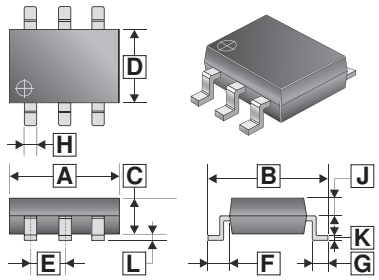
**-2.4A , -60V , $R_{DS(ON)}$ 175 mΩ**
**P-Channel Enhancement Mode MOSFET**

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

## DESCRIPTION

SST2611B utilized advanced processing techniques to achieve the lowest possible on-resistance, extremely efficient and cost-effectiveness device. The SOT-26 package is universally used for all commercial-industrial applications.

**SOT-26**

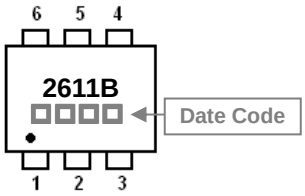



| REF. | Millimeter | | REF. | Millimeter | |
|---|---|---|---|---|---|
| | Min. | Max. | | Min. | Max. |
| A | 2.70 | 3.10 | G | 0.37 REF. | |
| B | 2.60 | 3.00 | H | 0.30 | 0.55 |
| C | 1.20 REF. | | J | - | - |
| D | 1.40 | 1.80 | K | 0.12 REF. | |
| E | 0.95 REF. | | L | - | 0.10 |
| F | 0.60 REF. | | | | |

## FEATURES

- Simple Drive Requirement
- Smaller Outline Package
- Surface mount package

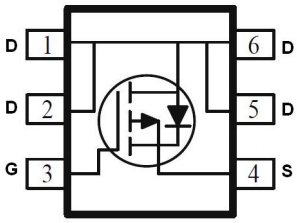
## MARKING




## PACKAGE INFORMATION

| Package | MPQ | Leader Size |
|---|---|---|
| SOT-26 | 3K | 7 inch |

**TOP VIEW**




## ABSOLUTE MAXIMUM RATINGS ($T_J$=25℃ unless otherwise specified)

| Parameter | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -60 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current @ $V_{GS}$=10V [1] | $T_A$=25℃ | $I_D$ | -2.4 | A |
| | $T_A$=70℃ | | -1.7 | |
| Pulsed Drain Current [2] | | $I_{DM}$ | -4.5 | A |
| Power Dissipation [3] | $T_A$=25℃ | $P_D$ | 1.1 | W |
| Linear Derating Factor | | | 0.009 | W / ℃ |
| Operating Junction and Storage Temperature Range | | $T_j$, $T_{stg}$ | -55~150 | ℃ |
| **Thermal Resistance Rating** | | | | |
| Maximum Junction to Ambient [1] | | $R_{\theta JA}$ | 110 | ℃ / W |

## ELECTRICAL CHARACTERISTICS ($T_J$=25°C unless otherwise specified)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit | Teat Conditions |
|---|---|---|---|---|---|---|---|
| **Static** | | | | | | | |
| Drain-Source Breakdown Voltage | | $BV_{DSS}$ | -60 | - | - | V | $V_{GS}$=0, $I_D$= -250uA |
| Gate-Threshold Voltage | | $V_{GS(th)}$ | -1 | - | -3 | V | $V_{DS}$=$V_{GS}$, $I_D$= -250uA |
| Gate-Body Leakage Current | | $I_{GSS}$ | - | - | ±100 | nA | $V_{GS}$=±20V |
| Drain-Source Leakage Current | $T_J$=25°C | $I_{DSS}$ | - | - | -1 | μA | $V_{DS}$= -48V, $V_{GS}$=0 |
| | $T_J$=55°C | | - | - | -5 | | |
| Drain-Source On-Resistance [2] | | $R_{DS(ON)}$ | - | - | 175 | mΩ | $V_{GS}$= -10V, $I_D$= -2A |
| | | | - | - | 220 | | $V_{GS}$= -4.5V, $I_D$= -1A |
| Forward Transconductance | | $g_{fs}$ | - | 5.8 | - | S | $V_{DS}$= -10V, $I_D$= -2A |
| **Dynamic** | | | | | | | |
| Total Gate Charge[2] | | $Q_g$ | - | 4.59 | - | nC | $V_{DS}$= -20V, $V_{GS}$= -4.5V, $I_D$= -2A |
| Gate-Source Charge | | $Q_{gs}$ | - | 1.39 | - | | |
| Gate-Drain Charge | | $Q_{gd}$ | - | 1.62 | - | | |
| Turn-on Delay Time[2] | | $T_{d(on)}$ | - | 17.4 | - | nS | $V_{DS}$= -15V, $V_{GS}$= -10V, $R_G$=3.3Ω, $I_D$= -1A |
| Rise Time | | $T_r$ | - | 5.4 | - | | |
| Turn-off Delay Time | | $T_{d(off)}$ | - | 37.2 | - | | |
| Fall Time | | $T_f$ | - | 2.4 | - | | |
| Input Capacitance | | $C_{iss}$ | - | 531 | - | pF | $V_{GS}$=0, $V_{DS}$= -15V, f=1.0MHz |
| Output Capacitance | | $C_{oss}$ | - | 59 | - | | |
| Reverse Transfer Capacitance | | $C_{rss}$ | - | 38 | - | | |
| **Source-Drain Diode** | | | | | | | |
| Diode Forward Voltage [2] | | $V_{SD}$ | - | - | -1.2 | V | $I_S$= -1A, $V_{GS}$=0 |
| Continuous Source Current [1,4] | | $I_S$ | - | - | -2.4 | A | $V_G$= $V_D$=0 |
| Pulsed Source Current [2,4] | | $I_{SM}$ | - | - | -4.5 | A | Force Current |

Notes:
1. Surface mounted on a 1 inch2 FR-4 board with 2OZ copper, 156℃/W when mounted on Min. copper pad.
2. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.
3. The power dissipation is limited by 150℃ junction temperature.
4. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

## CHARACTERISTIC CURVES

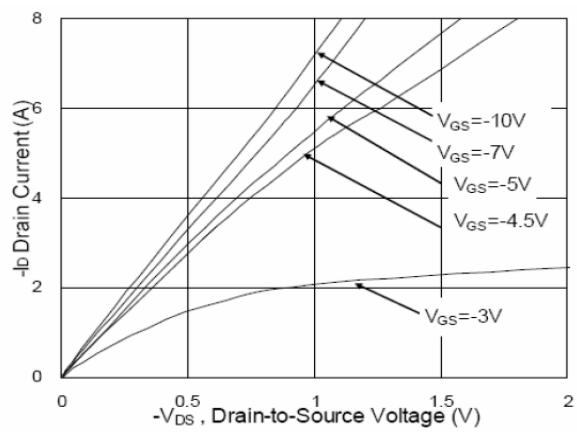



Fig.1 Typical Output Characteristics

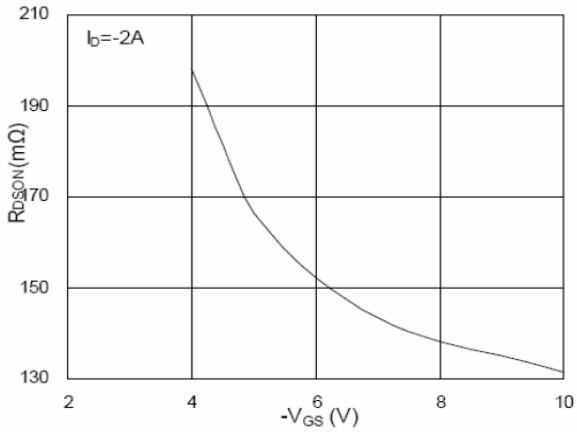



Fig.2 On-Resistance v.s Gate-Source

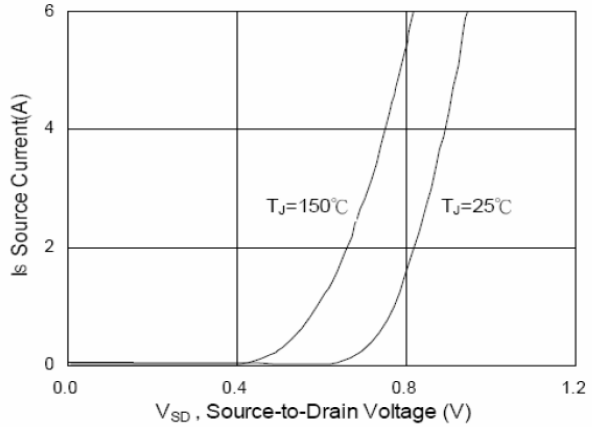



Fig.3 Forward Characteristics Of Reverse

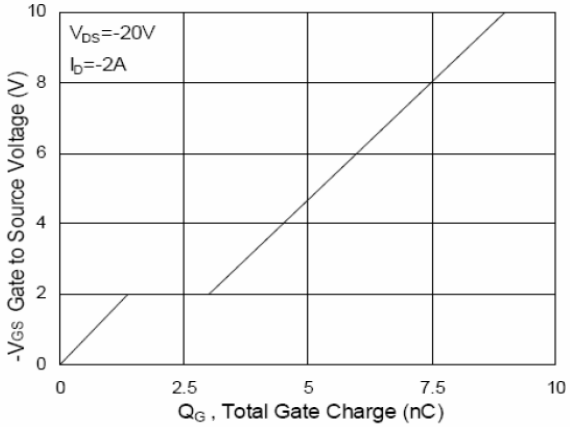



Fig.4 Gate-Charge Characteristics

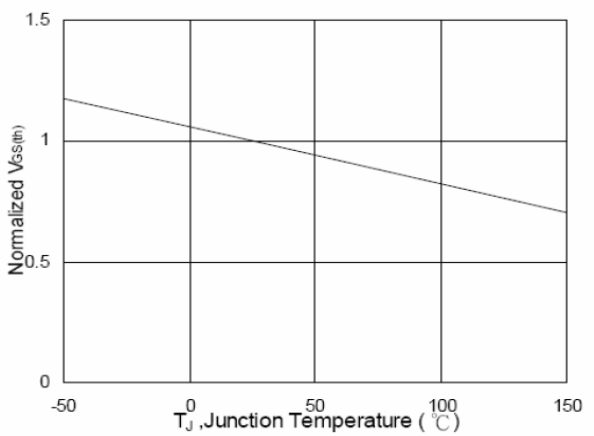



Fig.5 Normalized $V_{GS(th)}$ v.s $T_J$

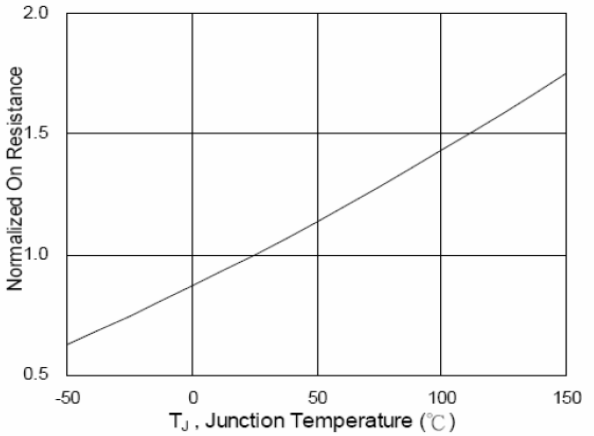



Fig.6 Normalized $R_{DSON}$ v.s $T_J$

## CHARACTERISTIC CURVES

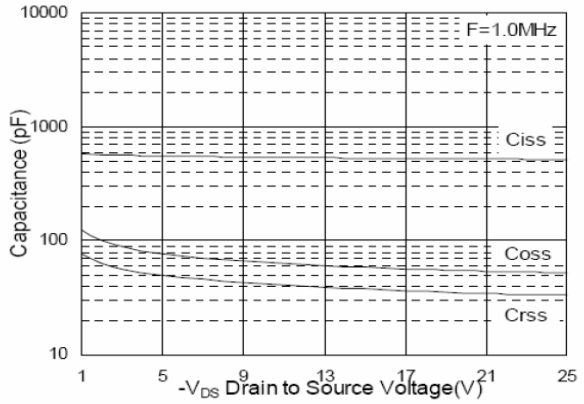



Fig.7 Capacitance

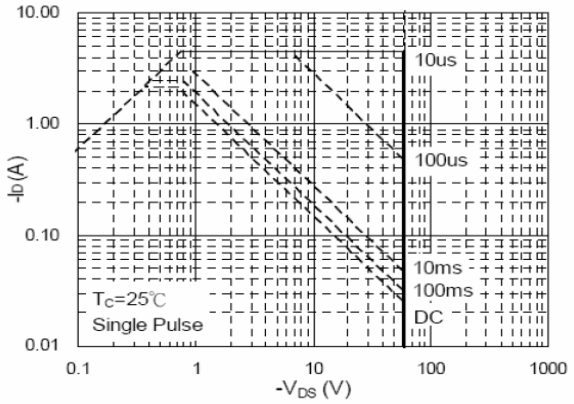



Fig.8 Safe Operating Area

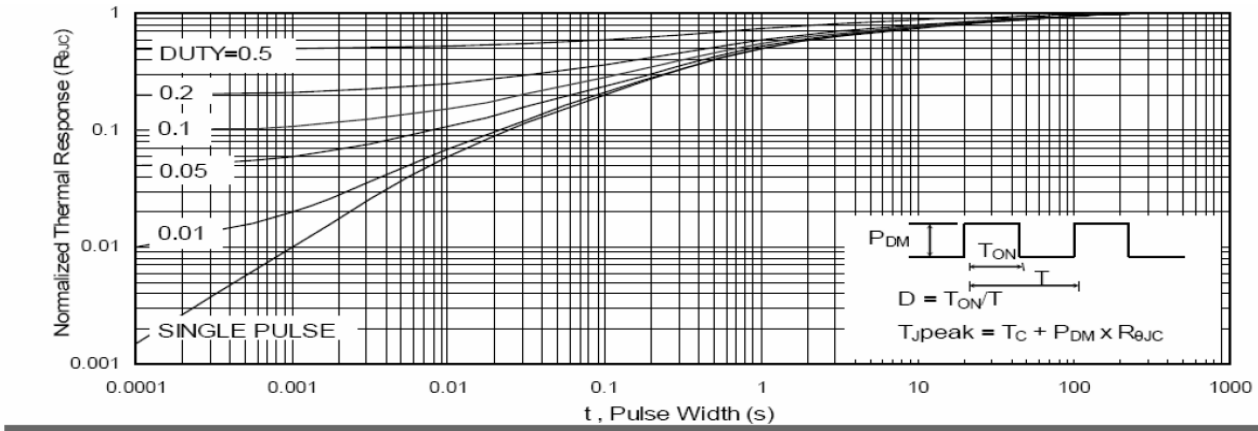



Fig.9 Normalized Maximum Transient Thermal Impedance

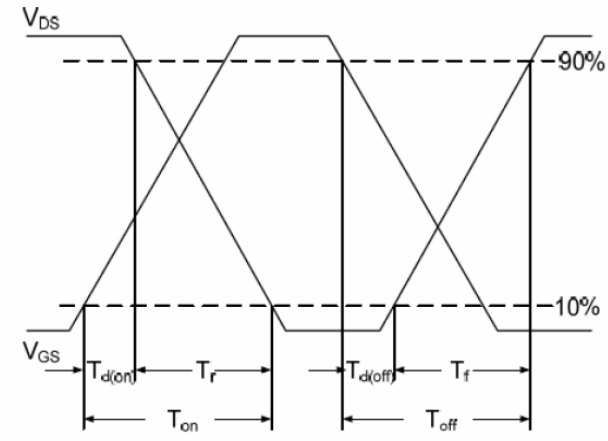



Fig.10 Switching Time Waveform

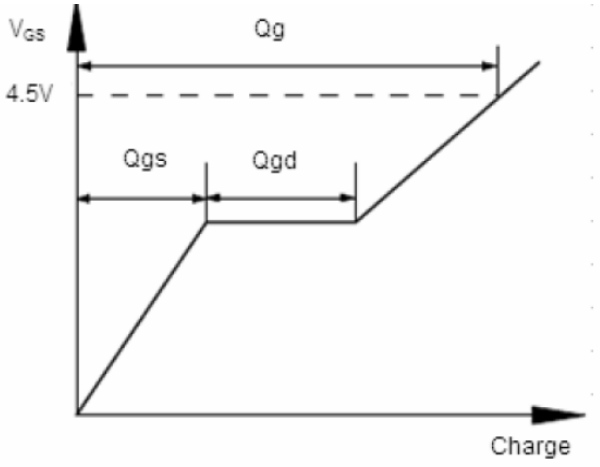



Fig.11 Gate Charge Waveform