BCM® in a VIA Package Bus Converter

BCM4414xD1E13A2yzz

Isolated Fixed-Ratio DC-DC Converter

Features & Benefits

- Up to 125A continuous low voltage side current
- Fixed transformation ratio (K) of 1/32
- Up to 711W/in^3 power density
- 97.1% peak ef ciency
- Built-in EMI ltering and inrush limiting circuit
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 4414 package
- High MTBF
- Thermally enhanced VIA package
- PMBus management interface
- Suitable for Hot-Swap applications

Typical Applications

- 380V_{DC} Power Distribution
- Information and Communication Technology (ICT) Equipment
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Energy Systems
- Transportation
- Green Buildings and Microgrids

Product Ratings	
V_{HI} = 384V (260 – 410V)	I_{LO} = up to 125A
V_{LO} = 12V (8.1 – 12.8V) (NO LOAD)	K = 1/32

Product Description

The BCM in a VIA package is a high efficiency Bus Converter, operating from a 260 to 410V_{DC} high voltage bus to deliver an isolated 8.1 to 12.8V_{DC} unregulated, low voltage.

This unique ultra-low profile module incorporates DC-DC conversion, integrated filtering and PMBus™ commands and controls in a chassis or PCB mount form factor.

The BCM offers low noise, fast transient response and industry leading efficiency and power density. A low voltage side referenced PMBus™ compatible telemetry and control interface provides access to the BCM's configuration, fault monitoring, and other telemetry functions.

Leveraging the thermal and density benefits of Vicor's VIA packaging technology, the BCM module offers flexible thermal management options with very low top and bottom side thermal impedances.

When combined with downstream Vicor DC-DC conversion components and regulators, the BCM allows the Power Design Engineer to employ a simple, low-profile design which will differentiate the end system without compromising on cost or performance metrics.

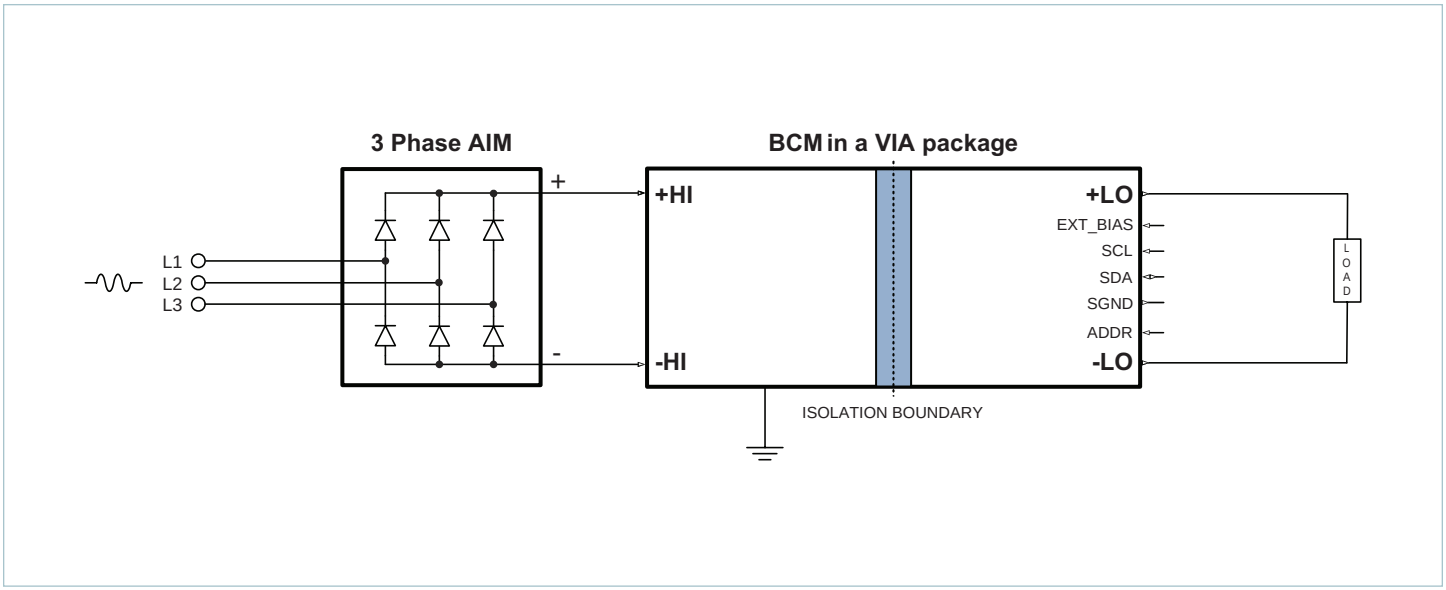
Size:
4.35 x 1.40 x 0.37 in
110.55 x 35.54 x 9.40mm

Part Ordering Information

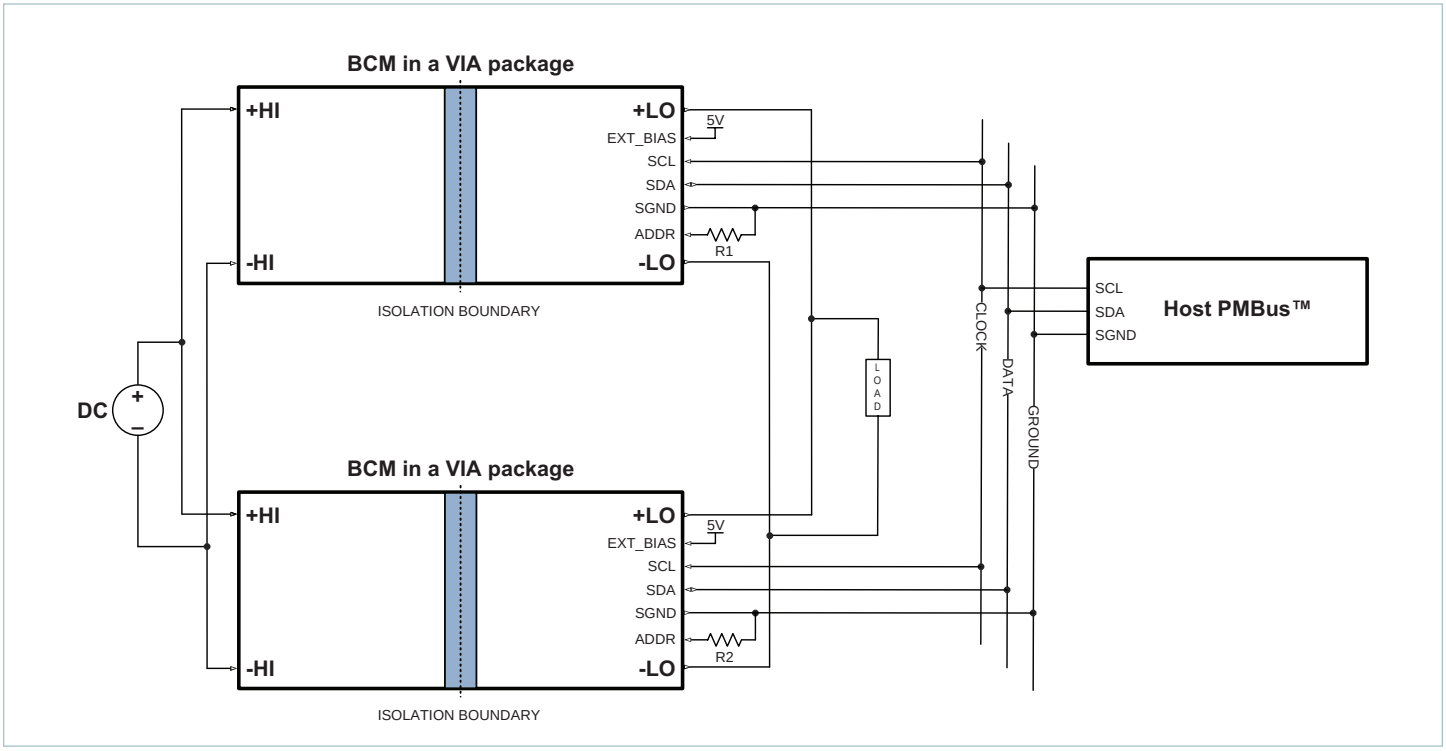
Product Function	Package Length	Package Width	Package Type	Max High Side Voltage	High Side Voltage Range Ratio	Max Low Side Voltage	Max Low Side Current	Product Grade (Case Temperature)	Option Field
BCM	44	14	x	D1	E	13	A2	y	zz
BCM = Bus Converter Module	Length in Inches x 10	Width in Inches x 10	B = Board VIA V = Chassis VIA	Internal Reference				C = -20 to 100°C[1] T = -40 to 100°C[1]	02 = Chassis/PMBus 06 = Short Pin/PMBus 10 = Long Pin/PMBus

[1] High temperature current derating may apply; See Figure 1, specified thermal operating area.

Typical Applications

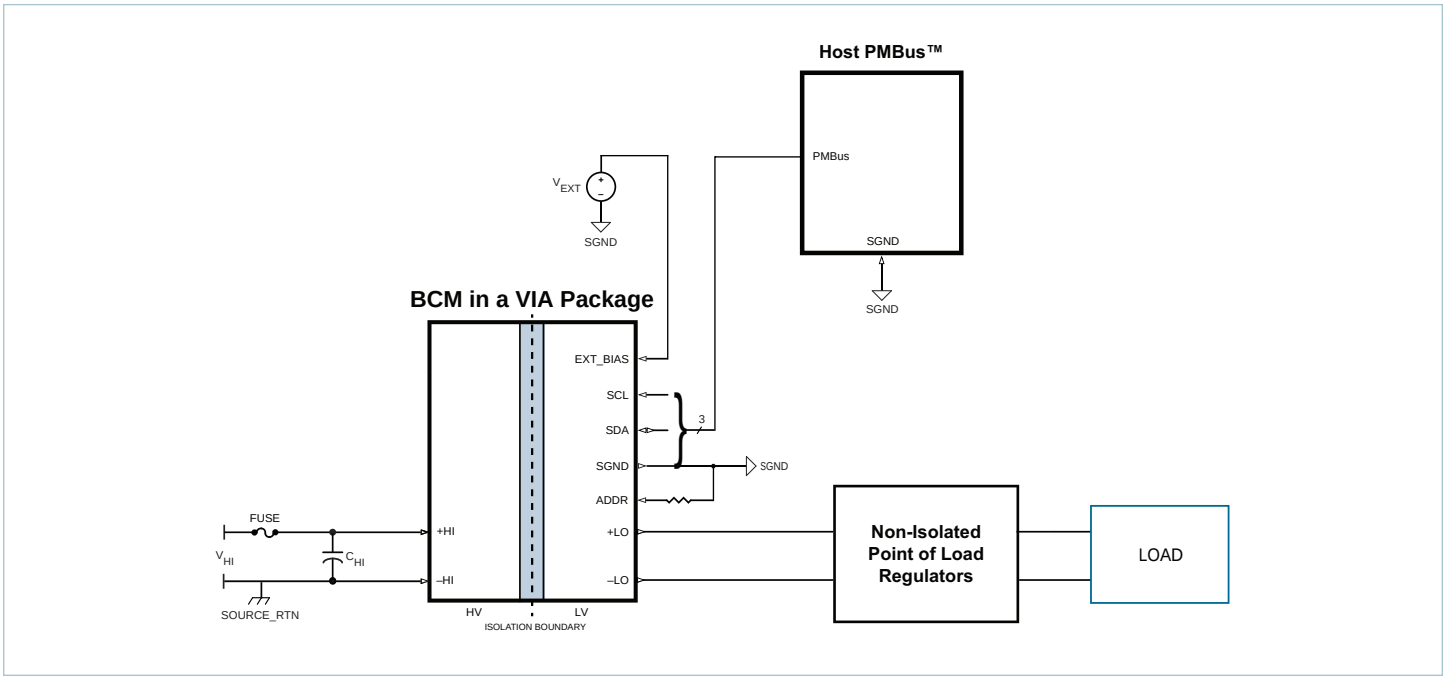


3 phase AC to point of load (3 phase AIM + BCM4414xD1E13A2yzz)

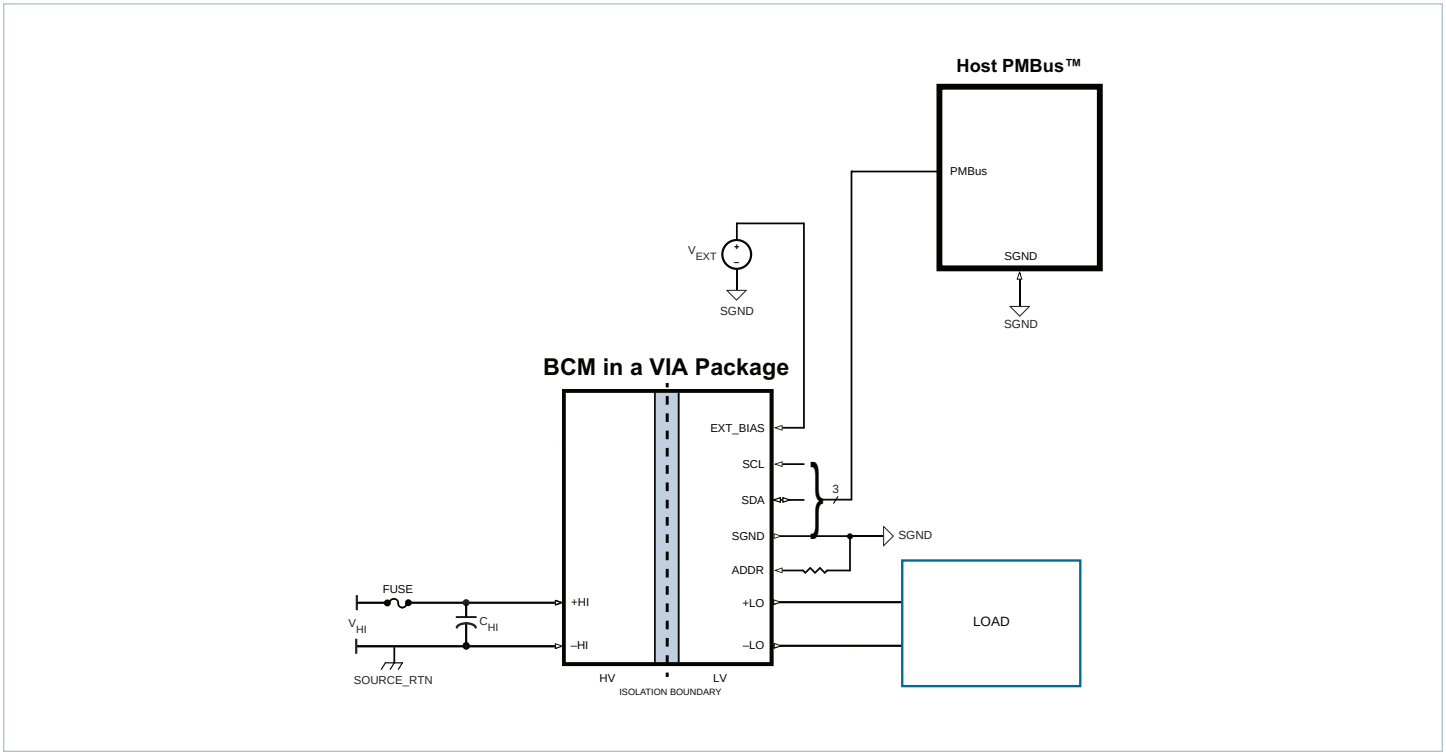


Paralleling BCM in a VIA package – connection to Host PMBus

Typical Applications (Cont.)

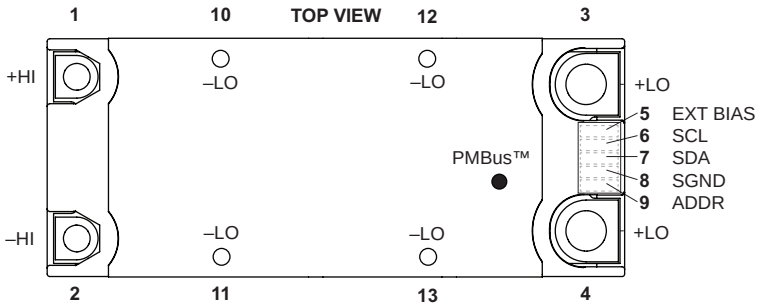


BCM4414xD1E13A2yzz at point of load – connection to Host PMBus

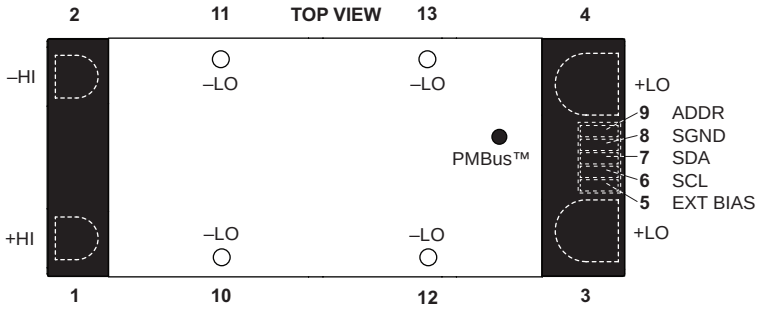


BCM4414xD1E13A2yzz direct to load – connection to Host PMBus

Pin Configuration



BCM in a 4414 VIA Package - Chassis (Lug) Mount



BCM in a 4414 VIA Package - Board (PCB) Mount

Note: The dot on the VIA housing indicates the location of the signal pin 9.

Pin Descriptions

Pin Number	Signal Name	Type	Function
1	+HI	HIGH SIDE POWER	High voltage side positive power terminal
2	–HI	HIGH SIDE POWER RETURN	High voltage side negative power terminal
3, 4	+LO	LOW SIDE POWER	Low voltage side positive power terminal
5	EXT BIAS	INPUT	5V supply input
6	SCL	INPUT	I^2C Clock, PMBus™ Compatible
7	SDA	INPUT/OUTPUT	I^2C Data, PMBus Compatible
8	SGND	LOW SIDE SIGNAL RETURN	Signal Ground
9	ADDR	INPUT	Address assignment - Resistor based
10, 11, 12, 13	–LO	LOW SIDE POWER RETURN	Low voltage side negative power terminal

Notes: All signal pins (5, 6, 7, 8, 9) are referenced to the low voltage side and isolated from the high voltage side.
Keep SGND signal separated from the low voltage side power return terminal (–LO) in electrical design.

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+HI to –HI		-1	480	V
HI_DC or LO_DC slew rate			N/A	V/µs
+LO to –LO		-1	15	V
EXT BIAS to SGND		-0.3	10	V
			0.15	A
SCL to SGND		-0.3	5.5	V
SDA to SGND		-0.3	5.5	V
ADDR to SGND		-0.3	3.6	V
Isolation Voltage / Dielectric Withstand	(High voltage side to case)	2121		V_{DC}
	Basic Insulation (High voltage side to low voltage side) [1]	2121		V_{DC}
	(Low voltage side to case)	N/A		V_{DC}

[1] The absolute maximum rating listed above for the Dielectric Withstand (high voltage side to the low voltage side) refers to the VIA package. The internal safety approved isolating component (ChiP) provides reinforced insulation (4242V) from the high voltage side to the low voltage side. However, the VIA package itself can only be tested at a basic insulation value (2121V).

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side)						
HI Side Voltage Range, Continuous	V_{HI_DC}		**260**		**410**	V
HI Side Voltage Range, Transient	V_{HI_TRANS}		**260**		**410**	V
HI Side Voltage Initialization Threshold	$V_{\mu C_ACTIVE}$	HI side voltage where internal controller is initialized, (powertrain inactive)			130	V
HI Side Quiescent Current	I_{HI_Q}	Disabled, V_{HI_DC} = 384V		2		mA
		T_{CASE} ≤ 100°C			4	
No Load Power Dissipation	P_{HI_NL}	V_{HI_DC} = 384V, T_{CASE} = 25°C		11	15	W
		V_{HI_DC} = 384V	**5.9**		**24**	
		V_{HI_DC} = 260V to 410V, T_{CASE} = 25 °C			16	
		V_{HI_DC} = 260V to 410V			**25**	
HI Side Inrush Current Peak	$I_{HI_INR_PK}$	V_{HI_DC} = 410V, C_{LO_EXT} = 1000µF, R_{LOAD_LO} = 25% of full load current		10		A
		T_{CASE} ≤ 100°C			15	
DC HI Side Current	$I_{HI_IN_DC}$	At $I_{LO_OUT_DC}$ = 125A, T_{CASE} ≤ 90°C			4.1	A
Transformation Ratio	K	High Voltage to Low Voltage, K = V_{LO_DC} / V_{HI_DC}, at no load		1/32		V/V
LO Side Current (continuous)	$I_{LO_OUT_DC}$	T_{CASE} ≤ 90°C			125	A
LO Side Current (pulsed)	$I_{LO_OUT_PULSE}$	2ms pulse, 25% duty cycle, $I_{LO_OUT_AVG}$ ≤ 50% rated $I_{LO_OUT_DC}$			167	A
Efficiency (ambient)	η_{AMB}	V_{HI_DC} = 384V, $I_{LO_OUT_DC}$ = 125A	96.2	97		%
		V_{HI_DC} = 260V to 410V, $I_{LO_OUT_DC}$ = 125A	95.2			
		V_{HI_DC} = 384V, $I_{LO_OUT_DC}$ = 62.5A	96.5	97.4		
Efficiency (hot)	η_{HOT}	V_{HI_DC} = 384V, $I_{LO_OUT_DC}$ = 125A, T_{CASE} = 85°C	95.8	97		%
Efficiency (over load range)	$\eta_{20\%}$	25A < $I_{LO_OUT_DC}$ < 125A	95			%
LO Side Output Resistance	R_{LO_COLD}	V_{HI_DC} = 384V, $I_{LO_OUT_DC}$ = 125A, T_{CASE} = -40°C	1.6	1.9	2.3	mΩ
	R_{LO_AMB}	V_{HI_DC} = 384V, $I_{LO_OUT_DC}$ = 125A	2.0	2.4	2.8	
	R_{LO_HOT}	V_{HI_DC} = 384V, $I_{LO_OUT_DC}$ = 125A, T_{CASE} = 85°C	2.5	2.8	3.2	
Switching Frequency	F_{SW}	LO side voltage ripple frequency = 2x F_{SW}	**0.95**	1.00	**1.05**	MHz
LO Side Voltage Ripple	$V_{LO_OUT_PP}$	C_{LO_EXT} = 0µF, $I_{LO_OUT_DC}$ = 125A, V_{HI_DC} = 384V, 20MHz BW		195		mV
		T_{CASE} ≤ 100°C			250	

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side) Cont.						
Effective HI Side Capacitance (Internal)	C_{HI_INT}	Effective Value at 384V_{HI_DC}		0.4		µF
Effective LO Side Capacitance (Internal)	C_{LO_INT}	Effective Value at 12V_{LO_DC}		238		µF
Rated LO Side Capacitance (External)	$C_{LO_OUT_EXT}$	Excessive capacitance may drive module into SC protection			**1000**	µF
Rated LO Side Capacitance (External), parallel array operation	$C_{LO_OUT_AEXT}$	$C_{LO_OUT_AEXT}$ Max = N * 0.5 * $C_{LO_OUT_EXT\ MAX}$, where N = the number of units in parallel				
Powertrain Hardware Protection Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side)						
• These built-in powertrain protections are fixed in hardware and cannot be configured through PMBus™. • When duplicated in supervisory limits, hardware protections serve a secondary role and become active when supervisory limits are disabled through PMBus.						
Auto Restart Time	$t_{AUTO_RESTART}$	Startup into a persistent fault condition. Non-latching fault detection given V_{HI_DC} > V_{HI_UVLO+}	**290**		**360**	ms
HI Side Overvoltage Lockout Threshold	V_{HI_OVLO+}		**430**	440	**450**	V
HI Side Overvoltage Recovery Threshold	V_{HI_OVLO-}		**410**	430	**440**	V
HI Side Overvoltage Lockout Hysteresis	$V_{HI_OVLO_HYST}$			10		V
HI Side Overvoltage Lockout Response Time	t_{HI_OVLO}			100		µs
HI Side Soft-Start Time	$t_{HI_SOFT-START}$	From powertrain active. Fast current limit protection disabled during soft-start		1		ms
LO Side Overcurrent Trip Threshold	$I_{LO_OUT_OCP}$		**135**	170	**210**	A
LO Side Overcurrent Response Time Constant	$t_{LO_OUT_OCP}$	Effective internal RC filter		3		ms
LO Side Short Circuit Protection Trip Threshold	$I_{LO_OUT_SCP}$		**187**			A
LO Side Short Circuit Protection Response Time	$t_{LO_OUT_SCP}$			1		µs
Overtemperature Shutdown Threshold	t_{OTP+}	Internal	**125**			°C

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Supervisory Limits Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side)						
• These supervisory limits are set in the internal controller and can be reconfigured or disabled through PMBus™. • When disabled, the powertrain protections presented in the previous table will intervene during fault events.						
HI Side Overvoltage Lockout Threshold	V_{HI_OVLO+}		**420**	434.5	**450**	V
HI Side Overvoltage Recovery Threshold	V_{HI_OVLO-}		**405**	424	**440**	V
HI Side Overvoltage Lockout Hysteresis	$V_{HI_OVLO_HYST}$			10.5		V
HI Side Overvoltage Lockout Response Time	t_{HI_OVLO}			100		µs
HI Side Undervoltage Lockout Threshold	V_{HI_UVLO-}		**200**	226	**250**	V
HI Side Undervoltage Recovery Threshold	V_{HI_UVLO+}		**225**	244	**259**	V
HI Side Undervoltage Lockout Hysteresis	$V_{HI_UVLO_HYST}$			15		V
HI Side Undervoltage Lockout Response Time	t_{HI_UVLO}			100		µs
HI Side Undervoltage Startup Delay	$t_{HI_UVLO+_DELAY}$	From V_{HI_DC} = V_{HI_UVLO+} to powertrain active, (i.e One time startup delay from application of V_{HI_DC} to V_{LO_DC})		20		ms
LO Side Overcurrent Trip Threshold	$I_{LO_OUT_OCP}$		**159**	168	**177**	A
LO Side Overcurrent Response Time Constant	$t_{LO_OUT_OCP}$	Effective internal RC filter		2		ms
Overtemperature Shutdown Threshold	t_{OTP+}	Internal	**125**			°C
Overtemperature Recovery Threshold	t_{OTP-}	Internal	105	110	115	°C
Undertemperature Shutdown Threshold (Internal)	t_{UTP}	C-Grade			-25	°C
		T-Grade			-45	
Undertemperature Restart Time	$t_{UTP_RESTART}$	Startup into a persistent fault condition. Non-latching fault detection given V_{HI_DC} > V_{HI_UVLO+}		3		s

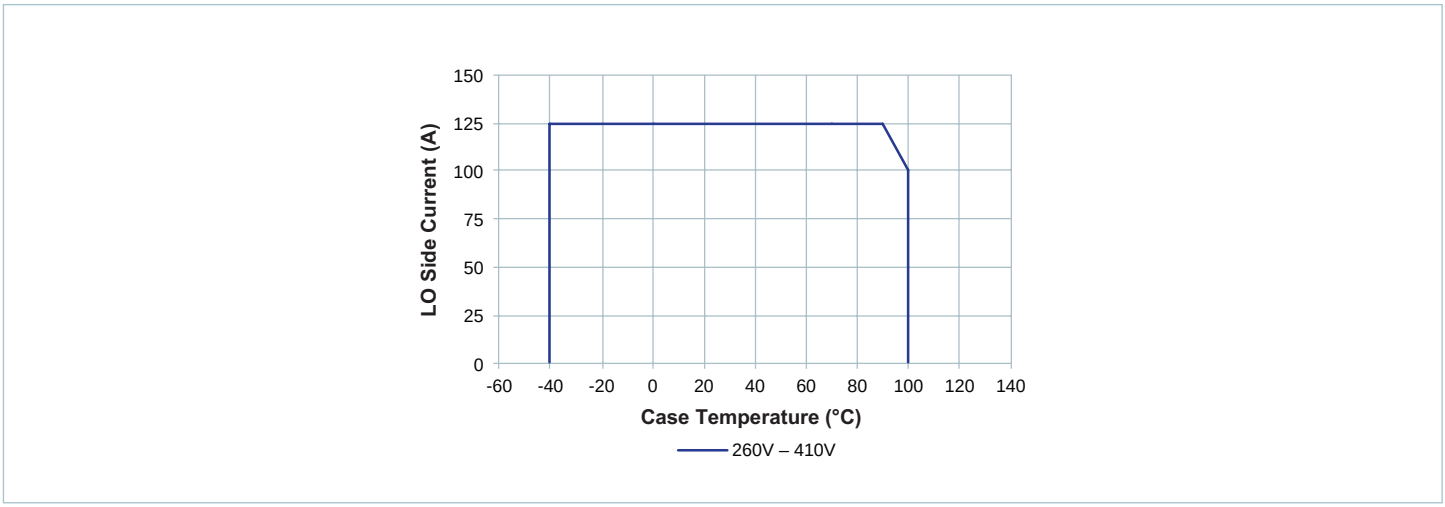


Figure 1 *— Specified thermal operating area*

1. The BCM in a VIA package is cooled through bottom case (bottom housing).
2. The thermal rating is based on typical measured device efficiency.
3. The case temperature in the graph is the measured temperature of the bottom housing, such that internal operating temperature does not exceed 125°C.

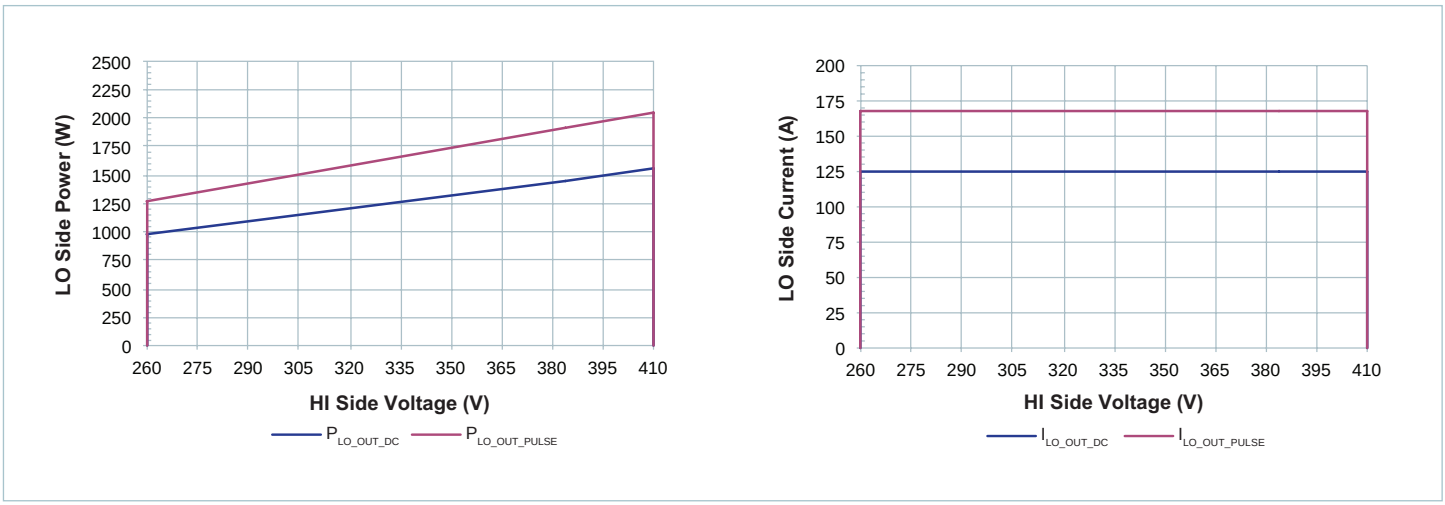


Figure 2 *— Specified electrical operating area using rated R_{LO_HOT}*

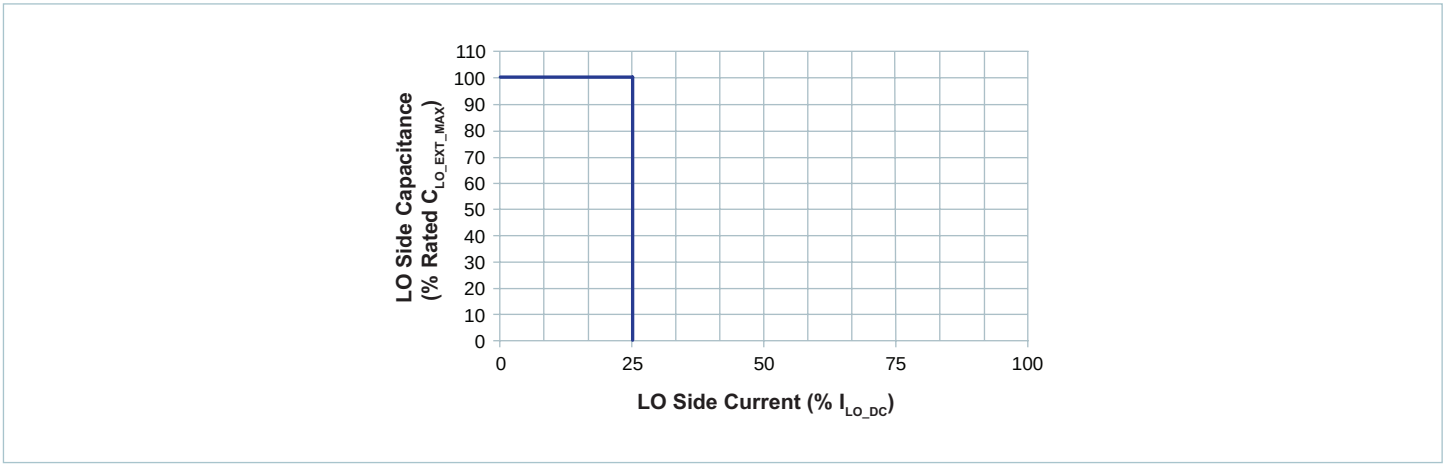


Figure 3 *— Specified HI side startup into load current and external capacitance*

PMBus™ Reported Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Monitored Telemetry					
ATTRIBUTE	**PMBus™ READ COMMAND**	**ACCURACY (RATED RANGE)**	**FUNCTIONAL REPORTING RANGE**	**UPDATE RATE**	**REPORTED UNITS**
HI Side Voltage	(88h) READ_VIN	± 5%(LL - HL)	130V to 450V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
HI Side Current	(89h) READ_IIN	± 20%(10 - 20% of FL) ± 5%(20 - 133% of FL)	-0.85A to 5.9A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-3}$
LO Side Voltage[1]	(8Bh) READ_VOUT	± 5%(LL - HL)	4.25V to 14V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
LO Side Current	(8Ch) READ_IOUT	± 20%(10 - 20% of FL) ± 5%(20 - 133% of FL)	-27A to 190A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
LO Side Resistance	(D4h) READ_ROUT	± 5%(50 - 100% of FL) at NL ± 10%(50 - 100% of FL)(LL - HL)	1.0mΩ to 3.0mΩ	100ms	$R_{ACTUAL} = R_{REPORTED} \times 10^{-5}$
Temperature[2]	(8Dh) READ_TEMPERATURE_1	± 7°C(Full Range)	- 55°C to 130°C	100ms	$T_{ACTUAL} = T_{REPORTED}$

[1] Default READ LO Side Voltage returned when unit is disabled = -300V.
[2] Default READ Temperature returned when unit is disabled = -273°C.

Variable Parameters					
• Factory setting of all Thresholds and Warning limits listed below are 100% of specified protection values. • Variables can be written only when module is disabled with $V_{HI} < V_{HI_UVLO-}$ and external bias (VDDB) applied. • Module must remain in a disabled mode for 3ms after any changes to the variables below to allow sufficient time to commit changes to EEPROM.					
ATTRIBUTE	**PMBus™ COMMAND**	**CONDITIONS / NOTES**	**ACCURACY (RATED RANGE)**	**FUNCTIONAL REPORTING RANGE**	**DEFAULT VALUE**
HI Side Overvoltage Protection Limit	(55h) VIN_OV_FAULT_LIMIT	V_{HI_OVLO-} is automatically 3% lower than this setpoint	± 5%(LL - HL)	130V to 435V	100%
HI Side Overvoltage Warning Limit	(57h) VIN_OV_WARN_LIMIT		± 5%(LL - HL)	130V to 435V	100%
HI Side Undervoltage Protection Limit	(D7h) DISABLE_FAULTS	Can only be disabled to a preset default value	± 5%(LL - HL)	130V to 260V	100%
HI Side Overcurrent Protection Limit	(5Bh) IIN_OC_FAULT_LIMIT		± 20%(10 - 20% of FL) ± 5%(20 - 133% of FL)	0 to 5.25A	100%
HI Side Overcurrent Warning Limit	(5Dh) IIN_OC_WARN_LIMIT		± 20%(10 - 20% of FL) ± 5%(20 - 133% of FL)	0 to 5.25A	100%
Overtemperature Protection Limit	(4Fh) OT_FAULT_LIMIT	Internal Temperature	± 7°C(Full Range)	0 to 125°C	100%
Overtemperature Warning Limit	(51h) OT_WARN_LIMIT	Internal Temperature	± 7°C(Full Range)	0 to 125°C	100%
Turn on Delay	(60h) TON_DELAY	Additional time delay to the Undervoltage Startup Delay	± 50µs	0 to 100ms	0 ms

Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted. **Please Note:** For chassis mount model, Vicor part number 42550 will be needed for applications requiring the use of the signal pins. Signal cable 42550 is rated up to five insertions and extractions. To avoid unnecessary stress on the connector, the cable should be appropriately strain relieved.

EXT. BIAS (VDDB) Pin

- VDDB powers the internal controller.
- VDDB needs to be applied to enable and disable the BCM through PMBus™ control (using OPERATION COMMAND), and to adjust warning and protection thresholds.
- VDDB voltage not required for telemetry; however, if VDDB is not applied, telemetry information will be lost when V_{IN} is removed.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
INPUT	Regular Operation	VDDB Voltage	V_{VDDB}		4.5	5	9	V
		VDDB Current Consumption	I_{VDDB}				50	mA
	Startup	Inrush Current Peak	I_{VDDB_INR}	V_{VDDB} slew rate = 1V/µs		3.5		A
		Turn On Time	t_{VDDB_ON}	From V_{VDDB_MIN} to PMBus active		1.5		ms

SGND Pin

- All PMBus signals (SCL, SDA, ADDR) are referenced to SGND pin.
- SGND pin also serves as return pin (ground pin) for VDDB.
- Keep SGND signal separated from the low voltage side power return terminal (–LO) in electrical design.

Address (ADDR) Pin

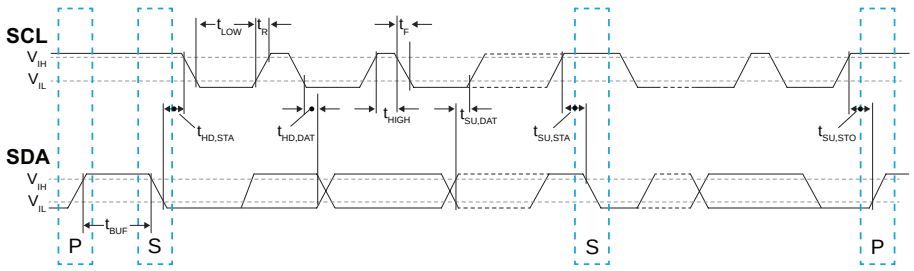
- This pin programs the address using a resistor between ADDR pin and signal ground.
- The address is sampled during startup and is stored until power is reset. This pin programs only a Fixed and Persistent address.
- This pin has an internal 10kΩ pullup resistor to 3.3V.
- 16 addresses are available. The range of each address is 206.25mV (total range for all 16 addresses is 0V to 3.3V).

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
MULTI–LEVEL INPUT	Regular Operation	ADDR Input Voltage	V_{SADDR}	See address section	0		3.3	V
		ADDR leakage current	I_{SADDR}	Leakage current			1	µA
	Startup	ADDR registration time	t_{SADDR}	From V_{VDDB_MIN}		1		ms

Serial Clock input (SCL) AND Serial Data (SDA) Pins

- High-power SMBus specification and SMBus physical layer compatible. Note that optional SMBALERT# is not supported.
- PMBus™ command compatible.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT	Regular Operation	**Electrical Parameters**						
		Input Voltage Threshold	V_{IH}		2.1			V
			V_{IL}				0.8	V
		Output Voltage Threshold	V_{OH}		3			V
			V_{OL}				0.4	V
		Leakage current	I_{LEAK_PIN}	Unpowered device			10	µA
		Signal Sink Current	I_{LOAD}	V_{OL} = 0.4V	4			mA
		Signal Capacitive Load	C_I	Total capacitive load of one device pin			10	pF
		Signal Noise Immunity	V_{NOISE_PP}	10MHz to 100MHz	300			mV
		Timing Parameters						
		Operating Frequency	F_{SMB}	Idle state = 0Hz	10		400	kHz
		Free time between Stop and Start Condition	t_{BUF}		1.3			µs
		Hold time after Start or Repeated Start condition	$t_{HD:STA}$	First clock is generated after this hold time	0.6			µs
		Repeat Start Condition Setup time	$t_{SU:STA}$		0.6			µs
		Stop Condition setup time	$t_{SU:STO}$		0.6			µs
		Data Hold time	$t_{HD:DAT}$		300			ns
		Data Setup time	$t_{SU:DAT}$		100			ns
		Clock low time out	$t_{TIMEOUT}$		25		35	ms
		Clock low period	t_{LOW}		1.3			µs
		Clock high period	t_{HIGH}		0.6		50	µs
		Cumulative clock low extend time	$t_{LOW:SEXT}$				25	ms
		Clock or Data Fall time	t_F		20		300	ns
		Clock or Data Rise time	t_R		20		300	ns



Application Characteristics

Temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the forward direction (high voltage side to low voltage side). See associated figures for general trend data.

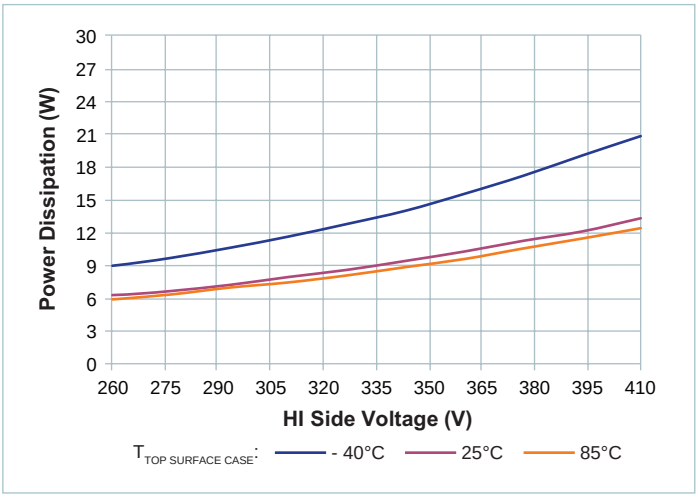


Figure 4 — *No load power dissipation vs. V_{HI_DC}*

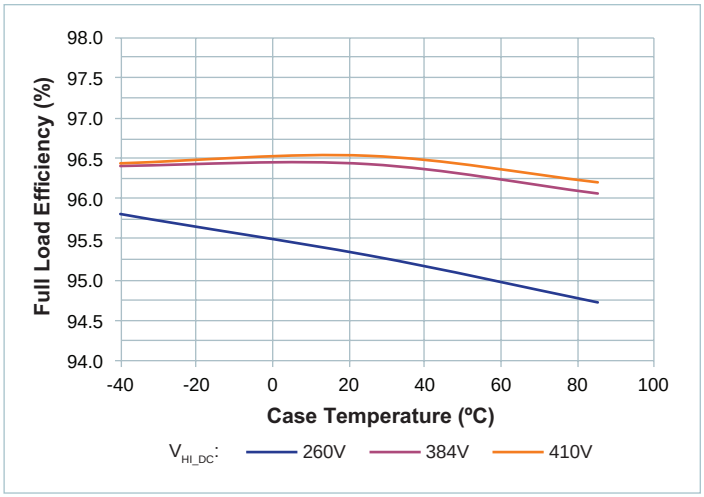


Figure 5 — *Full load efficiency vs. temperature*

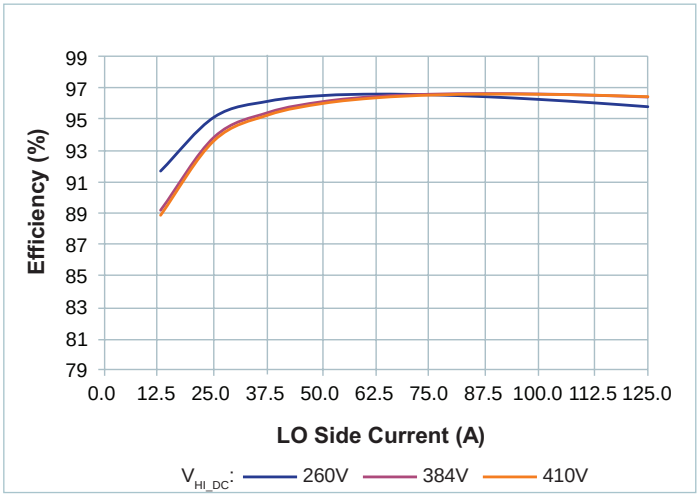


Figure 6 — *Efficiency at T_{CASE} = -40°C*

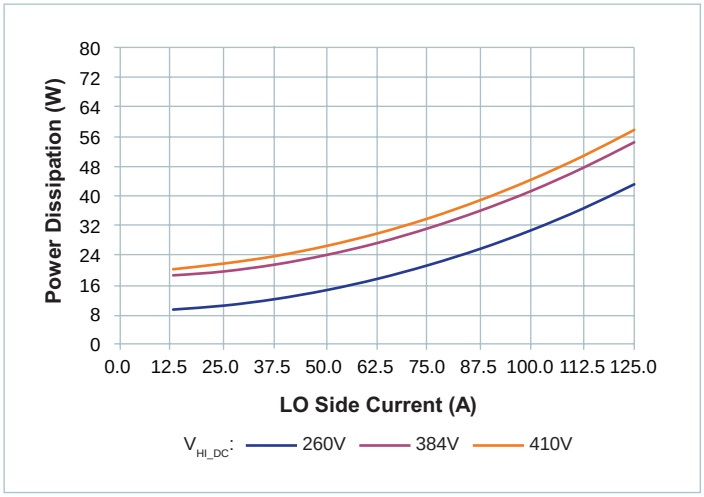


Figure 7 — *Power dissipation at T_{CASE} = -40°C*

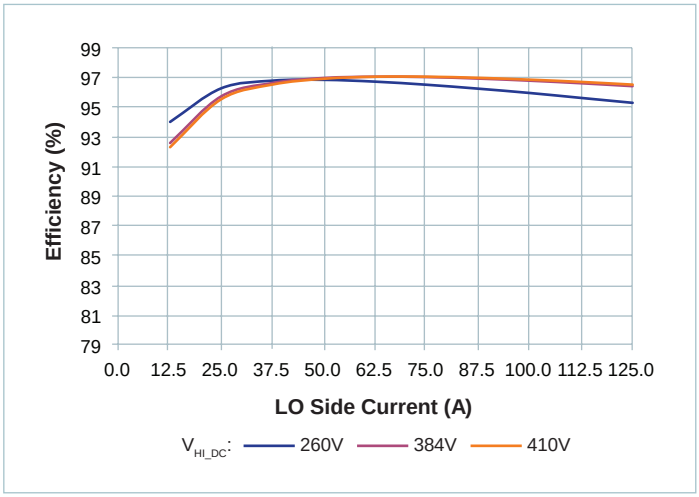


Figure 8 — *Efficiency at T_{CASE} = 25°C*

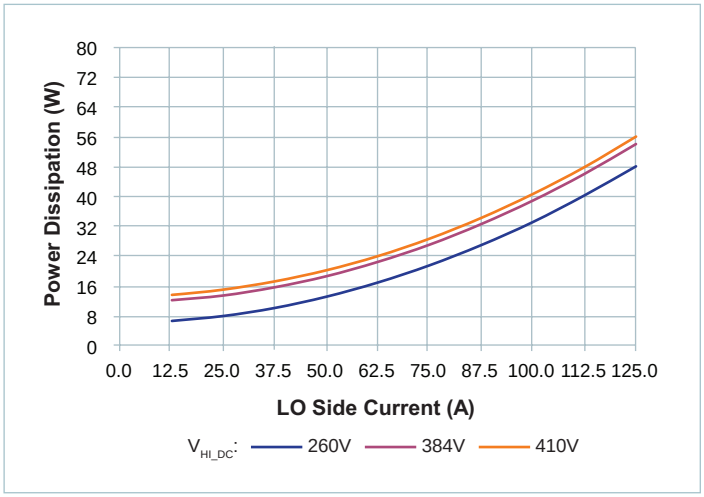


Figure 9 — *Power dissipation at T_{CASE} = 25°C*

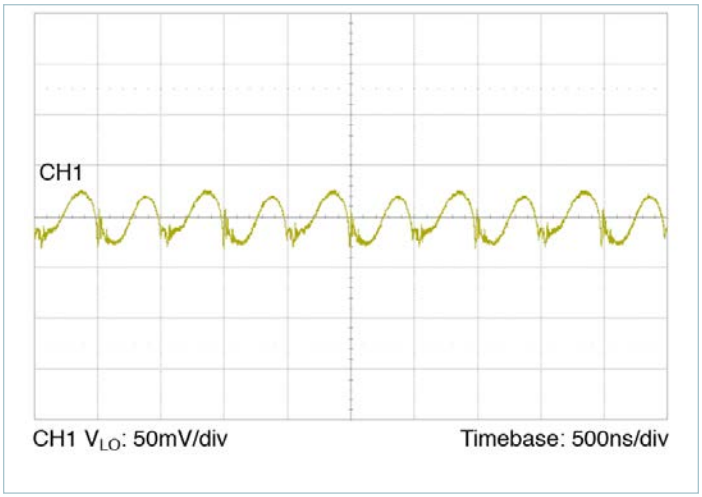


Figure 14 — *Full load LO side voltage ripple, 10 µF $C_{HI_IN_EXT}$; No external $C_{LO_OUT_EXT}$. Board mounted module, scope setting : 20MHz analog BW*

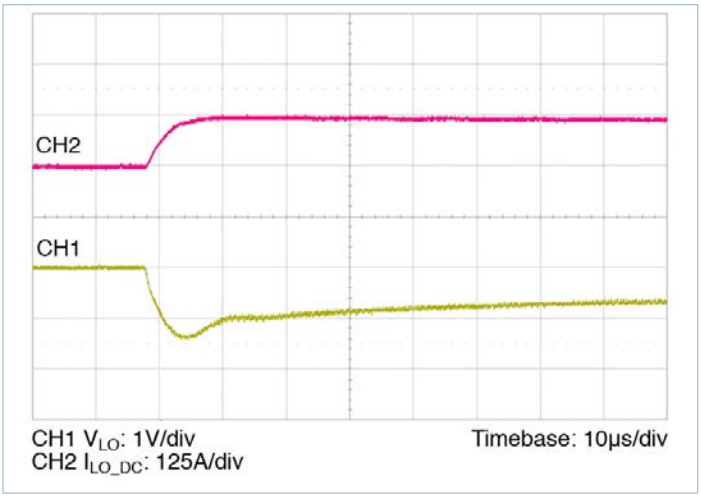


Figure 15 — *0A – 125A transient response: $C_{HI_IN_EXT}$ = 10µF, no external $C_{LO_OUT_EXT}$*

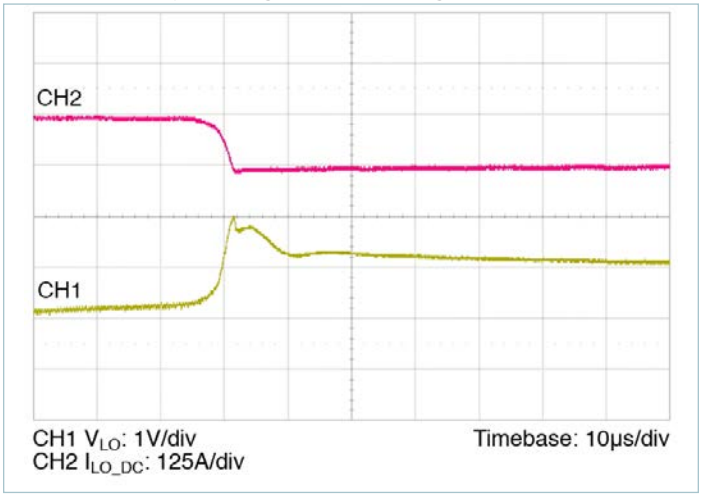


Figure 16 — *125A – 0A transient response: $C_{HI_IN_EXT}$ = 10µF, no external $C_{LO_OUT_EXT}$*

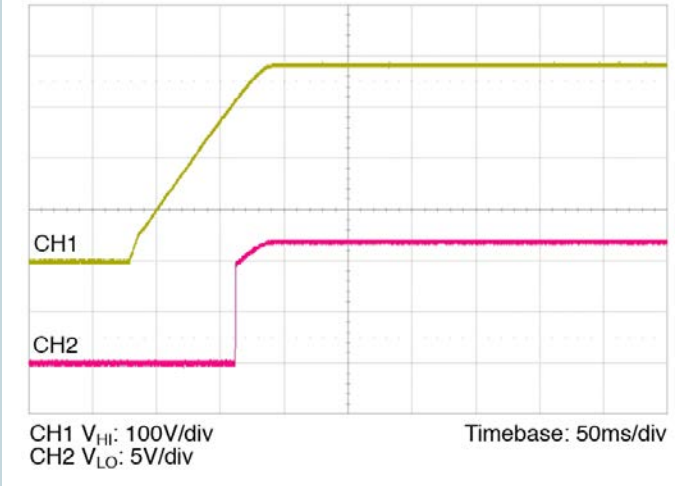


Figure 17 — *Startup from application of V_{HI_DC} = 384V, 25% I_{LO_DC}, 100% $C_{LO_OUT_EXT}$*

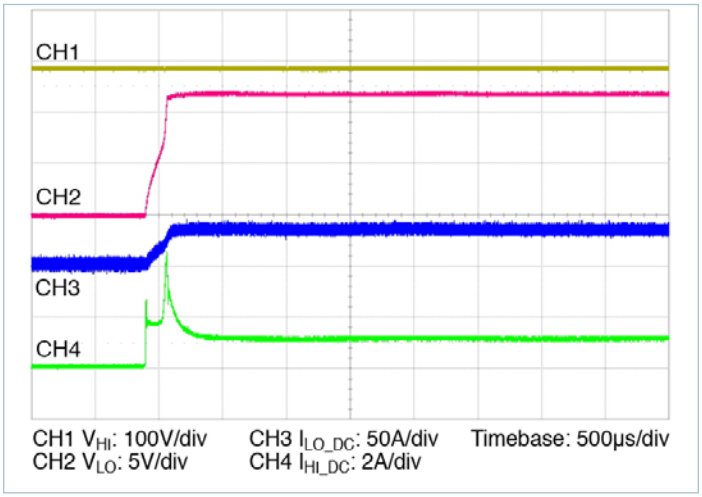


Figure 18 — *Startup from application of OPERATION COMMAND with pre-applied V_{HI_DC} = 384V, 25% I_{LO_DC}, 100% $C_{LO_OUT_EXT}$*

General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L	Lug (Chassis) Mount	110.30 / [4.34]	110.55 / [4.35]	110.80 / [4.36]	mm / [in]
Length	L	PCB (Board) Mount	112.51 / [4.43]	112.76 / [4.44]	113.01 / [4.45]	mm / [in]
Width	W		35.29 / [1.39]	35.54 / [1.40]	35.79 / [1.41]	mm / [in]
Height	H		9.019 / [0.355]	9.40 / [0.37]	9.781 / [0.385]	mm / [in]
Volume	Vol	Without heatsink		36.93 / [2.25]		cm^3/ [in^3]
Weight	W			140.5 / [4.96]		g / [oz]
Pin Material		C145 copper				
Underplate		Low stress ductile Nickel	50		100	µin
Pin Finish (Gold)		Palladium	0.8		6	µin
		Soft Gold	0.12		2	
Pin Finish (Tin)		Whisker resistant matte Tin	200		400	
Thermal						
Operating Internal Temperature	T_{INT}	BCM4414xD1E13A2yzz (T-Grade)	-40		125	°C
		BCM4414xD1E13A2yzz (C-Grade)	-20		125	
Operating Case Temperature	T_{CASE}	BCM4414xD1E13A2yzz (T-Grade), derating applied, see safe thermal operating area	-40		100	
		BCM4414xD1E13A2yzz (C-Grade), derating applied, see safe thermal operating area	-20		100	
Thermal Resistance Top Side	Φ_{INT_TOP}	Estimated thermal resistance to maximum temperature internal component from isothermal top		0.97		°C/W
Thermal Resistance Coupling Between Top Case and Bottom Case	Φ_{HOU}	Estimated thermal resistance of thermal coupling between the top and bottom case surfaces		0.57		°C/W
Thermal Resistance Bottom Side	Φ_{INT_BOT}	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		0.67		°C/W
Thermal Capacity				54		Ws/°C
Assembly						
Storage Temperature	T_{ST}	BCM4414xD1E13A2yzz (T-Grade)	-40		125	°C
		BCM4414xD1E13A2yzz (C-Grade)	-40		125	°C
ESD Withstand	ESD_{HBM}	Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2kV)	1000			
	ESD_{CDM}	Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V)	200			

General Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Safety						
Isolation Capacitance	C_{HI_LO}	Unpowered unit	620	780	940	pF
Isolation Resistance	R_{HI_LO}	At 500V_{DC}	10			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer		2.31		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		3.41		MHrs
Agency Approvals / Standards						
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

BCM in a VIA Package

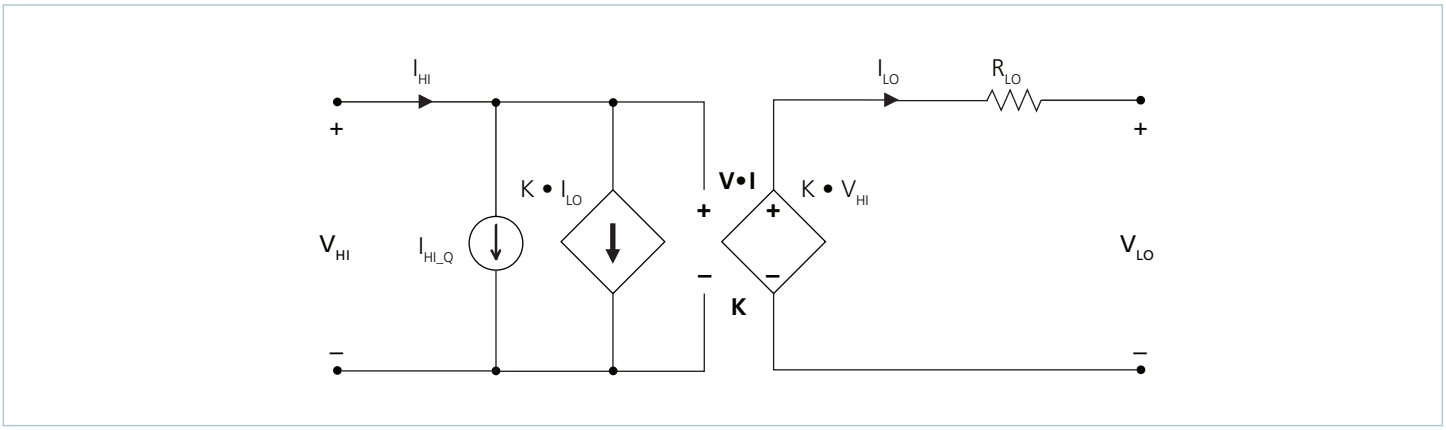


Figure 19 *— BCM DC model (Forward Direction)*

The BCM uses a high frequency resonant tank to move energy from the high voltage side to the low voltage side and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of the HI side voltage and the LO side current. A small amount of capacitance embedded in the high voltage side and low voltage side stages of the module is sufficient for full functionality and is key to achieving high power density.

The BCM4414xD1E13A2yzz can be simplified into the model shown in Figure 19.

At no load:

$$V_{LO} = V_{HI} \bullet K \qquad (1)$$

K represents the "turns ratio" of the BCM.
Rearranging Eq (1):

$$K = \frac{V_{LO}}{V_{HI}} \qquad (2)$$

In the presence of a load, V_{LO} is represented by:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R_{LO} \qquad (3)$$

and I_{LO} is represented by:

$$I_{LO} = \frac{I_{HI} - I_{HI_Q}}{K} \qquad (4)$$

R_{LO} represents the impedance of the BCM and is a function of the R_{DS_ON} of the HI side and LO side MOSFETs, PC board resistance of HI side and LO side boards and the winding resistance of the power transformer. I_{HI_Q} represents the HI side quiescent current of the BCM controller, gate drive circuitry and core losses.

The effective DC voltage transformer action provides additional interesting attributes. Assuming that $R_{LO} = 0\Omega$ and $I_{HI_Q} = 0A$, Eq. (3) now becomes Eq. (1) and is essentially load independent, resistor R is now placed in series with V_{HI}.

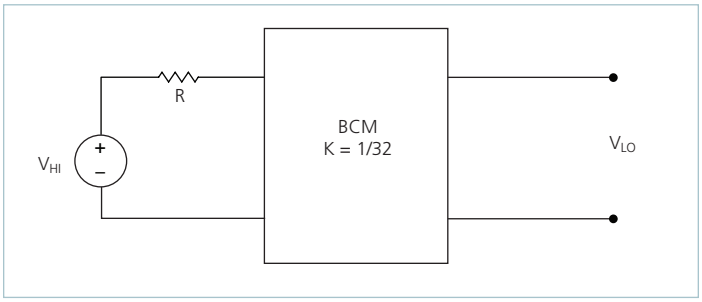


Figure 20 *— K = 1/32 BCM with series HI side resistor*

The relationship between V_{HI} and V_{LO} becomes:

$$V_{LO} = (V_{HI} - I_{HI} \bullet R) \bullet K \qquad (5)$$

Substituting the simplified version of Eq. (4) (I_{HI_Q} is assumed = 0A) into Eq. (5) yields:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Eq. (3), where R_{LO} is used to represent the characteristic impedance of the BCM. However, in this case a real resistor, R, on the high voltage side of the BCM is effectively scaled by K^2 with respect to the low voltage side.

Assuming that R = 1Ω, the effective R as seen from the low voltage side is 1.0mΩ, with K = 1/32.

A similar exercise can be performed with the addition of a capacitor or shunt impedance at the high voltage side of the BCM. A switch in series with V_{HI} is added to the circuit. This is depicted in Figure 21.

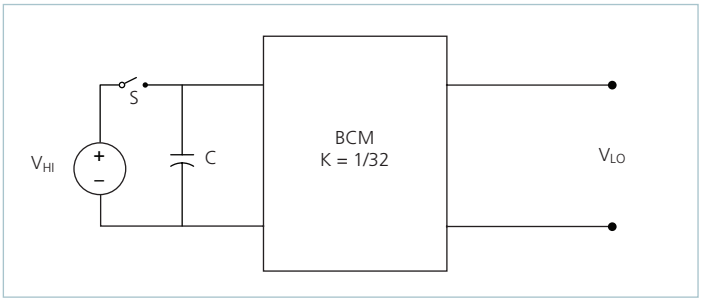


Figure 21 — *BCM with High side capacitor*

A change in V_{HI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{HI}}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{HI}, the switch is opened and the capacitor is discharged through the idealized BCM. In this case,

$$I_C = I_{LO} \bullet K \qquad (8)$$

substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{LO}(t) = \frac{C}{K^2} \bullet \frac{dV_{LO}}{dt} \qquad (9)$$

The equation in terms of the LO side has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the low voltage side when expressed in terms of the high voltage side. With K = 1/32 as shown in Figure 21, C = 1µF would appear as C = 1024µF when viewed from the low voltage side.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a BCM between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, these benefits are not achieved if the series impedance of the BCM is too high. The impedance of the BCM must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the BCM low involves switching at a high frequency. This enables the use of small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM module are:

- No load power dissipation (P_{HI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{LO}}$): refers to the power loss across the BCM module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{HI_NL} + P_{R_{LO}} \qquad (10)$$

Therefore,

$$P_{LO_OUT} = P_{HI_IN} - P_{DISSIPATED} = P_{HI_IN} - P_{HI_NL} - P_{R_{LO}} \qquad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{LO_OUT}}{P_{HI_IN}} = \frac{P_{HI_IN} - P_{HI_NL} - P_{R_{LO}}}{P_{HI_IN}} \qquad (12)$$

$$= \frac{V_{HI} \bullet I_{HI} - P_{HI_NL} - (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}$$

$$= 1 - \left(\frac{P_{HI_NL} + (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}\right)$$

Thermal Considerations

The VIA package provides effective conduction cooling from either of the two module surfaces. Heat may be removed from the top surface, the bottom surface or both. The extent to which these two surfaces are cooled is a key component for determining the maximum power that can be processed by a VIA, as can be seen from specified thermal operating area in Figure 1. Since the VIA has a maximum internal temperature rating, it is necessary to estimate this temperature based on a system-level thermal solution. For this purpose, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 22 shows the "thermal circuit" for the VIA module.

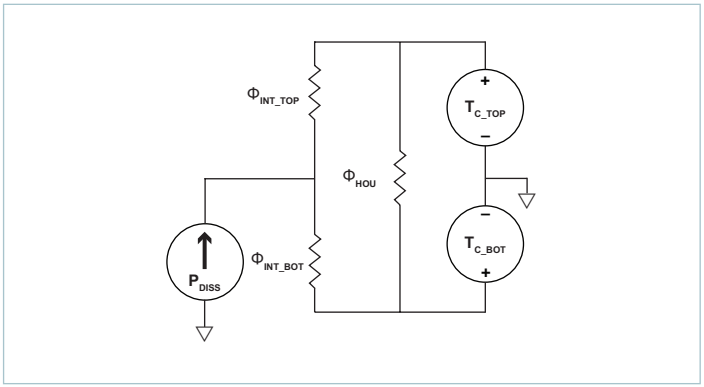


Figure 22 *— Double-sided cooling VIA thermal model*

In this case, the internal power dissipation is P_{DISS}, Φ_{INT_TOP} and Φ_{INT_BOT} are the thermal resistance characteristics of the VIA module and the top and bottom surface temperatures are represented as T_{C_TOP}, and T_{C_BOT}. It is interesting to notice that the package itself provides a high degree of thermal coupling between the top and bottom case surfaces (represented in the model by the resistor Φ_{HOU}). This feature enables two main options regarding thermal designs:

- Single side cooling: the model of Figure 22 can be simplified by calculating the parallel resistor network and using one simple thermal resistance number and the internal power dissipation curves; an example for bottom side cooling only is shown in Figure 23.

In this case, Φ_{INT} can be derived as follows:

$$\Phi_{INT} = \frac{(\Phi_{INT_TOP} \cdot \Phi_{HOU}) \cdot \Phi_{INT_BOT}}{\Phi_{INT_TOP} + \Phi_{HOU} + \Phi_{INT_BOT}} \qquad (1)$$

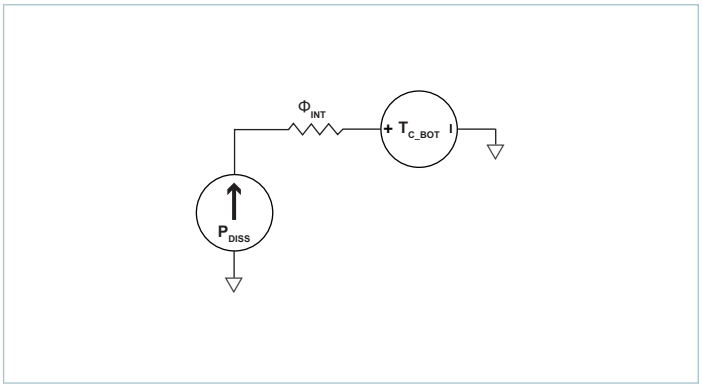


Figure 23 *— Single-sided cooling VIA thermal model*

- Double side cooling: while this option might bring limited advantage to the module internal components (given the surface-to-surface coupling provided), it might be appealing in cases where the external thermal system requires allocating power to two different elements, such as heatsinks with independent airflows or a combination of chassis/air cooling.

Current Sharing

The performance of the BCM is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array, they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load, ensuring equal current sharing among modules requires that BCM array impedances be matched.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes/wires within the PCB/Chassis to deliver and return the current to the modules.
- Provide as symmetric a PCB/Wiring layout as possible among modules

For further details see AN:016 Using BCM Bus Converters in High Power Arrays.

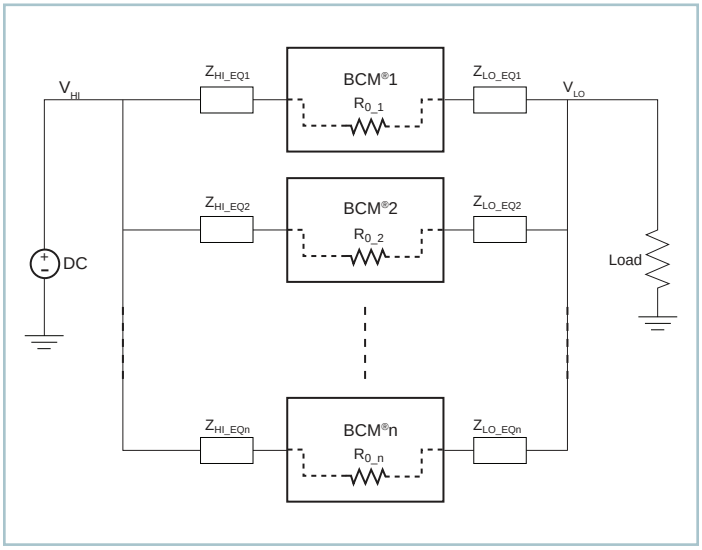


Figure 24 *— BCM module array*

Fuse Selection

In order to provide flexibility in configuring power systems, BCM in a VIA package modules are not internally fused. Input line fusing of BCM products is recommended at the system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of BCM module)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: 10A Littelfuse 505 Series or
  10A Littelfuse 487 Series (HI side)

Reverse Operation

BCM modules are capable of reverse power operation. Once the unit is started, energy will be transferred from the low side voltage back to the high voltage side whenever the low voltage side exceeds $V_{HI} \bullet K$. The module will continue operation in this fashion for as long as no faults occur.

The BCM4414xD1E5135yzz has not been qualified for continuous operation in a reverse power condition. However, fault protections that help to protect the module in forward operation will also protect the module in reverse operation.

Transient operation in reverse is expected in cases where there is significant energy storage on the low voltage side and transient voltages appear on the high voltage side.

Dielectric Withstand

The chassis of the BCM in a VIA package is required to be connected to Protective Earth when installed in the end application and must satisfy the requirements of IEC 60950-1 for Class I products.

The BCM in a VIA package contains an internal safety approved isolating component (VI ChiP) that provides the Reinforced Insulation from high voltage side to low voltage side. The isolating component is individually tested for Reinforced Insulation from the high voltage side to the low voltage side at $4242V_{DC}$ prior to final assembly of the VIA. The Reinforced Insulation can only be tested on the completed VIA assembly at Basic Insulation values, as specified in the electric strength Test Procedure noted in clause 5.2.2 of IEC 60950-1.

Test Procedure Note from IEC 60950-1

"For equipment incorporating both REINFORCED INSULATION and lower grades of insulation, care is taken that the voltage applied to the REINFORCED INSULATION does not overstress BASIC INSULATION or SUPPLEMENTARY INSULATION."

Summary

The final VIA assembly provides basic insulation from the high voltage side to case, basic insulation from the high voltage side to the low voltage side and functional insulation from low voltage side to case. The case is required to be connected to protective earth in the final installation. The protective earth connection can be accomplished through dedicated wiring harness (example: ring terminal clamped by mounting screw) or surface contact (example: pressure contact on bare conductive chassis or PCB copper layer with no solder mask).

The ground connection of the top case must be 3 orders of magnitude more resistive than the current return connection to the bottom case. The construction of the VIA can be summarized by describing it as a "Class II" component installed in a "Class I" subassembly. The insulation from the high voltage side to the low voltage side can only be tested at basic insulation values on the fully assembled VIA product.

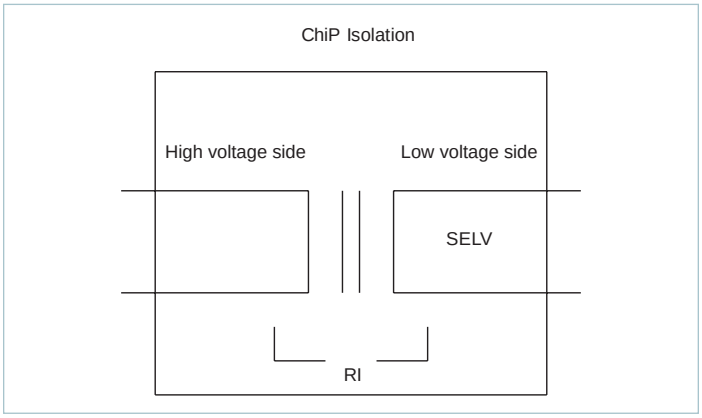


Figure 25 *— ChiP before final assembly in the VIA*

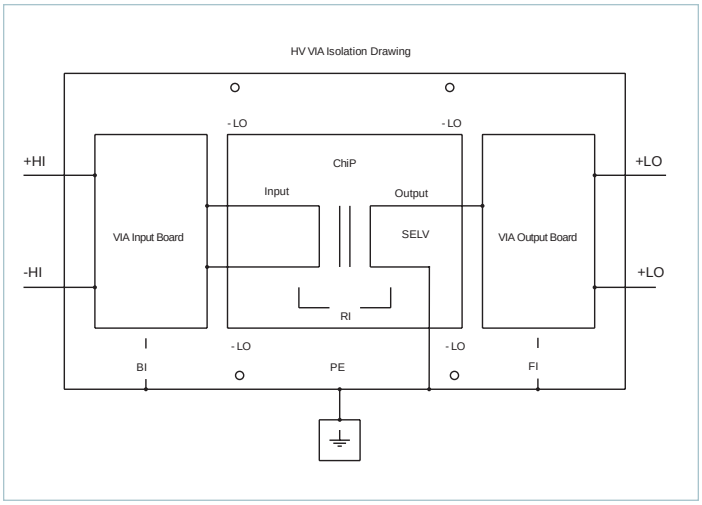


Figure 26 *— BCM in a VIA package after final assembly*

Filtering

The BCM in a VIA package has built-in single stage EMI filtering with Hot-Swap circuitry located on the high voltage side. The integrated EMI filtering consists of a common mode choke, differential mode capacitors, and Y2 common mode capacitors. A typical test set-up block diagram for conducted emissions is shown in Figure 27.

The built-in EMI filtering reduces the HI side voltage ripple. External LO side filtering can be added as needed, with ceramic capacitance used as a LO side bypass for this purpose. The filtering, along with Hot-Swap circuitry, protects the BCM in a VIA package from overvoltage transients imposed by a system that would exceed maximum ratings. VIA HI side and LO side voltage ranges shall not be exceeded. An internal overvoltage function prevents operation outside of the normal operating HI side range. However, the VIA is exposed to the applied voltage even when disabled and must withstand it.

The source response is generally the limiting factor in the overall system response, given the wide bandwidth of the BCM. Anomalies in the response of the source will appear at the LO side of the module multiplied by its K factor.

Total load capacitance at the LO side of the BCM shall not exceed the specified maximum to ensure correct operation in startup. Due to the wide bandwidth and small LO side impedance of the BCM, low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the HI side of the BCM.

At frequencies less than 500kHz, the BCM appears as an impedance of R_{LO} between the source and load. Within this frequency range, capacitance connected at the HI side appears as an effective scaled capacitance on the LO side per the relationship defined in equation (15).

This enables a reduction in the size and number of capacitors used

$$C_{LO} = \frac{C_{HI}}{K^2} \qquad (15)$$

in a typical system.

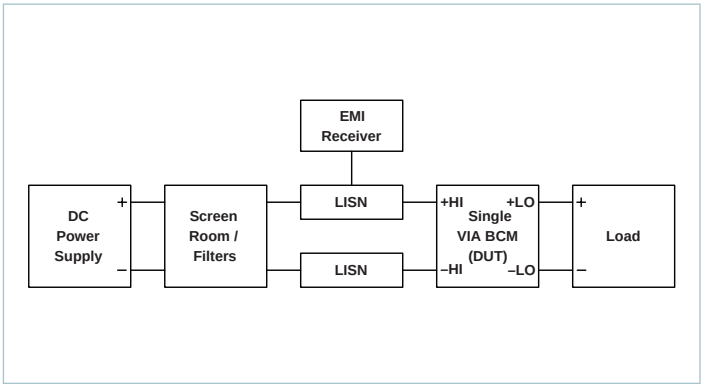


Figure 27 *— Typical test setup block diagram for Conducted Emissions*

Hot-Swap

Many applications use a power architecture based on a $380V_{DC}$ distribution bus. This supply level is emerging as a new standard for efficient distribution of power through board, rack and chassis mounted Telecom and Datacom systems. The interconnection between the different modules is accomplished with a backplane and motherboard. Power is commonly provided to the various module slots via a $380V_{DC}$ distribution bus.

In the event of a fault, removal of the faulty module from the rack is relatively easy, provided that the remaining power modules can support the step increase in load. Plugging in the replacement module has more potential for problems, as it presents an uncharged capacitor load and will draw a large inrush current. This could cause a momentary, but unacceptable interruption or sag in the backplane power bus if not limited. Additional problems may arise if ordinary power module connectors are used, since the connector pins will engage and disengage in a random and unpredictable sequence during insertion and removal.

Hot-Swap or hot-plug is a highly desirable feature in many applications, but also results in several issues that must be addressed in the system design. A number of related phenomena occur with a live insertion and removal event, including contact bouncing, arcing between HI side connector pins, and large voltage and current transients. Hot-Swap circuitry in the converter modules protects the module itself and the rest of the system from the problems associated with live insertion.

This module provides a high level of integration for DC-DC converters in $380V_{DC}$ distribution systems, saving design time and board space. To allow for the maintenance, reconfiguration, redundancy and system upgrades, the BCM in a VIA package is designed to address the function of Hot-Swapping at the $380V_{DC}$ distribution bus. Hot-Swap circuitry, as shown in Figure 28, uses an active MOSFET switching device in series with the HI side line. During module insertion, the MOSFET is driven into a resistive state to limit the inrush current as the input capacitance of the inserted unit is charged. The MOSFET is fully enhanced once the module's HI side capacitor has sufficiently charged to minimize losses during normal operation. Verification of the Hot-Swap circuitry performance is illustrated through plots of the module's response to a live insertion event in Figures 30 and 31.

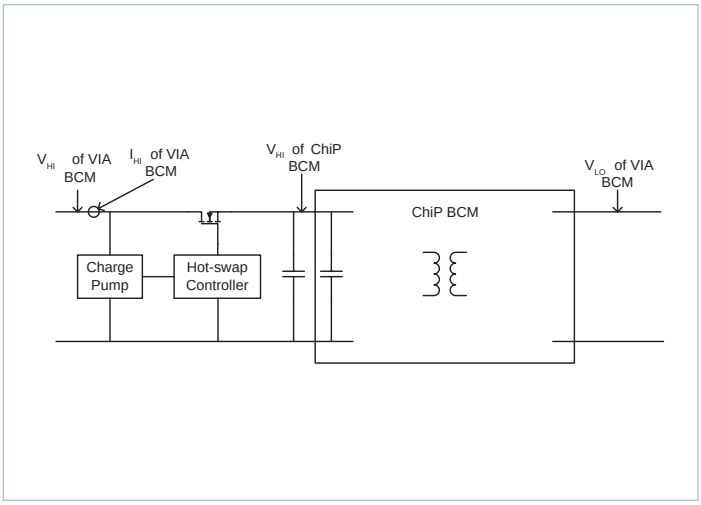


Figure 28 *— High level diagram for 384V_{DC} BCM in a VIA Package showing internal Hot-Swap circuitry and ChiP BCM*

The BCM in a VIA package provides the opportunity to incorporate Hot-Swap capabilities into redundant power module arrays. This allows telecoms and other mission critical applications to continue operating without interruption even through failure and replacement of one or more power modules.

Hot-Swap Test – Test circuit and Procedure

- Two parallel BCMs in a VIA package with mercury relay#1 open
- Close mercury relay#1 and measure inrush current going into BCM#2

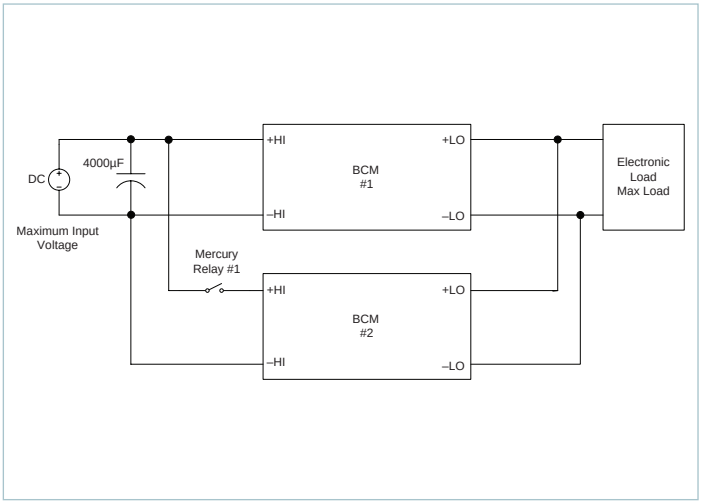


Figure 29 *— Test Circuit*

Hot-Swap Test – Scope Pictures

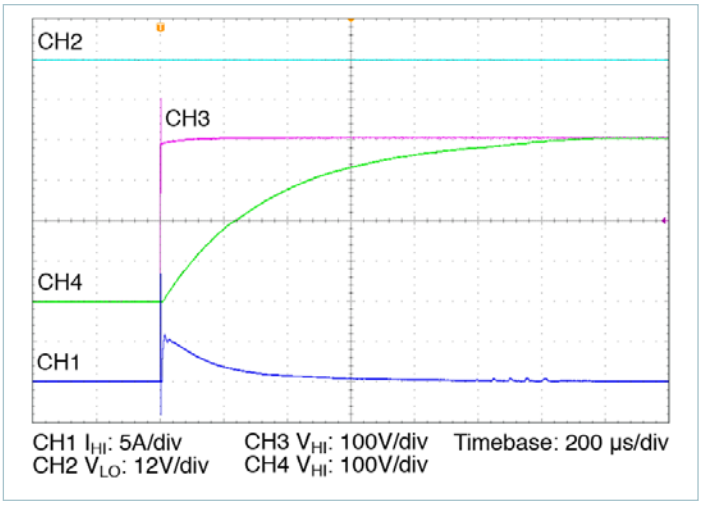


Figure 30 *— Hot-Swap start-up*

Ch1: I_{HI} of BCM#2

Ch2: V_{LO} of BCM#2

Ch3: V_{HI} of BCM#2 shows the fast voltage transient at the high side terminal of BCM#2

Ch4: V_{HI} of internal ChiP BCM#2 shows the soft start charging of the high side capacitor.

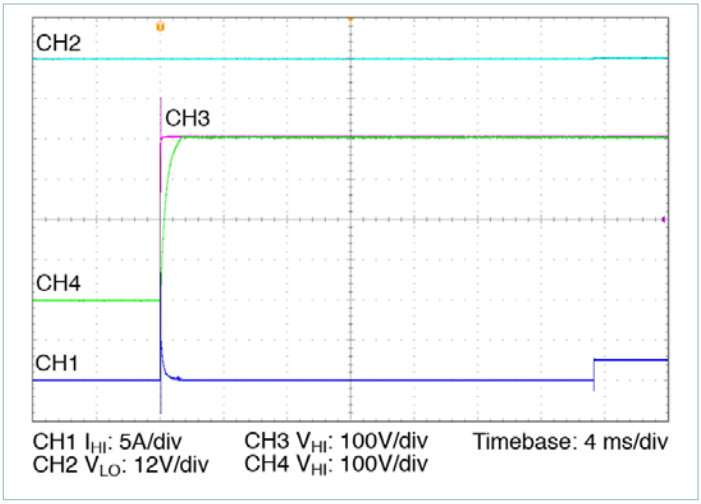
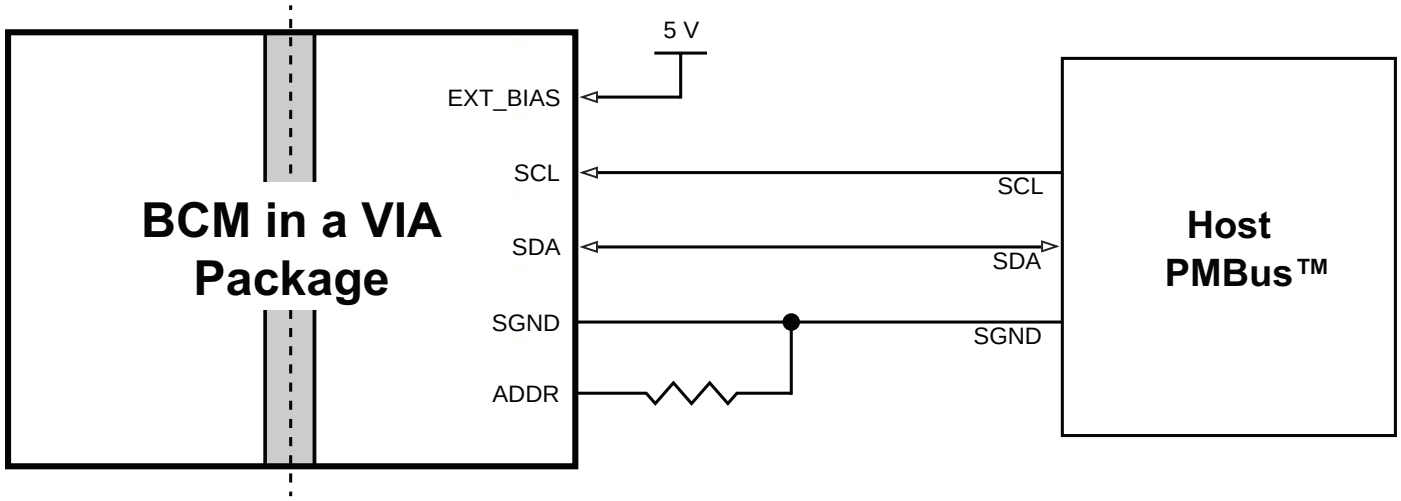


Figure 31 *— Larger time scale version of Figure 30 showing startup of BCM#2*

System Diagram for PMBus™ Interface



The controller of the BCM in a VIA package is referenced to low voltage side signal ground (SGND).

The BCM in a VIA package provides the Host PMBus system with accurate telemetry monitoring and reporting, threshold and warning limits adjustment, in addition to corresponding status flags. The standalone BCM is periodically polled for status by the host PMBus. Direct communication to the BCM is enabled by a page command. For example, the page (0x00) prior to a telemetry inquiry points to the controller data and pages (0x01) prior to a telemetry inquiry points to the BCM parameters. The BCM constantly polls its data through the PMBus.

The BCM enables the PMBus compatible host interface with an operating bus speed of up to 400kHz. The BCM follows the PMBus command structure and specification.

PMBus™ Interface

Refer to "PMBus Power System Management Protocol Specification Revision 1.2, Part I and II" for complete PMBus specifications details visit http://pmbus.org.

Device Address

The PMBus address (ADDR Pin) should be set to one of a predetermined 16 possible addresses shown in the table below using a resistor between ADDR pin and SGND pin.

The BCM accepts only a fixed and persistent address and does not support SMBus address resolution protocol. At initial power up, the BCM controller will sample the address pin voltage, and will keep this address until device power is removed.

ID	Slave Address	HEX	Recommended Resistor R_{ADDR} (Ω)
1	1010 000b	50h	487
2	1010 001b	51h	1050
3	1010 010b	52h	1870
4	1010 011b	53h	2800
5	1010 100b	54h	3920
6	1010 101b	55h	5230
7	1010 110b	56h	6810
8	1010 111b	57h	8870
9	1011 000b	58h	11300
10	1011 001b	59h	14700
11	1011 010b	5Ah	19100
12	1011 011b	5Bh	25500
13	1011 100b	5Ch	35700
14	1011 101b	5Dh	53600
15	1011 110b	5Eh	97600
16	1011 111b	5Fh	316000

Reported DATA Formats

The BCM controller employs a direct data format where all reported measurements are in Volts, Amperes, Degrees Celsius, or Seconds. The host uses the following PMBus specification to interpret received values metric prefixes. Note that the COEFFICIENTS command is not supported:

$$X = \left(\frac{1}{m}\right) \bullet (Y \bullet 10^{-R} - b)$$

Where:

X, is a "real world" value in units (A, V, °C, s)

Y, is a two's complement integer received from the BCM controller

m, b and R are two's complement integers defined as follows:

Command	Code	m	R	b
TON_DELAY	60h	1	3	0
READ_VIN	88h	1	1	0
READ_IIN	89h	1	3	0
READ_VOUT [1]	8Bh	1	1	0
READ_IOUT	8Ch	1	2	0
READ_TEMPERATURE_1 [2]	8Dh	1	0	0
READ_POUT	96h	1	0	0
MFR_VIN_MIN	A0h	1	0	0
MFR_VIN_MAX	A1h	1	0	0
MFR_VOUT_MIN	A4h	1	0	0
MFR_VOUT_MAX	A5h	1	0	0
MFR_IOUT_MAX	A6h	1	0	0
MFR_POUT_MAX	A7h	1	0	0
READ_K_FACTOR	D1h	65536	0	0
READ_BCM_ROUT	D4h	1	5	0

[1] Default READ LO side voltage returned when BCM unit is disabled = –300V.
[2] Default READ Temperature returned when BCM unit is disabled = –273°C.

No special formatting is required when lowering the supervisory limits and warnings.

Supported Command List

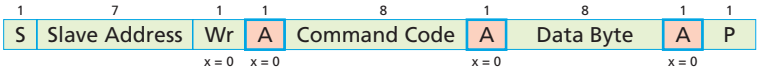
Command	Code	Function	Default Data Content	Data Bytes
PAGE	00h	Access BCM stored information	00h	1
OPERATION	01h	Turn BCM on or off	80h	1
CLEAR_FAULTS	03h	Clear all faults	N/A	None
CAPABILITY	19h	PMBus™ key capabilities set by factory	20h	1
OT_FAULT_LIMIT	4Fh[1]	Overtemperature protection	64h	2
OT_WARN_LIMIT	51h[1]	Overtemperature warning	64h	2
VIN_OV_FAULT_LIMIT	55h[1]	High voltage side overvoltage protection	64h	2
VIN_OV_WARN_LIMIT	57h[1]	High voltage side overvoltage warning	64h	2
IIN_OC_FAULT_LIMIT	5Bh[1]	High voltage side overcurrent protection	64h	2
IIN_OC_WARN_LIMIT	5Dh[1]	High voltage side overcurrent warning	64h	2
TON_DELAY	60h[1]	Startup delay in addition to fixed delay	00h	2
STATUS_BYTE	78h	Summary of faults	00h	1
STATUS_WORD	79h	Summary of fault conditions	00h	2
STATUS_IOUT	7Bh	Overcurrent fault status	00h	1
STATUS_INPUT	7Ch	Overvoltage and undervoltage fault status	00h	1
STATUS_TEMPERATURE	7Dh	Overtemperature and undertemperature fault status	00h	1
STATUS_CML	7Eh	PMBus communication fault	00h	1
STATUS_MFR_SPECIFIC	80h	Other BCM status indicator	00h	1
READ_VIN	88h	Reads HI side voltage	FFFFh	2
READ_IIN	89h	Reads HI side current	FFFFh	2
READ_VOUT	8Bh	Reads LO side voltage	FFFFh	2
READ_IOUT	8Ch	Reads LO side current	FFFFh	2
READ_TEMPERATURE_1	8Dh	Reads internal temperature	FFFFh	2
READ_POUT	96h	Reads LO side power	FFFFh	2
PMBUS_REVISION	98h	PMBus compatible revision	22h	1
MFR_ID	99h	BCM controller ID	"VI"	2
MFR_MODEL	9Ah	Internal controller or BCM model	Part Number	18
MFR_REVISION	9Bh	Internal controller or BCM revision	FW and HW revision	18
MFR_LOCATION	9Ch	Internal controller or BCM factory location	"AP"	2
MFR_DATE	9Dh	Internal controller or BCM manufacturing date	"YYWW"	4
MFR_SERIAL	9Eh	Internal controller or BCM serial number	Serial Number	16
MFR_VIN_MIN	A0h	Minimum rated high side voltage	Varies per BCM	2
MFR_VIN_MAX	A1h	Maximum rated high side voltage	Varies per BCM	2
MFR_VOUT_MIN	A4h	Minimum rated low side voltage	Varies per BCM	2
MFR_VOUT_MAX	A5h	Maximum rated low side voltage	Varies per BCM	2
MFR_IOUT_MAX	A6h	Maximum rated low side current	Varies per BCM	2
MFR_POUT_MAX	A7h	Maximum rated low side power	Varies per BCM	2
READ_K_FACTOR	D1h	Reads K factor	Varies per BCM	2
READ_BCM_ROUT	D4h	Low voltage side output resistance	Varies per BCM	2
SET_ALL_THRESHOLDS	D5h[1]	Set supervisory warning and protection thresholds	646464646464h	6
DISABLE_FAULT	D7h[1]	Disable overvoltage, overcurrent or undervoltage supervisory faults	00h	2

[1] The BCM must be in a disabled state with $V_{HI} < V_{HI_UVLO-}$ and VDDB applied during a write message.

Command Structure Overview

Write Byte protocol:

The Host always initiates PMBus™ communication with a START bit. All messages are terminated by the Host with a STOP bit. In a write message, the master sends the slave device address followed by a write bit. Once the slave acknowledges, the master proceeds with the command code and then similarly the data byte.



S Start Condition

Sr Repeated start Condition

Rd Read

Wr Write

X Indicated that field is required to have the value of x

A Acknowledge (bit may be 0 for an ACK or 1 for a NACK)

P Stop Condition

From Master to Slave

From Slave to Master

... Continued next line

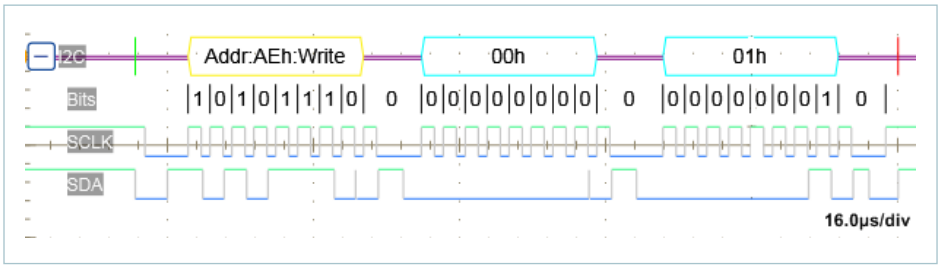
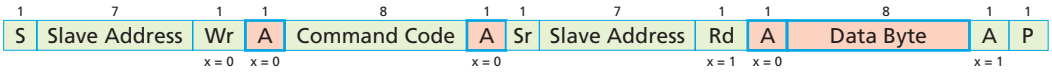


Figure 1 *— PAGE COMMAND (00h), WRITE BYTE PROTOCOL*

Read Byte protocol:

A Read message begins by first sending a Write Command, followed by a REPEATED START Bit and a slave Address. After receiving the READ bit, the BCM controller begins transmission of the Data responding to the Command. Once the Host receives the requested Data, it terminates the message with a NACK preceding a stop condition signifying the end of a read transfer.



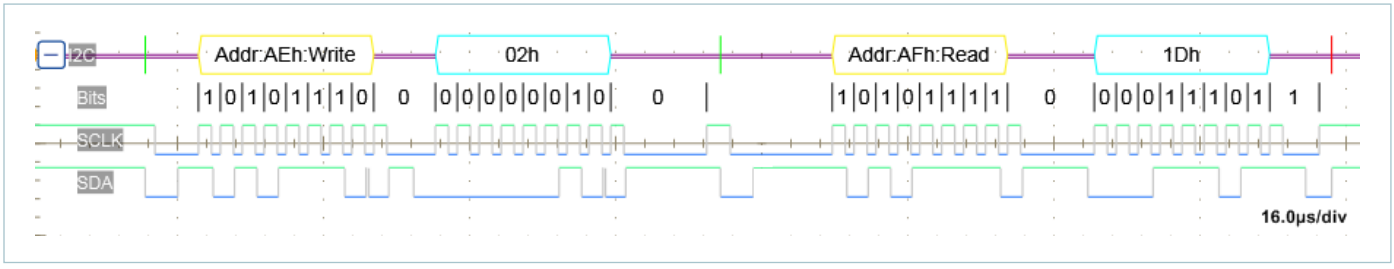
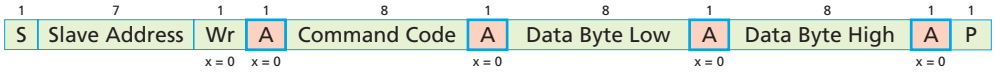


Figure 2 *— ON_OFF_CONFIG COMMAND (02h), READ BYTE PROTOCOL*

Write Word protocol:

When transmitting a word, the lowest order byte leads the highest order byte. Furthermore, when transmitting a Byte, the least significant bit (LSB) is sent last. Refer to System Management Bus (SMBus) specification version 2.0 for more details.

Note: Extended command and Packet Error Checking Protocols are not supported.



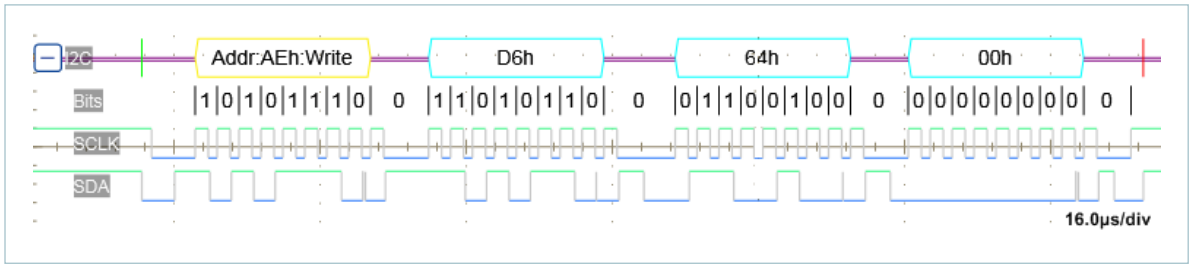
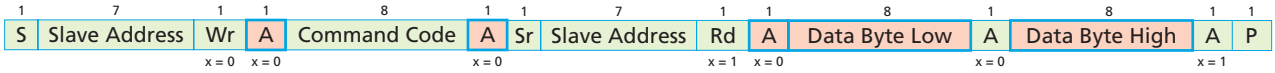


Figure 3 *— TON_DELAY COMMAND (60h)_WRITE WORD PROTOCOL*

Read Word protocol:



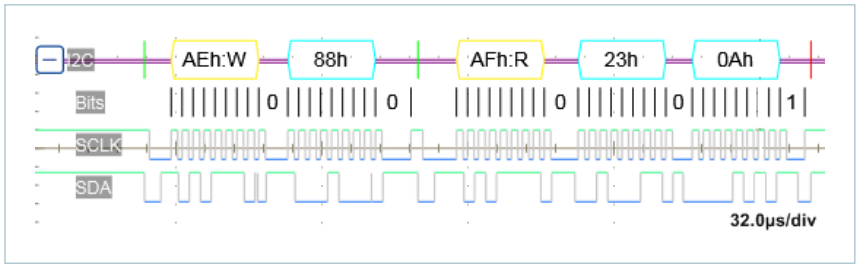
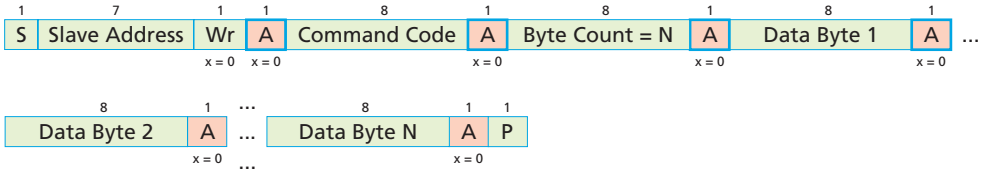


Figure 4 *— MFR_VIN_MIN COMMAND (A0h)_READ WORD PROTOCOL*

Write Block protocol:



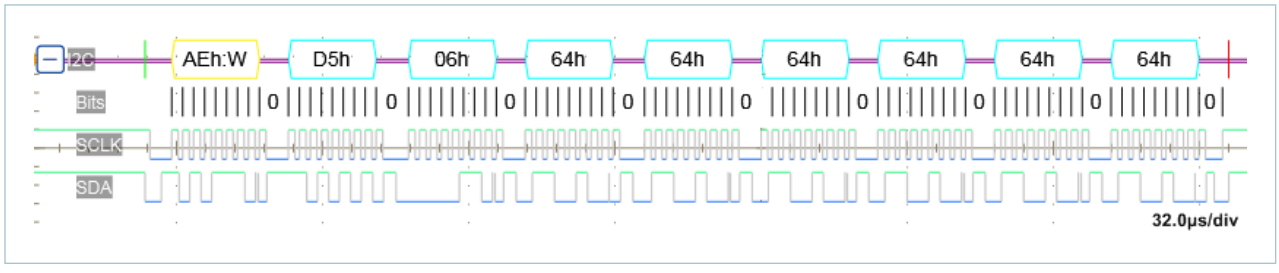
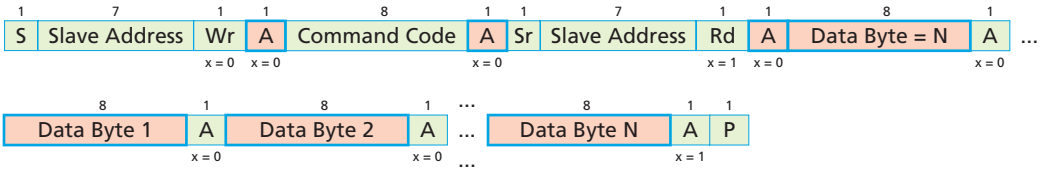


Figure 5 *— SET_ALL_THRESHOLDS COMMAND (D5h)_WRITE BLOCK PROTOCOL*

Read Block protocol:



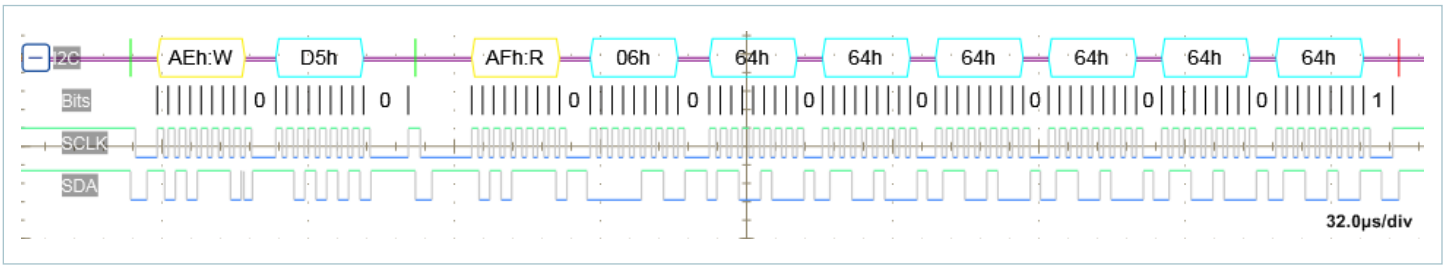
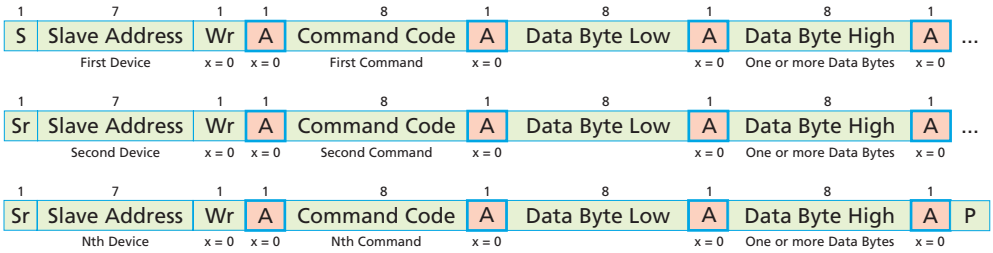


Figure 6 *— SET_ALL_THRESHOLDS COMMAND (D5h)_READ BLOCK PROTOCOL*

Write Group Command protocol:

Note that only one command per device is allowed in a group command.



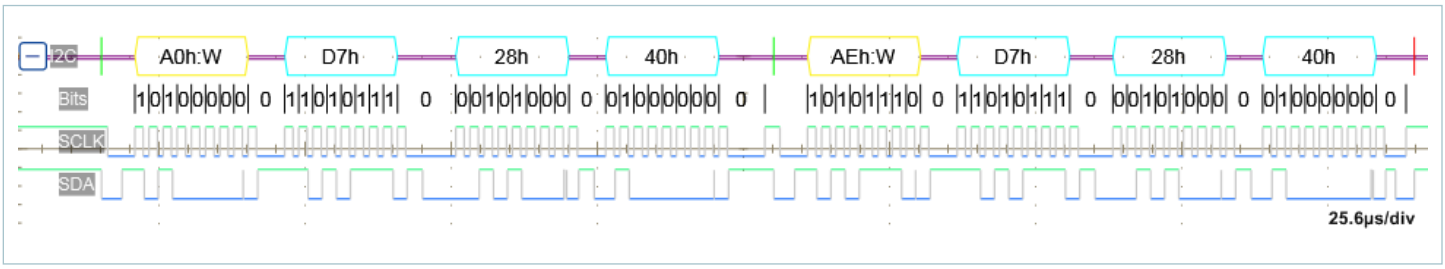


Figure 7 *— DISABLE_FAULT COMMAND (D7h)_WRITE*

Supported Commands Transaction type

A direct communication to the BCM controller and a simulated communication to non-PMBus™ devices is enabled by a page command. Supported command access privileges with a pre-selected PAGE are defined in the following table. Deviation from this table generates a communication error in STATUS_CML register.

Command	Code	PAGE Data Byte Access Type	
		00h	01h
PAGE	00h	R/W	R/W
OPERATION	01h	R	R/W
CLEAR_FAULTS	03h	W	W
CAPABILITY	19h	R	
OT_FAULT_LIMIT	4Fh		R/W
OT_WARN_LIMIT	51h		R/W
VIN_OV_FAULT_LIMIT	55h		R/W
VIN_OV_WARN_LIMIT	57h		R/W
IIN_OC_FAULT_LIMIT	5Bh		R/W
IIN_OC_WARN_LIMIT	5Dh		R/W
TON_DELAY	60h		R/W
STATUS_BYTE	78h	R/W	R
STATUS_WORD	79h	R	R
STATUS_IOUT	7Bh	R	R/W
STATUS_INPUT	7Ch	R	R/W
STATUS_TEMPERATURE	7Dh	R	R/W
STATUS_CML	7Eh	R/W	
STATUS_MFR_SPECIFIC	80h	R	R/W
READ_VIN	88h		R
READ_IIN	89h	R	R
READ_VOUT	8Bh		R
READ_IOUT	8Ch	R	R
READ_TEMPERATURE_1	8Dh	R	R
READ_POUT	96h	R	R
PMBUS_REVISION	98h	R	
MFR_ID	99h	R	
MFR_MODEL	9Ah	R	R
MFR_REVISION	9Bh	R	R
MFR_LOCATION	9Ch	R	R
MFR_DATE	9Dh	R	R
MFR_SERIAL	9Eh	R	R
MFR_VIN_MIN	A0h	R	R
MFR_VIN_MAX	A1h	R	R
MFR_VOUT_MIN	A4h	R	R
MFR_VOUT_MAX	A5h	R	R
MFR_IOUT_MAX	A6h	R	R
MFR_POUT_MAX	A7h	R	R
READ_K_FACTOR	D1h		R
READ_BCM_ROUT	D4h		R
SET_ALL_THRESHOLDS	D5h		R/W
DISABLE_FAULT	D7h		R/W

Page Command (00h)

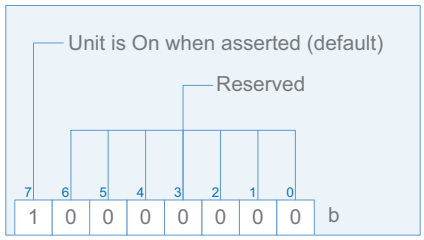
The page command data byte of 00h prior to a command call will address the BCM controller specific data and a page data byte of 01h would broadcast to the BCM. The value of the Data Byte corresponds to the pin name trailing number with the exception of 00h and FFh.

Data Byte	Description
00h	BCM controller
01h	BCM

OPERATION Command (01h)

The OPERATION command can be used to turn on and off the connected BCM.

If synchronous startup is required in the system, it is recommended to use the command from host PMBus in order to achieve simultaneous array startup.

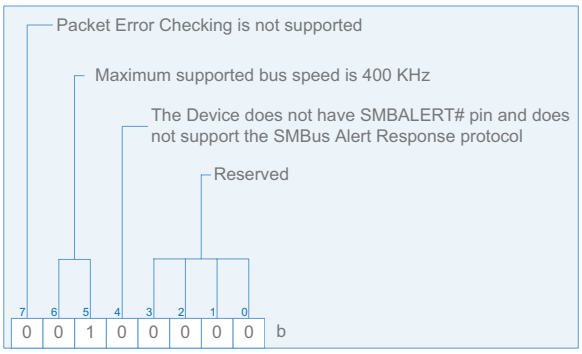


This command accepts only two data values: 00h and 80h. If any other value is sent the command will be rejected and a CML Data error will result.

CLEAR_FAULTS Command (03h)

This command clears all status bits that have been previously set. Persistent or active faults are re-asserted again once cleared. All faults are latched once asserted in the BCM controller. Registered faults will not be cleared when shutting down the BCM powertrain by recycling the BCM high side voltage, or sending the OPERATION command.

CAPABILITY Command (19h)



The BCM controller returns a default value of 20h. This value indicates that the PMBus™ frequency supported is up to 400kHz and that both Packet Error Checking (PEC) and SMBALERT# are not supported.

OT_FAULT_LIMIT Command (4Fh),
OT_WARN_ LIMIT Command (51h),
VIN_OV_FAULT_ LIMIT Command (55h),
VIN_OV_WARN_ LIMIT Command (57h),
IIN_OC_FAULT_ LIMIT Command (5Bh),
IIN_OC_WARN_ LIMIT Command (5Dh)

The values of these registers are set in non-volatile memory and can only be written when the BCMs are disabled.

The values of the above mentioned fault and warning are set by default to 100% of the respective BCM model supervisory limits. However, these limits can be set to a lower value. For example: In order for a limit percentage to be set to 80% one would send a write command with a (50h) Data Word.

Any values outside the range of (00h – 64h) sent by a host will be rejected, will not override the currently stored value and will set the Unsupported Data bit in STATUS_CML.

The SET_ALL_THRESHOLDS COMMAND (D5h) combines in one block overtemperature fault and warning limits, V_{HI} overvoltage fault and warning limits as well as I_{LO} overcurrent fault and warning limits. A delay prior to a read command of up to 200ms following a write of new value is required.

The VIN_UV_WARN_LIMIT (58h) and VIN_UV_FAULT_LIMIT (59h) are set by the factory and cannot be changed by the host. However, a host can disable the undervoltage setting using the DISABLE_FAULT COMMAND (D7h).

All FAULT_RESPONSE commands are unsupported. The BCM powertrain supervisory limits and powertrain protection will behave as described in the Electrical Specifications. In general, once a fault is detected, the BCM powertrain will shut down and attempt to auto-restart after a predetermined delay.

TON_DELAY Command (60h)

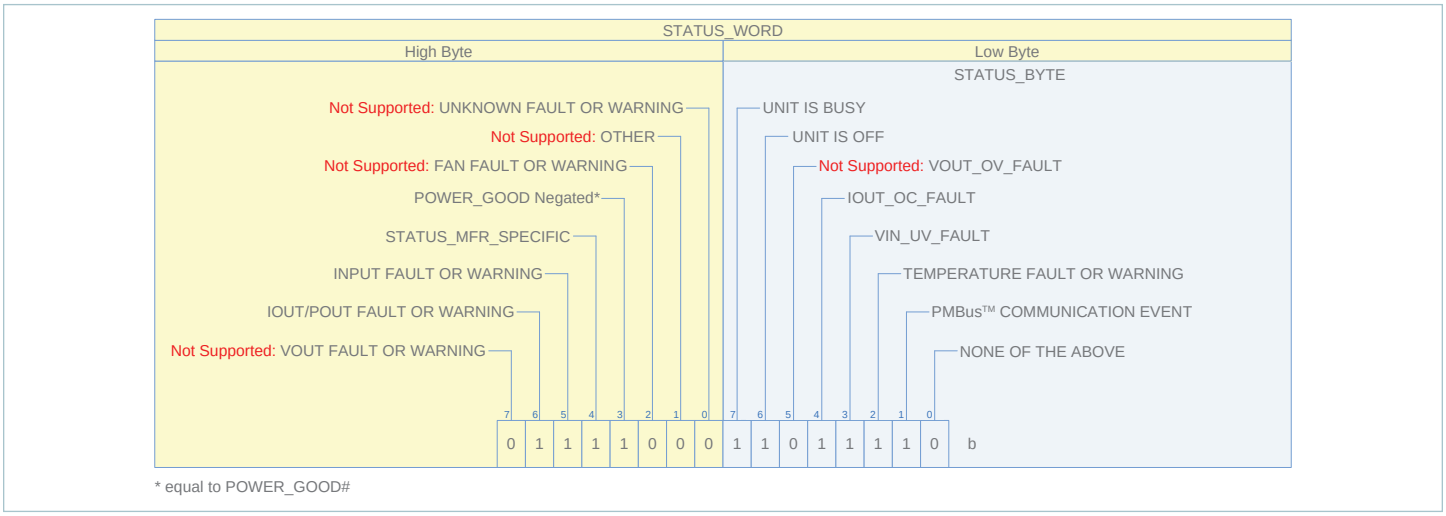
The value of this register word is set in non-volatile memory and can only be written when the BCMs are disabled.

The maximum possible delay is 100ms. Default value is set to (00h). Follow this equation below to interpret the reported value.

$$TON_DELAY_{ACTUAL} = t_{REPORTED} \bullet 10^{-3}(s)$$

Staggering startup in an array is possible with the TON_DELAY Command. This delay will be in addition to any startup delay inherent in the BCM module. For example: startup delay from application of V_{HI} is typically 20ms. When TON_DELAY is greater than zero, the set delay will be added to it.

STATUS_BYTE (78h) and STATUS_WORD (79h)



All fault or warning flags, if set, will remain asserted until cleared by the host or once the BCM and VDDB power is removed. This includes undervoltage fault, overvoltage fault, overvoltage warning, overcurrent warning, overtemperature fault, overtemperature warning, undertemperature fault, reverse operation, communication faults and analog controller shutdown fault.

Asserted status bits in all status registers, with the exception of STATUS_WORD and STATUS_BYTE, can be individually cleared. This is done by sending a data byte with one in the bit position corresponding to the intended warning or fault to be cleared. Refer to the PMBus™ Power System Management Protocol Specification – Part II – Revision 1.2 for details.

The POWER_GOOD# bit reflects the state of the device and does not reflect the state of the POWER_GOOD# signal limits. The POWER_GOOD_ON COMMAND (5Eh) and POWER_GOOD_OFF COMMAND (5Fh) are not supported. The POWER_GOOD# bit is set anytime the BCM is not in the active state, to indicate that the powertrain is inactive and not switching. The POWER_GOOD# bit is cleared when the BCM is in the active state, 5ms after the powertrain is activated allowing for soft-start to elapse. POWER_GOOD# and OFF bits cannot be cleared as they always reflect the current state of the device.

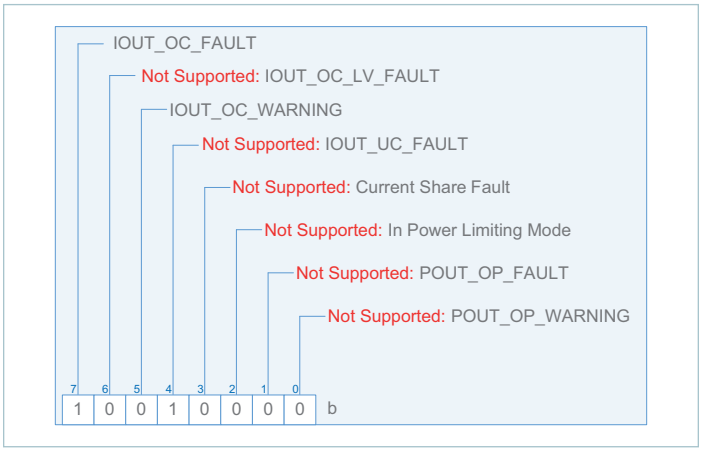
The Busy bit can be cleared using CLEAR_ALL Command (03h) or by writing either data value (40h, 80h) to PAGE (00h) using the STATUS_BYTE (78h).

Fault reporting, such as SMBALERT# signal output, and host notification by temporarily acquiring bus master status is not supported.

If the BCM controller is powered through VDDB, it will retain the last telemetry data and this information will be available to the user via a PMBus Status request. This is in agreement with the PMBus standard which requires that status bits remain set until specifically cleared. Note that in the case where the BCM V_{HI} is lost, the status will always indicate an undervoltage fault, in addition to any other fault that occurred.

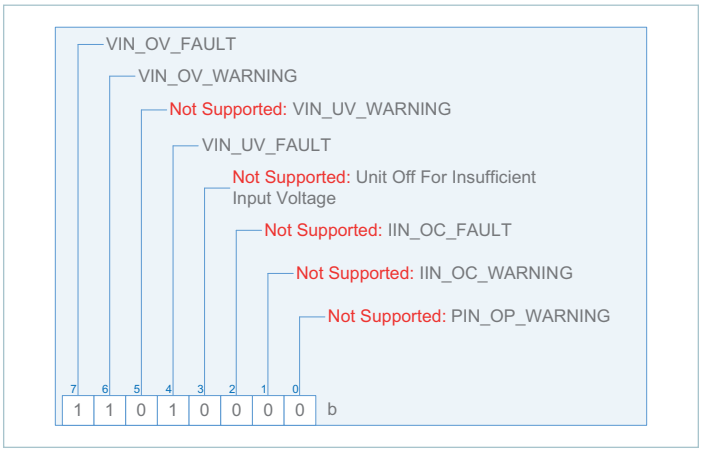
NONE OF THE ABOVE bit will be asserted if either the STATUS_MFR_SPECIFIC (80h) or the High Byte of the STATUS WORD is set.

STATUS_IOUT (7Bh)



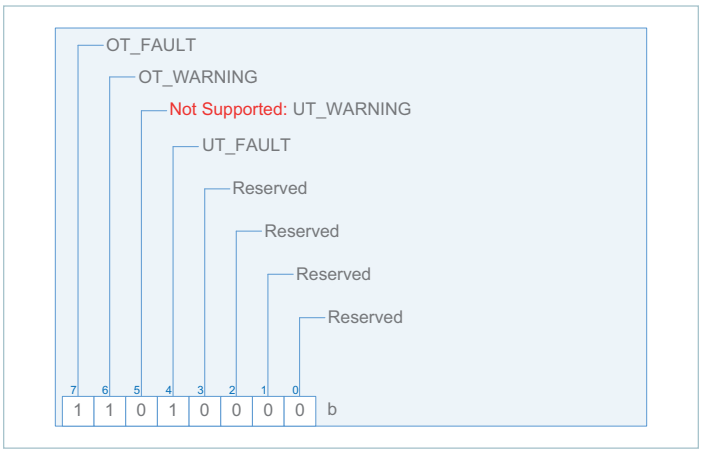
Unsupported bits are indicated above. A one indicates a fault.

STATUS_INPUT (7Ch)



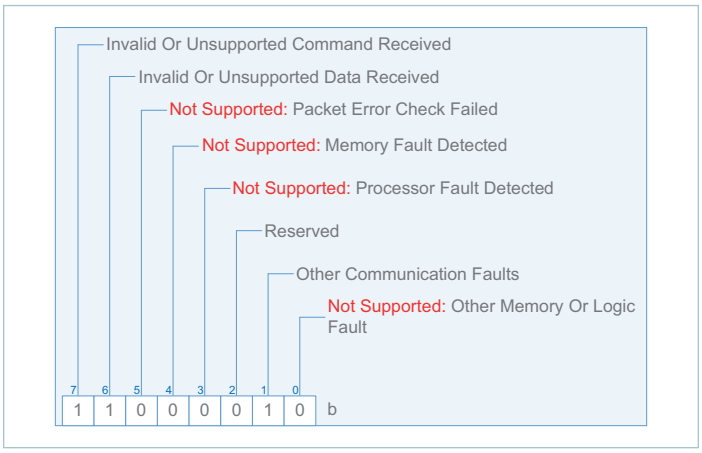
Unsupported bits are indicated above. A one indicates a fault.

STATUS_TEMPERATURE (7Dh)



Unsupported bits are indicated above. A one indicates a fault.

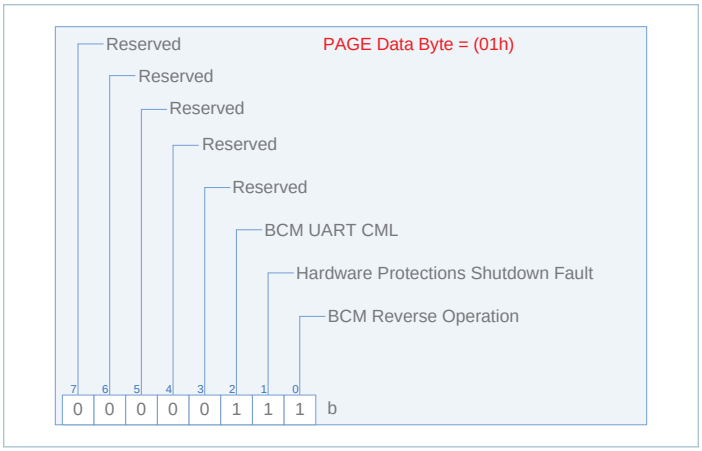
STATUS_CML (7Eh)



Unsupported bits are indicated above. A one indicates a fault.

The STATUS_CML data byte will be asserted when an unsupported PMBus™ command or data or other communication fault occurs.

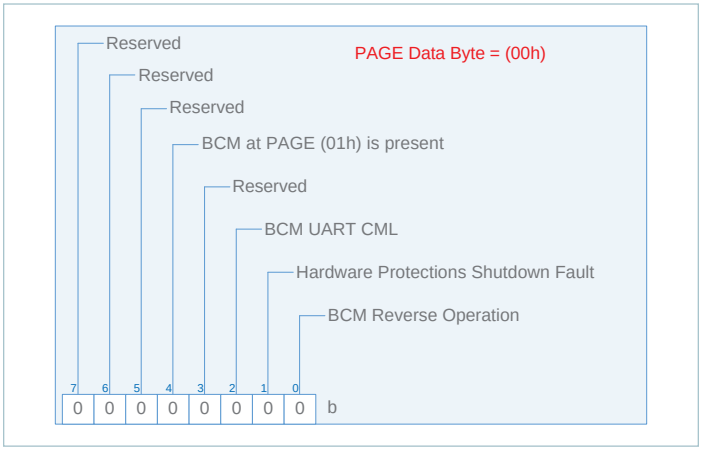
STATUS_MFR_SPECIFIC (80h)



The reverse operation bit, if asserted, indicates that the BCM is processing current in reverse. Reverse current reported value is not supported.

The BCM has hardware protections and supervisory limits. The hardware protections provide an additional layer of protection and have the fastest response time. The Hardware Protections Shutdown Fault, when asserted, indicates that at least one of the powertrain protection faults is triggered. This fault will also be asserted if a disabled fault event occurs after asserting any bit using the DISABLE_FAULTS COMMAND.

The BCM UART is designed to operate with the controller UART. If the BCM UART CML is asserted, it may indicate a hardware or connection issue between both devices.



When the PAGE COMMAND (00h) data byte is equal to (00h), the BCM Reverse operation, Analog Controller Shutdown Fault, and BCM UART CML bit will return the result of the active BCM. The BCM UART CML will also be asserted if the active BCM stops responding. The BCM must communicate at least once to the internal controller in order to trigger this FAULT. The BCM UART CML can be cleared using the PAGE (00h) CLEAR_FAULTS (03h) Command.

READ_VIN Command (88h)

If PAGE data byte is equal to (01h - 04h), command will return a reported individual BCM's HI side voltage in the following format:

$$V_{HI_ACTUAL} = V_{HI_REPORTED} \bullet 10^{-1}(V)$$

READ_IIN Command (89h)

If PAGE data byte is equal to (01h - 04h), command will return a reported individual BCM's HI side current in the following format:

$$I_{HI_ACTUAL} = I_{HI_REPORTED} \bullet 10^{-3}(A)$$

If PAGE data byte is equal (00h), command will return the sum of active BCM's HI side current.

READ_VOUT Command (8Bh)

If PAGE data byte is equal to (01h - 04h), command will return a reported individual BCM's LO side voltage in the following format:

$$V_{LO_ACTUAL} = V_{LO_REPORTED} \bullet 10^{-1}(V)$$

READ_IOUT Command (8Ch)

If PAGE data byte is equal to (01h - 04h), command will return a reported individual BCM's LO side current in the following format:

$$I_{LO_ACTUAL} = I_{LO_REPORTED} \bullet 10^{-2}(A)$$

If PAGE data byte is equal (00h), command will return the sum of active BCM's LO side current.

READ_TEMPERATURE_1 Command (8Dh)

If PAGE data byte is equal to (01h - 04h), command will return a reported individual BCM's temperature in the following format:

$$T_{ACTUAL} = \pm T_{REPORTED}\ (°C)$$

If PAGE data byte is equal (00h), command will return the maximum temperature of active BCM's.

READ_POUT Command (96h)

If PAGE data byte is equal to (01h - 04h), command will return a reported individual BCM's LO side power in the following format:

$$P_{LO_ACTUAL} = P_{LO_REPORTED}\ (W)$$

If PAGE data byte is equal to (00h), command will return the sum of active BCM's LO side power.

MFR_VIN_MIN Command (A0h), MFR_VIN_MAX Command (A1h), MFR_VOUT_MIN Command (A4h), MFR_VOUT_MAX Command (A5h), MFR_IOUT_MAX Command (A6h), MFR_POUT_MAX Command (A7h)

These values are set by the factory and indicate the device HI side/ LO side voltage and LO side current range and LO side power capacity.

The internal controller will report the rated BCM HI side voltage minimum and maximum in Volts, LO side voltage minimum and maximum in Volts, LO side current maximum in Amperes and LO side power maximum in Watts.

If PAGE data byte is equal to (00h) then:

- MFR_VIN_MIN COMMAND (A0h) will return the highest MFR_VIN_MIN of all active BCMs
- MFR_VIN_MAX COMMAND (A1h) will return the lowest MFR_VIN_MAX of all active BCMs
- MFR_VOUT_MIN COMMAND (A4h) will return the highest MFR_VOUT_MIN of all active BCMs
- MFR_VOUT_MAX COMMAND (A5h) will return the lowest MFR_VOUT_MAX of all active BCMs
- MFR_IOUT_MAX COMMAND (A6h) will return the SUM of MFR_IOUT_MAX of all active BCMs
- MFR_POUT_MAX COMMAND (A7h) will return the SUM of MFR_POUT_MAX of all active BCMs

READ_K_FACTOR Command (D1h)

If PAGE data byte is equal to (01h - 04h), command will return a reported individual BCM's K factor in the following format:

$$K_FACTOR_{ACTUAL} = K_FACTOR_{REPORTED} \bullet 2^{-16} (V/V)$$

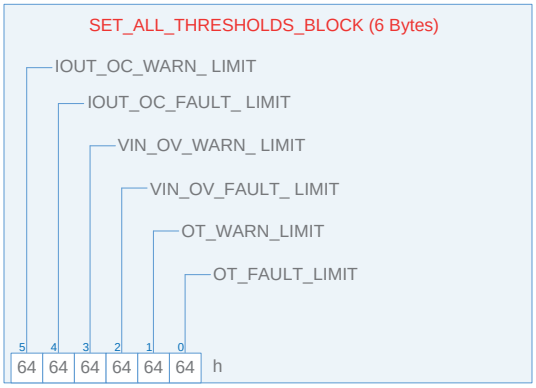
The K factor is defined in a BCM to represent the ratio of the transformer winding and hence is equal to V_{LO} / V_{HI}.

READ_BCM_ROUT Command (D4h)

If PAGE data byte is equal to (01h - 04h), command will return a reported individual BCM's LO side resistance in the following format:

$$BCM_R_{LO_ACTUAL} = BCM_R_{LO_REPORTED} \bullet 10^{-5} (\Omega)$$

SET_ALL_THRESHOLDS Command (D5h)



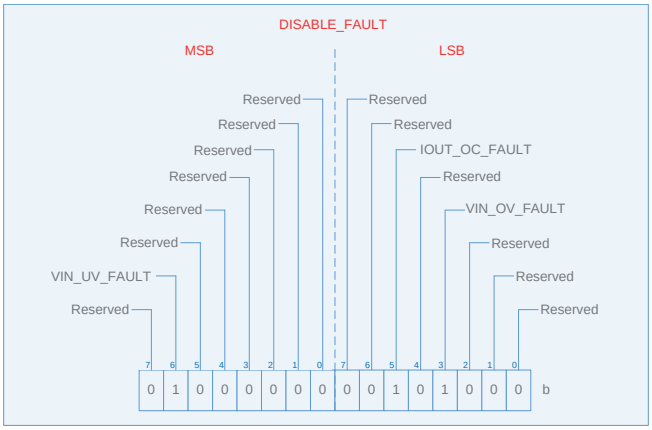
The values of this register block are set in non-volatile memory and can only be written when the BCMs are disabled.

This command provides a convenient way to configure all of the limits, or any combination of limits described previously using one command.

V_{HI} overvoltage, overcurrent and overtemperature values are all set to 100% of the specified supervisory limits by default and can only be set to a lower percentage.

To leave a particular threshold unchanged, set the corresponding threshold data byte to a value greater than (64h).

DISABLE_FAULT Command (D7h)



Unsupported bits are indicated above. A one indicates that the supervisory fault associated with the asserted bit is disabled.

The values of this register block are set in non-volatile memory and can only be written when the BCMs are disabled.

This command allows the host to disable the supervisory faults and respective statuses. It does not disable the powertrain analog protections or warnings with respect to the set limits in the SET_ ALL_THRESHOLDS Command.

The HI side undervoltage can only be disabled to a pre-set low limit as shown in the functional reporting range in the BCM data sheet.

The BCM Controller Implementation vs. PMBus™ Specification Rev 1.2

The BCM controller is an I²C compliant, SMBus™ compatible device and PMBus command compliant device. This section denotes some deviation, perceived as differences from the PMBus Part I and Part II specification Rev 1.2.

1. The PMBus interface meets all Part I and II PMBus specification requirements with the following differences to the transport requirement.

Unmet DC parameter Implementation vs SMBus™ spec						
Symbol	Parameter	PMBus Interface		SMBus™ Rev 2.0		Units
		Min	Max	Min	Max	
V_{IL}[a]	Input Low Voltage	-	0.99	-	0.8	V
V_{IH}[a]	Input High Voltage	2.31	-	2.1	V_{VDD_IN}	V
I_{LEAK_PIN}[b]	Input Leakage per Pin	10	22	-	±5	µA

[a] V_{VDD_IN} = 3.3V
[b] V_{BUS} = 5V

2. The BCM accepts 38 PMBus command codes. Implemented commands execute functions as described in the PMBus specification.

- Deviations from the PMBus specification:

a. Section 15, fault related commands

- The limits and Warnings unit implemented is percentage (%) a range from decimal (0-100) of the factory set limits.

3. The unsupported PMBus command code response as described in the Fault Management and Reporting:

- Deviations from the PMBus specification:

a. PMBus section 10.2.5.3, exceptions

- The busy bit of the STATUS_BYTE as implemented can be cleared (80h). In order to maintain compatibility with the specification, (40h) can also be used.

- Manufacturer Implementation of the PMBus Spec

a. PMBus section 10.5, setting the response to a detected fault condition

- All powertrain responses are pre-set and cannot be changed.

b. PMBus section 10.6, reporting faults and warnings to the Host

- SMBALERT# signal and Direct PMBus Device to Host Communication are not supported. However, the PMBus™ interface will set the corresponding fault status bits and will wait for the host to poll.

c. PMBus section 10.7, clearing a shutdown due to a fault

- There is no RESET pin or EN pin in the BCM. Cycling power to the BCM will not clear a BCM Shutdown. The BCM will clear itself once the fault condition is removed.

d. PMBus Section 10.8.1, corrupted data transmission faults:

- Packet error checking is not supported.

Data Transmission Faults Implementation

This section describes data transmission faults as implemented in the BCM controller.

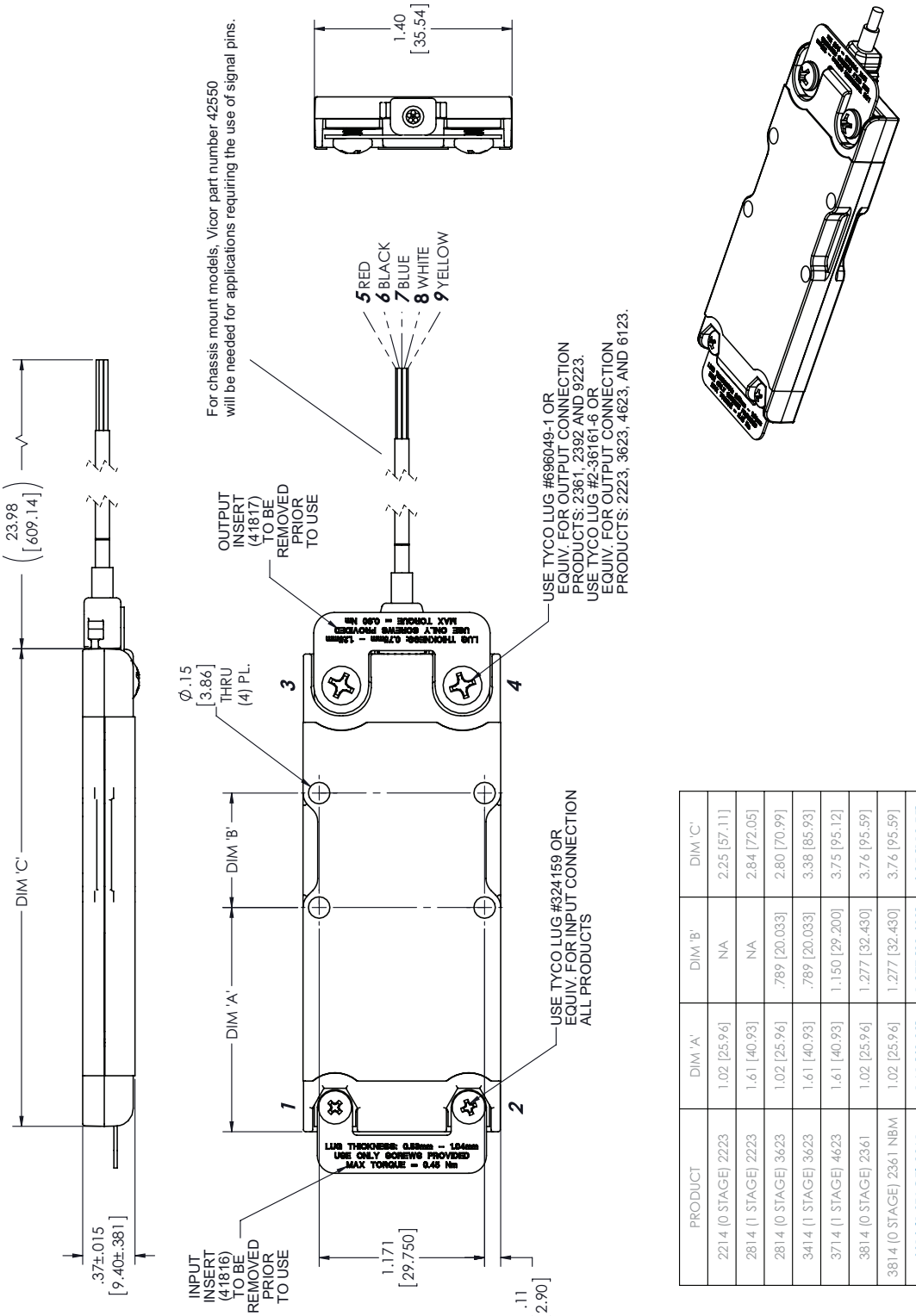
Section	Description	Response to Host		STATUS_BYTE	STATUS_CML		Notes
		NAK	FFh	CML	Other Fault	Unsupported Data	
10.8.1	Corrupted data						No response; PEC not supported
10.8.2	Sending too few bits			X	X		
10.8.3	Reading too few bits			X	X		
10.8.4	Host sends or reads too few bytes			X	X		
10.8.5	Host sends too many bytes	X		X		X	
10.8.6	Reading too many bytes		X	X	X		
10.8.7	Device busy	X	X				Device will ACK own address BUSY bit in STATUS_BYTE even if STATUS_WORD is set

Data Content Faults Implementation

This section describes data content fault as implemented in the BCM controller.

Section	Description	Response to Host	STATUS_BYTE	STATUS_CML			Notes
		NAK	CML	Other Fault	Unsupported Command	Unsupported Data	
10.9.1	Improperly Set Read Bit In The Address Byte	X	X	X			
10.9.2	Unsupported Command Code	X	X		X		
10.9.3	Invalid or Unsupported Data		X			X	
10.9.4	Data Out of Range		X			X	
10.9.5	Reserved Bits						No response; not a fault

BCM in VIA Package Chassis (Lug) Mount Package Mechanical Drawing



NOTES:

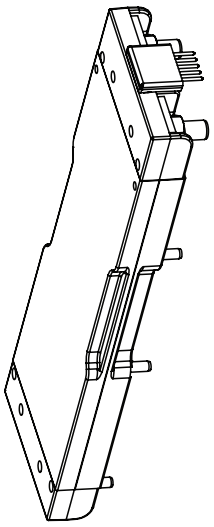
1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.

2- SEE PRODUCT DATA SHEET FOR PIN DESIGNATIONS.

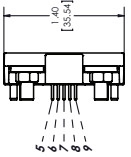
PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'
2214 (0 STAGE) 2223	1.02 [25.96]	NA	2.25 [57.11]
2814 (1 STAGE) 2223	1.61 [40.93]	NA	2.84 [72.05]
2814 (0 STAGE) 3623	1.02 [25.96]	.789 [20.033]	2.80 [70.99]
3414 (1 STAGE) 3623	1.61 [40.93]	.789 [20.033]	3.38 [85.93]
3714 (1 STAGE) 4623	1.61 [40.93]	1.150 [29.200]	3.75 [95.12]
3814 (0 STAGE) 2361	1.02 [25.96]	1.277 [32.430]	3.76 [95.59]
3814 (0 STAGE) 2361 NBM	1.02 [25.96]	1.277 [32.430]	3.76 [95.59]
4414 (1 STAGE) 2361	**1.61 [40.93]**	**1.277 [32.430]**	**4.35 [110.55]**
4414 (1 STAGE) 6123	1.61 [40.93]	1.757 [44.625]	4.35 [110.55]
5614 (1 STAGE) 2392	1.61 [40.93]	2.490 [63.250]	5.57 [141.37]
5614 (1 STAGE) 9223	1.61 [40.93]	2.970 [75.445]	5.57 [141.37]

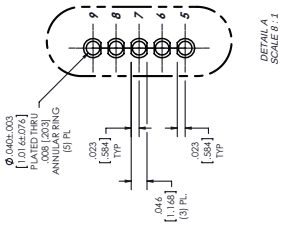
BCM in VIA Package PCB (Board) Mount Package Mechanical Drawing and Recommended Hole Pattern

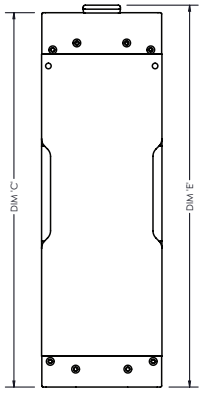
PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'	DIM 'D'	DIM 'E'	DIM 'F'	DIM 'G'
38.14 (0 STAGE) 2361	1.02 [25.96]	1.277 [32.430]	3.76 [95.59]	3.368 [85.554]	3.85 [97.80]	.850 [21.590]	3.632 [92.243]
38.14 (0 STAGE) 2361 NBM	1.02 [25.96]	1.277 [32.430]	3.76 [95.59]	3.368 [85.554]	3.85 [97.780]	.850 [21.590]	3.632 [92.243]
4414 (1 STAGE) 2361	**1.61 [40.93]**	**1.277 [32.430]**	**4.35 [110.55]**	**3.957 [100.517]**	**4.44 [112.76]**	**1.439 [36.553]**	**4.221 [107.206]**
56.14 (1 STAGE) 2392	1.61 [40.93]	2.490 [63.250]	5.57 [141.37]	5.171 [131.337]	5.65 [143.58]	1.439 [36.553]	5.434 [138.026]

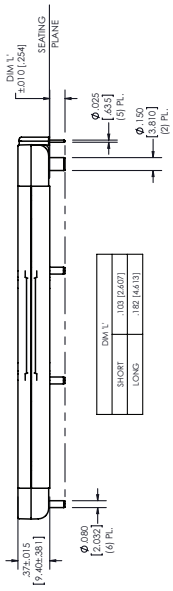


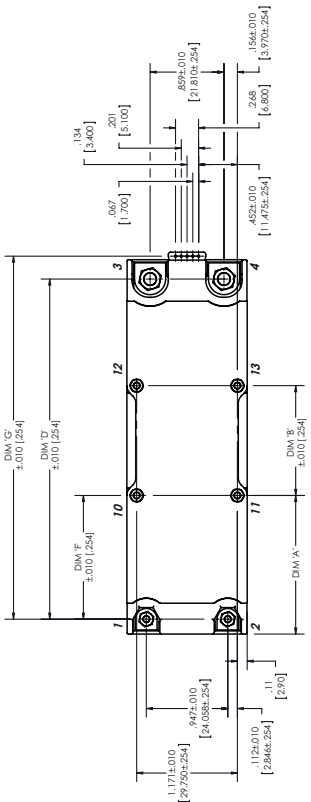
NOTES:
1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.
2- SEE PRODUCT DATA SHEET FOR PIN DESIGNATIONS.

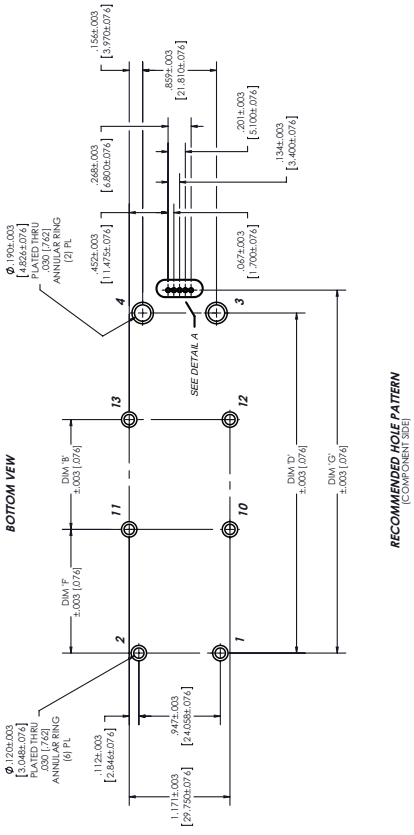












Revision History

Revision	Date	Description	Page Number(s)
1.0	03/3/16	Initial release	n/a
1.1	05/2/16	New Power Pin Nomenclature	All
1.2	06/17/16	Notes update	2, 3, 10
1.3	08/01/16	Charts format update	13, 14, 15
1.4	09/26/16	Value of R correction for READ_BCM_ROUT	25
1.5	10/28/16	Content improvements PMBus Supported Commands update Pin Finish update	All 26 – 37 17

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Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715

email
Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com