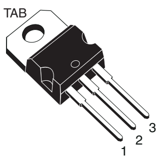
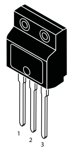
N-channel 620 V, 0.95 Ω typ., 7.0 A Power MOSFET in I²PAKFP and TO-220

Datasheet - production data

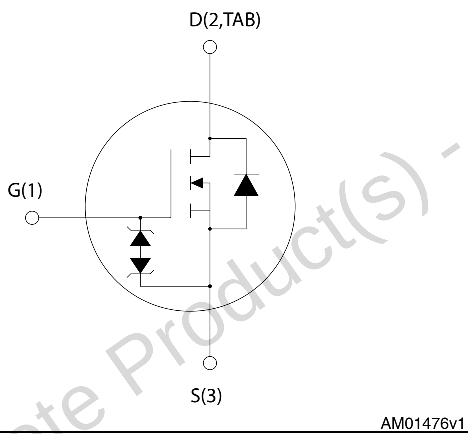


TO-220



I²PAKFP

Figure 1. Internal schematic diagram



Features

Order codes	V_{DSS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STFILED627	620 V	< 1.2 Ω	7.0 A	30 W
STPLED627				

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- LED lighting applications

Description

These Power MOSFETs boast extremely low on-resistance and very good dv/dt capability, rendering them suitable for buck-boost and flyback topologies.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STFILED627	LED627	I²PAKFP	Tube
STPLED627		TO-220	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		I²PAKFP	TO-220	
V_{DS}	Drain-source voltage	620		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	7.0(1)		A
I_D	Drain current (continuous) at T_C = 100 °C	4.0(1)		A
I_{DM}(2)	Drain current (pulsed)	22(1)		A
P_{TOT}	Total dissipation at T_C = 25 °C	30	90	W
I_{AR}(3)	Avalanche current, repetitive or not-repetitive	5.5		A
E_{AS}(4)	Single pulse avalanche energy	140		mJ
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	2.5		kV
dv/dt(5)	Peak diode recovery voltage slope	12		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2500		V
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. Pulse width limited by T_j max.
4. Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.
5. $I_{SD} \leq 5.5$ A, di/dt $\leq$ 400 A/µs, V_{DD} = 80% $V_{(BR)DSS}$, $V_{DSpeak} \leq V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	I²PAKFP	TO-220	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	4.17	1.39	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max.	62.5		°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	620			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 620 V V_{DS} = 620 V, T_C = 125 °C			0.8 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 9	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.6	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.8 A		0.95	1.2	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	890 110 18	-	pF
C_{oss}	Output capacitance		-	110	-	pF
C_{rss}	Reverse transfer capacitance		-	18	-	pF
$C_{oss(er)}$ (1)	Equivalent output capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 480 V	-	28	-	pF
$C_{oss(tr)}$ (2)	Equivalent output capacitance time related		-	63	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 496 V, I_D = 5.5 A, V_{GS} = 10 V (see *Figure 18*)	-	35	-	nC
Q_{gs}	Gate-source charge		-	4.5	-	nC
Q_{gd}	Gate-drain charge		-	23	-	nC

1. It is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.
2. It is defined as a constant equivalent capacitance giving the same storage energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 310 V, I_D = 2.75 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 17*)	-	22	-	ns
t_r	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off-delay time		-	49	-	ns
t_f	Fall time		-	20	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5.5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		27	A
V_{SD} (2)	Forward on voltage	I_{SD} = 5.5 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 5.5 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 22*)	-	290		ns
Q_{rr}	Reverse recovery charge			1.9		µC
I_{RRM}	Reverse recovery current			13.5		A
t_{rr}	Reverse recovery time	I_{SD} = 5.5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 22*)	-	335		ns
Q_{rr}	Reverse recovery charge			2.4		µC
I_{RRM}	Reverse recovery current			14.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage (I_D = 0)	Igs = ± 1 mA	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

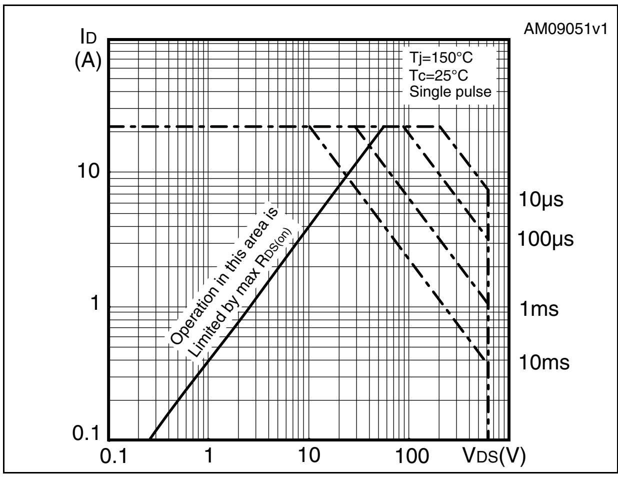


Figure 3. Thermal impedance for TO-220

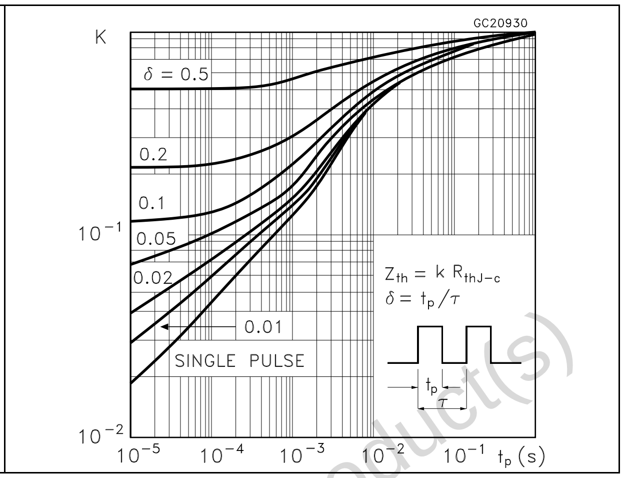


Figure 4. Safe operating area for I²PAKFP

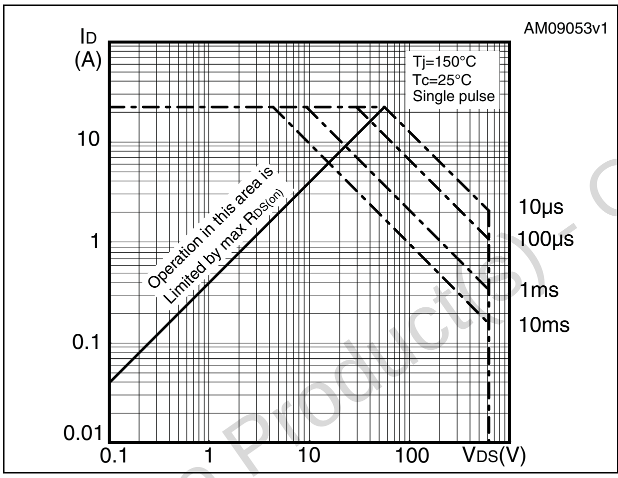


Figure 5. Thermal impedance for I²PAKFP

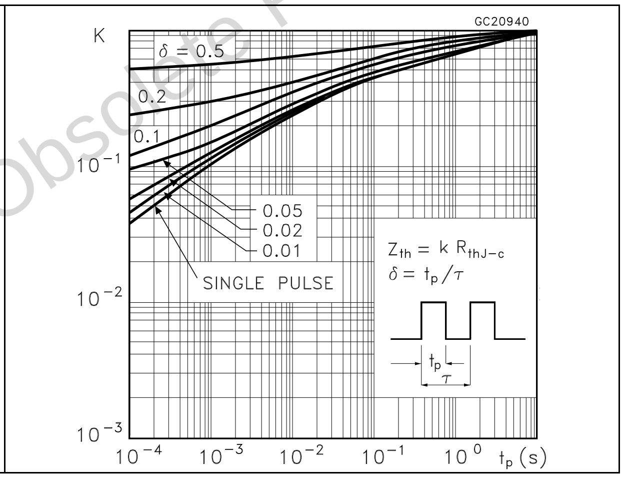


Figure 6. Output characteristics

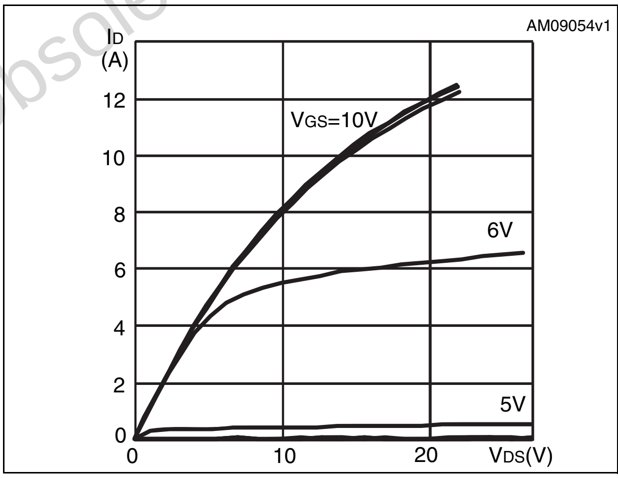


Figure 7. Transfer characteristics

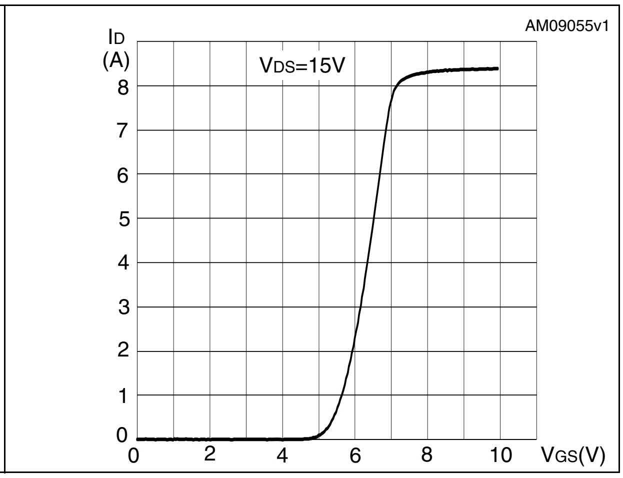


Figure 8. Gate charge vs gate-source voltage

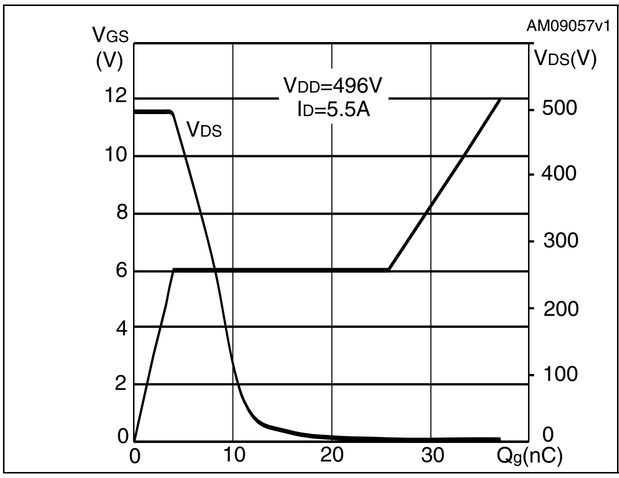


Figure 9. Static drain-source on-resistance

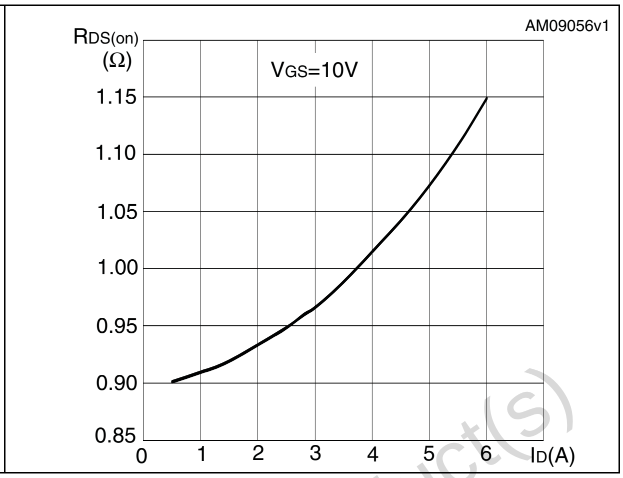


Figure 10. Capacitance variations

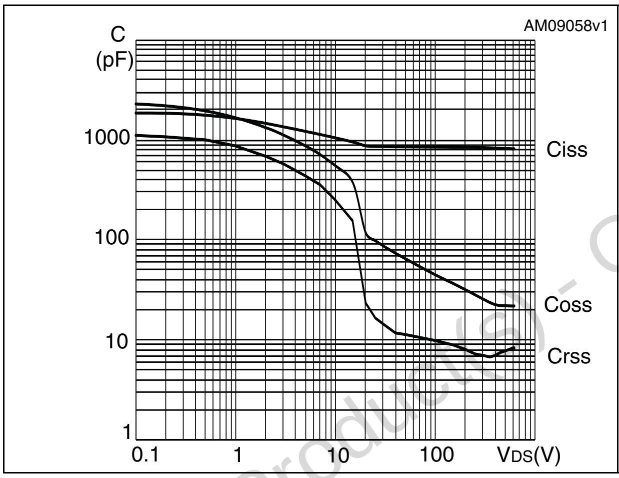


Figure 11. Output capacitance stored energy

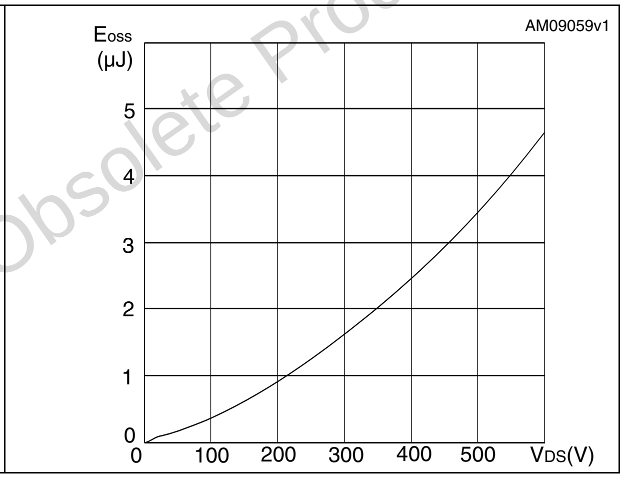


Figure 12. Normalized gate threshold voltage vs temperature

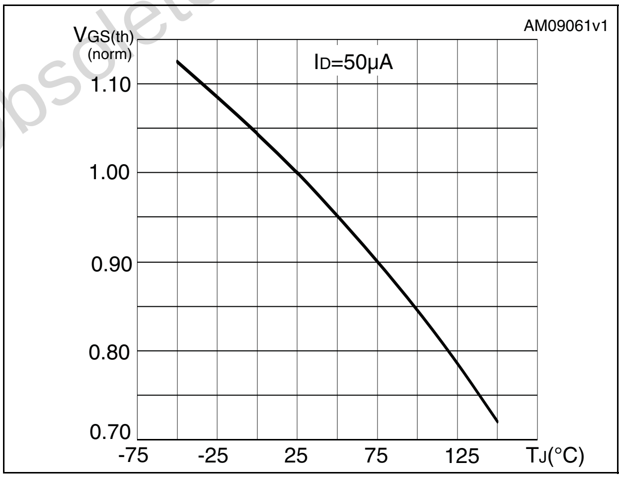


Figure 13. Normalized on-resistance vs temperature

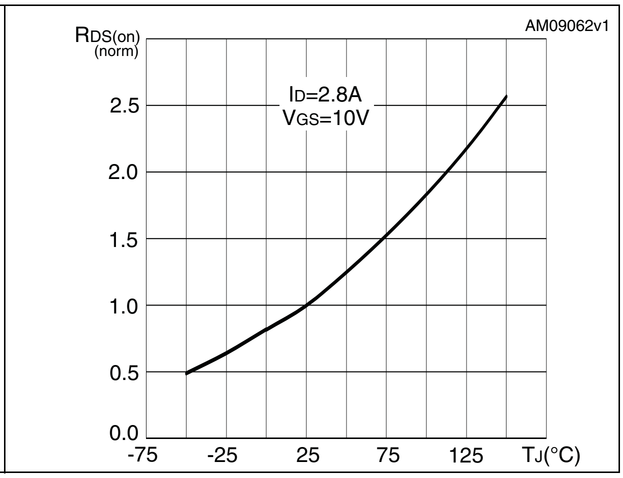


Figure 14. Normalized B_{VDSS} vs temperature

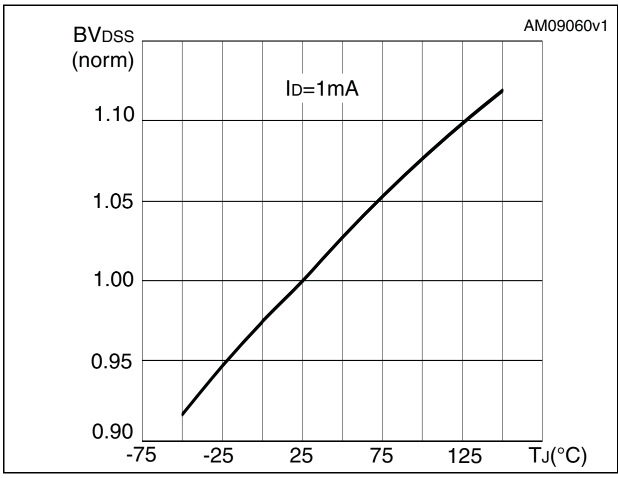


Figure 15. Source-drain diode forward characteristics

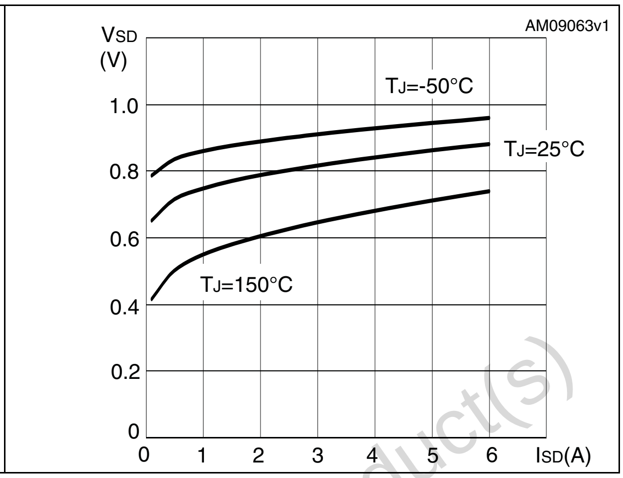
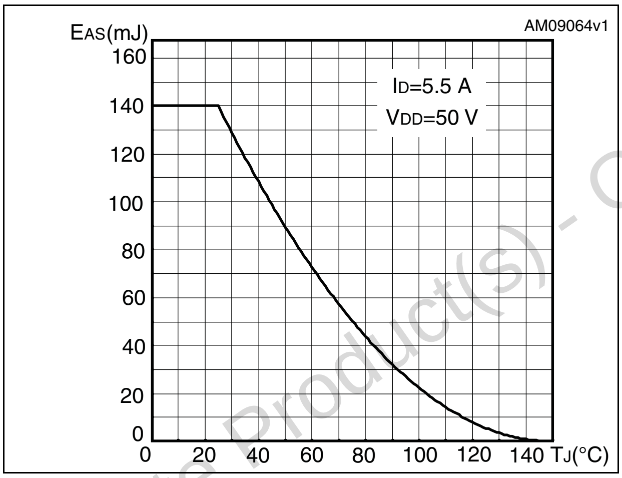


Figure 16. Maximum avalanche energy vs temperature



3 Test circuits

Figure 17. Switching times test circuit for resistive load

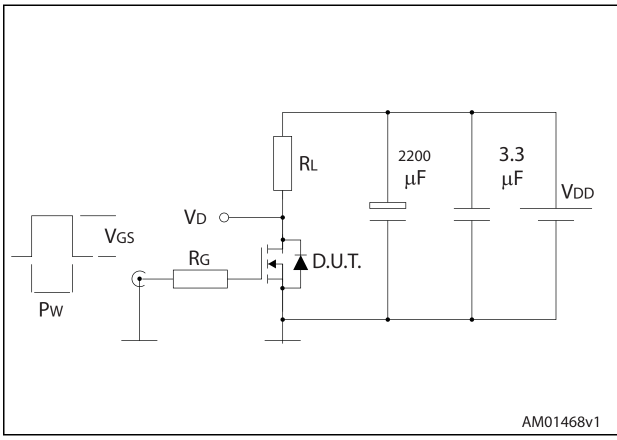


Figure 18. Gate charge test circuit

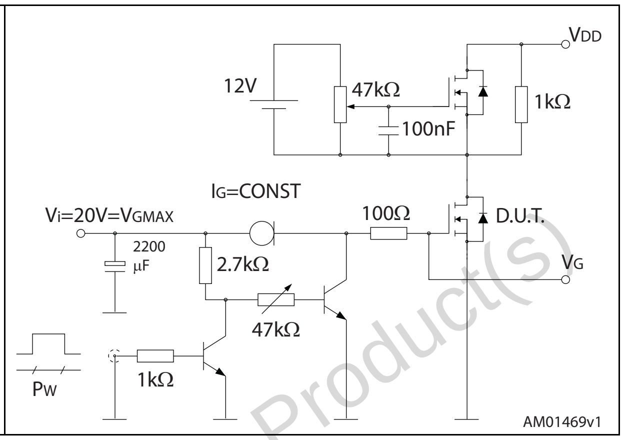


Figure 19. Test circuit for inductive load switching and diode recovery times

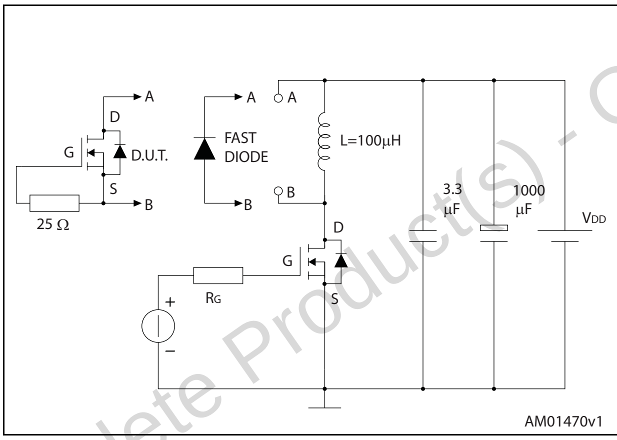


Figure 20. Unclamped Inductive load test circuit

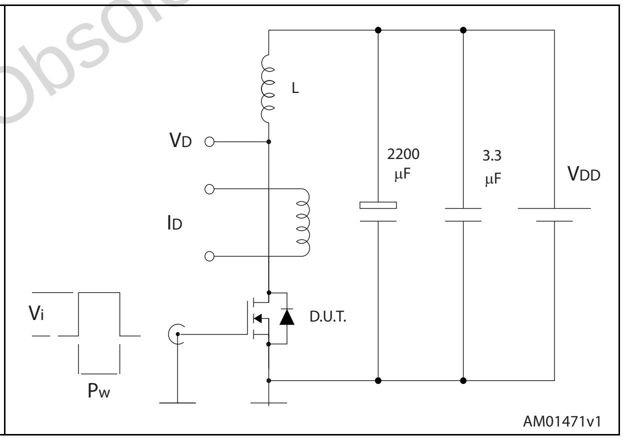


Figure 21. Unclamped inductive waveform

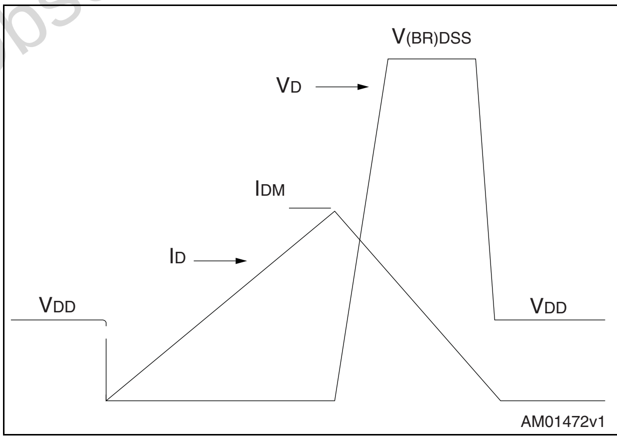
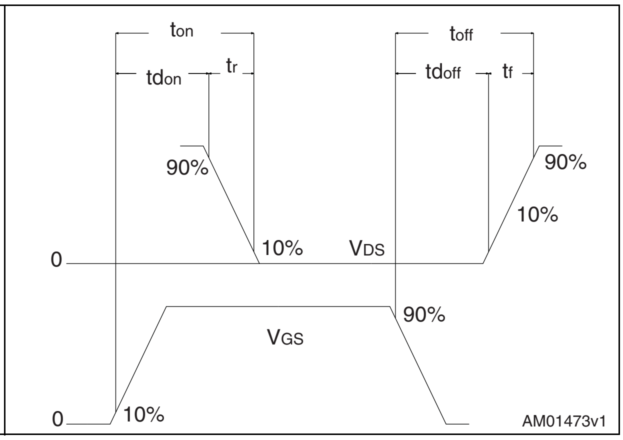


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. I^2PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 23. I²PAKFP (TO-281) drawings

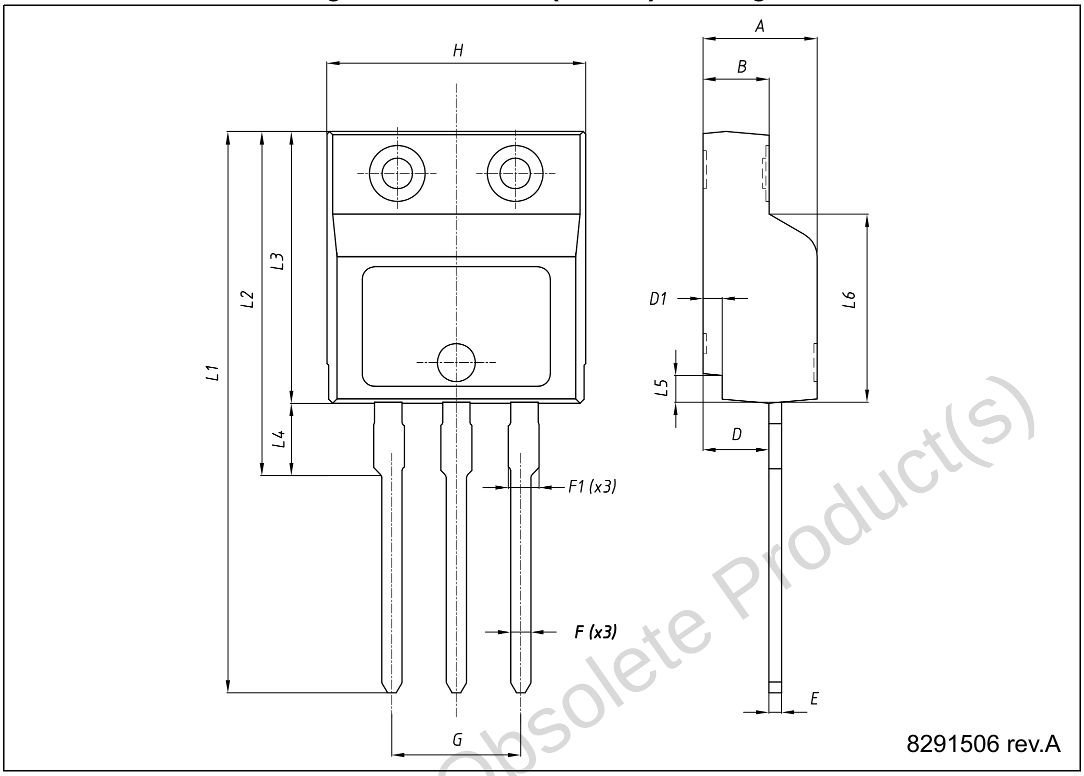
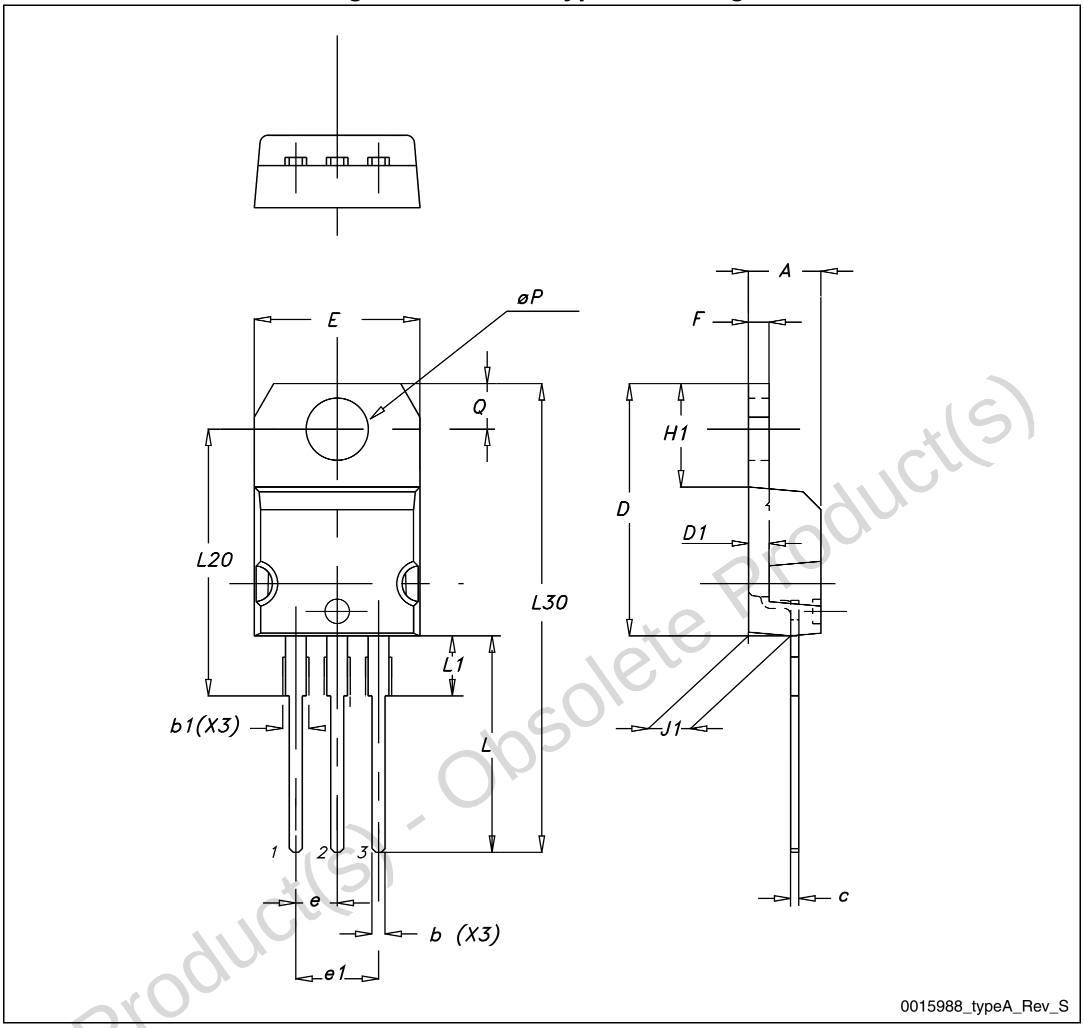


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 24. TO-220 type A drawings



5 Revision history

Table 11. Document revision history

Date	Revision	Changes
28-Aug-2013	1	First release.