PI6C557-01BQ

PCIe 3.0 Clock Generator with 1 HCSL Outputs

Features

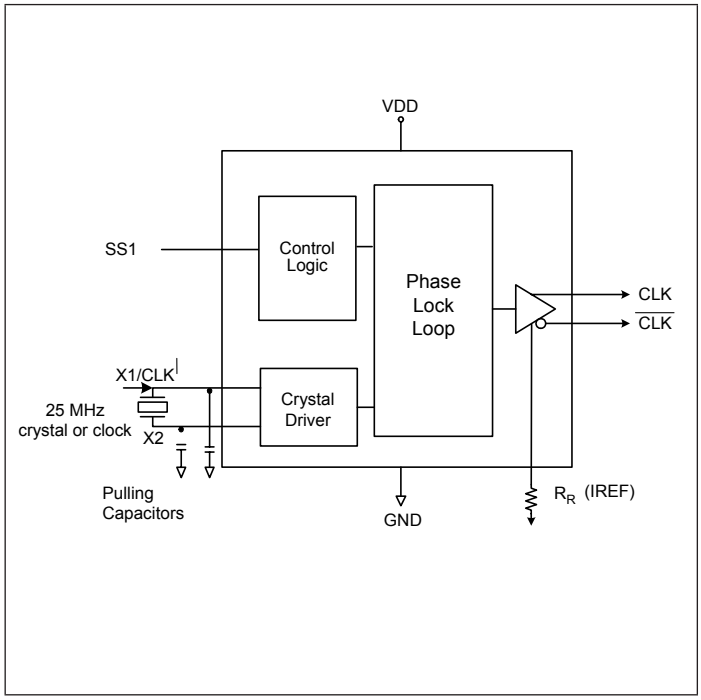
- PCIe® 3.0 compliant
  - Phase jitter - 0.45ps RMS (High Freq. Typ.)
- LVDS compatible output
- Supply voltage of 3.3V ±10%
- 25MHz crystal or clock input frequency
- HCSL outputs, 0.8V Current mode differential pair
- Jitter 35ps cycle-to-cycle (typ)
- Spread of -0.5% and no spread
- Industrial temperature range
- Spread Bypass option available
- Spread selection via external pins
- Packaging: (Pb-free and Green)
  - 16-pin TQFN

Description

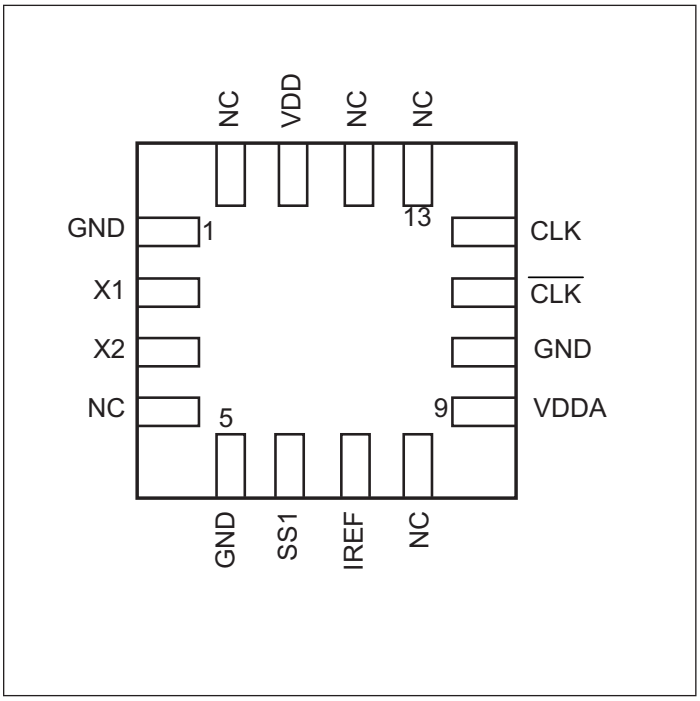
The PI6C557-01BQ is a spread spectrum clock generator compliant to PCI Express® 3.0 and Ethernet requirements. The device is used for Automotive systems.

The PI6C557-01BQ provides one differential (HCSL) or LVDS spread spectrum output. Using Pericom's patented Phase-Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces one pair of differential outputs (HCSL) at 100MHz. It also provides spread selection of -0.5% and no spread.

Block Diagram



Pin Configuration (16-Pin TQFN)



Pin Description

Pin #	Pin Name	I/O Type	Description
1	GND	Power	Connect to ground
2	X1	Input	Crystal or reference clock in
3	X2	Output	Xtal out. Leave unconnected for clock input.
4	NC	-	No connect. Must not be connected to GND
5	GND	Power	Connect to ground
6	SS1	Input	Spread select 1. Internall pull up resistor
7	IREF	Output	475Ω precision resistor attached to this pin is connected to the internal current reference.
8	NC	-	No connect. Must not be connected to GND
9	VDDA	Power	Connect to 3.3V source
10	GND	Power	Connect to ground
11	$\overline{\text{CLK}}$	Output	HCSL complimentary clock output
12	CLK	Output	HCSL clock output
13	NC	-	No connect. Must not be connected to GND
14	NC	-	No connect. Must not be connected to GND
15	VDD	Power	Connect to 3.3V source for OSC and core
16	NC	-	No connect. Must not be connected to GND

Table 1: Spread Selection Table

SS1	Spread
0	Down -0.5%
1	No Spread

Application Information

Decoupling Capacitors

Decoupling capacitors of 0.01µF should be connected between each V_{DD} pin and the ground plane and placed as close to the V_{DD} pin as possible.

Crystal

Use a 25MHz fundamental mode parallel resonant crystal with less than 300PPM of error across temperature.

Crystal Capacitors

C_L = Crystals's load capacitance in pF

Crystal Capacitors (pF) = (C_L - 8) *2

For example, for a crystal with 16pF load caps, the external effective crystal cap would be 16 pF. (16-8)*2=16.

Current Source (IREF) Reference Resistor - R_R

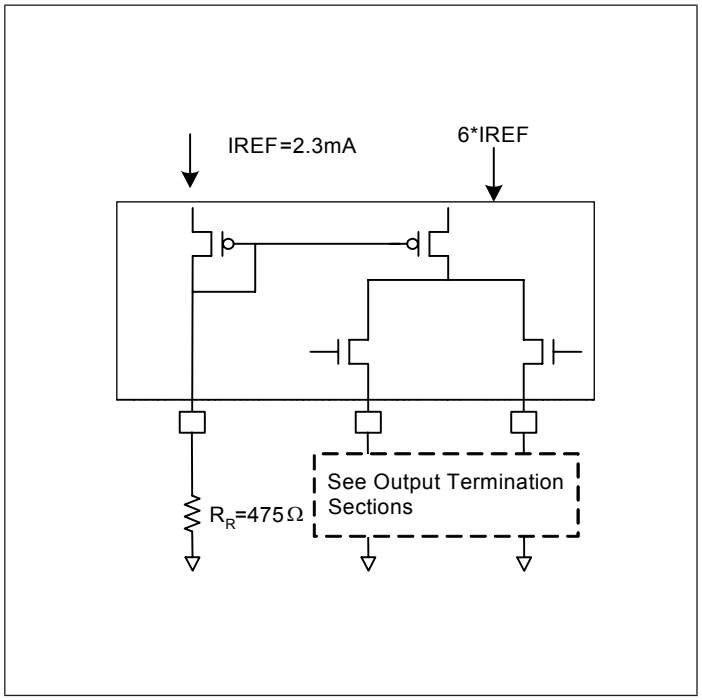
If board target trace impedance is 50Ω,
then R_R = 475Ω providing an IREF of 2.32 mA. The output current (I_{OH}) is 6*IREF.

Output Termination

The PCI Express differential clock outputs of the PI6C557-01BQ are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the PCI Express Layout Guidelines section.

The PI6C557-01BQ can be configured for LVDS compatible voltage levels. See the LVDS Compatible Layout Guidelines section.

Output Structures



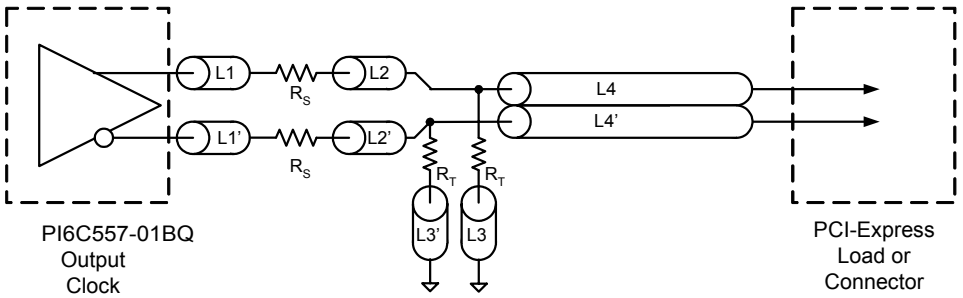
PCI Express Layout Guidelines

Common Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
L3 length, route as non-coupled 50Ω trace.	0.2 max	inch
R_S	33	Ω
R_T	49.9	Ω

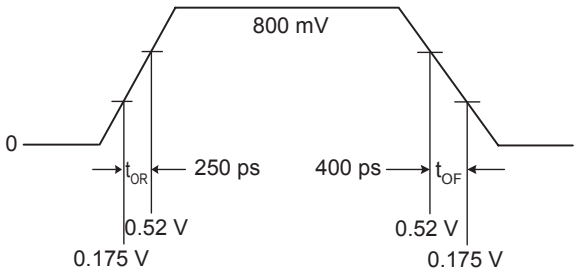
Differential Routing on a Single PCB	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace.	2 min to 16 max	inch
L4 length, route as coupled stripline 100Ω differential trace.	1.8 min to 14.4 max	inch

Differential Routing to a PCI Express connector	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace.	0.25 min to 14 max	inch
L4 length, route as coupled stripline 100Ω differential trace.	0.225 min to 12.6 max	inch

PCI Express Device Routing



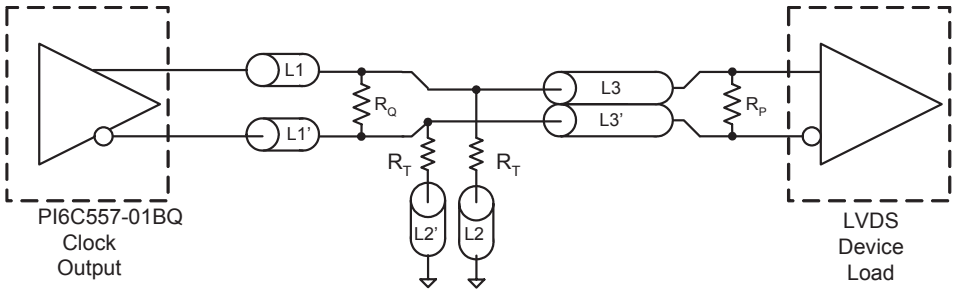
Typical PCI Express (HCSL) Waveform



Application Information

LVDS Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
RP	100	Ω
RQ	100	Ω
RT	150	Ω
L3 length, route as 100Ω differential trace.		
L3 length, route as 100Ω differential trace.		

LVDS Device Routing



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential 5.5V
All Inputs and Outputs . . . . . -0.5V to V_{DD}+0.5V
Ambient Operating Temperature . . . . . -40 to +85°C
Storage Temperature . . . . . -65 to +150°C
Junction Temperature . . . . . 150°C
Soldering Temperature . . . . . 260°C
ESD Protection (Input) . . . . . 2000 V min (HBM)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Specifications

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Characteristics (V_{DD} = 3.3V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage			3.0	3.3	3.6	V
V_{IH}	Input High Voltage(1)			2.0		V_{DD} +0.3	V
V_{IL}	Input Low Voltage(1)			GND -0.3		0.8	V
I_{IL}	Input Leakage Current	0 < Vin < V_{DD}	With input pull-up and pull-downs	-20		20	µA
			Without input pull-up and pull-downs	-5		5	
I_{DD}	Operating Supply Current	R_L = 50Ω, C_L = 2pF				95	mA
C_{IN}	Input Capacitance	@ 55MHz				7	pF
C_{OUT}	Output Capacitance	@ 55MHz				6	pF
L_{PIN}	Pin Inductance					5	nH
R_{OUT}	Output Resistance	CLK Outputs		3.0			kΩ

Notes:

1. Single edge is monotonic when transitioning through region.

HCSL Output AC Characteristics (V_{DD} = 3.3V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{IN}	Input Frequency			25		MHz
F_{OUT}	Output Frequency			100		MHz
V_{OH}	Output High Voltage (1,2)	100 MHz HCSL output @ V_{DD} = 3.3V	660	800	900	mV
V_{OL}	Output Low Voltage(1,2)		-150	0		mV
V_{CPA}	Crossing Point Voltage(1,2)	Absolute	250	350	550	mV
V_{CN}	Crossing Point Voltage(1,2,4)	Variation over all edges			140	mV
J_{CC}	Jitter, Cycle-to-Cycle(1,3)			35	60	ps
J_{RMS}	PCIe 2.0 RMS Jitter	PCIe 2.0 Test Method @ 100MHz Output			3.1	ps
$J_{RMS3.0}$	PCIe 3.0 RMS Jitter	PLL L-BW @ 2M & 5M 1st H3		1.75	3	ps
		PLL L-BW @ 2M & 4M 1st H3		2.18	3	ps
		PLL H-BW @ 2M & 5M 1st H3		0.45	1	ps
		PLL H-BW @ 2M & 4M 1st H3		0.45	1	ps
MF	Modulation Frequency	Spread Spectrum	30	31.5	33	kHz
t_{OR}	Rise Time(1,2)	From 0.175V to 0.525V	175		500	ps
t_{OF}	Fall Time(1,2)	From 0.525V to 0.175V	175		500	ps
$T_{DUTY-CYCLE}$	Duty Cycle(1,3)		45		55	%
t_{STABLE}	From power-up to V_{DD}=3.3V	From Power-up V_{DD}=3.3V		3.0		ms
t_{SPREAD}	Setting period after spread change	Setting period after spread change		3.0		ms

Notes:
1. R_L = 50-Ohm with C_L = 2 pF
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point

Thermal Characteristics

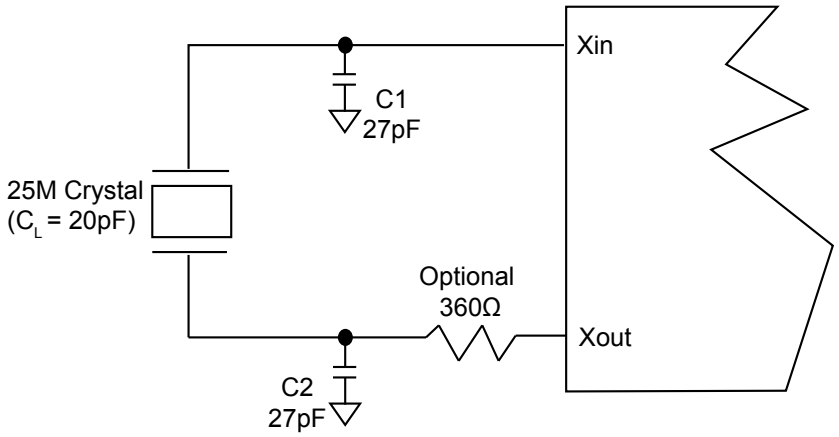
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
θ_{JA}	Thermal Resistance Junction to Ambient	Still air			57.70	°C/W
θ_{JC}	Thermal Resistance Junction to Case				32.20	°C/W

Recomended Crystal Specification

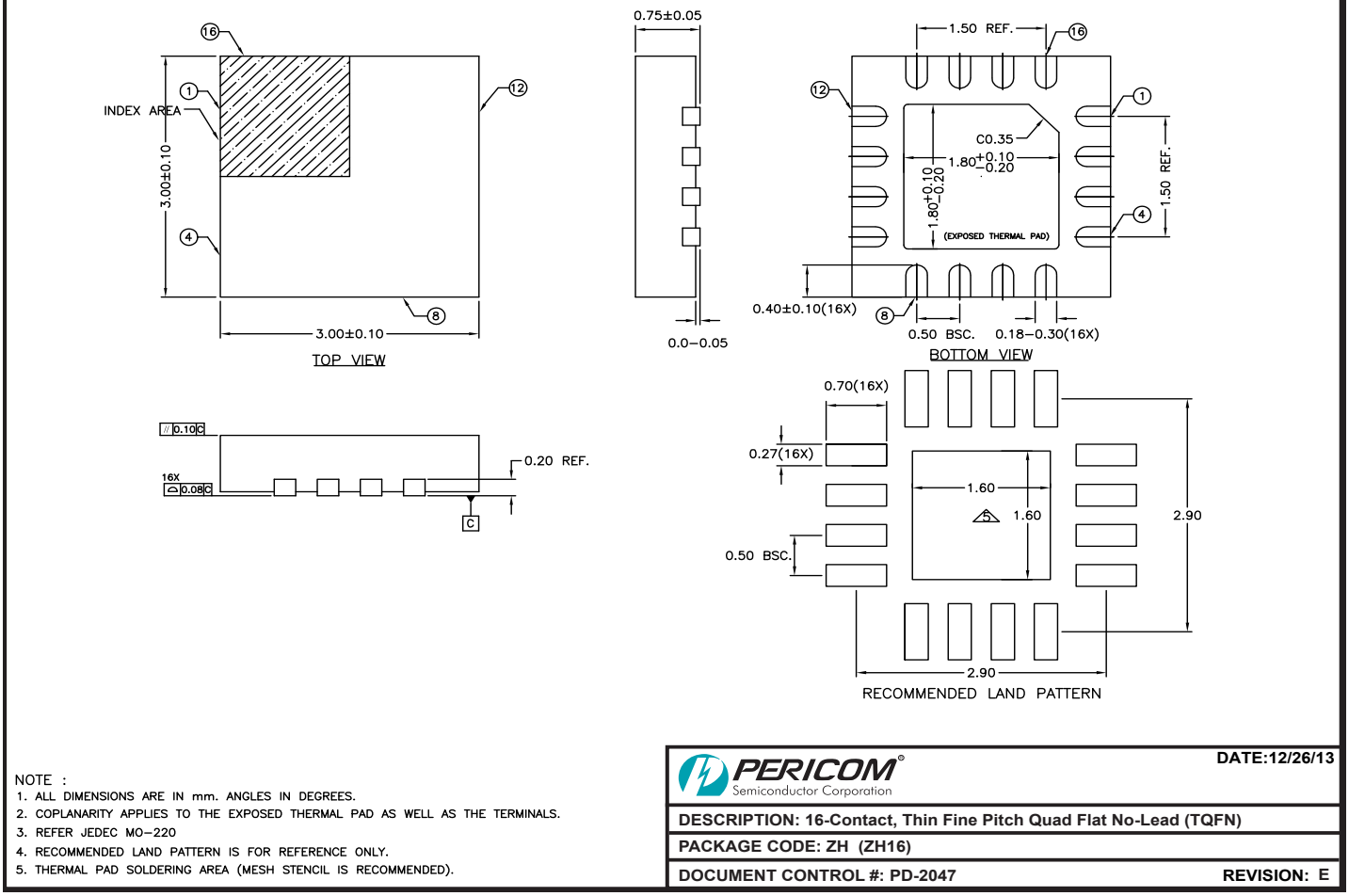
Pericom recommends:
a) FL2500184Q, SMD 3.2x2.5(4P), 25M, CL=20pF, Frequency Tolerance ±15ppm, Stability ±20ppm
(http://www.pericom.com/pdf/datasheets/se/FL.pdfb)

Recommended Crystal Circuit

The following diagram shows PI6C557-05Q crystal circuit connection with a parallel crystal. For the C L=20pF parallel crystal, it is suggested to use C1=27 pF, C2=27 pF in general. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillation according to different board layouts. R1=360 ohm is recommended in layout for smaller size crystal drive level adjustment.



Packaging Mechanical: 16-Pin TQFN (ZH)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL IS RECOMMENDED).

PERICOM Semiconductor Corporation — DATE:12/26/13

DESCRIPTION: 16-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH (ZH16)

DOCUMENT CONTROL #: PD-2047 REVISION: E

Note: For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C557-01BQZHIEX	ZH	Pb-free & Green, 16-pin TQFN	Industrial

Notes:

• Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

• "E" denotes Pb-free and Green

• Adding an "X" at the end of the ordering code denotes tape and reel packaging