STODD01

Monolithic power management for high definition ODD with true shut-down, reset, and programmable step-up voltage

Features

- 1.2 MHz DC-DC current mode PWM converter
- Dual step-down of up to 800 mA
- Single step-up of up to 700 mA
- 2 % DC output voltage tolerance for step-down
- 3 % DC output voltage tolerance for step-up
- Programmable step-up output voltage by S-WIRE
- Synchronous rectification
- Power save mode at light load for step-down
- Typical efficiency: > 90 %
- Internal soft start with controlled inrush current
- Reset function
- Enable function for step-up
- True cut-off function for step-up
- Low switching quiescent current: max 2.2 mA overtemperature range
- Uses tiny capacitors and inductors
- Available in QFN16 (4 x 4 mm.)

QFN16L (4 x 4 mm.)

Description

The STODD01 is a complete power management for Blu-Ray, based on high density optical storage devices. It integrates two step-down converters and one step-up. The step-down converters are optimized for powering low-voltage digital core, up to 0.8 A, in ODD applications and, generally, to replace the high current linear solution when power dissipation may cause a high heating of the application environment. The step-up provides the necessary voltage to supply the blue laser in mobile applications where only 5 V is available. The output voltage is programmable by using the S-Wire protocol, in the range of 6.5 V to 14 V, with a current capability of 0.7 A. The integrated low R_{DSon} for N-channel and P-channel MOSFET switches contribute to obtaining high efficiency. The enable function for the step-up section, and reset function for monitoring the input voltage, make the device particularly suitable for optical storage applications. The high switching frequency (1.2 MHz typ.) allows the use of tiny surface mounted components. Furthermore, a low output ripple is achieved by the current mode PWM topology and by the use of X7R or X5R low ESR SMD ceramic capacitors. The device includes soft-start control, thermal shutdown, and peak current limit, to prevent damage due to accidental overload. The STODD01 is packaged in QFN16 (4 x 4 mm.).

Table 1. Device summary

Part number	Order code	Marking	Package
STODD01	STODD01PQR	ODD01	QFN16 (4 x 4 mm.)

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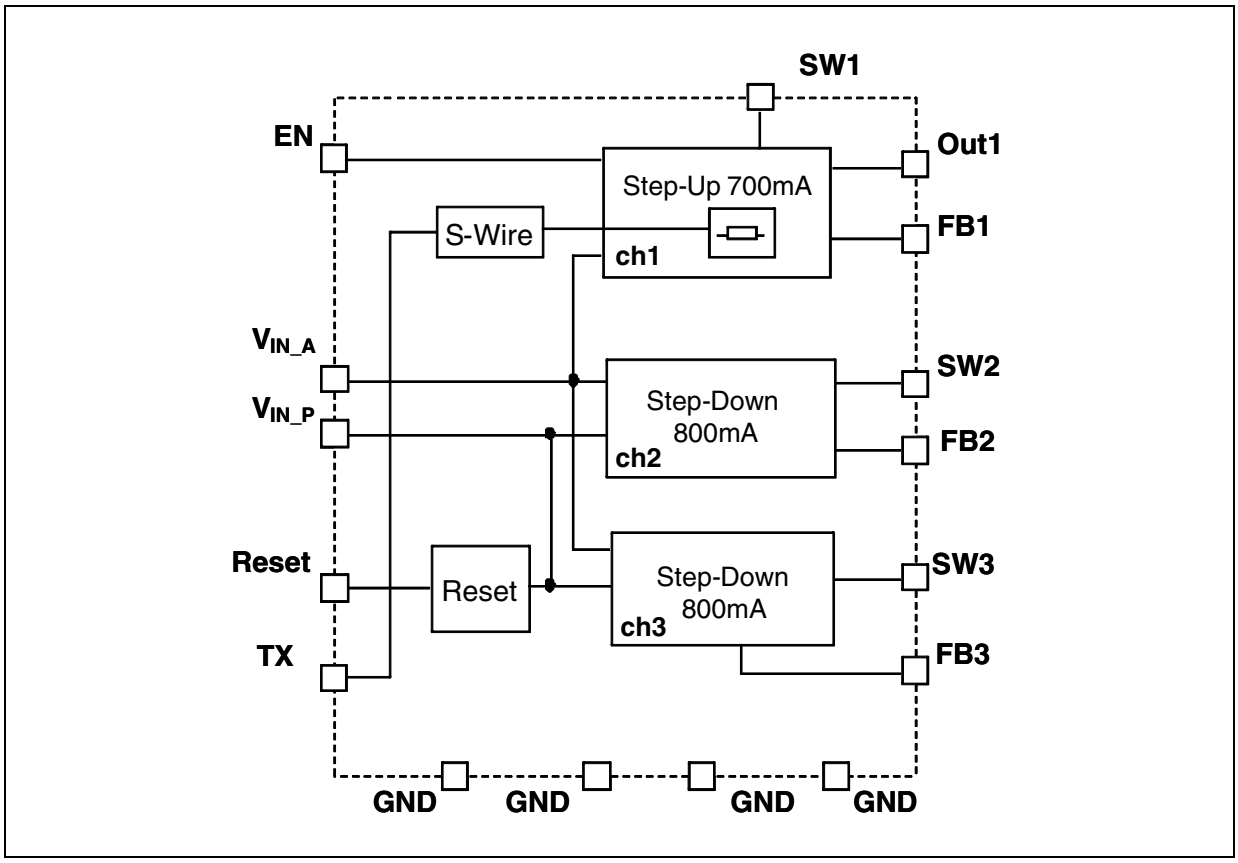
1 Block diagram

Figure 1. STODD01 block diagram



2 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN_A}	Analog input voltage	- 0.3 to 7	V
V_{IN_P}	Power input voltage	- 0.3 to 7	V
EN	Enable voltage	- 0.3 to 7	V
SW1	Switch pin for ch1	- 0.3 to 16	V
SW2,SW3	Switch pin for ch2 and ch3	- 0.3 to 7	V
OUT1	Output voltage for ch1	- 0.3 to 16	V
FB1	Feedback pin for ch1	- 0.3 to 2.5	V
FB2	Feedback pin for ch2	- 0.3 to 5	V
FB3	Feedback pin for ch3	- 0.3 to 2.5	V
Reset	Reset pin	- 0.3 to V_{IN} + 0.3	V
TX	S-wire pin	- 0.3 to 7	V
T_J	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	- 65 to + 150	°C
T_{JOP}	Operating junction temperature range	- 25 to + 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	2.5	°C/W
R_{thJA}	Thermal resistance junction-ambient	46	°C/W

Table 4. ESD

Symbol	Parameter	Value	Unit
HBM	Human body model	2	kV
MM	Machine model	200	V

3 Pin configuration

Figure 2. Pin connection (top through view)

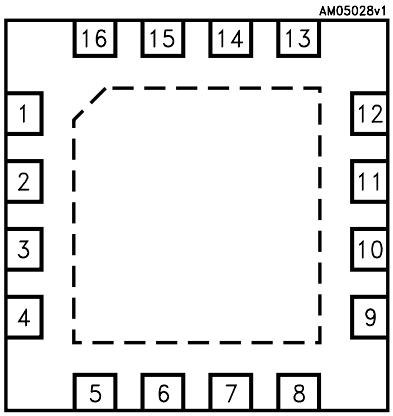


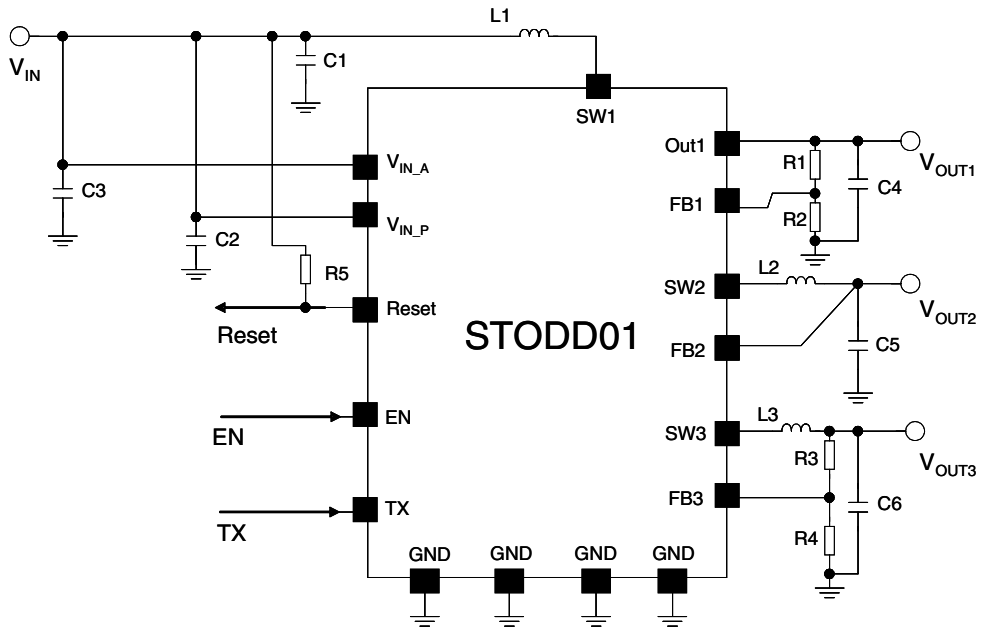
Table 5. Pin description

Pin n°	Symbol	Name and function
1	GND_P	Power Ground pin (ch1)
2	FB1	Step-up feedback pin (ch1)
3	V_{IN_A}	Power Supply for internal analog circuits
4	FB2	Step-down feedback pin (ch2)
5	GND_P	Power Ground pin (ch2)
6	SW2	Step-down switching pin (ch2)
7	V_{IN_P}	Power input voltage pin
8	SW3	Step-down switching pin (ch3)
9	GND_P	Power Ground pin (ch3)
10	FB3	Step-down feedback pin (ch3)
11	GND_A	Analog Ground pin
12	OUT1	Step-up output voltage
13	TX	S-Wire pin. If connected to GND, V_{FB1}=0.8V (1)
14	SW1	Step-up switching pin (ch1)
15	EN	Enable pin. Connecting the pin to a voltage higher than 1.2 V the step-up is ON.Connecting the pin to a voltage lower than 0.4 V the step-up is OFF, resulting in no current flow to the load
16	Reset	Reset pin. It is an open drain output
	Exposed pad	Ground and thermal dissipation pad

1. If this function is not used, the TX pin must be connected to GND

4 Typical application

Figure 3. Application circuit



Note: If the S-wire function is not used, the TX pin must be connected to GND.

Table 6. List of external components (1)

Component	Manufacturer	Part number	Value	Size
C1, C2, C3	Murata	GRM21BR61A106KE19L	10 µF	0805
C4, C5, C6	Murata	GRM32ER61C226KE20L	22 µF	1210
L1	Coilcraft	LPS6225-472MLB	4.7 µH	6 x 6 x 2.5
L2, L3	Coilcraft	LPS4018-332MLB	3.3 µH	4.1 x 4.1 x 1.8
R1		33 kΩ (V_{OUT1} = 8.8 V)	(2)	0603
R2		3.3 kΩ		0603
R3		27 kΩ (V_{OUT3}= 1.2 V)	(3)	0603
R4		47 kΩ		0603
R5		100 kΩ	(4)	0603

1. The components listed above refer to typical applications. Operation of the STODD01 is not limited to the choice of these external components.
2. R1 and R2 are calculated according to the following formula:

R1 = R2 x (V_{OUT1}/V_{FB1}- 1). It is recommended to use resistors with values in the range of 1 kΩ to 50 kΩ.

3. R3 and R4 are calculated according to the following formula:

R3 = R4 x (V_{OUT3}/V_{FB3} - 1). It is recommended to use resistors with values in the range of 1 kΩ to 50 kΩ.

4. It is recommended to use resistors with values in the range of 100kΩ to 1MΩ.

5 Electrical characteristics

$V_{IN\_P} = V_{IN\_A} = V_{EN} = 5$ V, $V_{OUT1} = 9$ V, $V_{OUT2} = 3.3$ V, $V_{OUT3} = 1.2$ V, $C_{1,2,3} = 10$ µF, $C_{4,5,6} = 22$ µF, L1 = 4.7 µH, L2 = L3 = 3.3 µH, T_J = - 25 to 125 °C (unless otherwise specified; typical values are referred to T_J = 25 °C).

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range		4		6	V
I_{SUPPLY}	Supply current	V_{EN} > 1.2 V, No Switching		1.6	2.2	mA
		V_{EN} < 0.4 V, No Switching		1.2	2.0	mA
Step-up section						
V_{OUT}	Output voltage range		6.5		14	V
V_{FB1}	Prog. feedback voltage range	I_{OUT1}= 50 mA (prog. by S-Wire see *Figure 9* and *Table 9*)	0.776	0.8	0.824	V
	Feedback voltage accuracy		-3		3	%
I_{FB1}	Feedback current	V_{FB1}= 0 V, V_{EN}= 2 V		600		nA
I_{OUT1_OFF} (leak)	Output leakage current	V_{EN}= 0 V, T_J = -25 to 80 °C			20	µA
V_{OUT1} OVP	Overvoltage protection (1)	V_{FB1}= 0 V	14.8	15.3	15.8	V
R_{DSon_N}	Internal N-channel R_{DSon}	I_{SW1}=400 mA		300		mΩ
R_{DSon_P}	Internal P-channel R_{DSon}	I_{SW1}=400 mA		300		
$I_{SW1\ (leak)}$	Internal leakage current	V_{SW1}= 4 V, V_{FB1}= 2 V, V_{EN}= 0 V		2		µA
$I_{SW1\ (LIM)}$	SW Current limitation	V_{OUT1}= 9.2 V		2.6		A
PWM f_s	Oscillator frequency	to be measured on t_{SW1} pin	0.75	1.2	1.5	MHz
D_{MAX}	Max duty cycle	on SW1 pin, V_{FB1} = 0.7 V	70	90		%
ν	Efficiency	I_{OUT1}=50 mA, V_{OUT1}=7 V		80		%
		I_{OUT1}=700 mA, V_{OUT1}=7 V		90		%
		I_{OUT1}=100 mA, V_{OUT1}=9 V		75		%
		I_{OUT1}=700 mA, V_{OUT1}=9 V		90		%
V_{EN_H}	Enable threshold high	V_{IN} =4 to 6 V, I_{OUT1} = 50 mA	1.2			V
V_{EN_L}	Enable threshold low	V_{IN} = 4 to 6 V, I_{OUT1} = 50 mA			0.4	
I_{EN}	Enable pin current	V_{EN} = V_{IN} = 5 V		2		µA
$\Delta V_{OUT1}/\Delta V_{IN}$	Line transient response (2)	V_{IN} from 4 to 6 V, I_{OUT1} = 500 mA, t_R = t_F => 30 µs, T_J=25 °C	-5		5	% V_{OUT}
$\Delta V_{OUT1}/\Delta I_{OUT}$	Load transient response (2)	V_{IN} = 5 V, I_{OUT1} from 100 mA to 500 mA, t_R = t_F => 5µs, T_J=25 °C	-5		5	% V_{OUT}
$\Delta V_{OUT1}/\Delta V_{IN}$	Startup transient (2)	V_{IN} from 0 to 5 V, I_{OUT1}= 500 mA	-10		10	% V_{OUT}

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{START}	Startup time	V_{EN} from 0 to 5 V, I_{OUT1}=100 mA		500		µs
	Inrush current	V_{OUT}=9.25 V, I_{OUT}=100 mA		1.3		A
Step-down section						
FB_2	Feedback voltage		3.23	3.3	3.37	V
I_{FB2}	FB2 Pin bias current	V_{FB2}= 3.5 V		15	20	µA
FB_3	Feedback voltage		0.784	0.8	0.816	mV
I_{FB3}	FB3 Pin bias current	V_{FB3}= 1 V			600	nA
$I_{OUT2,3}$	Output current (3)	V_{IN} = 4 to 6 V	700	800		mA
I_{OUT_MIN}	Minimum output current		0			mA
$\Delta V_{OUT2,3}$	Reference load regulation	10 mA < $I_{OUT2,3}$ < 0.8 A		5.5	15	mV
PWM f_S	PWM Switching frequency	$I_{OUT2,3}$ = 0.3 A		1.2		MHz
$\%V_{OUT2}/\Delta V_{IN}$	Line regulation	4 V < V_{IN} < 6 V		0.032		% V_{OUT} /V_{IN}
$\%V_{OUT3}/\Delta V_{IN}$	Line regulation	4 V < V_{IN} < 6 V		0.15		% V_{OUT} /V_{IN}
D_{MAX}	Maximum duty cycle	V_{FB2} = 3.0 V, V_{FB3} = 0.7 V	85	94		%
I_{SWL}	Switching current limitation			1.5		A
$I_{LKP2,3}$	PMOS Leakage current	V_{FB2} = 3.5 V, V_{FB3} = 0.9 V, $V_{SW2,3}$= GND, T_J=- 25 to 80 °C		0.1		µA
$I_{LKN2,3}$	NMOS Leakage current	V_{FB2} = 3.5 V, V_{FB3} = 0.9 V, $V_{SW2,3}$ = 5 V, T_J =- 25 to 80 °C		0.1		µA
R_{DSon}-N	NMOS Switch on resistance	I_{SW} = 250 mA		0.2	0.4	W
R_{DSon}-P	PMOS Switch on resistance	I_{SW} = 250 mA		0.3	0.5	W
$\Delta V_{OUT2,3}/\Delta I_{OUT2,3}$	Load transient response (2)	100 mA < $I_{OUT2,3}$ < 500 mA, t_R = t_F => 100 ns, T_J = 25 °C	-5		+5	% V_{OUT}
ν	Efficiency V_{OUT3} = 1.2 V	I_{OUT3} = 100 mA		65		%
		I_{OUT3} = 800 mA		80		
ν	Efficiency V_{OUT2} = 3.3 V	I_{OUT2} = 100 mA		75		%
		I_{OUT2} = 800 mA		90		
Reset section						
t_{DEL}	Delay time	T_J = 25 °C		100		ms
V_{R_TH}	Reset threshold	V_{IN} Rising (see *Figure 12* and *Figure 29*) (measured on input voltage pin)		4.3	4.4	V
V_{R_TL}		V_{IN} Falling (see *Figure 12* and *Figure 29*) (measured on input voltage pin)	4.1	4.2		

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{RL}	Reset output voltage low	V_{IN}=4 V, I_{SINK}=6 mA open drain output			0.4	V
I_{RH}	Reset leakage current	V_{IN}=5 V, V_{RES}=5 V, T_J=-25 to 80 °C		5	200	nA
Thermal section						
T_{SHDN}	Thermal shutdown (2)		130	150		°C
T_{HYS}	Thermal shutdown hysteresis (2)			15		°C

1. If V_{OUT1} > OVP voltage the device stops to switch.
2. Guaranteed by design, but not tested in production.
3. V_{OUT} = 90 % of nominal value

6 S-wire protocol

Table 8. Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
S-Wire signal start (see *Figure 5*, *6*, *7*, *8*)	t_{SW_START}	300		500	µs
S-Wire signal stop (see *Figure 5*, *6*, *7*, *8*)	t_{SW_STOP}	300		500	µs
S-Wire signal off (see *Figure 5*, *6*, *7*, *8*)	t_{SW_OFF}		270		µs
S-Wire high (see *Figure 5*, *6*, *7*, *8*)	t_{SW_H}	25		50	µs
S-Wire low (see *Figure 5*, *6*, *7*, *8*)	t_{SW_L}	25		50	µs
S-Wire rising time (see *Figure 4*)	t_{SW_R}			200	ns
S-Wire falling time (see *Figure 4*)	t_{SW_F}			200	ns
FB Voltage delay	t_{SW_DELAY}		20		µs
S-Wire threshold high (see *Figure 4*)	V_{SW_TH}	1.6		V_{IN}	V
S-Wire threshold low (see *Figure 4*)	V_{SW_TL}	0		0.4	V

Note: These are recommended values for proper operation of the S-wire interface.

The S-wire input pin is able to detect pulses also outside these ranges. Consequently, care must be taken to avoid noise injected into the S-wire pin.

Figure 4. S-wire pulse thresholds

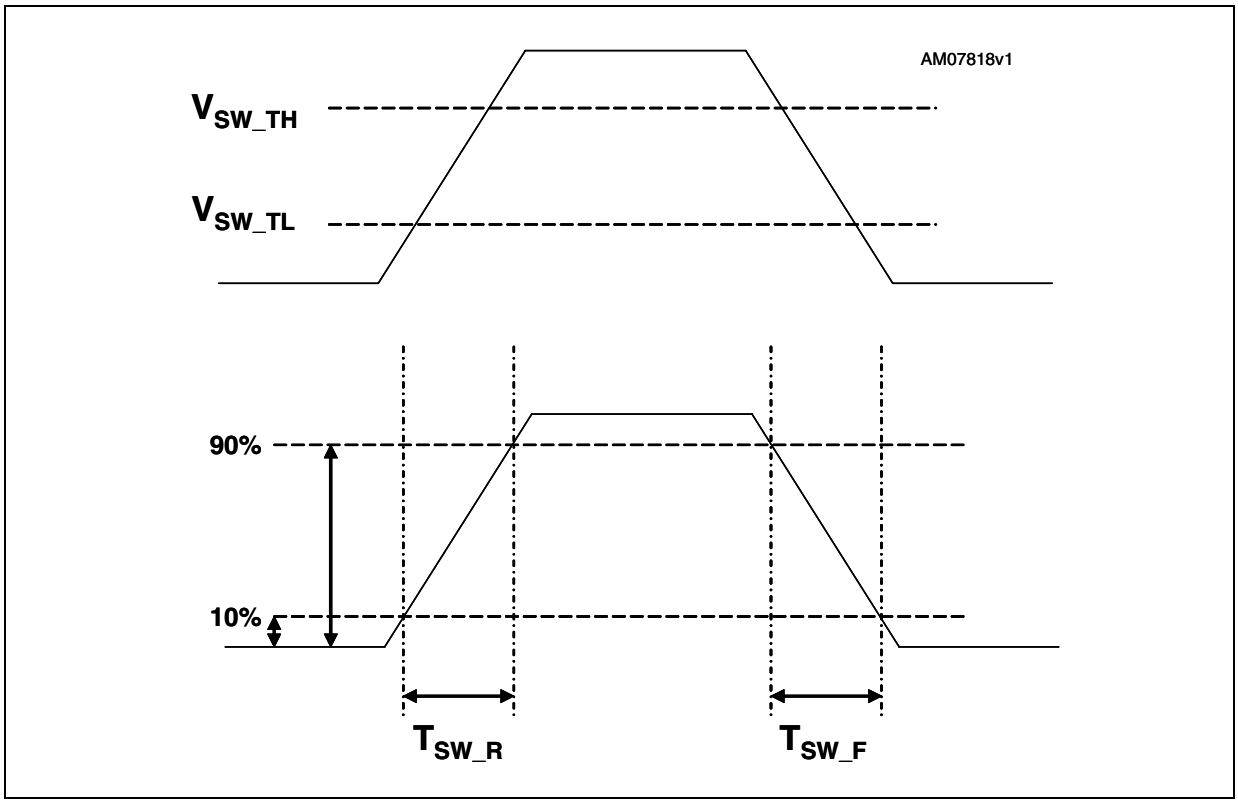


Figure 5. S-wire protocol timing diagrams (case a)

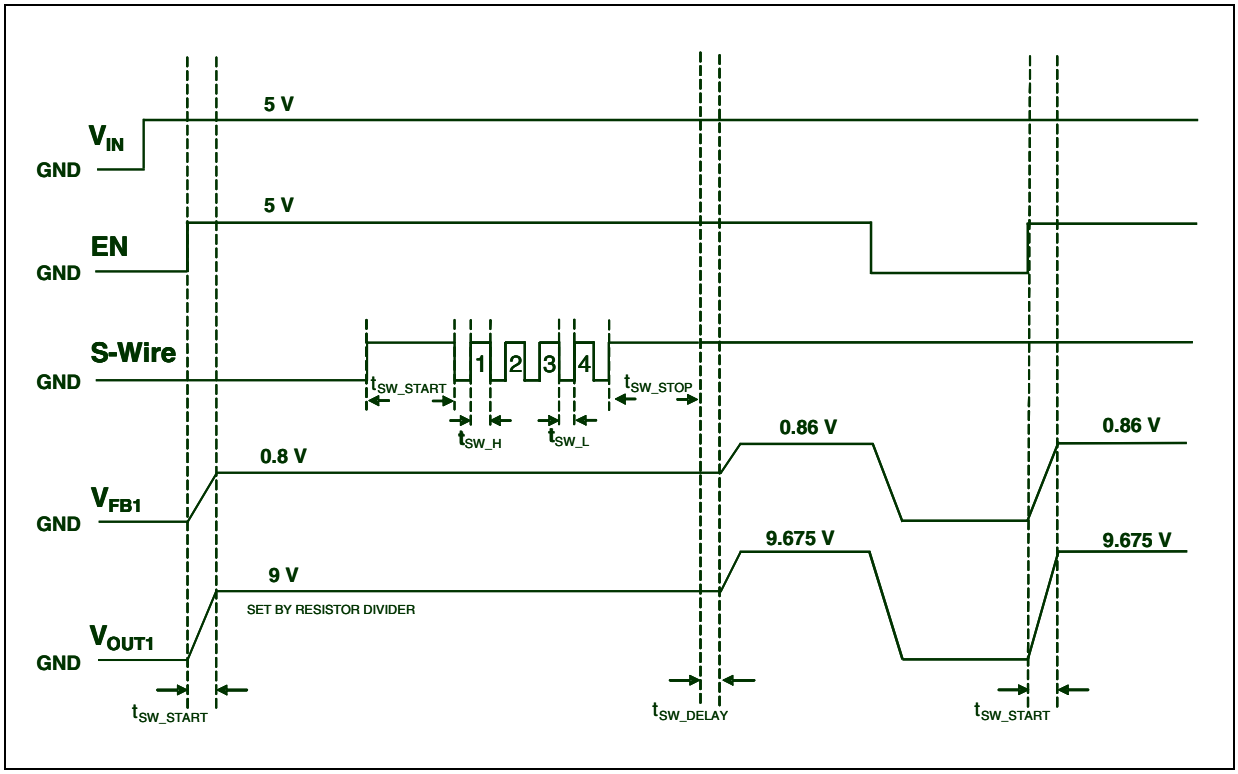


Figure 6. S-wire protocol timing diagrams (case b)

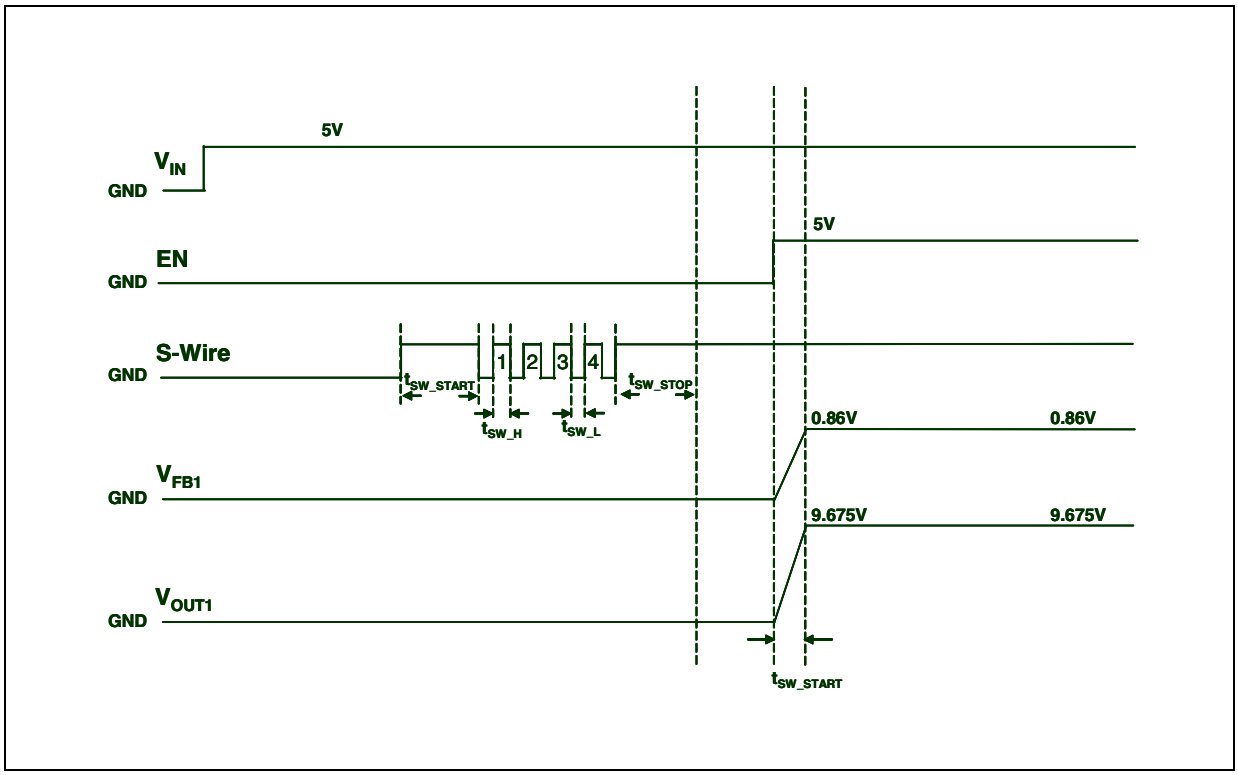


Figure 7. S-wire protocol timing diagrams (case c)

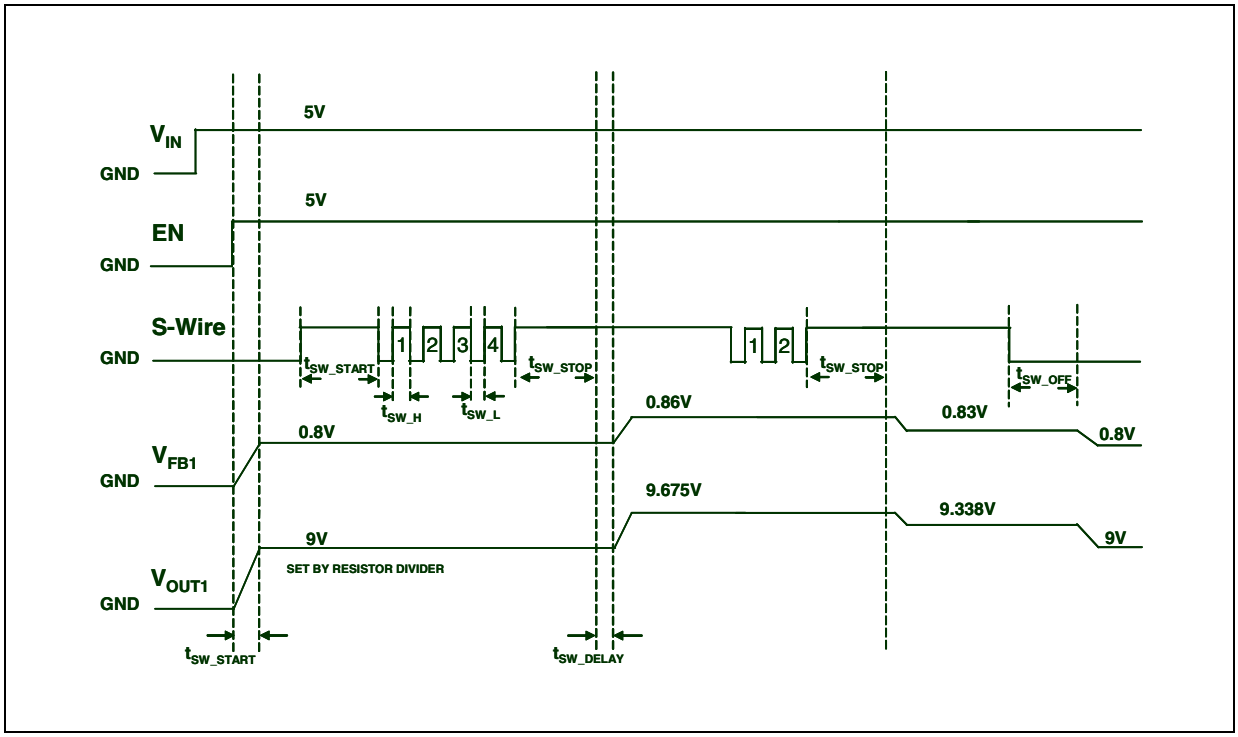


Figure 8. S-wire protocol timing diagrams (case d)

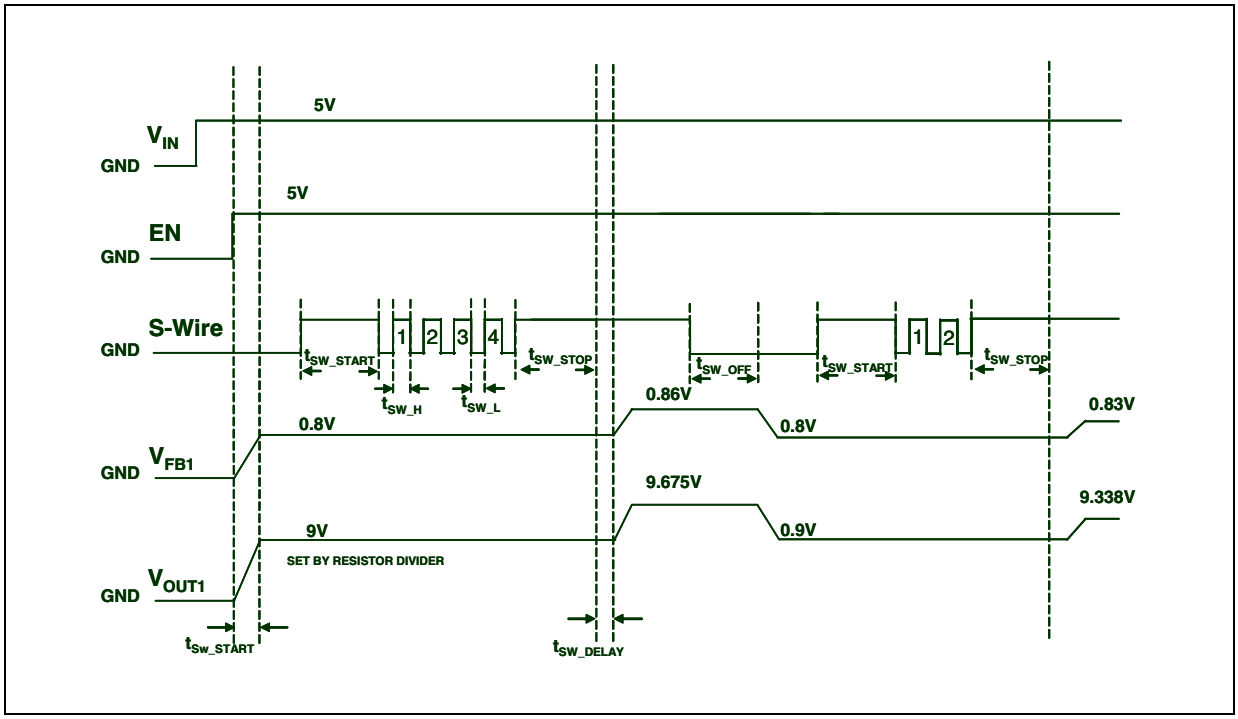
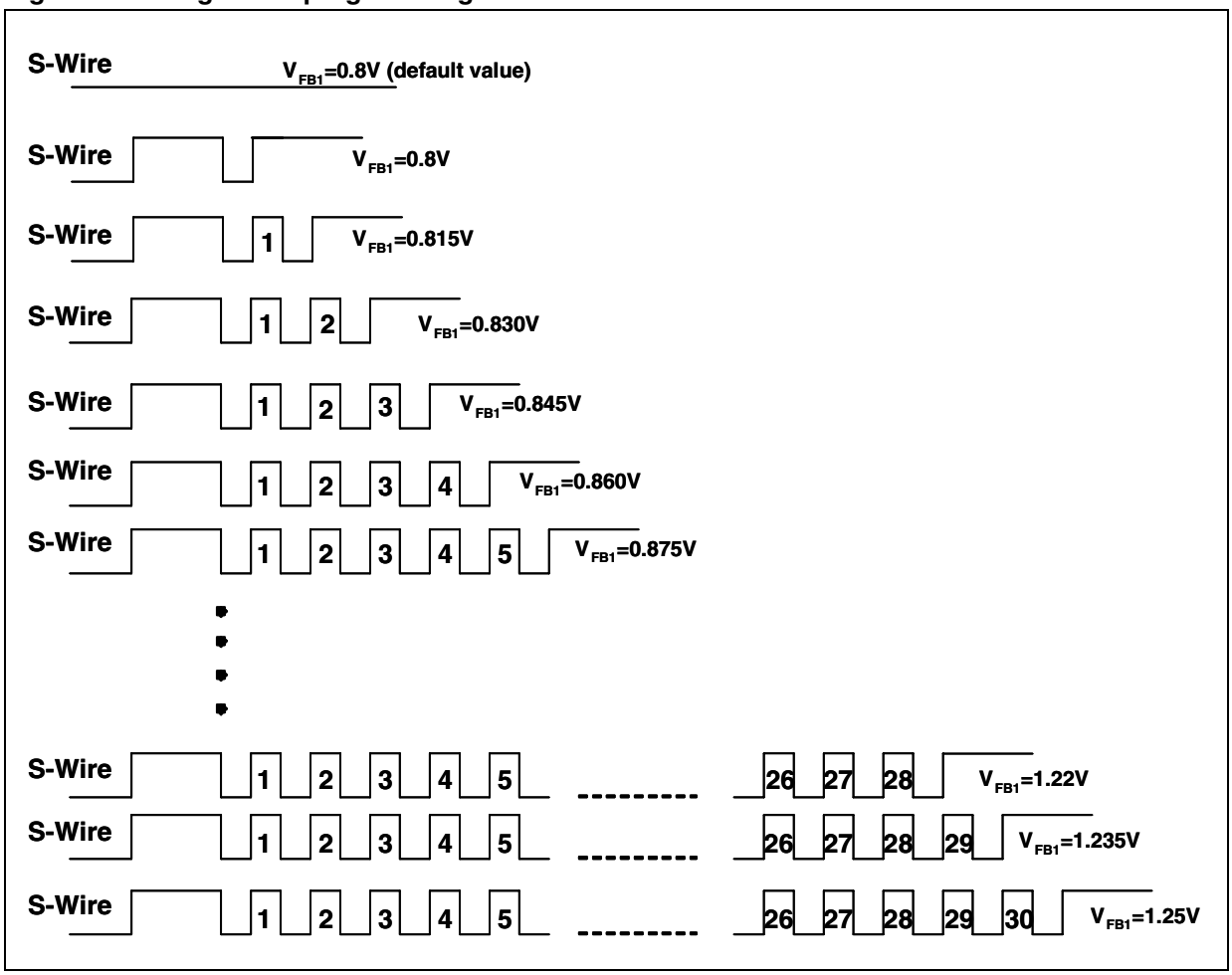


Table 9. Feedback one voltage level

S-Wire pulses	V_{FB1} (V)	S-Wire pulses	V_{FB1} (V)	S-Wire pulses	V_{FB1} (V)
0 (Default value)	0.800	11	0.965	22	1.130
1	0.815	12	0.980	23	1.145
2	0.830	13	0.995	24	1.160
3	0.845	14	1.010	25	1.175
4	0.860	15	1.025	26	1.190
5	0.875	16	1.040	27	1.205
6	0.890	17	1.055	28	1.220
7	0.905	18	1.070	29	1.235
8	0.920	19	1.085	30	1.250
9	0.935	20	1.100		
10	0.950	21	1.115		

Figure 9. Single wire programming



7 Detailed description

7.1 Brief overview

The STODD01 is a complete high efficiency switching power management. Inside it has a step-up converter with a current capability up to 0.7 A and two step-down converters with a current capability up to 0.8 A.

The controller uses an average current mode technique in order to obtain good stability in all application conditions.

The step-up converter, in order to guarantee the lowest switching ripple, operates in PWM (pulse width modulation) in all load conditions.

Both step-down converters, in order to maintain good efficiency, operate in power-save mode at light load. When the load increases, they automatically switch to PWM (pulse width modulation) mode and the output voltage ripple is minimized.

The STODD01 is self protected against overtemperature and accidental short circuit in the step down channel.

The soft-start function guarantees proper operation during startup.

7.2 Enable pin

The step-up section operates when the EN pin is set high. If the EN pin is set low the step-up turns OFF. In this condition the supply current is lower than 2 mA in the whole temperature range, and it represents the consumption of the step-down section.

When the EN pin is low, thanks to at the true cut-off function, implemented using two P-channel MOSFETs in a back-to-back configuration, as shown in *Figure 10*, the output current is stopped. In order to control and reduce the in-rush current, the true cut-off P-channel (P_O) manages the current during startup.

Figure 10. True cut-off block

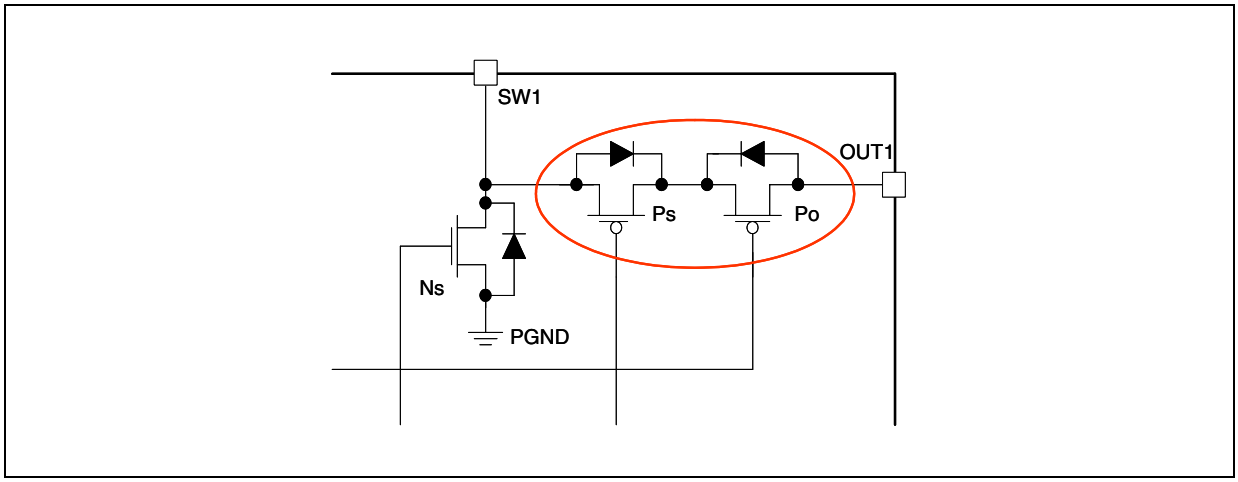


Figure 32 shows the in-rush current at enable transient. Initially, the C_4 capacitor is completely discharged and the current limitation is due only to the equivalent series resistor of the inductor, the power MOSFET parasitic diode, and the cut-off MOSFETs' R_{DSon}. As soon as the output voltage reaches the input voltage level, the device begins to switch and the current is limited cycle by cycle.

The EN pin does not have an internal pull-up, which means that the enable pin cannot be left floating.

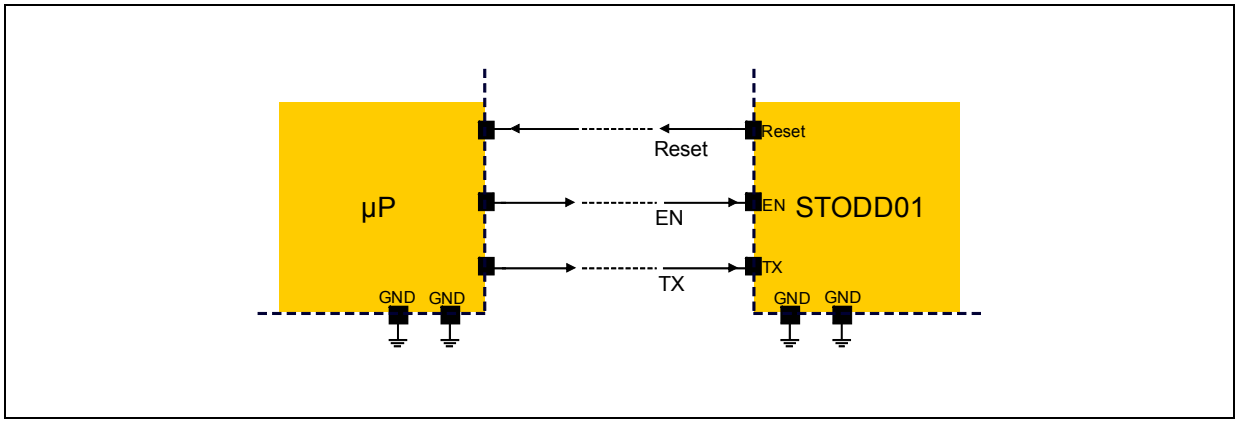
If the enable function is not used, the EN pin must be connected to V_{IN}.

7.3 TX pin

The device implements an S-wire bus communication, which uses one control signal coming from the microprocessor to program the step-up STODD01 output voltage (see *Figure 11*).

S-wire protocol allows the feedback voltage of the step-up section to be changed from 0.8 to 1.25 V, with steps of 15 mV (see *Table 9*).

Figure 11. S-Wire connection



This feature allows complete and easy control of the laser diode power during read and write operation.

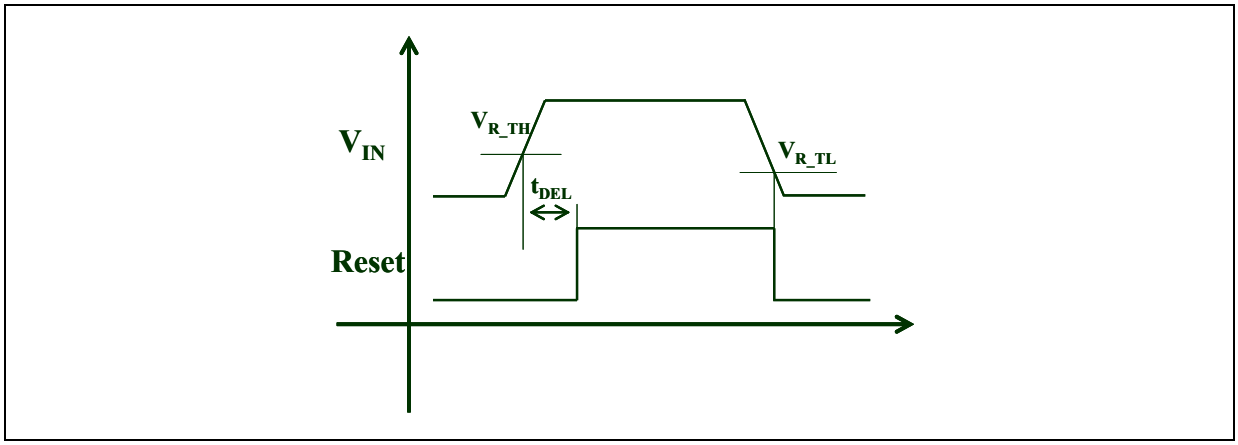
If this function is not used, the TX pin must be connected to GND.

7.4 Reset function

This flag shows that input voltage is in the correct range.

A comparator senses the input voltage. When it is higher than V_{R_TH}, the reset pin goes to high impedance, with a delay of 100 ms (typ.). If it is below V_{R_TL}, the reset pin goes to low impedance (see *Figure 12*).

Figure 12. Reset function



The use of the reset function requires an external pull-up resistor which must be connected between the reset pin and V_{IN} or any V_{OUT} voltage lower than 5 V. A pull-up resistor for reset in the range of 100 kΩ to 1 MΩ is recommended.

If the reset function is not used, the reset pin may remain floating on the board.

7.5 Overtemperature protection

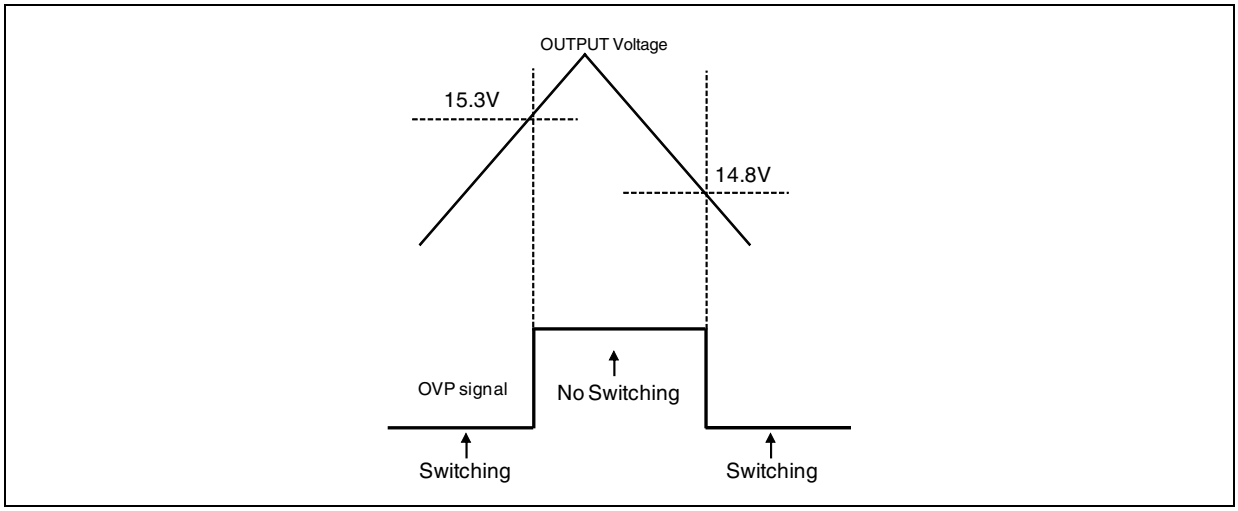
An internal temperature sensor continuously monitors the IC junction temperature. If the IC temperature exceeds 150 °C (typ.) the device stops operating. As soon as the temperature falls below 135 °C (typ.) normal operation is restored.

7.6 Overvoltage protection

The device provides overvoltage protection for monitoring the step-up output voltage.

If the sensed voltage on ch1 output exceeds 15.3 V (typ.) the step-up channel stops switching. As soon as the output capacitor is discharged and the sensed voltage is below 14.8 V, it re-starts to switch (see *Figure 13*).

Figure 13. OVP function



8 Typical performance characteristics

$C_{1,2,3}$ = 10 µF, $C_{4,5,6}$ = 22 µF, L1 = 4.7 µH, L2 = L3 = 3.3 µH.

Figure 14. Supply current vs. temperature

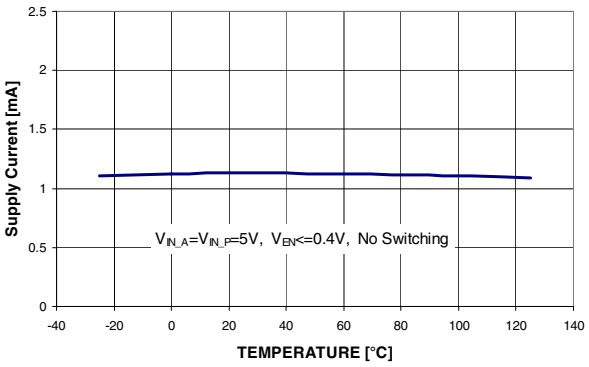


Figure 15. Feedback voltage vs. temperature

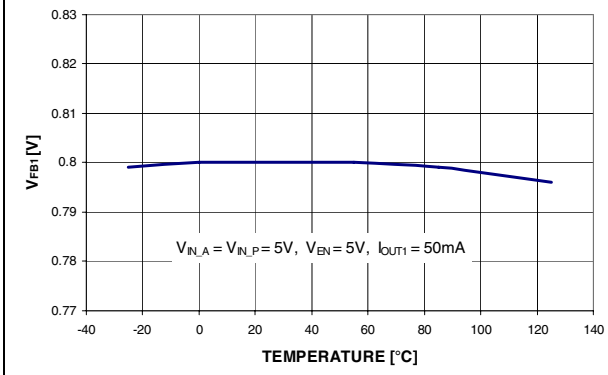


Figure 16. Feedback voltage vs. temperature

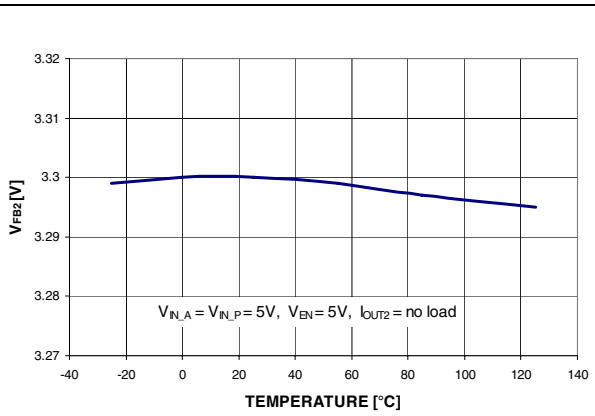


Figure 17. Feedback voltage vs. temperature

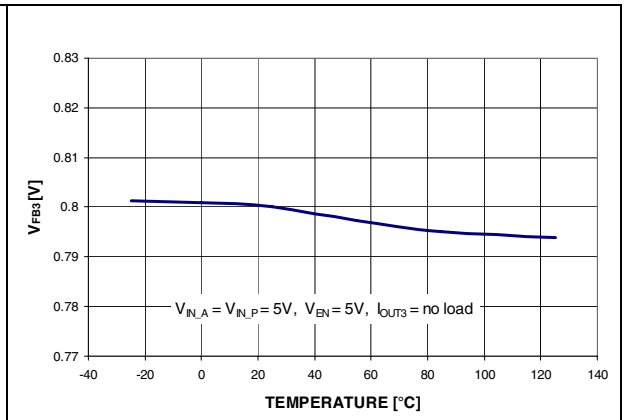


Figure 18. OVP vs. temperature

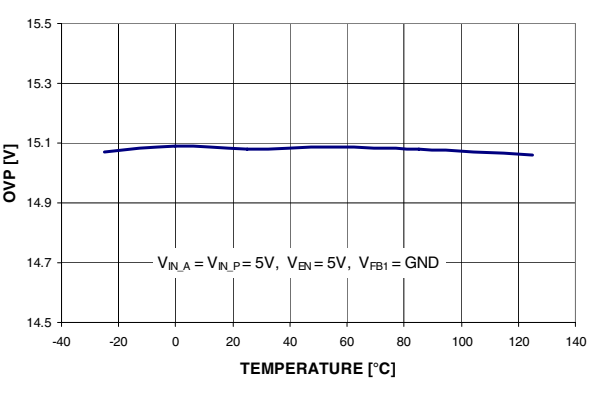


Figure 19. True shutdown voltage vs. temperature

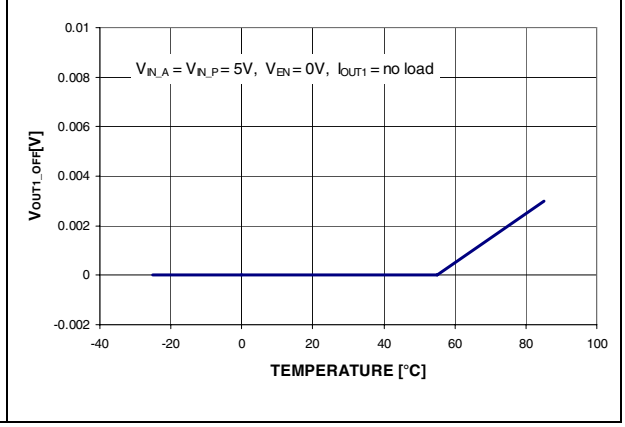


Figure 20. Output leakage current vs. temperature

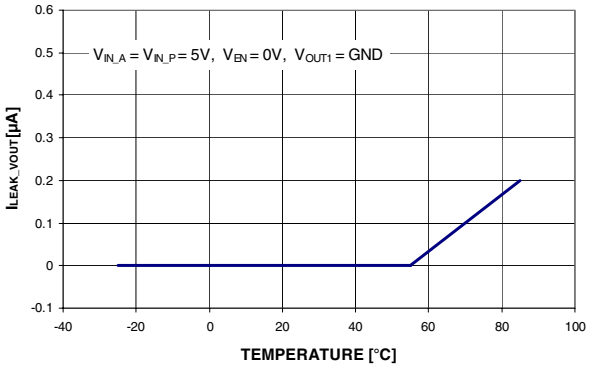


Figure 21. SW current limitation vs. temperature

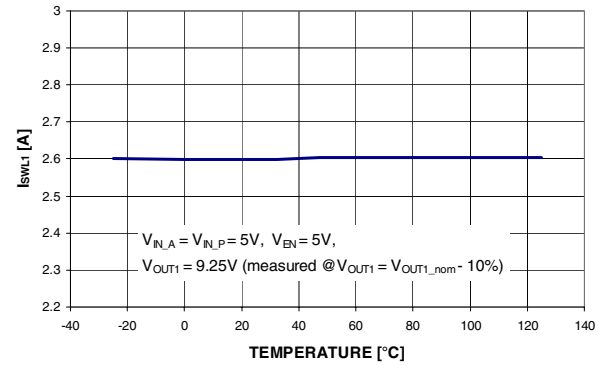


Figure 22. SW current limitation vs. temperature

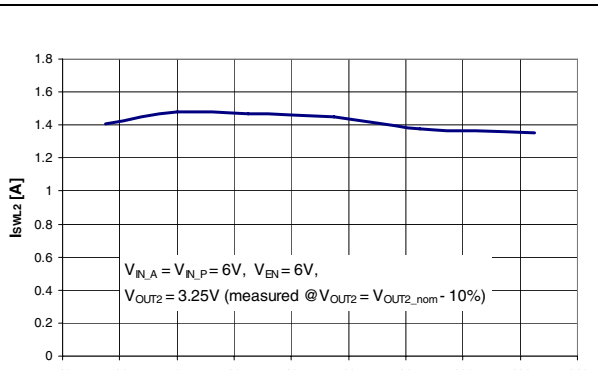


Figure 23. SW current limitation vs. temperature

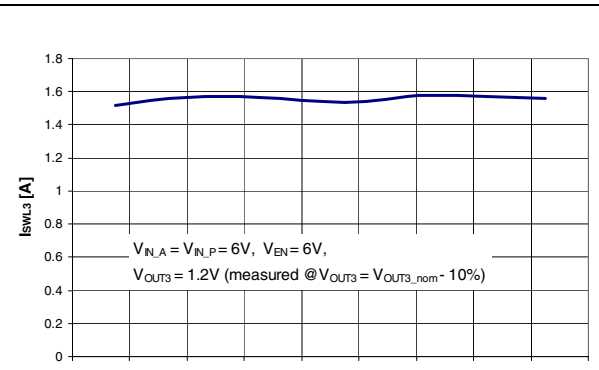


Figure 24. Oscillator frequency vs. temperature

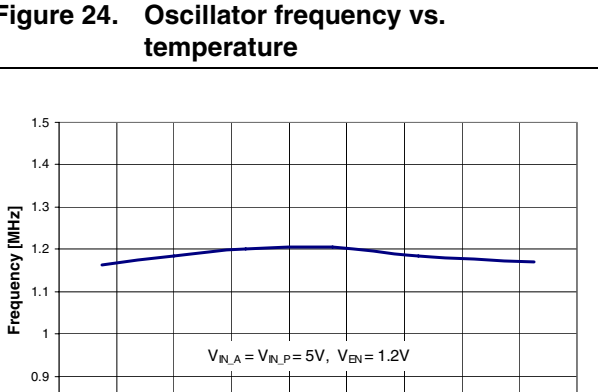


Figure 25. Enable vs. temperature

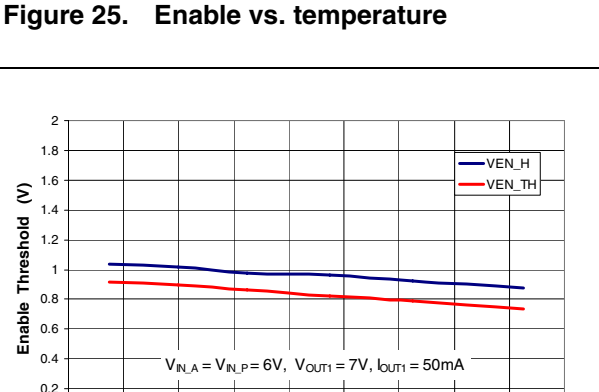


Figure 26. Enable vs. temperature

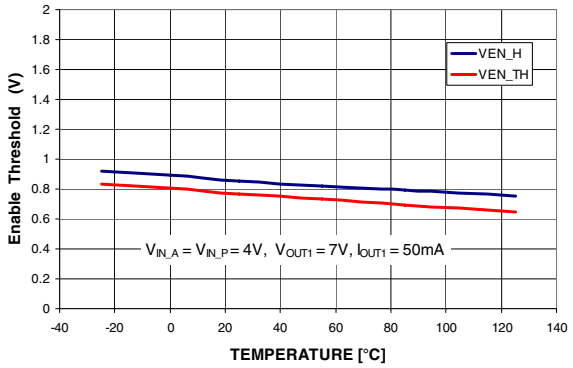


Figure 27. Efficiency step-up vs. output current

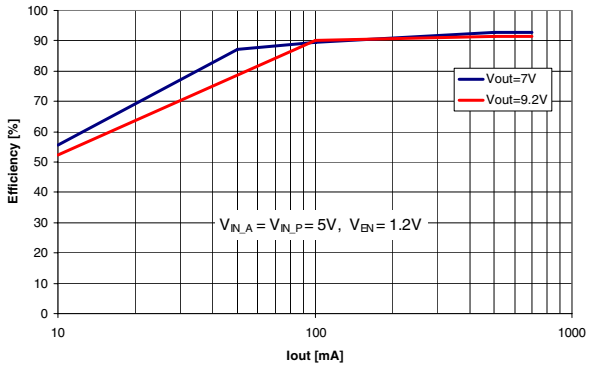
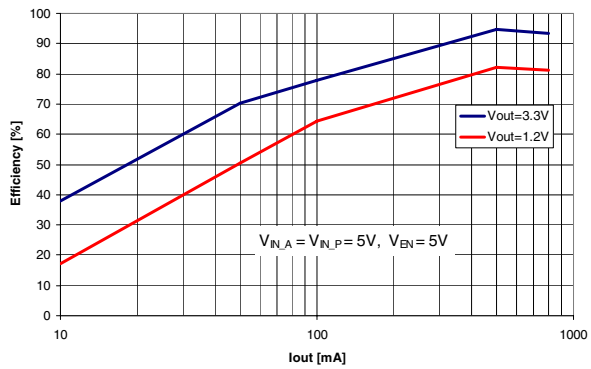


Figure 28. Efficiency step-down vs. output current



All efficiencies are relative to one channel, the other channel is at no-load.

Figure 29. Reset threshold vs. temperature

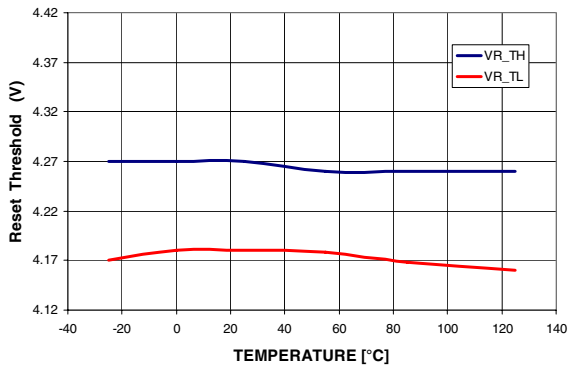


Figure 30. Startup transient

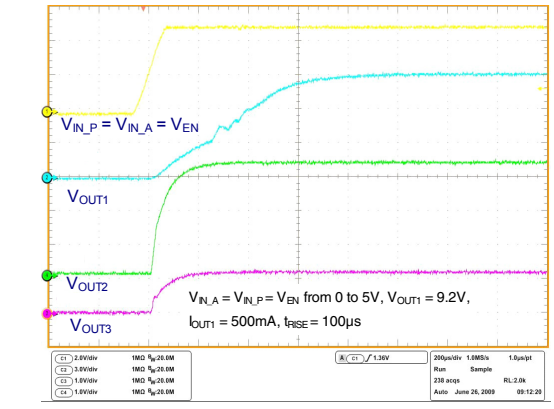


Figure 31. Enable transient

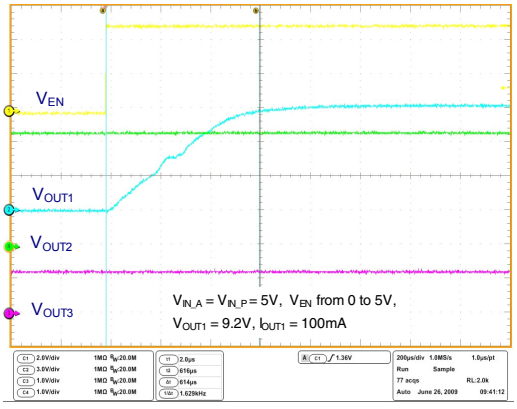


Figure 32. Inrush current

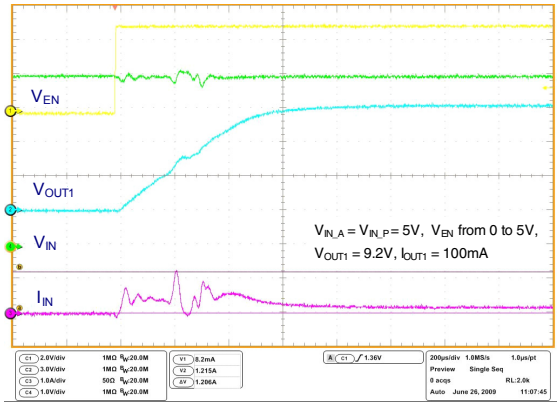
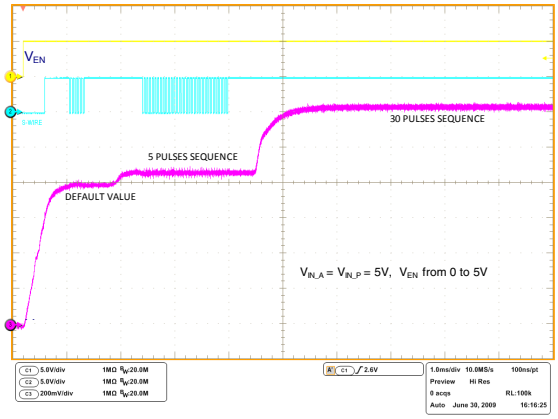


Figure 33. S-Wire protocol



9 Application information

9.1 Introduction

The following is some technical information for estimating the typical external components characteristics using standard literature equations. Nevertheless, it is strongly recommended to validate the external components suitability to the application requirements, thoroughly testing any solution at bench level on a real evaluation circuit.

9.2 Programming the output voltage

The output voltage for the step-up (ch1) can be adjusted from 6.5 V up to 14 V by connecting a resistor divider between the V_{OUT1} and the GND, the middle point of the divider must be connected to the FB1 pin, as shown in *Figure 3*.

The resistor divider should be chosen in accordance with the following equation:

Equation 1

$$V_{OUT1} = V_{FB1} \times \left(1 + \frac{R1}{R2}\right)$$

It is recommended to use a resistor with a value in the range of 1 kΩ to 50 kΩ. Lower values can also be suitable, but increase current consumption.

For ch2 the device integrates the resistor divider needed to set the correct output voltage. This allows 2 external components to be saved. The FB2 pin must be connected directly to V_{OUT2}.

The output voltage for Ch3 can be adjusted from 0.8 V up to 85 % of the input voltage value by connecting a resistor divider between V_{OUT3} and GND, the middle point of the divider must be connected to FB3 pin, as shown in *Figure 3*.

The resistor divider must be chosen according to the following equation:

Equation 2

$$V_{OUT3} = V_{FB3} \times \left(1 + \frac{R3}{R4}\right)$$

Using a resistor with a value in the range of 1 kΩ to 50 kΩ is recommended. Lower values are also suitable, but increase current consumption.

9.3 Inductor selection

The inductor is the key passive component for switching converters.

The inductor selection must take the boundary conditions in which the converter works into consideration, the maximum input voltage for the buck and the minimum input voltage for the boost.

The critical inductance values can then be obtained according to the following formulas:

for the step-down

Equation 3

$$L_{MIN} = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times F_{SW} \times \Delta I_L}$$

and for the step-up

Equation 4

$$L_{MIN} = \frac{V_{IN\_MIN} \times (V_{OUT} - V_{IN\_MIN})}{V_{OUT} \times F_{SW} \times \Delta I_L}$$

where:

F_{SW}: switching frequency

ΔI_L = the peak-to-peak inductor ripple current. As a rule of thumb, the peak-to-peak ripple can be set at 20 % - 40 % of the output current for the step-down and can be set at 20 % - 40 % of the input current for the step-up.

The peak current of the inductor can be calculated as:

Equation 5

$$I_{PEAK-STEP\_DOWN} = (I_{OUT} / 0.8) + \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{2 \times V_{IN\_MAX} \times F_{SW} \times L}$$

Equation 6

$$I_{PEAK-STEP\_UP} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN\_MIN}} + \frac{V_{IN\_MIN} \times (V_{OUT} - V_{IN\_MIN})}{2 \times V_{OUT} \times F_{SW} \times L}$$

In addition to the inductance value, in order to avoid saturation, the maximum saturation current of the inductor must be higher than that of the I_{PEAK}.

9.4 Input and output capacitor selection

It is recommended to use ceramic capacitors with X5R or X7R dielectric and low ESR as input and output capacitors, in order to filter any disturbance present in the input line and to obtain stable operation. The output capacitor is very important for satisfying the output voltage ripple requirement.

The output voltage ripple (V_{OUT_RIPPLE}), in continuous mode, for the step-down channel, can be calculated:

Equation 7

$$V_{OUT\_RIPPLE} = \Delta I_L \times \left[ESR + \frac{1}{8 \times C_{OUT} \times F_{SW}} \right]$$

where ΔI_L is the ripple current and F_{SW} is the switching frequency.

The output voltage ripple (V_{OUT_RIPPLE}), in continuous mode, for the step-up channel, is:

Equation 8

$$V_{OUT\_RIPPLE} = I_{OUT} \times \left[ESR + \frac{(V_{OUT} - V_{IN})}{V_{OUT} \times C_{OUT} \times F_{SW}} \right]$$

where F_{SW} is the switching frequency.

The use of ceramic capacitors with voltage ratings in the range higher than 1.5 times the maximum input or output voltage is recommended.

9.5 Layout considerations

Due to the high switching frequency and peak current, the layout is an important design step for all switching power supplies. Important parameters (efficiency, output voltage ripple, switching noise immunity, etc.) can be affected if the PCB layout is not designed with close attention to the following DC-DC general layout rules, such as:

- Short, wide traces must be implemented for mains current and for power ground paths. The input capacitor must be placed as close as possible to the IC pins as well as the inductor and output capacitor.
- The feedback pin (FB) connection to the external resistor divider is a high impedance node, so interference can be minimized by placing the routing of the feedback node as far as possible from the high current paths. To reduce pick up noise the resistor divider must be placed very close to the device.
- A common ground node minimizes ground noise.
- The exposed pad of the package must be connected to the common ground node.

Moreover, the exposed pad ground connection must be properly designed in order to facilitate the heat dissipation from the exposed pad to the ground layer using PCB vias, as shown in the recommended PCB layout of *Figure 34*, *35*, and *36*.

10 Recommended PCB layout

Figure 34. Component placement

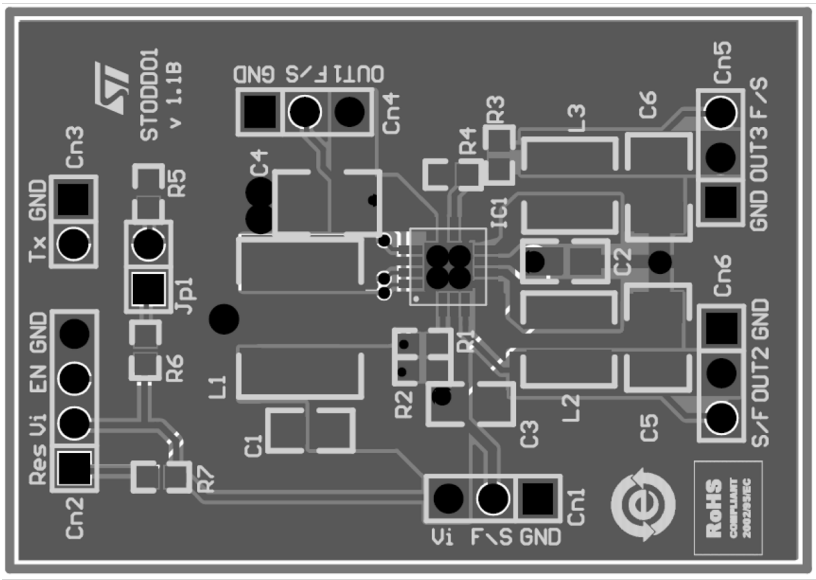


Figure 35. Top layer routing

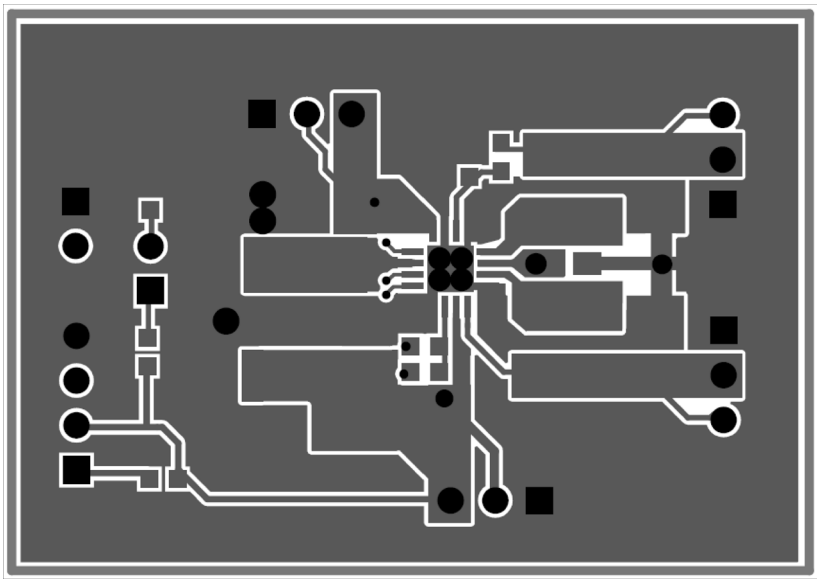
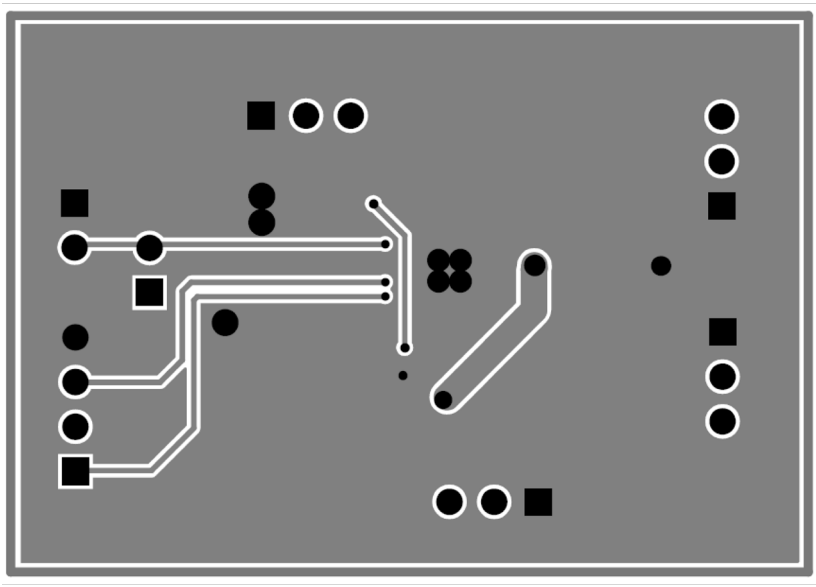


Figure 36. Bottom layer routing



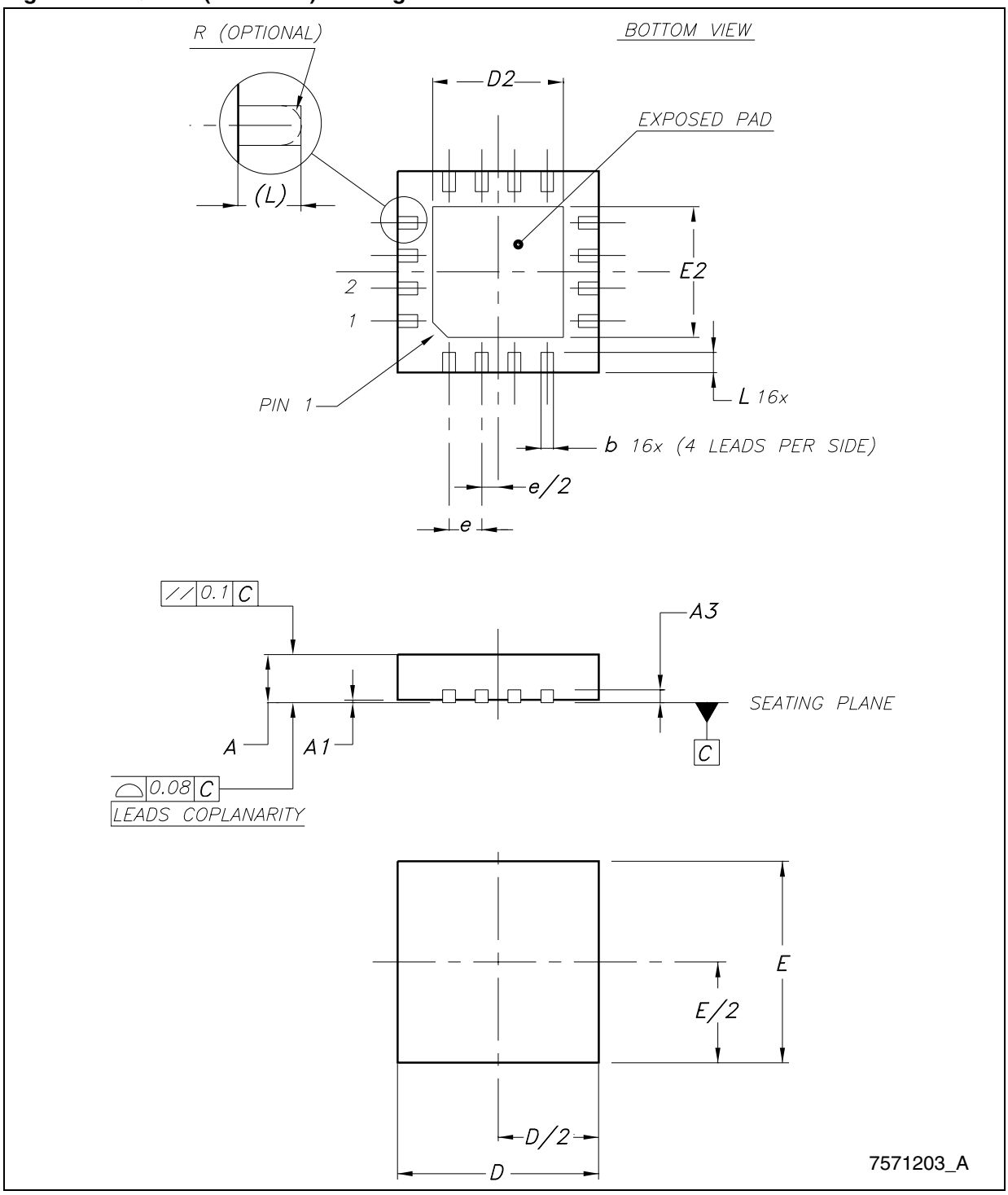
11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status, are available at www.st.com. ECOPACK is an ST trademark.

Table 10. QFN16 (4 x 4 mm.) mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	3.90	4.00	4.10
D2	2.50		2.80
E	3.90	4.00	4.10
E2	2.50		2.80
e		0.65	
L	0.30	0.40	0.50

Figure 37. QFN16 (4 x 4 mm.) drawing



Tape & reel QFNxx/DFNxx (4x4) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	99		101	3.898		3.976
T			14.4			0.567
Ao		4.35			0.171	
Bo		4.35			0.171	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	

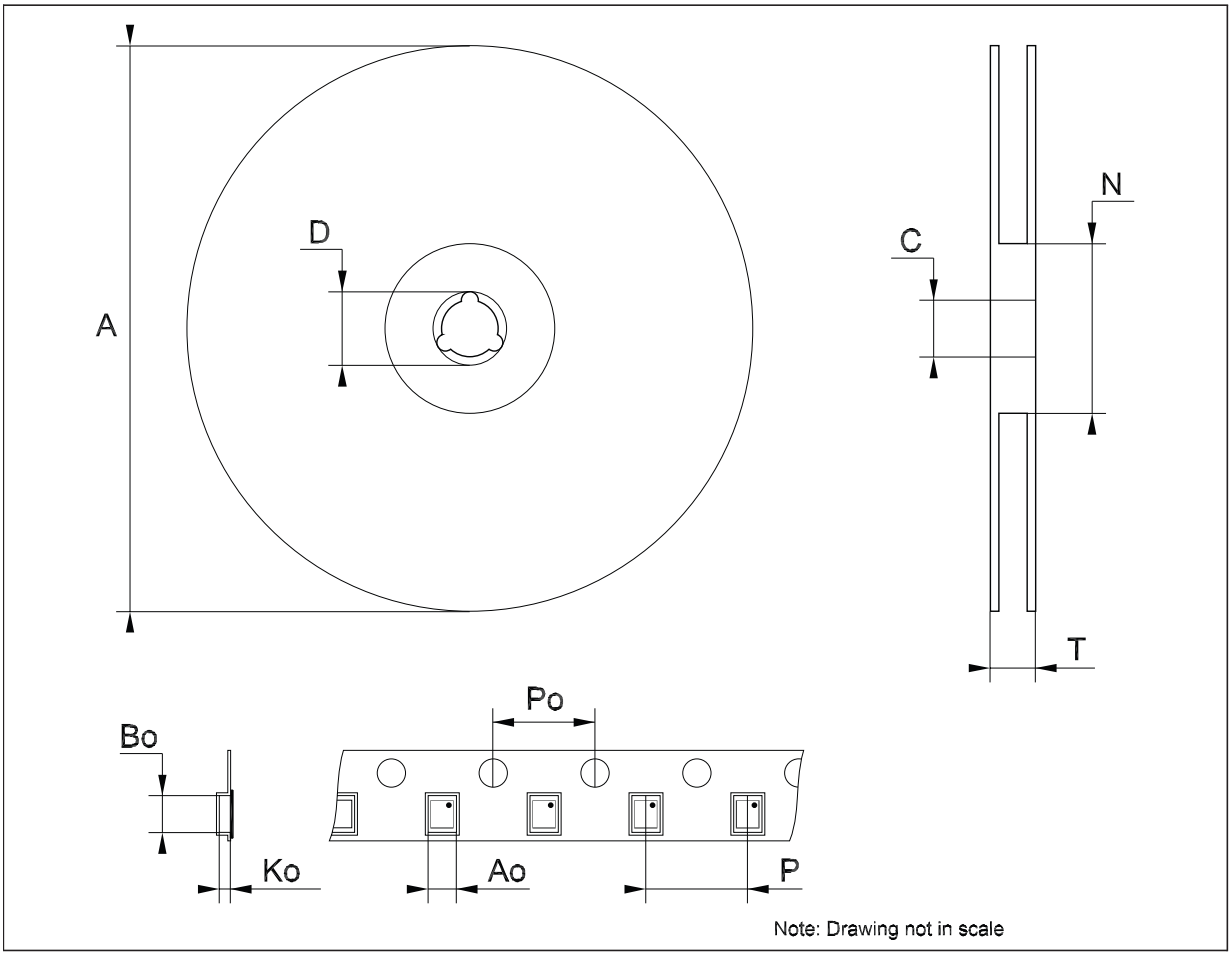
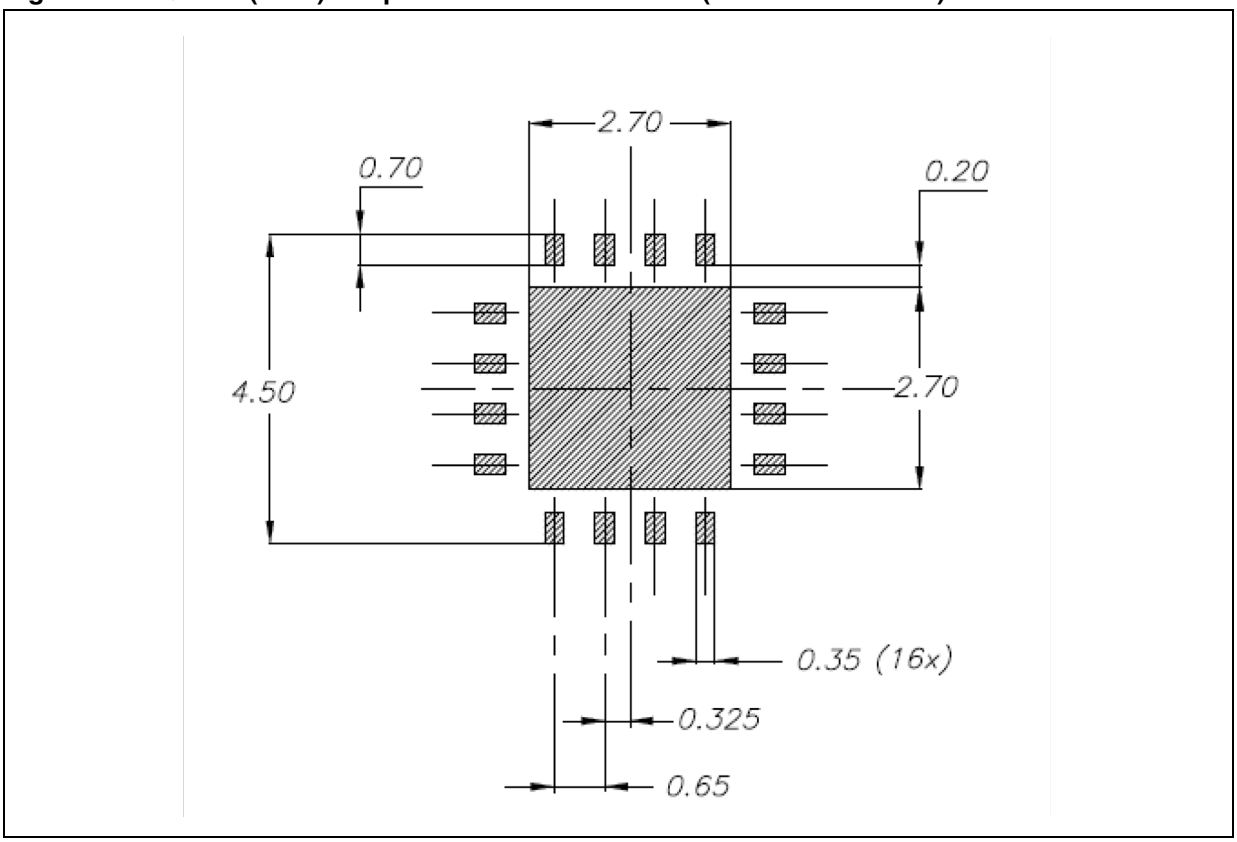


Figure 38. QFN16 (4 x 4) footprint recommended data (dimension in mm.)



12 Revision history

Table 11. Document revision history

Date	Revision	Changes
03-Aug-2010	1	First release.
28-Feb-2011	2	Updated QFN16 mechanical data *Table 10 on page 26*, *Figure 37 on page 27*.