



P-Channel Enhancement MOSFET

Features

- Drain-Source Breakdown Voltage V_{DSS} =40V
- Drain-Source On-Resistance
 $R_{DS(ON)}$ 15mΩ, at $V_{GS} = -10V$, $I_D = -12A$
 $R_{DS(ON)}$ 18mΩ, at $V_{GS} = -4.5V$, $I_D = -6A$
- Continuous Drain Current at $T_C=25^\circ C$ $I_D = -30A$
- Advanced high cell density Trench Technology
- RoHS Compliance & Halogen Free

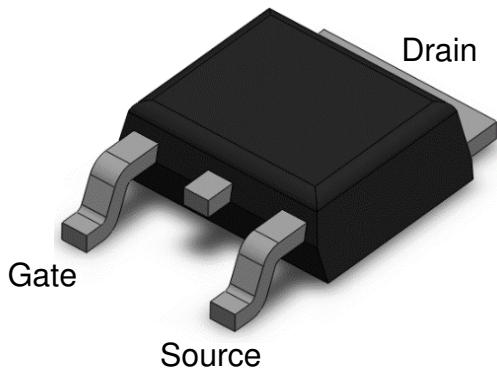
Description

The CTH3004PS-T52 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

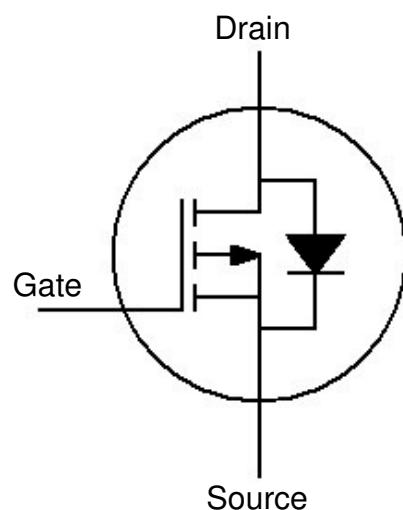
Applications

- Load Switch
- DC/DC Converter
- LCD Display inverter

Package Outline



Schematic





CTH3004PS-T52

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Absolute Maximum Rating at 25°C

Symbol	Parameters	Test Conditions	Min	Note
V _{DS}	Drain-Source Voltage	-40	V	
V _{GS}	Gate-Source Voltage	±20	V	
I _D	Continuous Drain Current @T _c =25°C	-30	A	1
I _{DM}	Pulsed Drain Current	-100	A	1
P _D	Total Power Dissipation @T _c =25°C	25	W	2
T _{STG}	Storage Temperature Range	-55 to 150	°C	
T _J	Operating Junction Temperature Range	-55 to 150	°C	

Thermal Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
R _{θJC}	Thermal Resistance Junction-Case		--	--	5	°C /W	1,4



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Electrical Characteristics $T_A = 25^\circ\text{C}$ (unless otherwise specified)

Static Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
V_{BDSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}$, $I_D = -250\mu\text{A}$	-40	-	-	V	
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = -40\text{V}$, $V_{GS} = 0\text{V}$	-	-	-1	μA	
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$	-	-	± 100	nA	

On Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS} = -10\text{V}$, $I_D = -12\text{A}$	-	15	18	$\text{m}\Omega$	3
		$V_{GS} = -4.5\text{V}$, $I_D = -6\text{A}$	-	18	25	$\text{m}\Omega$	3
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\mu\text{A}$	-1.5	-1.8	-3.0	V	3

Dynamic Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = -20\text{V}$ $f = 1\text{MHz}$	-	2760	3726	pF	
C_{oss}	Output Capacitance		-	260	-		
C_{rss}	Reverse Transfer Capacitance		-	85	-		

Switching Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$T_{D(ON)}$	Turn-On Delay Time	$V_{DS} = -15\text{V}$, $R_L = 15\Omega$, $V_{GS} = -10\text{V}$, $R_G = 6\Omega$, $I_D = -1\text{A}$	-	48	64	ns	
T_R	Rise Time		-	24	32		
$T_{D(OFF)}$	Turn-Off Delay Time		-	88	118		
T_F	Fall Time		-	34	45		
Q_G	Total Gate Charge	$V_{DS} = -20\text{V}$, $V_{GS} = -4.5\text{V}$, $I_D = -12\text{A}$	-	25	33	nC	
Q_{GS}	Gate-Source Charge		-	11	-		
Q_{GD}	Gate-Drain (Miller) Charge		-	9.5	-		



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Drain-Source Diode Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
V _{SD}	Body Diode Forward Voltage	V _{GS} = 0V, I _{SD} = -1.7A	-	-0.78	-1.2	V	1
I _{SD}	Body Diode Continuous Current		-	-	-1.7	A	1

Note:

1. The power dissipation is limited by 150°C junction temperature.
2. The data tested by pulsed , pulse width \leq 300μs , duty cycle \leq 2%
3. Thermal Resistance follow JESD51-3.



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Typical Characteristic Curves

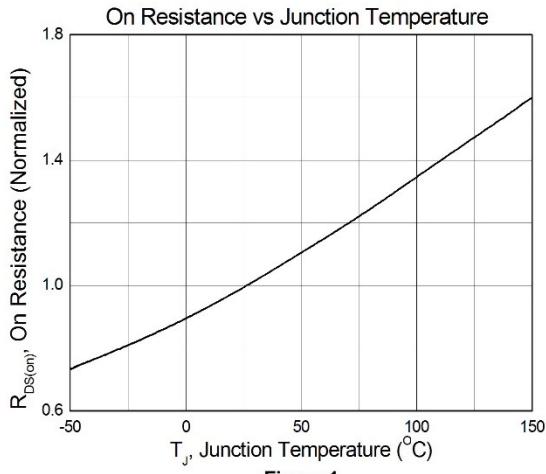


Figure 1

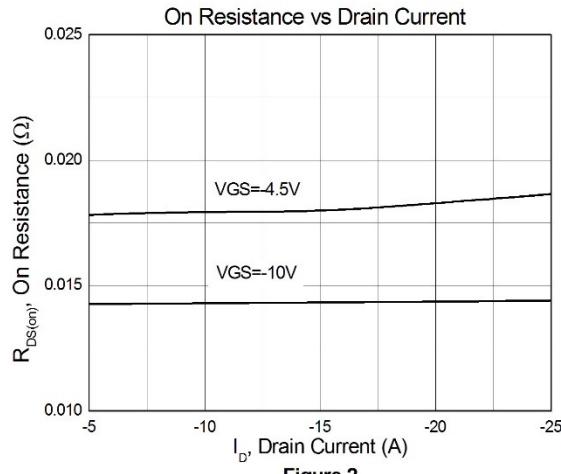


Figure 2

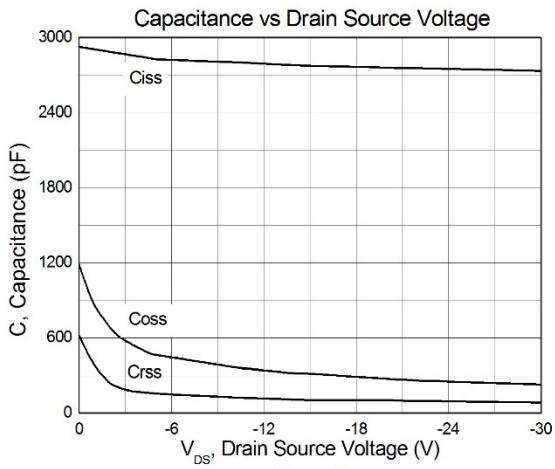


Figure 3

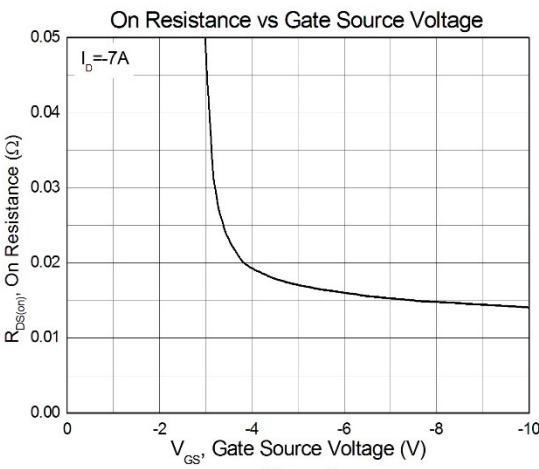


Figure 4

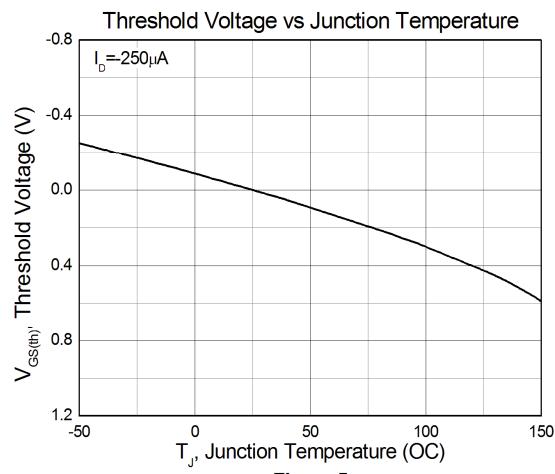


Figure 5

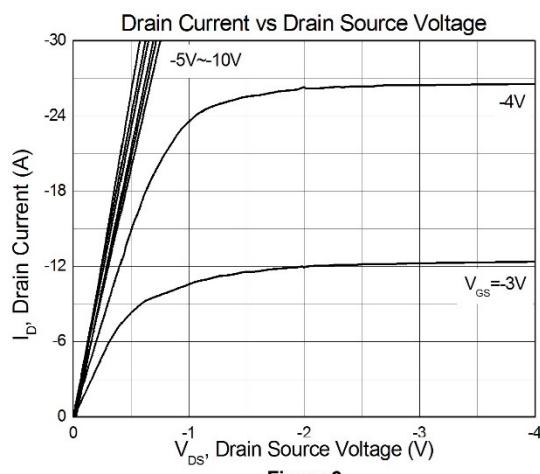


Figure 6



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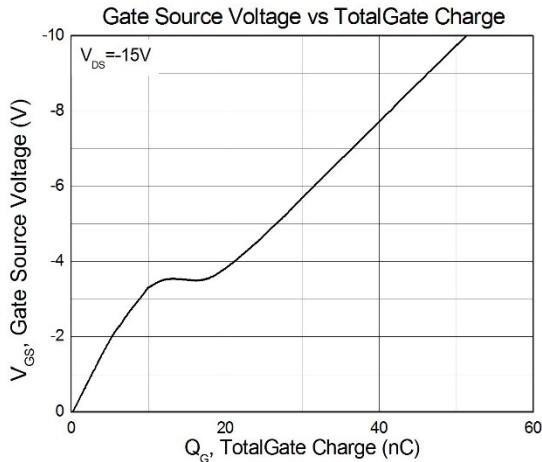


Figure 7

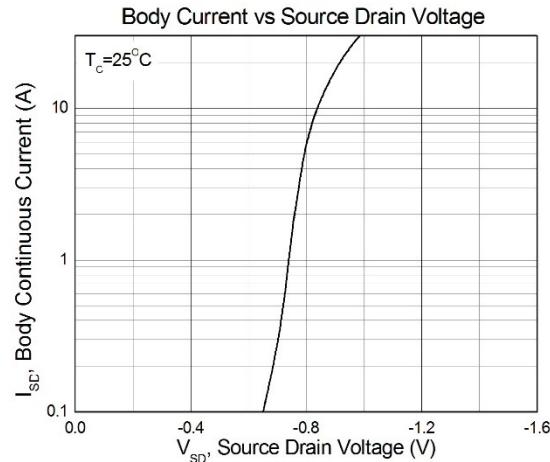


Figure 8



Test Circuits & Waveforms

Figure 9: Gate Charge Test Circuit

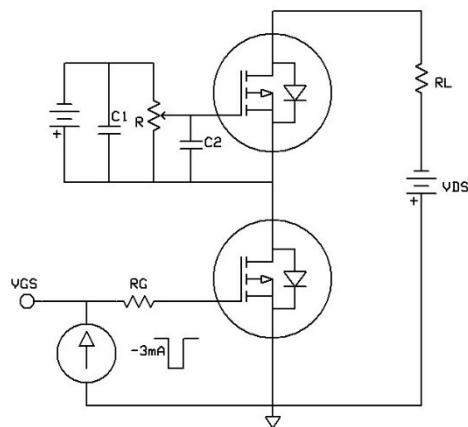


Figure 10: Gate Charge Waveform

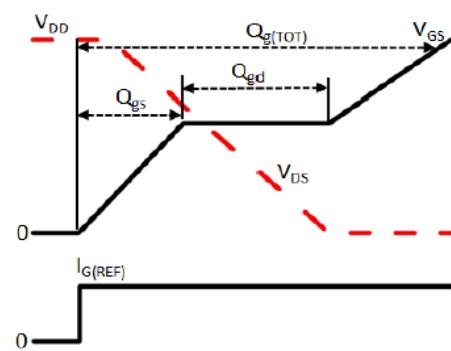


Figure 11: Switching Time Test Circuit

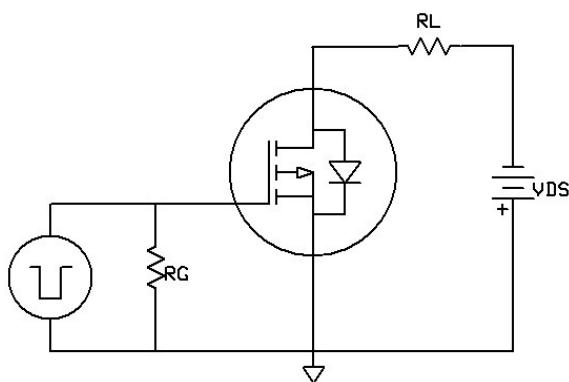
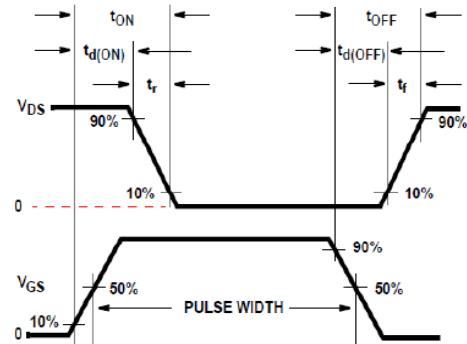


Figure 12: Switching Time Waveform

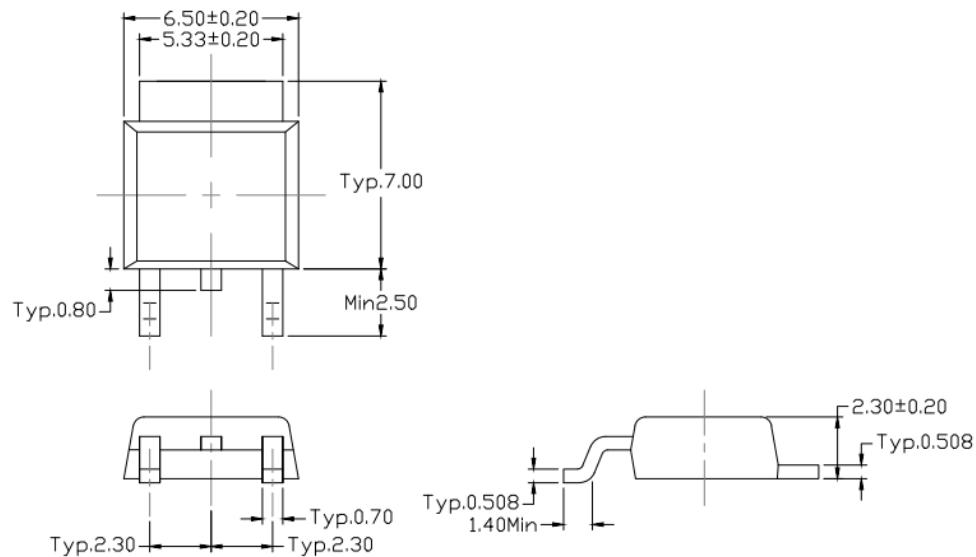




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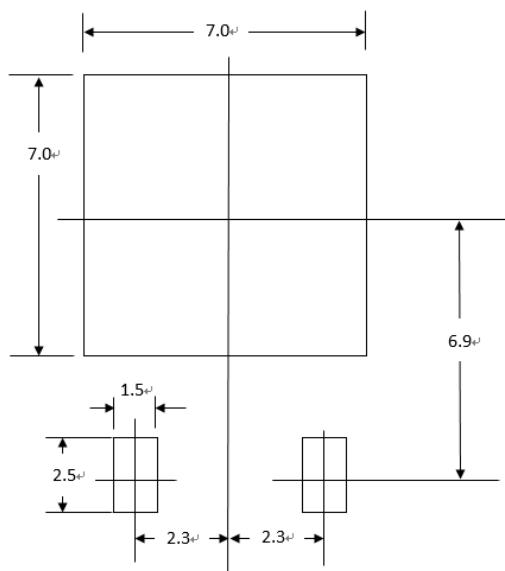
P-Channel Enhancement MOSFET

Package Dimension (TO-252)



Dimensions in mm unless otherwise stated

Recommended pad layout for surface mount leadform

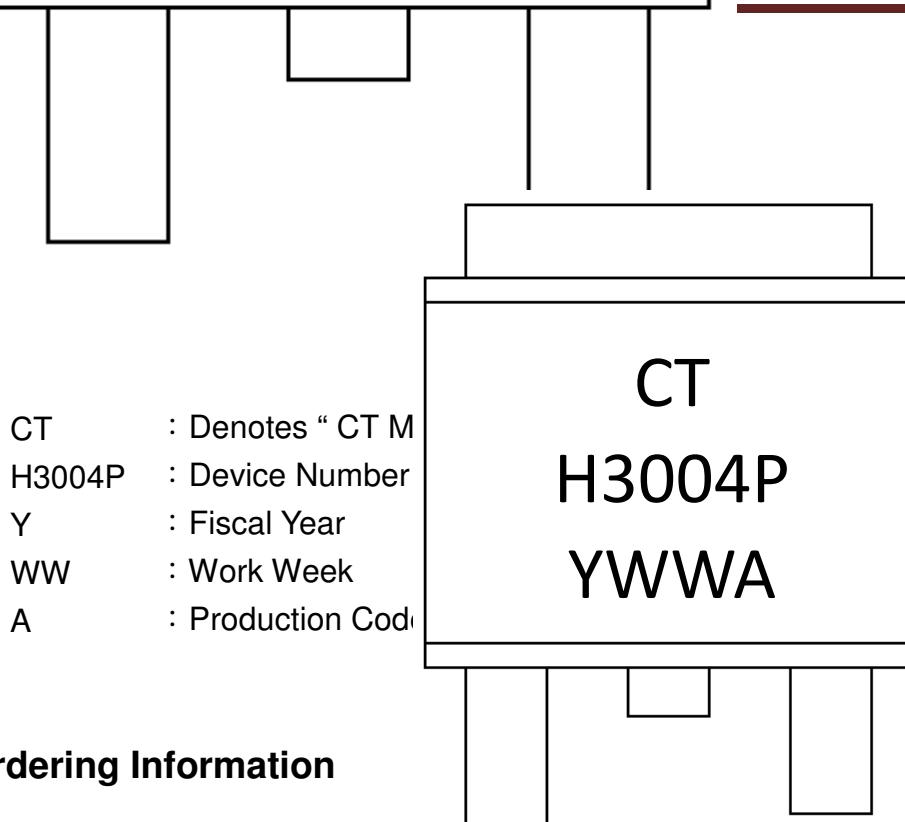


Dimensions in mm unless otherwise stated

CT H3004P
YWWA

CTH3004PS-T52

Channel Enhancement MOSFET



CT : Denotes "CT M"
H3004P : Device Number
Y : Fiscal Year
WW : Work Week
A : Production Code

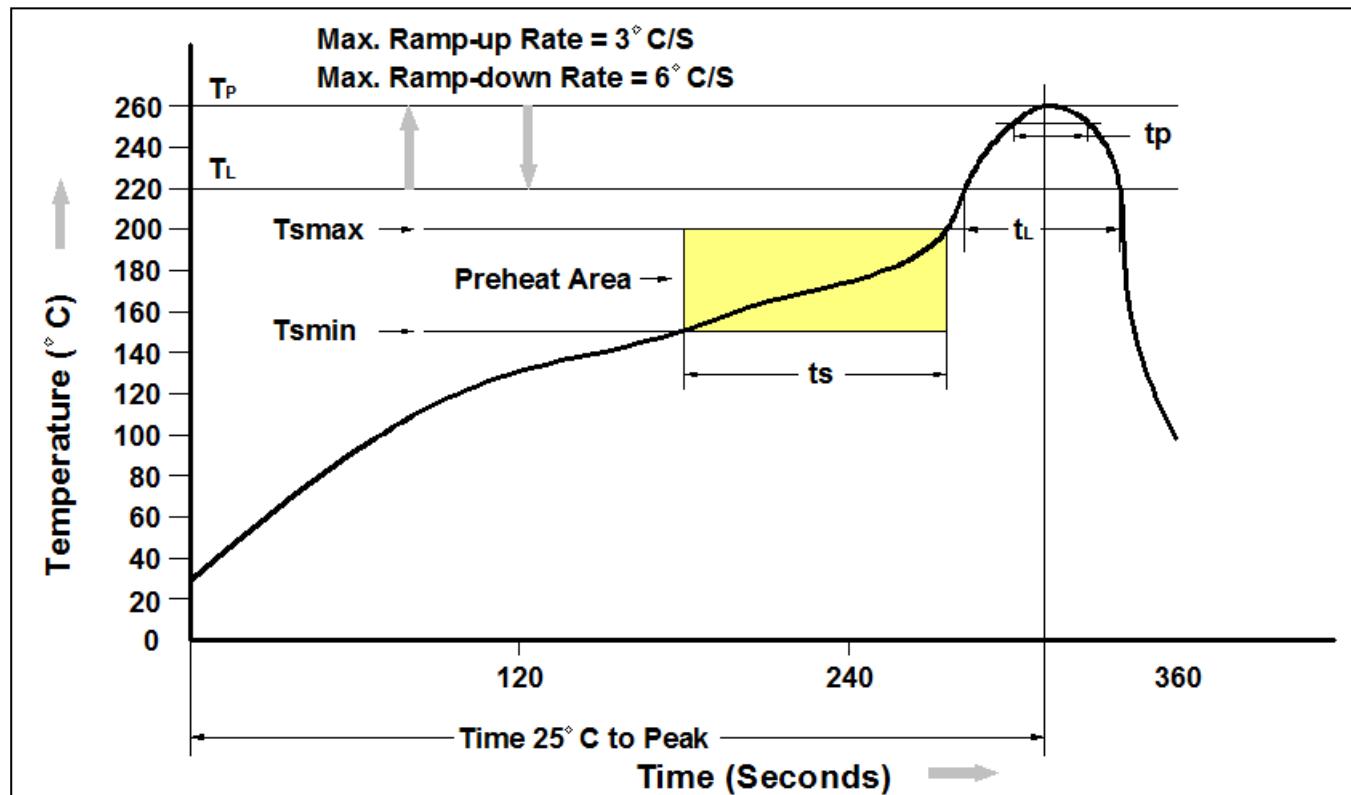
Ordering Information

Part Number	Description	Quantity
CTH3004PS-T52	TO-252 Reel	2500 pcs



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Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (T_{smin})	150°C
Temperature Max. (T_{smax})	200°C
Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds
Ramp-up Rate (t_L to t_P)	3°C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60 – 150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp-down Rate (T_P to T_L)	6°C/second max
Time 25°C to Peak Temperature	8 minutes max.



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