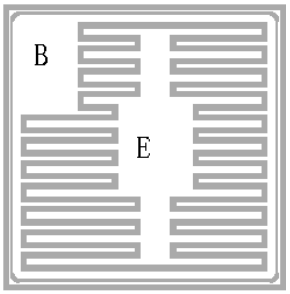
AMERICAN MICROSEMICONDUCTOR

Type: NPN PLANAR SILICON POWER TRANSISTOR

CHIP : AM-GN25C
DEVICE : AMCC44H5
PACKAGE : TO-220

CHIP Appearance	CHIP Dimensions		Size	
			in mils	in mm
	CHIP SIZE		100 X 100	2.5 X 2.5
	CHIP THICKNESS		10.6+/-0.8	0.270 +/- 0.020
	BONDING PAD	BASE	21.7 X 33.9	0.550 X 0.860
	DIMENSION	EMITTER	25.6. X 33.9	0.650 X 0.860
	SCRIBE TRACK WIDTH		3.1	0.08
	TOP METAL		Al	
	BACK METAL		Ag	
	WAFER SIZE		4" DIA(100mm)	
	SURFACE PASSIVATION		Si3N4	

ABSOLUTE MAXIMUM RATINGS

(Ratings at T_A = 25°C)

DESCRIPTION	Symbol	Value	Unit	
Collector Current	I_C	10	A	
Collector Power Dissipation	P_C	50	W	
Operating And Storage Junction Temperature	Tj, T_{stg}	-55 to +150	°C	
Overall Yield Assurance		95	%	
Yield to Prime Device		95	%	

Electrical Characterstics

ITEM	SYMBOL	MIN	TYP.	MAX.	UNIT	CONDITION
Collector- Emitter Voltage	BV_{CEO}	45	-	-	V	I_C=1.0 mA, I_B=0
Emitter- Base Voltage	BV_{EBO}	5	-	-	V	I_E=100 uA, I_C=0
Collector Cut-Off Current	I_{CES}	-	-	10	μA	V_{CE}=Rated V_{CEO}, V_{EB}=0
Emitter Cut-Off Current	I_{EBO}	-	-	100	uA	V_{EB}=5.0V, I_C=0
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	-	-	1.85	V	I_C=8A, I_B=0.4A
DC Gain	h_{FE}	60	-	-	-	V_{CE}=1V, I_C=2A

Notes

1. Wafer shall be 100% probed with minimum yield guarantee of 95% to target device, assuming assembly conditions as per international norms.
2. In case of partial wafers, wafer area shall be greater than 60%.
3. Other specifications shall be as per contract.