4 keys Touch Pad Detector IC

Outline

- The TTP224B TonTouch™ IC is capacitive sensing design specifically for touch pad controls. The device built in regulator for touch sensor. Stable sensing method can cover diversity conditions. Human interfaces control panel links through non-conductive dielectric material. The main application is focused at replacing of the mechanical switch or button. The ASSP can independently handle the 4 touch pads with 4 direct output pins

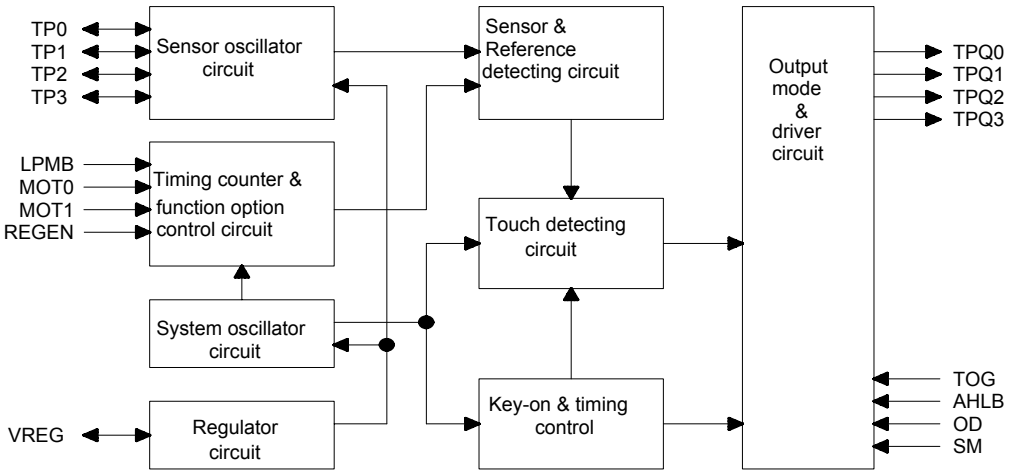
Characteristic

- Operating voltage 2.4V ~ 5.5V
- Built-in regulator with external enable/disable option (REGEN pin)
- Operating current, @VDD=3V no load
  At low power mode typical 2.5uA, At fast mode typical 13uA
- @VDD=3V operating voltage :
  The response time about 160mS at low power mode, 60mS at fast mode
- Sensitivity can adjust by the capacitance（1~50pF）outside for each touch pad
- Provides Fast mode and Low Power mode selection by pad option (LPMB pin)
- Provides direct mode or toggle mode、CMOS output or open drain output、
  active high or active low by pad option (TOG/OD/AHLB pin)
- Have the maximum on time 120sec/64sec/16sec/infinite by pad option(MOT1, MOT0 pin)
- Provides Single-key and Multi-key functions by pad option (SM pin)
- After power-on have about 0.5sec stable-time, during the time do not touch the key pad, and the function is disabled
- Auto calibration for life
- The re-calibration period is about 1 sec within 8 sec after power-on. When key has been touched within 8 sec or key has not been touched more than 8 sec after power-on, then the re-calibration period change to 4 sec

Applications

- Wide consumer products
- Button key replacement

Block diagram



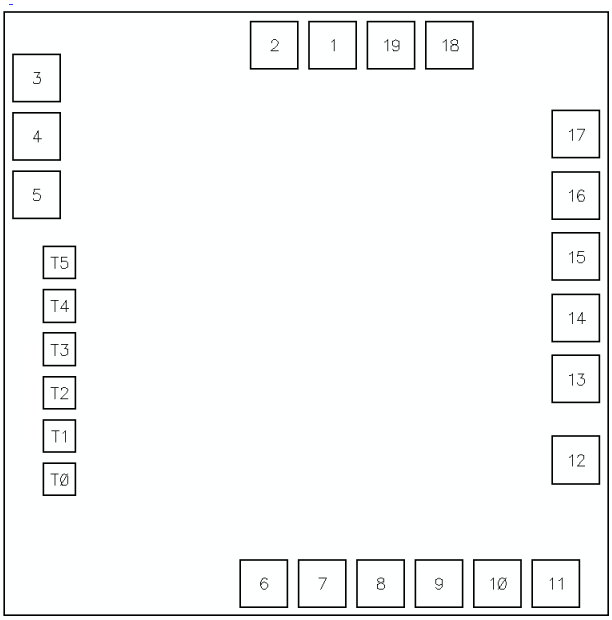
Pin Description

Pad NO	Pad Name	Type	Pad Description
1	TP0	I/O	Touch pad input pin
2	TP1	I/O	Touch pad input pin
3	TP2	I/O	Touch pad input pin
4	TP3	I/O	Touch pad input pin
5	AHLB	I-PL	Output active high or low option, default: 0
6	VDD	P	Positive power supply
7	VREG	P	Internal regulator output pin
8	TOG	I-PL	Output type option, default: 0
9	LPMB	I-PL	Low power/fast mode option, default: 0
10	MOT1	I-PH	Key maximum on time option, default: 1
11	MOT0	I-PH	
12	VSS	P	Negative power supply, ground
13	REGEN	I-PH	Internal regulator enable/disable function option, default: 1
14	OD	I-PH	Output open-drain option, default: 1
15	SM	I-PH	Single/multi key option, default: 1
16	TPQ3	O	Direct output for TP3 touch input pin
17	TPQ2	O	Direct output for TP2 touch input pin
18	TPQ1	O	Direct output for TP1 touch input pin
19	TPQ0	O	Direct output for TP0 touch input pin

Pin Type

- I　CMOS input only
- O　CMOS push-pull output
- I／O　CMOS I／O
- P　Power／Ground
- I-PH　CMOS input and pull-high resister
- I-PL　CMOS input and pull-low resister
- OD　Open drain output, have no Diode protective circuit

Pad's Diagram



CHIP SIZE: 1165um x 1165um
Substrate floating (recommend) or VSS

Pad's Coordinate

Pad NO.	Pad Name	X	Y
1	TP0	47.850	482.950
2	TP1	-57.150	482.950
3	TP2	-485.000	423.850
4	TP3	-485.000	318.850
5	AHLB	-485.000	213.850
6	VDD	-76.450	-485.000
7	VREG	28.550	-485.000
8	TOG	133.550	-485.000
9	LPMB	238.550	-485.000
10	MOT1	343.550	-485.000
11	MOT0	448.550	-485.000
12	VSS	485.000	-263.250
13	REGEN	485.000	-117.600
14	OD	485.000	-7.600
15	SM	485.000	102.400
16	TPQ3	485.000	212.400
17	TPQ2	485.000	322.400
18	TPQ1	257.850	482.950
19	TPQ0	152.850	482.950

Electrical Characteristics

- **Absolute maximum ratings**

Parameter	Symbol	Conditions	Rating	Unit
Operating Temperature	T_{OP}	—	-40～+85	℃
Storage Temperature	T_{STG}	—	-50～+125	℃
Supply Voltage	VDD	Ta=25°C	VSS-0.3～VSS+5.5	V
Input Voltage	V_{IN}	Ta=25°C	VSS-0.3～VDD+0.3	V
Human Body Mode	ESD	—	5	KV
Note：VSS symbolizes for system ground				

- **DC / AC characteristics：（Test condition at room temperature = 25 ℃）**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	Internal regulator disable	2.0		5.5	V
		Internal regulator enable	2.4		5.5	V
Internal Regulator Output	VREG		2.2	2.3	2.4	V
Operating Current	I_{OPL}	VDD=3V, At low power mode(regulator enable)		2.5		uA
	I_{OPF}	VDD=3V, At fast mode (regulator enable)		13.0		uA
Input Ports	V_{IL}	Input Low Voltage	0		0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8		1.0	VDD
Output Port Sink Current	I_{OL}	VDD=3V, V_{OL}=0.6V		8		mA
Output Port Source Current	I_{OH}	VDD=3V, V_{OH}=2.4V		-4		mA
Input Pin Pull-high Resistor	R_{PH}	VDD=3V		30K		ohm
Input Pin Pull-low Resistor	R_{PL}	VDD=3V		25K		ohm
Output Response Time	T_R	VDD=3V、 At fast mode		60		mS
		VDD=3V、 At low power mode		160		

Function Description

Ⅰ. Sensitivity adjustment

The total loading of electrode size and capacitance of connecting line on PCB can affect the sensitivity. So the sensitivity adjustment must according to the practical application on PCB. The TTP224B offers some methods for adjusting the sensitivity outside

1. by the electrode size

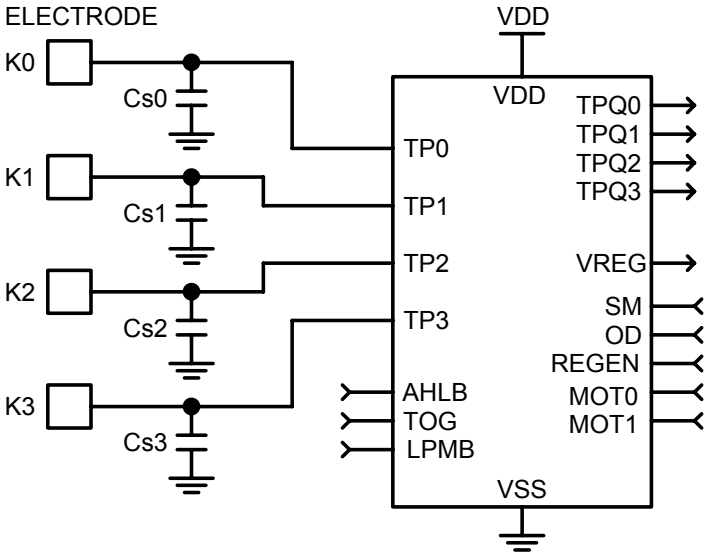
   Under other conditions are fixed. Using a larger electrode size can increase sensitivity. Otherwise it can decrease sensitivity. But the electrode size must use in the effective scope

2. by the panel thickness

   Under other conditions are fixed. Using a thinner panel can increase sensitivity. Otherwise it can decrease sensitivity. But the panel thickness must be below the maximum value

3. by the value of Cs0~Cs3（please see the down figure）

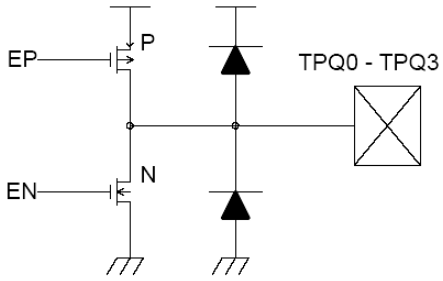
   Under other conditions are fixed. Add the capacitors Cs0~Cs3 can fine tune the sensitivity for single key, that lets all key's sensitivity identical. When do not use any capacitor to VSS, the sensitivity is most sensitive. When adding the values of Cs0~Cs3 will reduce sensitivity in the useful range（1≦Cs0~Cs3≦50pF）



Ⅱ. Output mode（By TOG、OD、AHLB pad option）

The TTP224B outputs（TPQ0~TPQ3）has direct mode active high or low by AHLB pad option, has toggle mode by TOG pad option and has open drain(have diode protective circuit) mode by OD pad option

TOG	OD	AHLB	Pad TPQ0 ～ TPQ3 option features	Remark
0	1	0	Direct mode, CMOS output active high	Default
0	1	1	Direct mode, CMOS output active low	
0	0	0	Direct mode, Open drain output active high	
0	0	1	Direct mode, Open drain output active low	
1	1	0	Toggle mode, CMOS output, Power on state=0	
1	1	1	Toggle mode, CMOS output, Power on state=1	
1	0	0	Toggle mode, Power on state high-Z, Active high	
1	0	1	Toggle mode, Power on state high-Z, Active low	



Ⅲ. Key operating mode（By SM pad option）

The TTP224B has the Single-key and Multi-key functions by SM pad option

SM	Option features	Remark
1	Multi-key mode	Default
0	Single key mode	

Multi-key mode：The TP0-TP3 can be detected 2 keys or above 2 keys at the same time

Single-key mode：The TP0-TP3 can be detected 1 key only at the same time, when any key be detected, the other 3 keys can not be detected

Ⅳ. Maximum key on duration time（By MOT1、MOT0 pad option）

If some objects cover in the sense pad, and causing the change quantity enough to be detected. To prevent this, the TTP224B sets a timer to monitor the detection. The timer is the maximum on duration time. When the detection is over the timer, the system will return to the power-on initial state, and the output becomes inactive until the next detection

MOT1	MOT0	Option features	Remark
0	0	Maximum on time 120 sec	
0	1	Maximum on time 64 sec	
1	0	Maximum on time 16 sec	
1	1	Infinite（Disable maximum on time）	Default

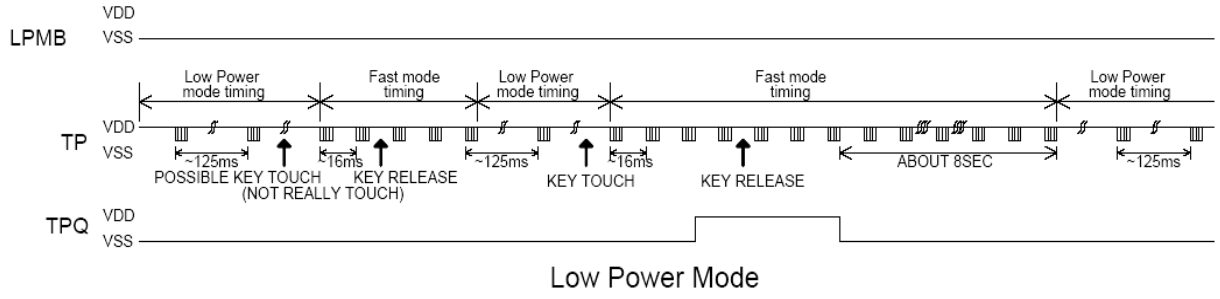
Ⅴ. Fast and Low power mode select（By LPMB pad option）

The TTP224B has Fast mode and Low Power mode to be selected. It depends on the state of LPMB pad. When the LPMB pin is connected to VDD, the TTP224B runs in Fast mode. When the LPMB pin is opened or connected to VSS, the TTP224B runs in Low Power mode.

In the Fast mode response time is faster, but the current consumption will be increased. In the Low Power mode it will be saving power, but will be slowing response time for first touch. When it awaked in fast mode, the response time is the same the fast mode. In this mode when detecting key touch, it will switch to Fast mode. Until the key touch is released and will keep a time about 8sec. Then it returns to Low Power mode.

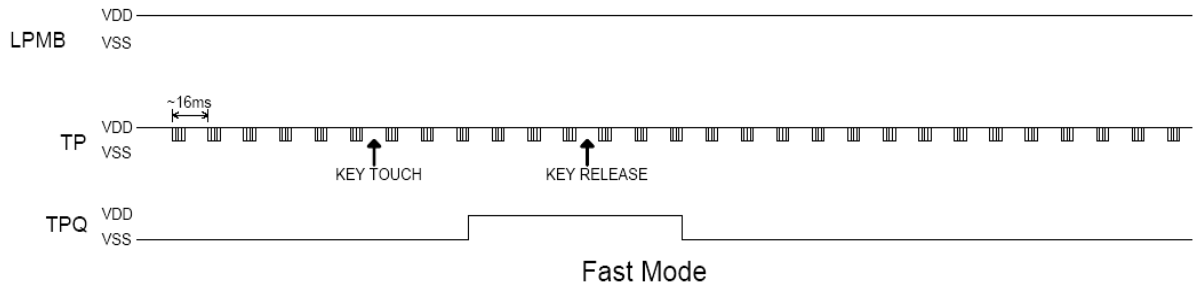
The states and timing of two modes please see below figure.

Low Power Mode timing diagram:



Low Power Mode

Fast Mode timing diagram:



Fast Mode

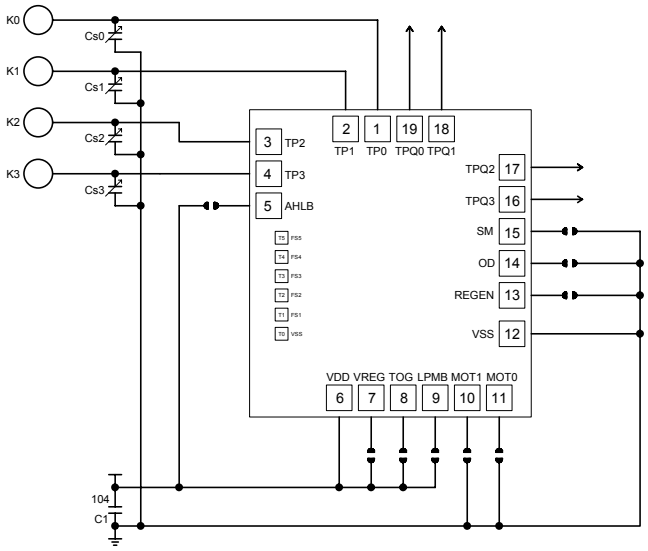
LPMB	Option features	Remark
1	Fast mode	
0	Low Power mode	Default

Ⅵ. Internal regulator enable/disable

The TTP224B built in regulator in the chip. The regulator can be set enable or disable by the REGEN pin. The REGEN pin is opened or connected to VDD, the regulator is enabled. The REGEN pin is connected to VSS, the regulator is disabled. When the internal regulator is disabled, the VREG pin must be connected to external VDD.

REGEN	Option features	Remark
1	Enable internal regulator	Default
0	Disable internal regulator	

Application circuit



Option table:

Output Mode:

TOG	OD	AHLB	Pad TPQ0~TP3 option features
OPEN	OPEN	OPEN	Direct mode, CMOS active high output
OPEN	OPEN	VDD	Direct mode, CMOS active low output
OPEN	VSS	OPEN	Direct mode, Open drain active high output
OPEN	VSS	VDD	Direct mode, Open drain active low output
VDD	OPEN	OPEN	Toggle mode, CMOS output, Power on state =0
VDD	OPEN	VDD	Toggle mode, CMOS output, Power on state =1
VDD	VSS	OPEN	Toggle mode, Power on state high-Z, Active high
VDD	VSS	VDD	Toggle mode, Power on state high-Z, Active low

Key operation mode:

SM	Option features
OPEN	Multi-key mode
VSS	Single key mode

Maximum key on duration time:

MOT1	MOT0	Option features
VSS	VSS	Maximum on time 120sec
VSS	OPEN	Maximum on time 64sec
OPEN	VSS	Maximum on time 16sec
OPEN	OPEN	Infinite(Disable maximum on time)

Internal regulator enable/disable:

REGEN	Option features
OPEN	Internal regulator enable
VSS	Internal regulator disable

Fast and Low power mode:

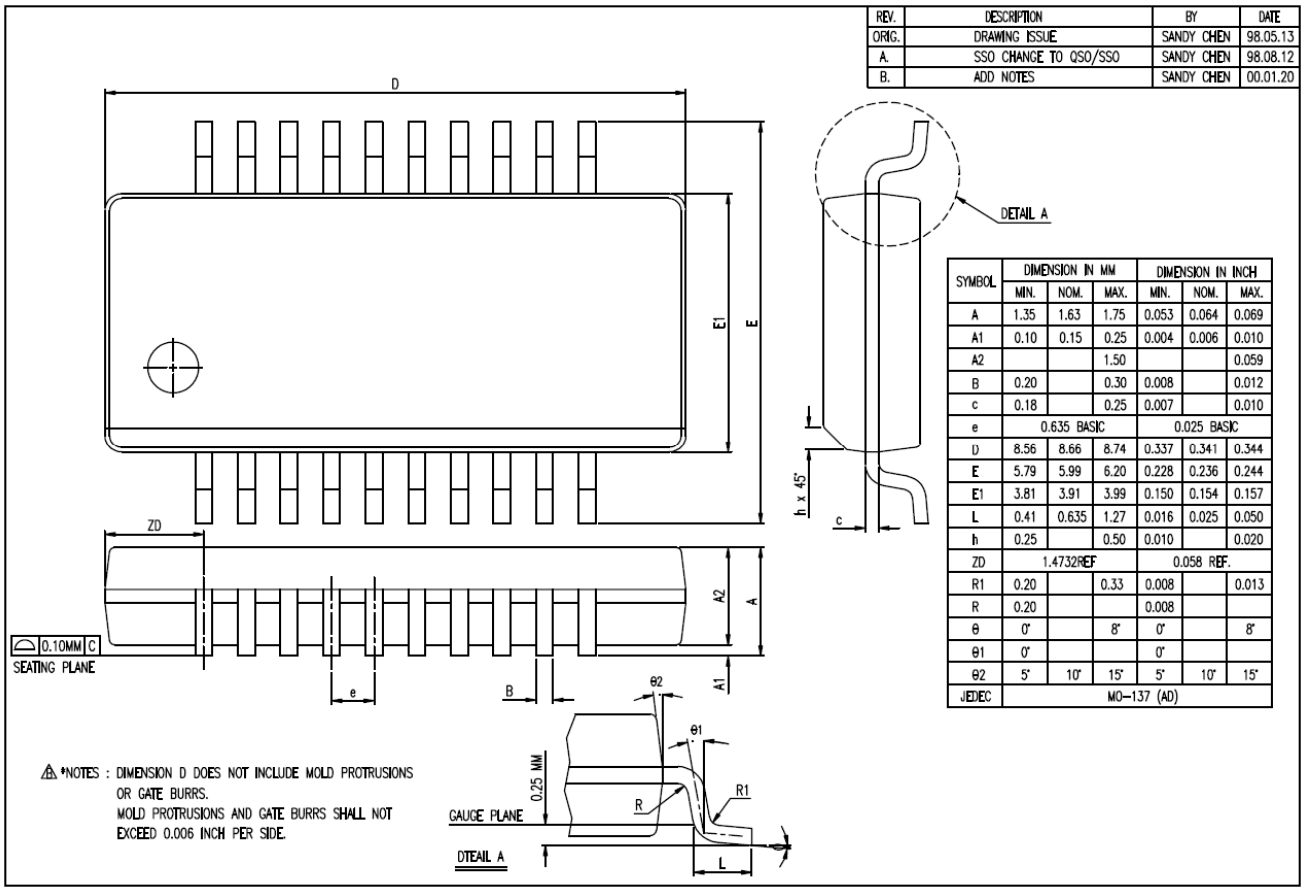
LPMB	Option features
VDD	Fast mode
OPEN	Low Power mode

P.S.：

1. On PCB, the length of lines from touch pad to IC pin shorter is better.
   And the lines do not parallel and cross with other lines.
2. The power supply must be stable. If the supply voltage drift or shift quickly, maybe causing sensitivity anomalies or false detections.
3. The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.
4. The C1 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins (TTP224B).
5. The capacitance Cs0~Cs3 can be used to adjust the sensitivity. The value of Cs0~Cs3 use smaller, then the sensitivity will be better. The sensitivity adjustment must according to the practical application on PCB. The range of Cs0~Cs3 value are 1~50pF.
6. The sensitivity adjustment capacitors（Cs0~Cs3）must use smaller temperature coefficient and more stable capacitors. Such are X7R, NPO for example. So for touch application, recommend to use NPO capacitor, for reducing that the temperature varies to affect sensitivity.

Package outline

Package Type: SSOP-20

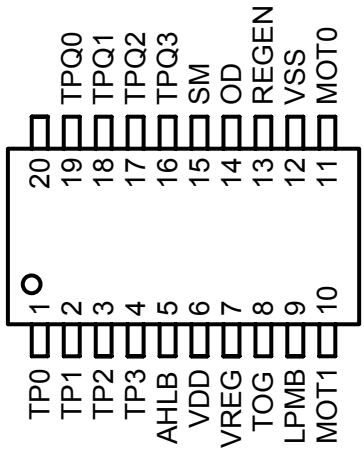


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			1.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025 BASIC		
D	8.56	8.66	8.74	0.337	0.341	0.344
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25		0.50	0.010		0.020
ZD	1.4732REF			0.058 REF.		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ1	0°			0°		
θ2	5°	10°	15°	5°	10°	15°
JEDEC	MO-137 (AD)					

Package configuration

TTP224B-ASD

Package Type SSOP-20



Ordering Information

TTP224B

Package Type	Chip Type	Wafer Type
TTP224B-XXX	TCP224B	TDP224B