# M68Z512

## 4 Mbit (512 Kbit x 8) Low Power SRAM with Output Enable

**FEATURES SUMMARY**

- ■ ULTRA LOW DATA RETENTION CURRENT
  - – 100nA (typical)
  - – 10µA (max)
- ■ OPERATION VOLTAGE: 5.0V ± 10%
- ■ 512 Kbit x 8 SRAM WITH OUTPUT ENABLE
- ■ EQUAL CYCLE and ACCESS TIMES: 70ns
- ■ LOW $V_{CC}$ DATA RETENTION: 2.0V
- ■ TRI-STATE COMMON I/O
- ■ CMOS FOR OPTIMUM SPEED/POWER
- ■ AUTOMATIC POWER-DOWN WHEN DESELECTED
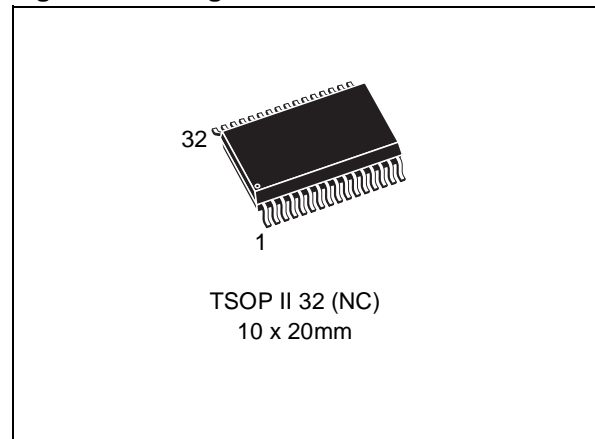- ■ INTENDED FOR USE WITH ST ZEROPOWER® AND TIMEKEEPER® CONTROLLERS

**Figure 1. Package**



TSOP II 32 (NC)
10 x 20mm

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## DESCRIPTION

The M68Z512 is a 4 Mbit (4,194,304 bit) CMOS SRAM, organized as 524,288 words by 8 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ±10% supply, and all inputs and outputs are TTL compatible.

This device has an automatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68Z512 is available in a 32-lead TSOP II (10 x 20mm) package.

### Figure 2. Logic Diagram
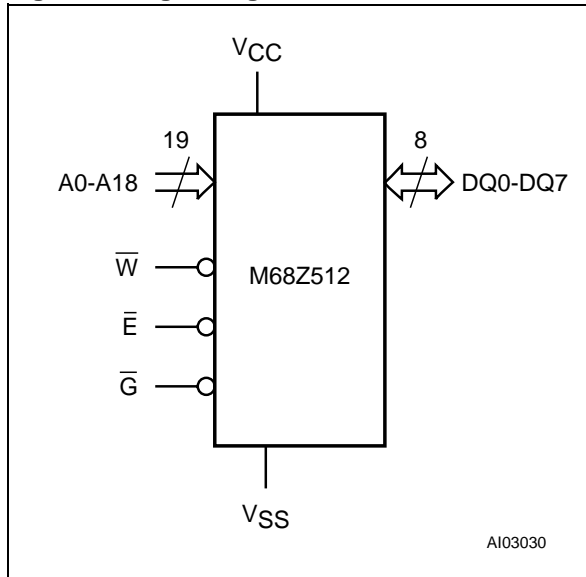


### Table 1. Signal Names

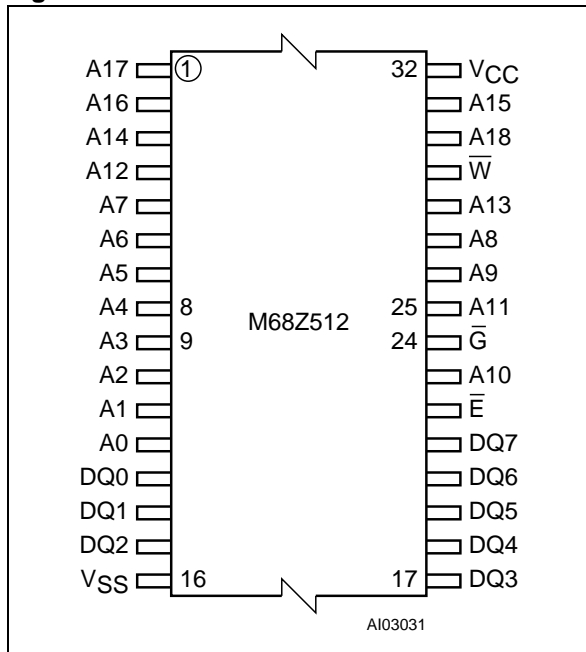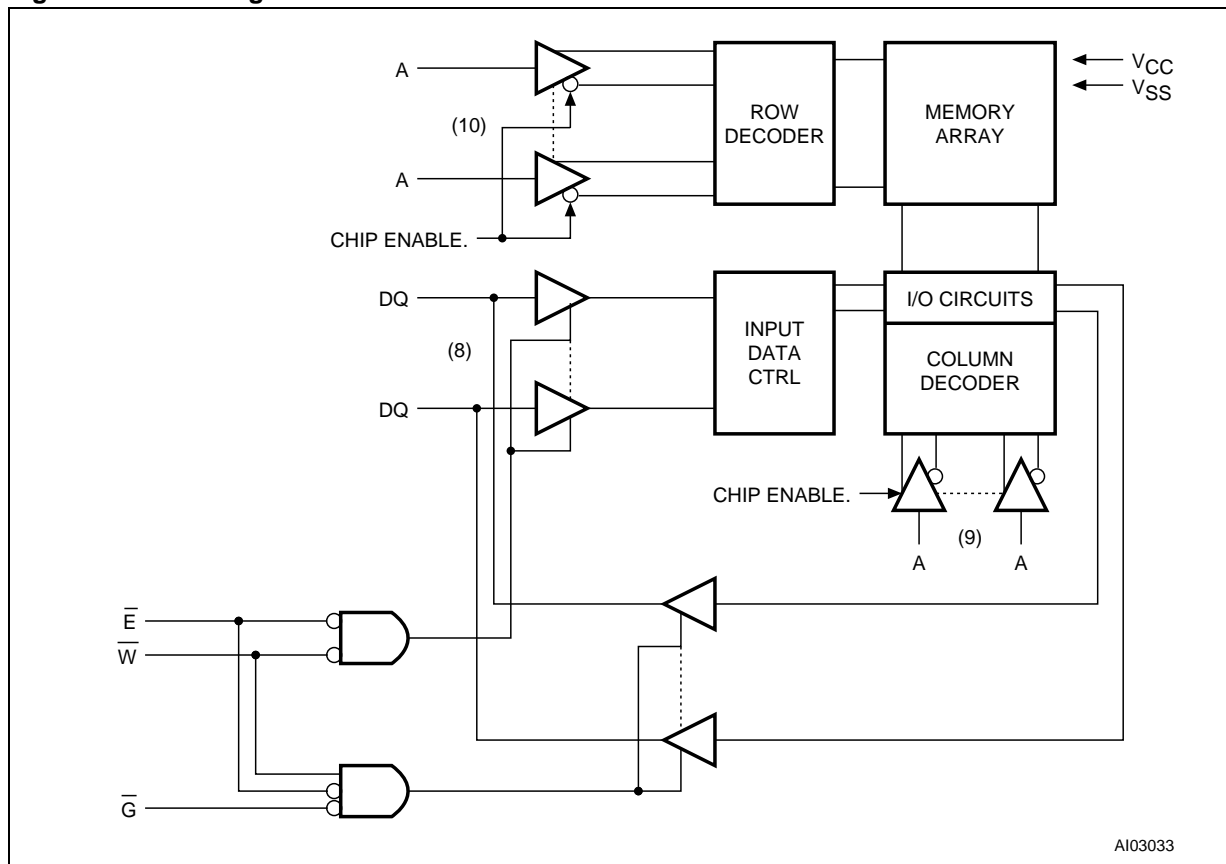| A0-A18 | Address Inputs |
|---|---|
| DQ0-DQ7 | Data Input/Output |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{W}$ | Write Enable |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |

### Figure 3. TSOP Connections

**Figure 4. Block Diagram**



AI03033

## MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 2. Absolute Maximum Ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | 0 to 70 | °C |
| $T_{STG}$[1] | Storage Temperature | −65 to 150 | °C |
| $V_{IO}$[2] | Input or Output Voltage | −0.3 to $V_{CC}$ + 0.3 | V |
| $V_{CC}$ | Supply Voltage | −0.3 to 7.0 | V |
| $I_O$[3] | Output Current | 20 | mA |
| $P_D$ | Power Dissipation | 1 | W |

Note: 1. Reflow at peak temperature of 215°C to 225°C for < 60 seconds (total thermal budget not to exceed 180°C for between 90 to 120 seconds).
2. Up to a maximum operating $V_{CC}$ of 5.5V only.
3. One output at a time, not to exceed 1 second duration.

## DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

**Table 3. DC and AC Measurement Conditions**

| Parameter | M68Z512 |
|---|---|
| $V_{CC}$ Supply Voltage | 4.5 to 5.5V |
| Ambient Operating Temperature | 0 to 70°C |
| Load Capacitance ($C_L$) | 100pF |
| Input Rise and Fall Times | $\leq$ 5ns |
| Input Pulse Voltages | 0 to 3V |
| Input and Output Timing Ref. Voltages | 1.5V |

Note: Output High Z is defined as the point where data is no longer driven (see Table 3, page 5).

**Figure 5. AC Testing Load Circuit**
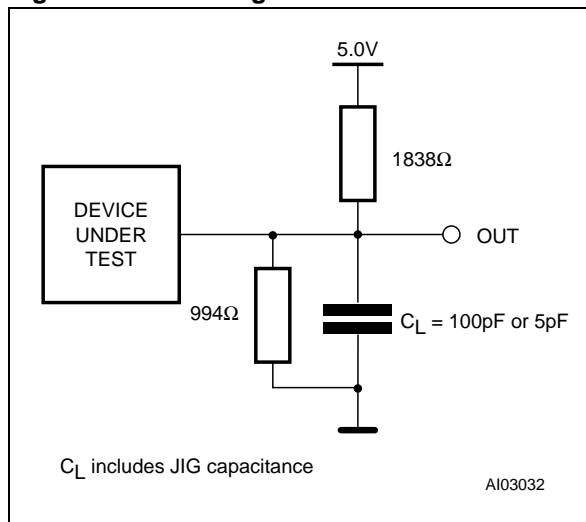


**Table 4. Capacitance**

| Symbol | Parameter[1,2] | Min | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance on all pins (except DQ) | | 6 | pF |
| $C_{OUT}$[3] | Output Capacitance | | 8 | pF |

Note: 1. Sampled only, not 100% tested.
2. Outputs deselected.
3. At 25°C.

### Table 5. DC Characteristics

| Symbol | Parameter | Test Condition[1] | Min | Typ | Max | Unit |
|--------|-----------|-------------------|-----|-----|-----|------|
| $I_{LI}$ | Input Leakage Current | $0V \leq VIN \leq V_{CC}$ | | | ±1 | µA |
| $I_{LO}$ | Output Leakage Current | $0V \leq V_{OUT} \leq V_{CC}$ | | | ±1 | µA |
| $I_{CC1}$[2] | Supply Current | $V_{CC} = 3.6V$ | | | 90 | mA |
| $I_{CC2}$[3] | Supply Current (Standby) TTL | $V_{CC} = 3.6V$, $\overline{E} = V_{IH}$ | | | 15 | mA |
| $I_{CC3}$[4] | Supply Current (Standby) CMOS | $V_{CC} = 3.6V$, $\overline{E} \geq V_{CC} - 0.3V$, $f = 0$ | | 1.6 | 20 | µA |
| $V_{IL}$ | Input Low Voltage | | −0.3 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.2 | | $V_{CC} + 0.3$ | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL} = 2.1mA$ | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH} = -1mA$ | 2.4 | | | V |

Note: 1. Valid for Ambient Operating Temperature: $T_A = 0$ to 70°C; $V_{CC} = 4.5$ to 5.5V (except where noted).
2. Average AC current, Outputs open, cycling at $t_{AVAV}$ minimum.
3. All other Inputs at $V_{IL} \leq 0.8V$ or $V_{IH} \geq 2.2V$.
4. All other Inputs at $V_{IL} \leq 0.3V$ or $V_{IH} \geq V_{CC} -0.3V$.

## OPERATION

The M68Z512 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E}$ = High). An Output Enable ($\overline{G}$) signal provides a high speed tri-state control, allowing fast READ/WRITE Cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$ as summarized in the Operating Modes table (see Table 6).

### Table 6. Operating Modes

| Operation | $\overline{E}$ | $\overline{W}$ | $\overline{G}$ | DQ0-DQ7 | Power |
|-----------|----------------|----------------|----------------|---------|-------|
| Read | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | Hi-Z | Active |
| Read | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | Data Output | Active |
| Write | $V_{IL}$ | $V_{IL}$ | X | Data Input | Active |
| Deselect | $V_{IH}$ | X | X | Hi-Z | Standby |

Note: X = $V_{IH}$ or $V_{IL}$.

## READ Mode

The M68Z512 is in the READ mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and Chip Enable ($\overline{E}$) is asserted. This provides access to data from eight of the 4,194,304 locations in the static memory array, specified by the 19 address inputs. Valid data will be available at the eight output pins within $t_{AVQV}$ after the last stable address, providing $\overline{G}$ is Low and $\overline{E}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter ($t_{ELQV}$ or $t_{GLQV}$) rather than the address. Data out may be indeterminate at $t_{ELQX}$ and $t_{GLQX}$, but data lines will always be valid at $t_{AVQV}$.

**Figure 6. Address Controlled, READ Mode AC Waveforms**
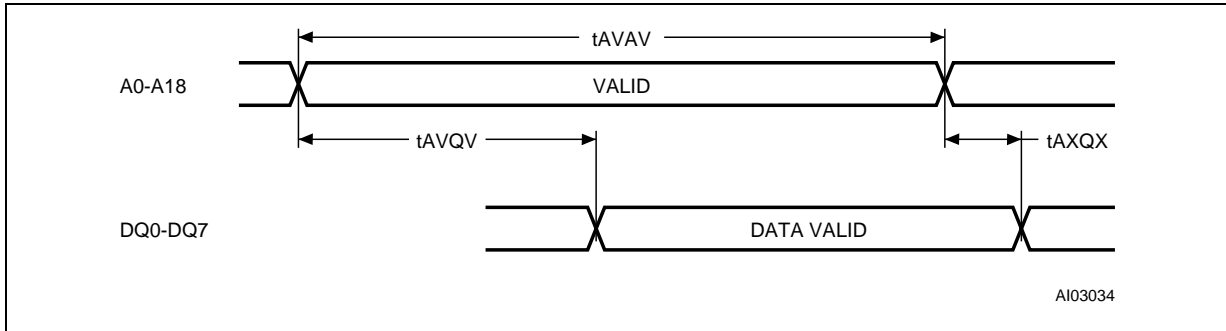


Note: $\overline{E}$ = Low, E2 = High, +$\overline{G}$ = Low, $\overline{W}$ = High.

**Figure 7. Chip Enable or Output Enable Controlled, READ Mode AC Waveforms**
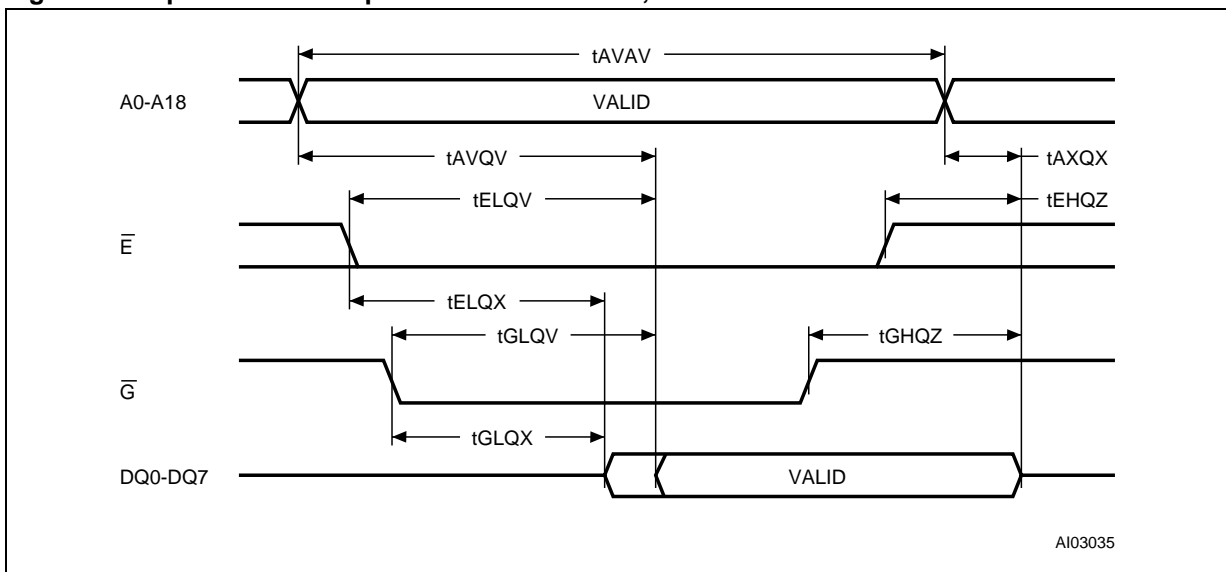


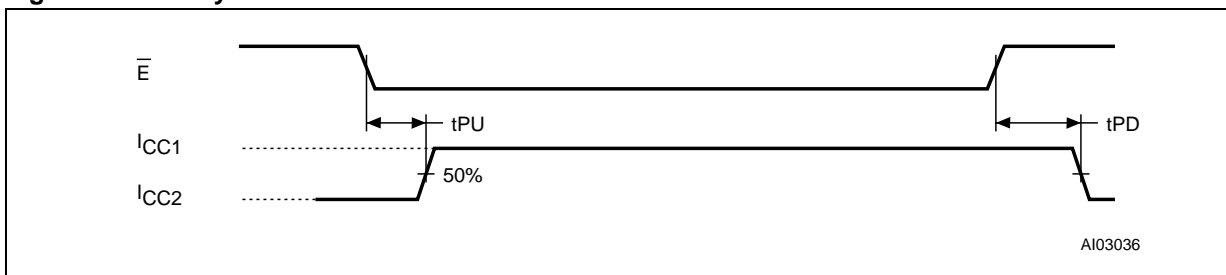Note: Write Enable ($\overline{W}$) = High.

**Figure 8. Standby Mode AC Waveforms**

### Table 7. READ and Standby Modes AC Characteristics

| Symbol | Parameter[1] | M68Z512 −70 Min | M68Z512 −70 Max | Unit |
|--------|--------------|-----|-----|------|
| $t_{AVAV}$ | READ Cycle Time | 70 | | ns |
| $t_{AVQV}$[2] | Address Valid to Output Valid | | 70 | ns |
| $t_{ELQV}$[2] | Chip Enable Low to Output Valid | | 70 | ns |
| $t_{GLQV}$[2] | Output Enable Low to Output Valid | | 35 | ns |
| $t_{ELQX}$[4] | Chip Enable Low to Output Transition | 10 | | ns |
| $t_{GLQX}$[4] | Output Enable Low to Output Transition | 5 | | ns |
| $t_{EHQZ}$[3,4] | Chip Enable High to Output Hi-Z | | 25 | ns |
| $t_{GHQZ}$[3] | Output Enable High to Output Hi-Z | | 25 | ns |
| $t_{AXQX}$[2] | Address Transition to Output Transition | 10 | | ns |
| $t_{PU}$ | Chip Enable Low to Power Up | 0 | | ns |
| $t_{PD}$ | Chip Enable High to Power Down | | 70 | ns |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V (except where noted).
2. $C_L$ = 100pF.
3. $C_L$ = 5pF.
4. At any given temperature and voltage condition, $t_{EHQZ}$ is less than $t_{ELQX}$ and $t_{GHQZ}$ is less than $t_{GLQX}$ for any given device.
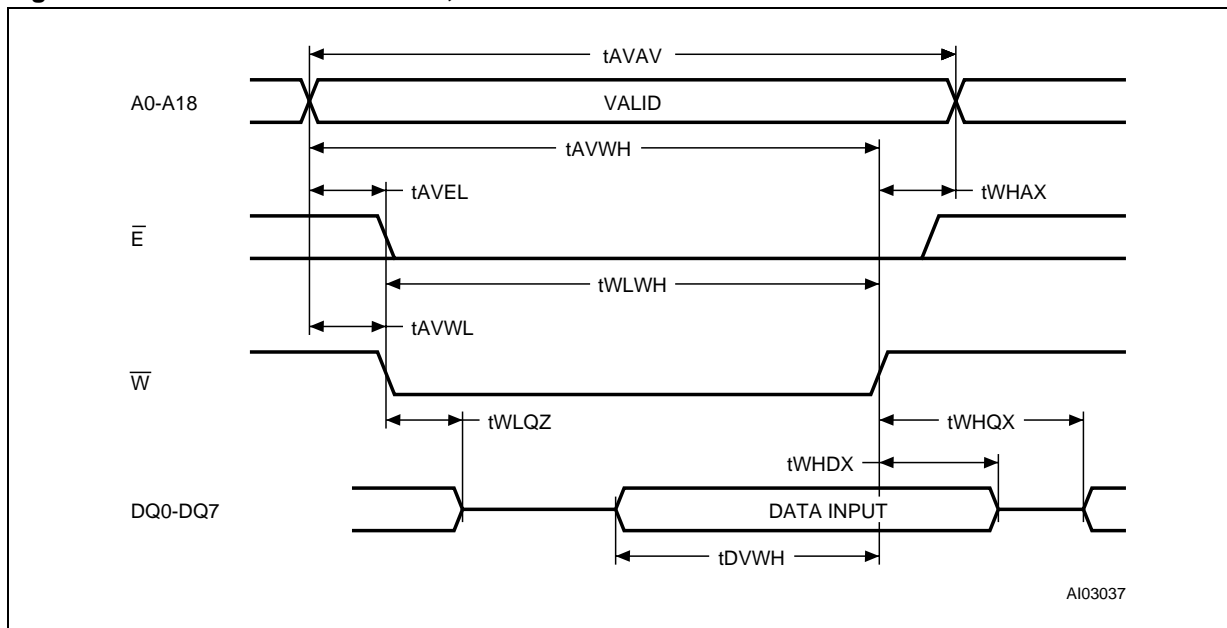
## WRITE Mode

The M68Z512 is in the WRITE mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Either the Chip Enable input ($\overline{E}$) or the WRITE Enable input ($\overline{W}$) must be deasserted during Address transitions for subsequent WRITE cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ low. Therefore, address setup time is referenced to WRITE Enable and Chip Enable as $t_{AVWL}$ and $t_{AVEH}$ respectively, and is determined by the latter occurring edge.

The WRITE Cycle can be terminated by the earlier rising edge of $\overline{E}$, or $\overline{W}$.

If the Output is enabled ($\overline{E}$ = Low and $\overline{G}$ = Low), then $\overline{W}$ will return the outputs to high impedance within $t_{WLQZ}$ of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for $t_{DVWH}$ before the rising edge of WRITE Enable, or for $t_{DVEH}$ before the rising edge of $\overline{E}$, whichever occurs first, and remain valid for $t_{WHDX}$ or $t_{EHDX}$.

**Figure 9. WRITE Enable Controlled, WRITE Mode AC Waveforms**



Note: Output Enable ($\overline{G}$) = Low.

### Figure 10. Chip Enable Controlled, WRITE Mode AC Waveforms
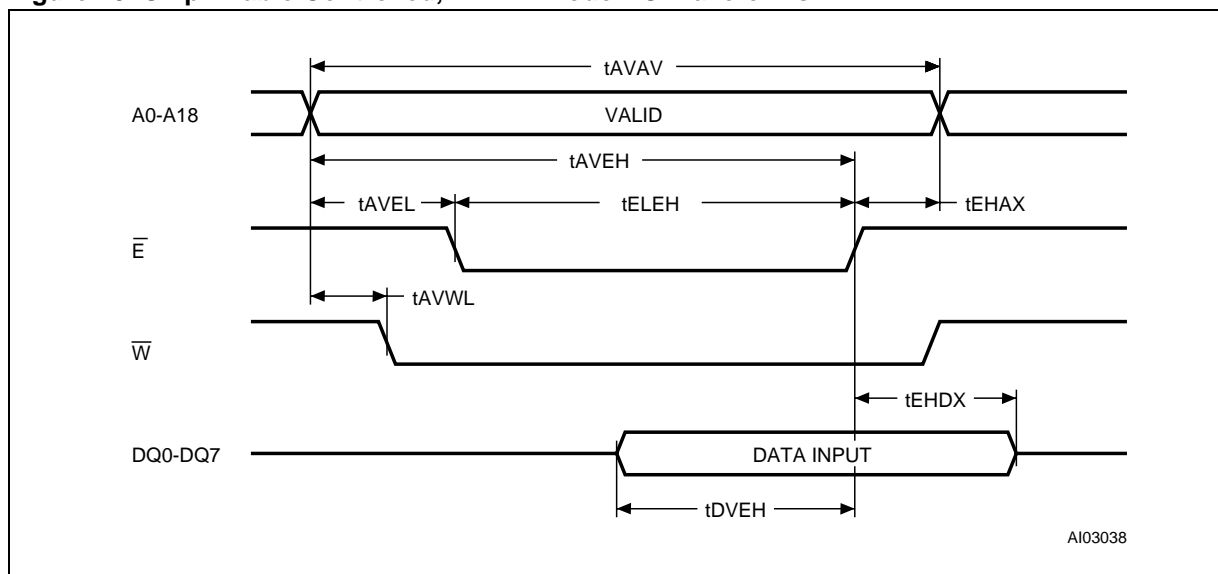


Note: Output Enable ($\overline{G}$) = High.
   If $\overline{E}$ goes High with $\overline{W}$ High, the output remains in a high-impedance state.

### Table 8. WRITE Mode AC Characteristics

| Symbol | Parameter[1] | M68Z512 −70 | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{AVAV}$ | WRITE Cycle Time | 70 | | ns |
| $t_{AVWL}$ | Address Valid to WRITE Enable Low | 0 | | ns |
| $t_{AVWH}$ | Address Valid to WRITE Enable High | 60 | | ns |
| $t_{AVEH}$ | Address Valid to Chip Enable High | 60 | | ns |
| $t_{WLWH}$ | WRITE Enable Pulse Width | 55 | | ns |
| $t_{WHAX}$ | WRITE Enable High to Address Transition | 0 | | ns |
| $t_{WHDX}$ | WRITE Enable High to Input Transition | 0 | | ns |
| $t_{WHQX}$[3] | WRITE Enable High to Output Transition | 5 | | ns |
| $t_{WLQZ}$[2,3] | WRITE Enable Low to Output Hi-Z | | 25 | ns |
| $t_{AVEL}$ | Address Valid to Chip Enable Low | 0 | | ns |
| $t_{ELEH}$ | Chip Enable Low to Chip Enable High | 45 | | ns |
| $t_{EHAX}$ | Chip Enable High to Address Transition | 0 | | ns |
| $t_{DVWH}$ | Input Valid to WRITE Enable High | 25 | | ns |
| $t_{DVEH}$ | Input Valid to Chip Enable High | 25 | | ns |

Note: 1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V (except where noted).
   2. $C_L$ = 5pF
   3. At any given temperature and voltage condition, $t_{WLQZ}$ is less than $t_{WHQX}$ for any given device.

**Figure 11. Low V$_{CC}$ Data Retention AC Waveforms**
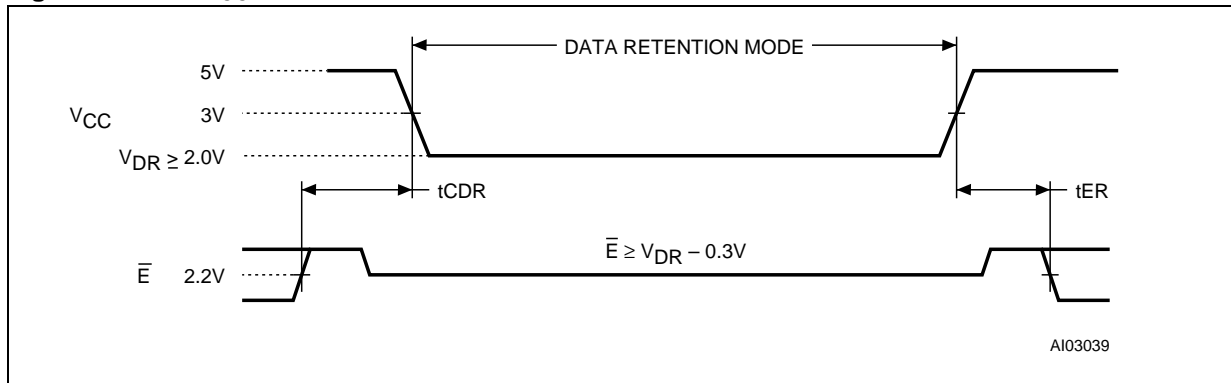


**Table 9. Low V$_{CC}$ Data Retention Characteristics**

| Symbol | Parameter[1] | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| I$_{CCDR}$[2] | Supply Current (Data Retention) | V$_{CC}$ = 3V, $\overline{E}$ ≥ V$_{CC}$ – 0.3V | | 0.4 | 10 | µA |
| V$_{DR}$ | Supply Voltage (Data Retention) | $\overline{E}$ ≥ V$_{CC}$ – 0.3V, f = 0 | 2 | | | V |
| t$_{CDR}$ | Chip Disable to Power Down | $\overline{E}$ ≥ V$_{CC}$ – 0.3V, f = 0 | 0 | | | ns |
| t$_{ER}$[3] | Operation Recovery Time | | t$_{AVAV}$ | | | ns |

Note: 1. Valid for Ambient Operating Temperature: T$_A$ = 0 to 70°C; V$_{CC}$ = 4.5 to 5.5V (except where noted).
2. Typical condition: T$_A$ = 25°C.
3. See Figure 11 for measurement points. Guaranteed but not tested. t$_{AVAV}$ is READ Cycle time.

## PART NUMBERING

### Table 10. Ordering Information Example

Example:                        M68Z    512    W    –70    NC    1    TR

**Device Type**

M68Z

**Device Function**

512 = 4 Mbit (512Kb x8)

**Operating Voltage**

blank = 4.5 to 5.5V

**Speed**

–70 = 70ns

**Package**

NC = TSOP II 32-Lead (10 x 20mm)

**Temperature Range**

1 = 0 to 70°C

**Shipping Method for SOIC**

blank = Tubes

TR = Tape & Reel


For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

## PACKAGE MECHANICAL INFORMATION

**Figure 12. TSOP II 32 – 32-lead Plastic Thin Small Outline II, 10 x 20 mm, Package Outline**



TSOP-d
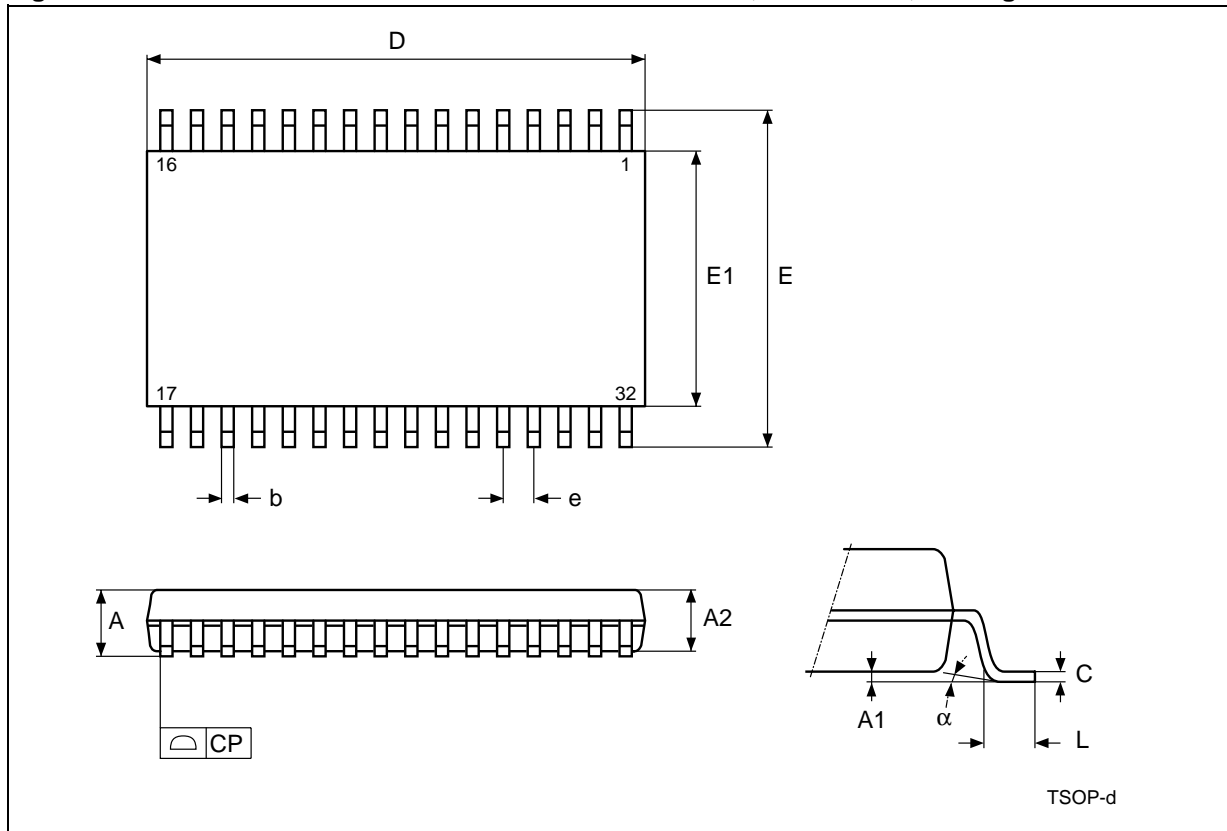
Note: Drawing is not to scale.

**Table 11. TSOP II 32 – 32-lead Plastic Thin Small Outline II, 10 x 20 mm, Package Mechanical Data**

| Symb | mm | | | inches | | |
|------|-----|-----|-----|-----|-----|-----|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.20 | | | 0.047 |
| A1 | | 0.05 | 0.15 | | 0.002 | 0.006 |
| A2 | | 0.95 | 1.05 | | 0.037 | 0.041 |
| b | | 0.30 | 0.52 | | 0.012 | 0.020 |
| C | | 0.12 | 0.21 | | 0.005 | 0.008 |
| CP | | | 0.10 | | | 0.004 |
| D | | 20.82 | 21.08 | | 0.820 | 0.830 |
| e | 1.27 | – | – | 0.050 | – | – |
| E | | 11.56 | 11.96 | | 0.455 | 0.471 |
| E1 | | 10.03 | 10.29 | | 0.395 | 0.405 |
| L | | 0.40 | 0.60 | | 0.016 | 0.024 |
| α | | 0° | 5° | | 0° | 5° |
| N | | 32 | | | 32 | |

**REVISION HISTORY**

**Table 12. Document Revision History**

| Date | Revision Details |
|------|------------------|
| May 1999 | First Issue |
| 03/14/00 | TSOP32 II Package Dimension Changed (Table 11)<br>From Preliminary Data to Data Sheet |
| 07/26/00 | Ordering Information Scheme changed (Table 10) |
| 09/21/00 | $I_{CCDR}$ Supply Current changed (Table 9) |
| 03/30/01 | Reformatted; temp./voltage info. added to tables (Table 4, 5, 7, 8, 9) |
| 05/13/02 | Add reflow time and temperature footnote (Table 2) |