CA3096, CA3096A, CA3096C

T-43-25

N-P-N/P-N-P Transistor Array

Five-Independent Transistors: Three n-p-n and Two p-n-p

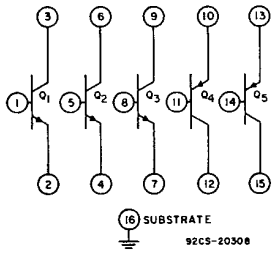
Applications:

- *Differential Amplifiers*
- *DC Amplifiers*
- *Sense Amplifiers*
- *Level Shifters*
- *Timers*
- *Lamp and Relay Drivers*
- *Thyristor Firing Circuits*
- *Temperature-Compensated Amplifiers*
- *Operational Amplifiers*

RCA-CA3096CE, CA3096E, and CA3096AE are general-purpose high-voltage silicon transistor arrays. Each array consists of five independent transistors (two p-n-p and three n-p-n types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096AE, CA3096E, and CA3096CE are identical, except that the CA3096AE specifications include parameter matching and greater stringency in I_{CBO}, I_{CEO}, and $V_{CE}(SAT)$. The CA3096CE is a relaxed version of the CA3096E.

The CA3096CE, CA3096E, and CA3096AE are supplied in 16-lead dual-in-line plastic packages. (E-suffix). The CA3096 is also available in chip form. (H suffix).



Schematic Diagram

CA3096AE, CA3096E, CA3096CE
ESSENTIAL DIFFERENCES

CHARACTERISTIC		CA3096AE	CA3096E	CA3096CE
$V_{(BR)CEO}$ (V) Min.	n-p-n	35	35	24
	p-n-p	−40	−40	−24
$V_{(BR)CBO}$ (V) Min.	n-p-n	45	45	30
	p-n-p	−40	−40	−24
h_{FE} @ 1 mA	n-p-n	150-500	150-500	100-670
	p-n-p	20-150	20-150	15-200
h_{FE} @ 100 μA	p-n p	40-200	40-200	30-300
I_{CBO} (nA) Max	n-p-n	40	100	100
	p-n-p	−40	−100	−100
I_{CEO} (nA) Max.	n-p-n	100	1000	1000
	p-n-p	−100	−1000	−1000
$V_{CE}(SAT)$ (V) Max.	p-n-p	0.5	0.7	0.7
$\lvert V_{IO}\rvert$ (mV) Max.	n-p-n	5	–	–
	p-n-p	5	–	–
$\lvert I_{IO}\rvert$ (μA) Max.	n-p-n	0.6	–	–
	p-n-p	0.25	–	–

File Number **595**

CA3096, CA3096A, CA3096C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	EACH N-P-N	EACH P-N-P	
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}:			
CA3096AE, CA3096E	35	−40	V
CA3096CE	24	−24	V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}:			
CA3096AE, CA3096E	45	−40	V
CA3096CE	30	−24	V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}:			
CA3096AE, CA3096E	45	–	V
CA3096CE	30	–	V
EMITTER-TO-SUBSTRATE VOLTAGE, V_{EIO}:			
CA3096AE, CA3096E	–	−40	V
CA3096CE	–	−24	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}:			
CA3096E, CA3096E	6	−40	V
CA3096CE	6	−24	V
COLLECTOR CURRENT, I_C (All Types)	50	−10	mA
POWER DISSIPATION, P_D:			
Up to $T_A = 55°C$:			
Device (Total)	750		mW
Each Transistor	200		mW
Above $T_A = 55°C$ derate linearly at	6.67		mW/°C
AMBIENT-TEMPERATURE RANGE, T_A:			
Operating	−55 to +125°C		
Storage	−65 to +150°C		
LEAD TEMPERATURE (DURING SOLDERING):			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	265°C		

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096AE			CA3096E			CA3096CE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each n-p-n Transistor											
I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	–	0.001	40	–	0.001	100	–	0.001	100	nA
I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	–	0.006	100	–	0.006	1000	–	0.006	1000	nA
$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	35	50	–	35	50	–	24	35	–	V
$V_{(BR)CBO}$	$I_C = 10\,\mu$A, $I_E = 0$	45	100	–	45	100	–	30	80	–	V
$V_{(BR)CIO}$	$I_{CI} = 10\,\mu$A, $I_B = I_E = 0$	45	100	–	45	100	–	30	80	–	V
$V_{(BR)EBO}$	$I_E = 10\,\mu$A, $I_C = 0$	6	8	–	6	8	–	6	8	–	V
V_Z	$I_Z = 10\,\mu$A	6	7.9	9.8	6	7.9	9.8	6	7.9	9.8	V
$V_{CE(SAT)}$	$I_C = 10$ mA, $I_B = 1$ mA	–	0.24	0.5	–	0.24	0.7	–	0.24	0.7	V
V_{BE}	$I_C = 1$ mA, $V_{CE} = 5$ V	0.6	0.69	0.78	0.6	0.69	0.78	0.6	0.69	0.78	V
h_{FE}		150	390	500	150	390	500	100	390	670	
$\lvert\Delta V_{BE}/\Delta T\rvert$	$I_C = 1$ mA, $V_{CE} = 5$ V	–	1.9	–	–	1.9	–	–	1.9	–	mV/°C

CA3096, CA3096A, CA3096C

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STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (Cont'd)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096AE			CA3096E			CA3096CE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each p-n-p Transistor											
I_{CBO}	V_{CB} = −10 V, I_E = 0	–	−0.006	−40	–	−0.06	−100	–	−0.06	−100	nA
I_{CEO}	V_{CE} = −10V, I_B = 0	–	−0.12	−100	–	−0.12	−1000	–	−0.12	−1000	nA
$V_{(BR)CEO}$	I_C = −100 μA, I_B = 0	−40	−75	–	−40	−75	–	−24	−30	–	V
$V_{(BR)CBO}$	I_C = −10 μA, I_E = 0	−40	−80	–	−40	−80	–	−24	−60	–	V
$V_{(BR)EBO}$	I_E = −10 μA, I_C = 0	−40	−100	–	−40	−100	–	−24	−80	–	V
$V_{(BR)EIO}$	I_{EI} = 10 μA, I_B = I_C = 0	−40	−100	–	−40	−100	–	−24	−80	–	V
$V_{CE(SAT)}$	I_C = −1 mA, I_B = −100 μA	–	−0.16	−0.4	–	−0.16	−0.4	–	−0.16	−0.4	V
V_{BE}	I_C = −100 μA, V_{CE} = −5 V	−0.5	−0.6	−0.7	−0.5	−0.6	−0.7	−0.5	−0.6	−0.7	V
h_{FE}	I_C = −100 μA, V_{CE} = −5 V	40	85	250	40	85	250	30	85	300	
	I_C = −1 mA, V_{CE} = −5 V	20	47	200	20	47	200	15	47	200	
$\lvert\Delta V_{BE}/\Delta T\rvert$	I_C = −100 μA, V_{CE} = −5 V	–	2.2	–	–	2.2	–	–	2.2	–	mV/°C

I_{CBO} Collector-Cutoff Current

I_{CEO} Collector-Cutoff Current

$V_{(BR)CEO}$ Collector-to-Emitter Breakdown Voltage

$V_{(BR)CBO}$ Collector-to-Base Breakdown Voltage

$V_{(BR)CIO}$ Collector-to-Substrate Breakdown Voltage

$V_{(BR)EBO}$ Emitter-to-Base Breakdown Voltage

V_Z Emitter-to-Base Zener Voltage

$V_{CE(SAT)}$ Collector-to-Emitter Saturation Voltage

V_{BE} Base-to-Emitter Voltage

h_{FE} DC Forward-Current Transfer Ratio

$\lvert\Delta V_{BE}/\Delta T\rvert$ Magnitude of Temperature Coefficient: (for each transistor)

CA3096, CA3096A, CA3096C

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (CA3096AE Only)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA3096AE Min.	Typ.	Max.	UNITS
For Transistors Q1 and Q2 (as a Differential Amplifier)					
Absolute Input Offset Voltage, $\lvert V_{IO}\rvert$	V_{CE} = 5 V, I_C = 1 mA	–	0.3	5	mV
Absolute Input Offset Current, $\lvert I_{IO}\rvert$		–	0.07	0.6	μA
Absolute Input Offset Voltage Temperature Coefficient, $\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		–	1.1	–	μV/°C
For Transistors Q4 and Q5 (As a Differential Amplifier)					
Absolute Input Offset Voltage, $\lvert V_{IO}\rvert$	V_{CE} = −5 V, I_C = −100 μA, R_S = 0	–	0.15	5	mV
Absolute Input Offset Current, $\lvert I_{IO}\rvert$		–	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient, $\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		–	0.54	–	μV/°C

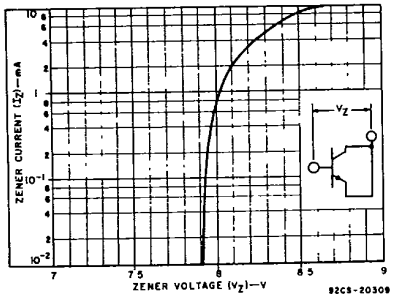


Fig. 1 – Base-to-emitter zener characteristic (n-p-n).

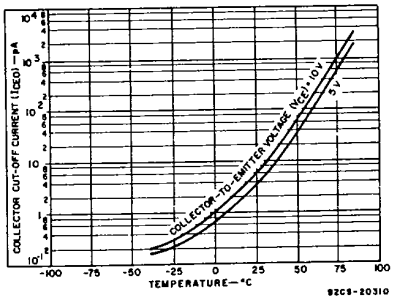


Fig. 2 – Collector cut-off current (I_{CEO}) as a function of temperature (n-p-n).

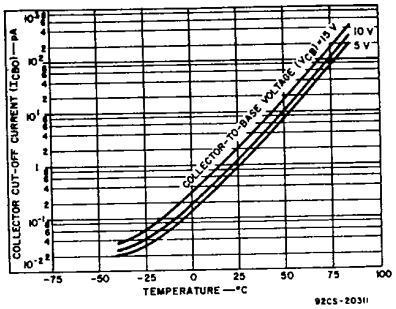


Fig. 3 – Collector cut-off current (I_{CBO}) as a function of temperature (n-p-n).

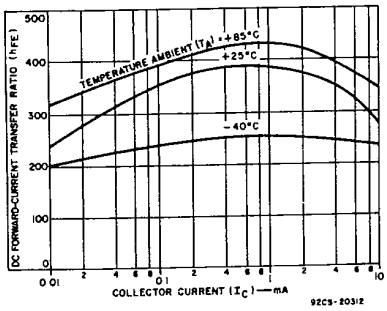


Fig. 4 – Transistor (n-p-n) h_{FE} as a function of collector current.

CA3096, CA3096A, CA3096C

T-43-25

DYNAMIC

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Typical Values Intended Only for Design Guidance

CHARACTERISTICS	TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each n-p-n Transistor			
Noise Figure (low frequency), NF	f = 1 kHz, V_{CE} = 5 V, I_C = 1 mA, R_S = 1 kΩ	2.2	dB
Low-Frequency, Input Resistance, R_i	f = 1.0 kHz, V_{CE} = 5 V, I_C = 1 mA	10	kΩ
Low-Frequency Output Resistance, R_o		80	kΩ
Admittance Characteristics:	f = 1 MHz, V_{CE} = 5 V, I_C = 1 mA		
Forward Transfer Admittance, $\frac{g_{fe}}{Y_{fe}\ b_{fe}}$		7.5 −j13	mmho
Input Admittance, $\frac{g_{ie}}{Y_{ie}\ b_{ie}}$		2.2 j3.1	mmho
Output Admittance, $\frac{g_{oe}}{Y_{oe}\ b_{oe}}$		0.76 j2.4	mmho
Gain-Bandwidth Product, f_T	V_{CE} = 5 V, I_C = 1.0 mA	280	MHz
	V_{CE} = 5 V, I_C = 5 mA	335	
Emitter-to-Base Capacitance, C_{EB}	V_{EB} = 3 V	0.75	pF
Collector-to-Base Capacitance, C_{CB}	V_{CB} = 3 V	0.46	pF
Collector-to-Substrate Capacitance, C_{CI}	V_{CI} = 3 V	3.2	pF
For Each p-n-p Transistor			
Noise Figure (low frequency), NF	f = 1 kHz, I_C = 100 μA, R_S = 1 kΩ	3	dB
Low-Frequency Input Resistance, R_i	f = 1 kHz, V_{CE} = 5 V, I_C = 100 μA	27	kΩ
Low-Frequency Output Resistance, R_o		680	kΩ
Gain-Bandwidth Product, f_T	V_{CE} = 5 V, I_C = 100 μA	6.8	MHz
Emitter-to-Base Capacitance, C_{EB}	V_{EB} = −3 V	0.85	pF
Collector-to-Base Capacitance, C_{CB}	V_{CB} = −3 V	2.25	pF
Base-to-Substrate Capacitance, C_{BI}	V_{BI} = 3 V	3.05	pF

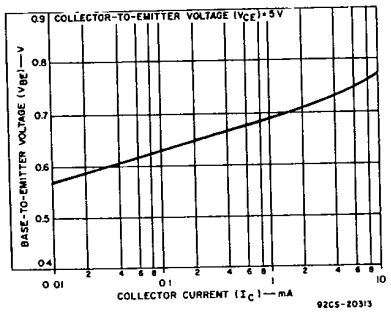


Fig. 5 – V_{BE} (n-p-n) as a function of collector current.

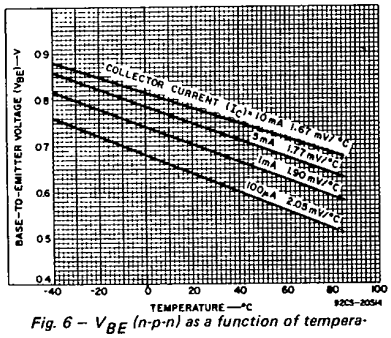


Fig. 6 – V_{BE} (n-p-n) as a function of temperature.

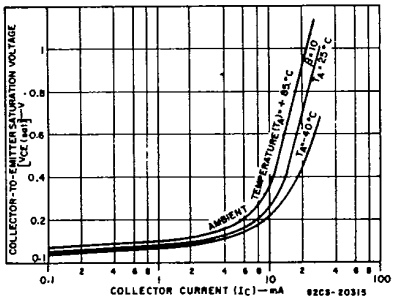


Fig. 7 – $V_{CE}(SAT)$ (n-p-n) as a function of collector current.

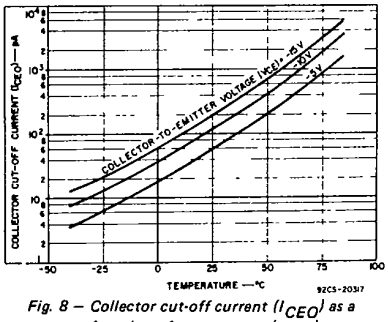


Fig. 8 – Collector cut-off current (I_{CEO}) as a function of temperature (p-n-p).

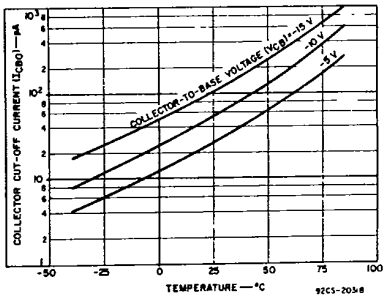


Fig. 9 – Collector cut-off current (I_{CBO}) as a function of temperature (p-n-p).

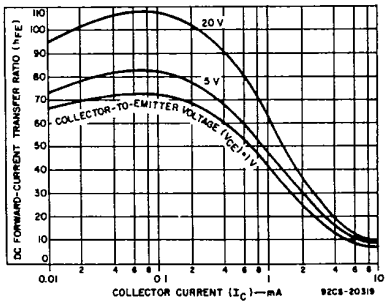


Fig. 10 – Transistor (p-n-p) h_{FE} as a function of collector current.

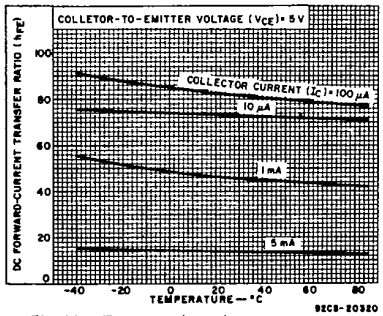


Fig. 11 – Transistor (p-n-p) h_{FE} as a function of temperature.

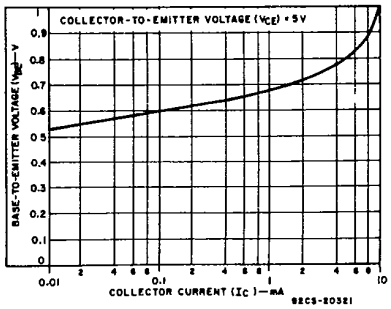


Fig. 12 – V_{BE} (p-n-p) as a function of collector current.

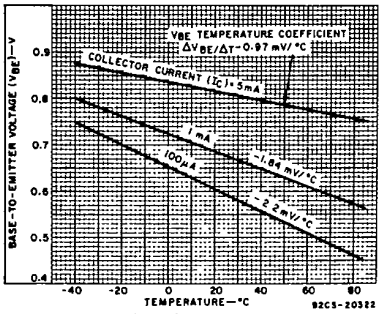


Fig. 13 – V_{BE} (p-n-p) as a function of temperature.

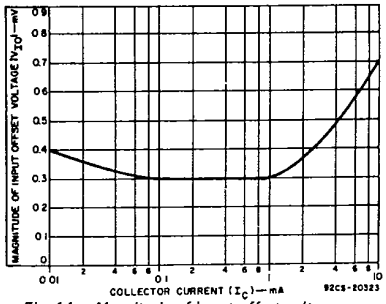


Fig. 14 – Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for n-p-n transistor Q_1–Q_2

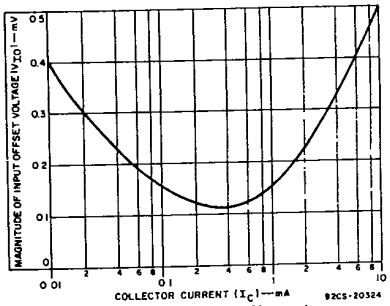


Fig. 15 – Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for p-n-p transistor Q_4–Q_5

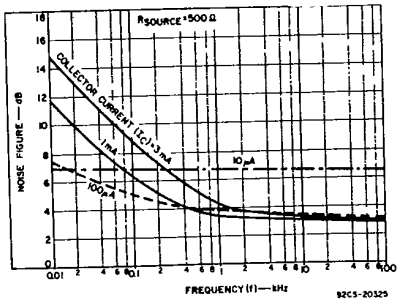


Fig. 16 – Noise figure as a function of frequency for n-p-n transistors.

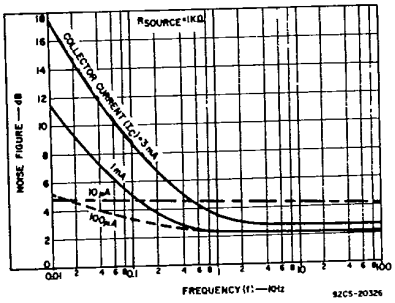


Fig. 17 – Noise figure as a function of frequency for n-p-n transistors.

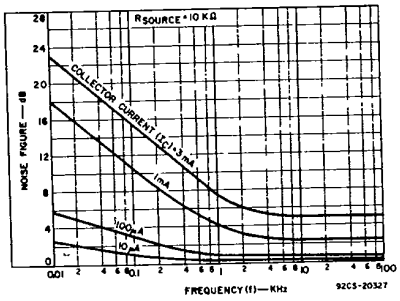


Fig. 18 – Noise as a function of frequency for n-p-n transistors.

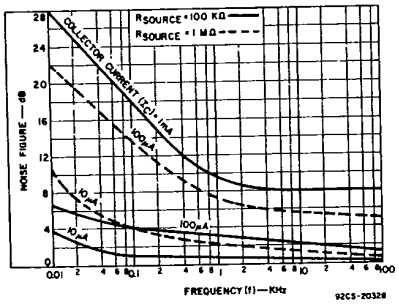


Fig. 19 – Noise figure as a function of frequency for n-p-n transistors.

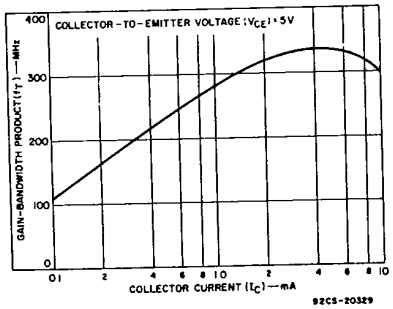


Fig. 20 – Gain-bandwidth product as a function of collector current (n-p-n).

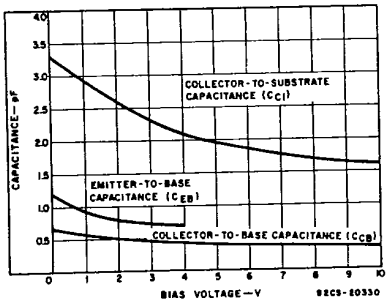


Fig. 21 – Capacitance as a function of bias voltage (n-p-n).

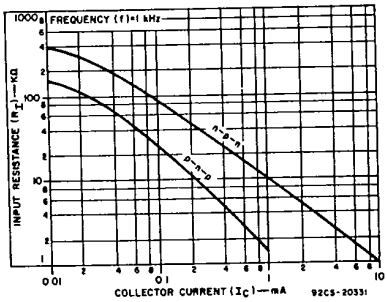


Fig. 22 – Input resistance as a function of collector current.

CA3096, CA3096A, CA3096C

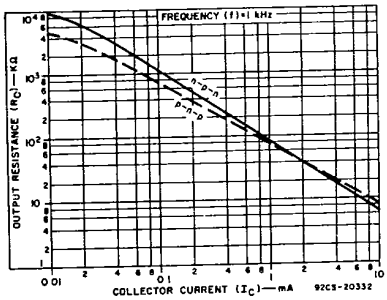


Fig. 23 – Output resistance as a function of collector current.

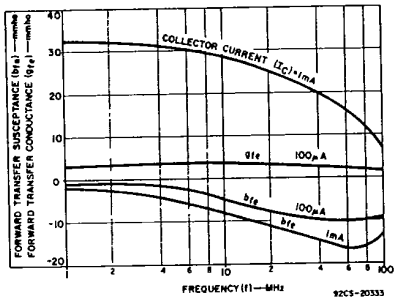


Fig. 24 – Forward transconductance as a function of frequency.

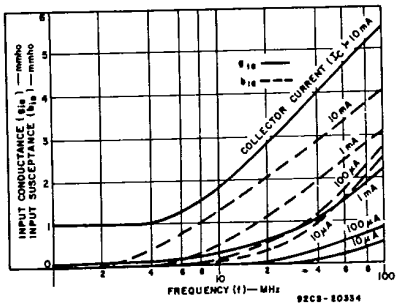


Fig. 25 – Input admittance as a function of frequency.

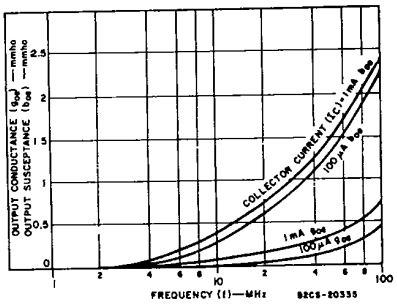


Fig. 26 – Output admittance as a function of frequency.

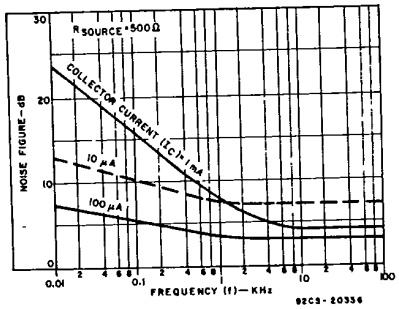


Fig. 27 – Noise figure as a function of frequency (p-n-p).

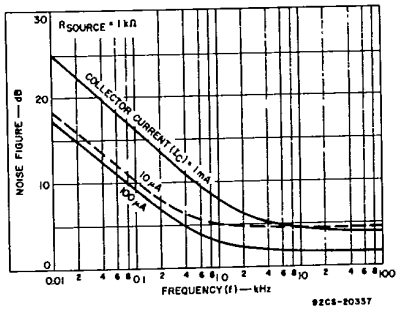


Fig. 28 – Noise figure as a function of frequency (p-n-p).

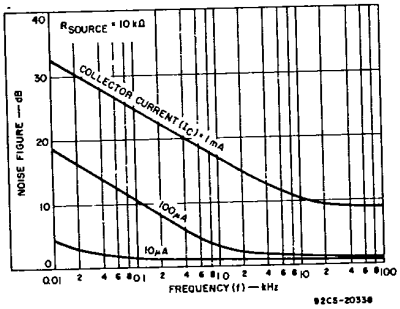


Fig. 29 – Noise figure as a function of frequency (p-n-p).

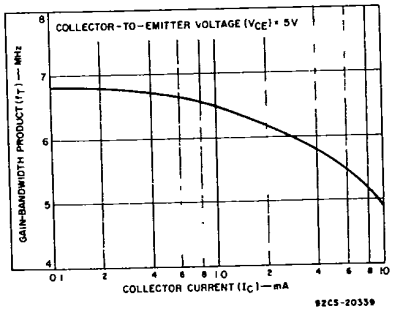


Fig. 30 – Gain-bandwidth product as a function of collector current (p-n-p).

CA3096, CA3096A, CA3096C

T-43-25

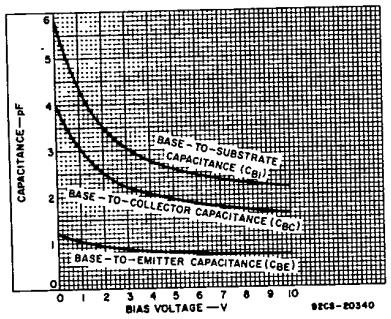


Fig. 31 – Capacitance as a function of bias voltage (p-n-p).

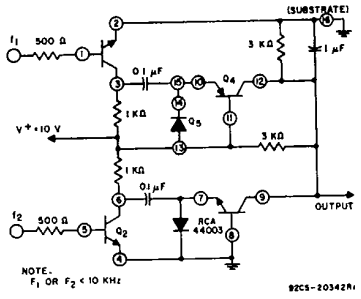


Fig. 32 – Frequency comparator using CA3096E.

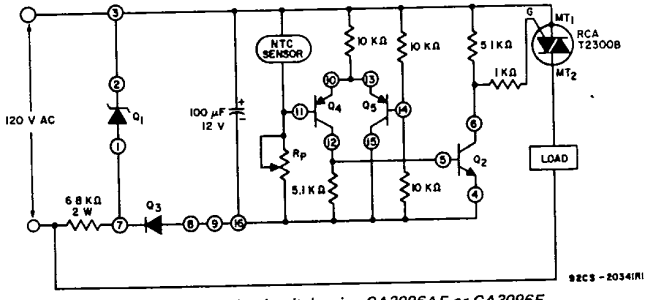


Fig. 33 – Line-operated level switch using CA3096AE or CA3096E.

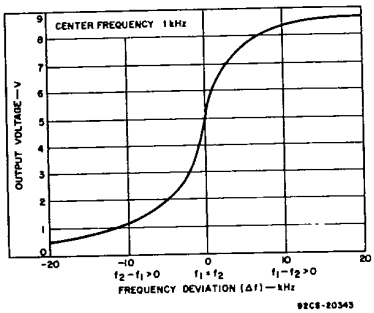


Fig. 34 – Frequency comparator characteristics.

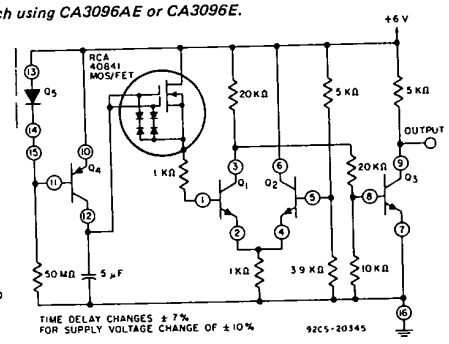


Fig. 35 – One-minute timer using CA3096AE and a MOS/FET.

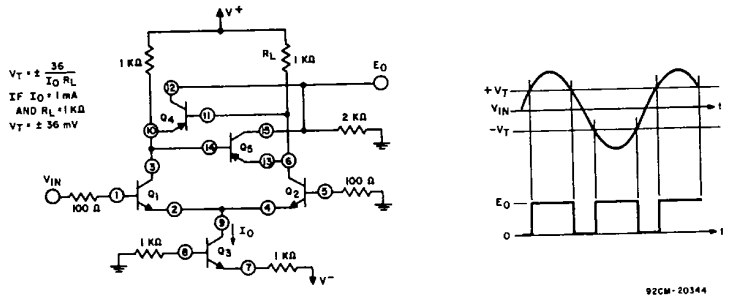


Fig. 36 – CA3096AE small-signal zero-voltage detector having noise immunity.

CA3096, CA3096A, CA3096C

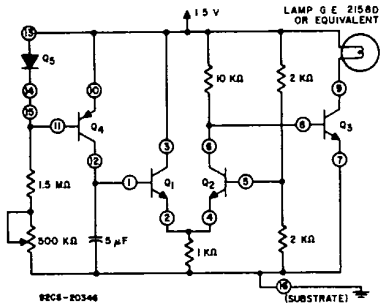


Fig. 37 – Ten-second timer operated form 1.5-volt supply using CA3096E.

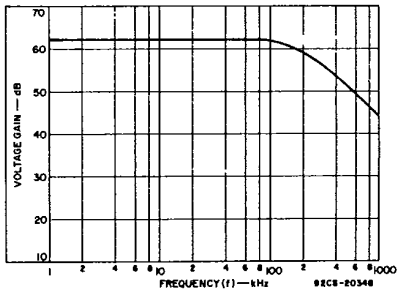


Fig. 38 – Gain-frequency characteristics.

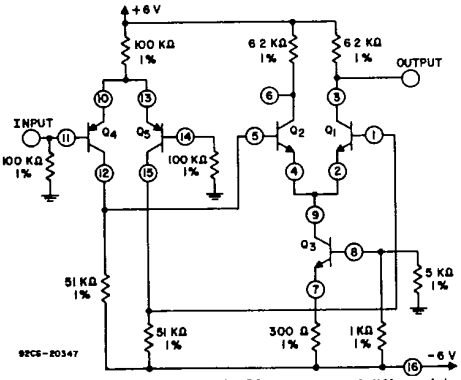
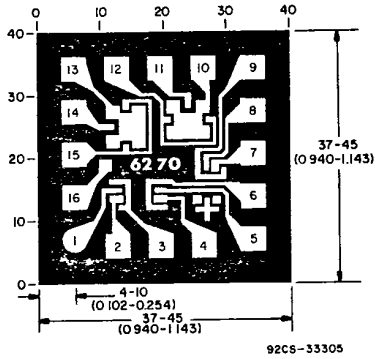


Fig. 39 – Cascade of differential amplifiers using CA3096AE.

Features:

1. Can be operated with either dual supply or single supply.
2. Wide-input common-mode range +5 V to −5 V.
3. Low bias current: $<1\ \mu A$.



CA3096H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.