SPV1020

Interleaved DC-DC boost converter with built-in MPPT algorithm

Datasheet – production data

Features

- PWM mode DC-DC boost converter
- Duty cycle controlled by MPPT algorithm with 0.2% accuracy
- Operating voltage range 6.5 - 40 V
- Overvoltage, overcurrent, overtemperature protection
- Interleaved 4-phase topology
- Built-in soft-start
- Up to 98% efficiency
- Power capability 320 W at 40 V output
- Automatic transition to burst mode for improved efficiency at low solar radiation
- SPI interface

Applications

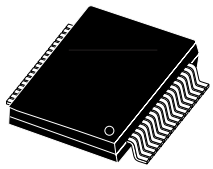
- Photovoltaic panels
- Battery charging with a CVCC controller

Description

The SPV1020 is a monolithic 4-phase interleaved DC-DC boost converter designed to maximize the power generated by photovoltaic panels independent of temperature and amount of solar radiation.

Optimization of the power conversion is obtained with embedded logic which performs the MPPT (max. power point tracking) algorithm on the PV cells connected to the converter.

One or more converters can be housed in the connection box of the PV panels, replacing the bypass diodes. As the maximum power point is locally computed, the efficiency at system level is higher than that of conventional topologies, where the MPP is computed in the main centralized inverter.



PowerSSO-36

For a cost effective application solution and to minimize size, the SPV1020 embeds power MOSFETs for active switches and synchronous rectifiers, minimizing the number of external devices. In addition, the 4-phase interleaved topology of the DC-DC converter obviates the need to use electrolytic capacitors, which may severely limit system lifetime.

The SPV1020 operates at fixed frequency in PWM mode, where the duty cycle is controlled by the embedded logic running a Perturb&Observe MPPT algorithm. The switching frequency, internally generated and set by default at 100 kHz, is externally adjustable from 50 kHz to 200 kHz, while the duty cycle can range from 5% to 90% with a step of 0.2%.

The safety of the application is guaranteed by stopping the drivers in the case of output overvoltage or overtemperature.

Multiple SPV1020s can be used in a panel array with one SPV1020 per panel. Panels can be connected in series, in parallel, or series/parallel combinations.

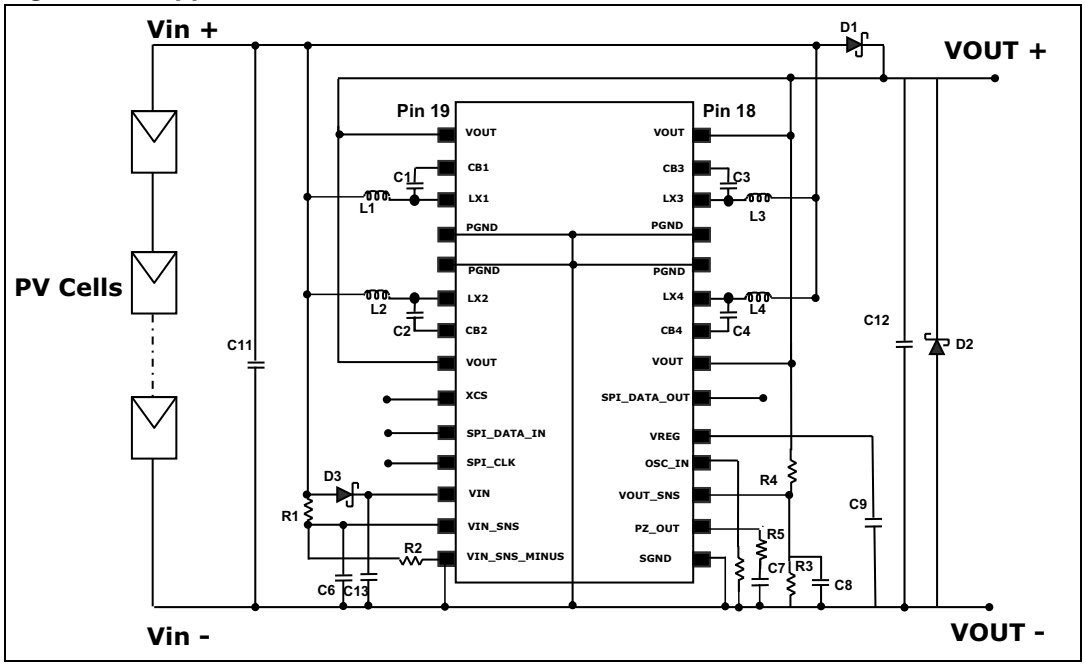
Table 1. Device summary

Order codes	Package	Packaging
SPV1020	PowerSSO-36	Tube

Contents

1 Application circuit

Figure 1. Application circuit



2 Pin connection

Figure 2. Pin connection (top view)

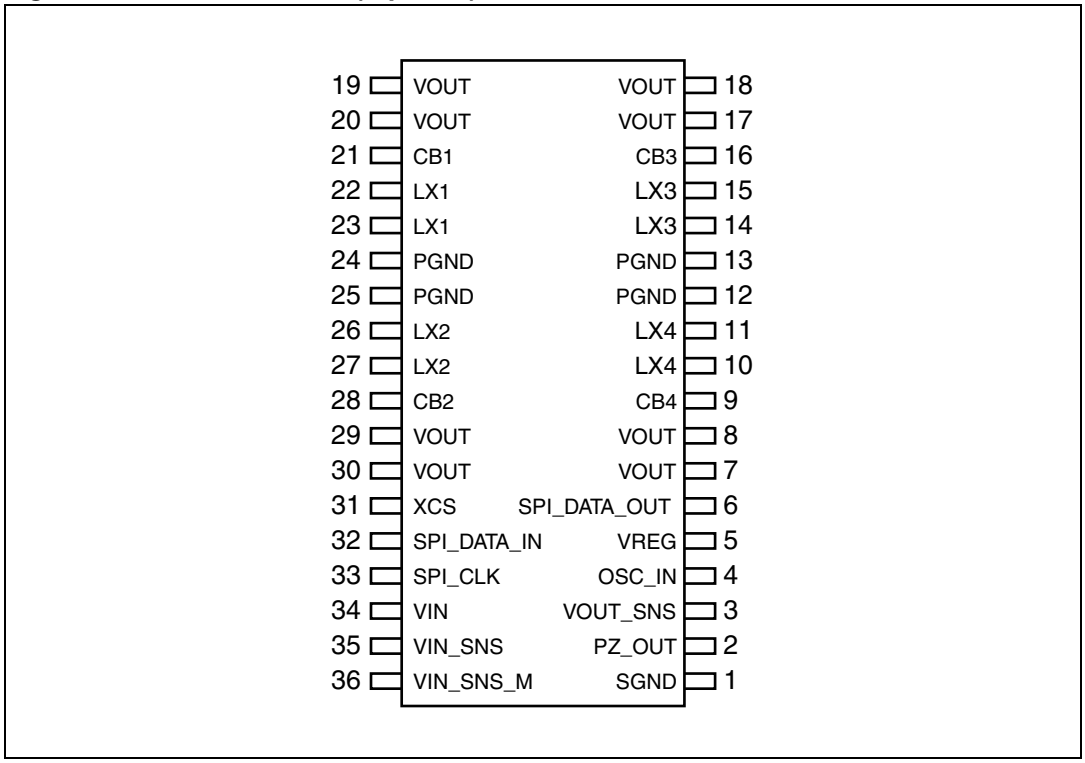


Table 2. Pin description

Pin	Name	Type	Description
PowerSSO-36			
34	VIN	Supply	DC input power supply unit.
7,8,17,18,19,20,29,30	VOUT	Supply	Booster output voltage
12,13,24,25	PGND	Ground	Power ground
1	SGND	Ground	Signal ground reference. The exposed pad is connected to PGND.
22,23,26,27,15,14,11,10	LX1…4	I	Booster inductor connection.
9,16,21,28	CB1…4	I/O	External bootstrap capacitors must be connected between these pins and LXi
5	VREG	I/O	Power supply for internal low voltage circuitry; an external capacitor must be connected to this pin referenced to SGND
35	VIN_SNS	I	Sense pin of input voltage. To be biased with a resistor divider between VIN and SGND
3	VOUT_SNS	I	Sense pin of output voltage. To be biased with a resistor divider between VOUT and SGND
31	XCS	I	Activates the SPI
36	VIN_SNS_M	I	Dedicated ground for VIN_SNS
2	PZ_OUT	I/O	Compensates the output voltage feedback loop. A series resistor and capacitor are connected between PZ_OUT and SGND.
6	SPI_DATA_OUT	O	Data OUT for SPI interface
33	SPI_CLK	I	Clock for SPI interface.
32	SPI_DATA_IN	I	Data IN for SPI interface.
4	OSC_IN	I	Pin for adjusting the switching frequency; to set the default value of 100 kHz, connect OSC_IN to VREG. Otherwise connect OSC_IN through a resistor to SGND.

3 Maximum ratings

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Range [min., max.]	Unit
VIN	Power supply	[-0.3, 40]	V
VOUT	Power supply	[-0.3, 40]	V
PGND	Power ground	0	V
SGND	Signal ground	[-0.3, 0.3]	V
VOUT_SNS	Analog input	[-0.3, VOUT + 0.3]	V
LX1….4	Analog input	[-0.3, VOUT + 0.3]	V
CB1…4	Analog input/output	[Lxi – 0.3, Lxi + 5]	V
VREG	Analog input/output	[-0.3, 6]	V
VIN_SNS	Analog input	[-0.3, 3.3 + 0.3]	V
XCS	Analog input	[-0.3, 3.3 + 0.3]	V
OSC_IN	Analog input	[-0.3, 3.3 + 0.3]	V
PZ_OUT	Analog input/output	[-0.3, VIN + 0.3]	V
SPI_DATA_OUT	Analog output	[-0.3, 3.3 + 0.3]	V
SPI_CLK	Digital input	[-0.3, 3.3 + 0.3]	V
SPI_DATA_IN	Digital input	[-0.3, 3.3 + 0.3]	V
VIN_SNS_M	Dedicated ground	[-0.3, 0.3]	V

Table 4. Thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_{thJA} (1)	Thermal resistance, junction to ambient		-	24	°C/W
Tj_{op}	Junction temperature operating range	-40	-	125	°C
Tstg	Storage temperature	-50	-	125	

1. R_{thja} was measured with a 4-layer pcb, FR4 70 um CU thickness exposed pad soldered area = 30 mm2

4 Electrical characteristics

V_{IN} = 36 V, T_A = 25 °C and T_J<125 °C, unless otherwise specified.

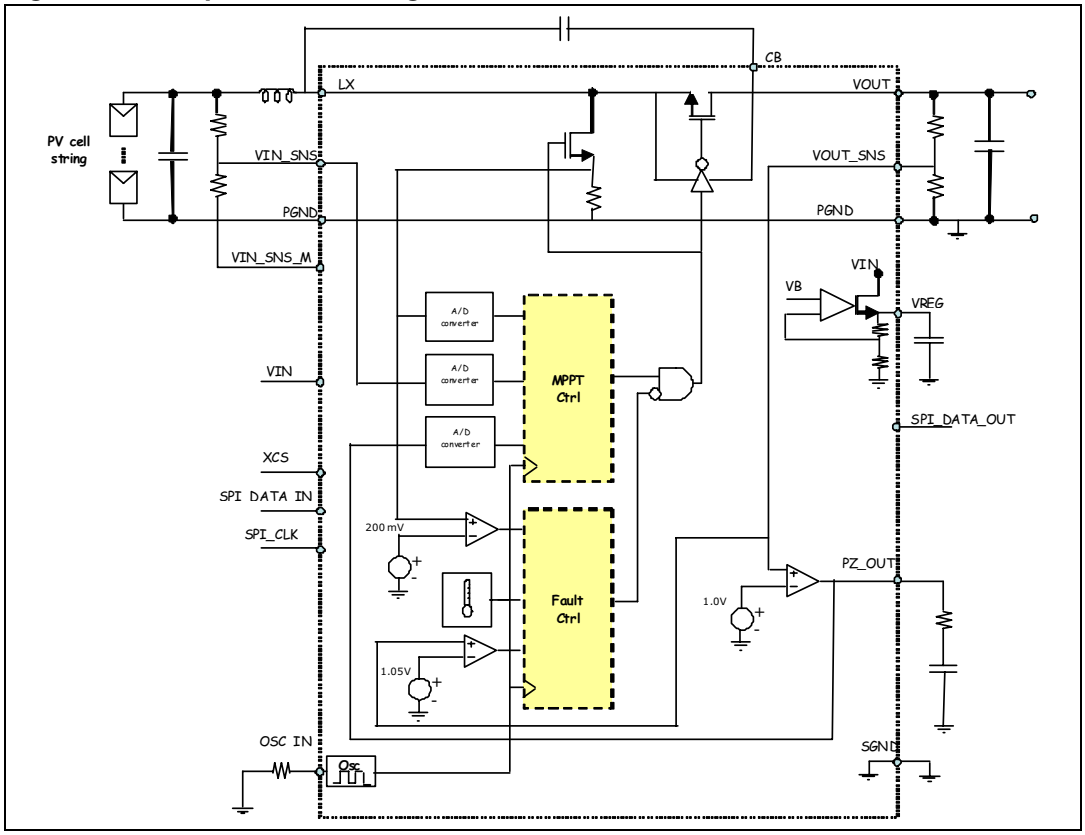
Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Input source section						
V_{IN}	Operating input voltage		6.5		40	V
I_q	Quiescent current	ILOAD=0 mA, VOUT=36 V, Tj=Tamb, PWM=5%		5		mA
I_{SD}	Shutdown mode current consumption	ILOAD=0 mA, VOUT=VIN=36 V, Tj=Tamb		1		mA
V_{UVLO}	Undervoltage lockout threshold for turn-on	VIN increasing		6.5		V
	Undervoltage lockout hysteresis			-0.5		V
Power section						
$R_{DSON-LS}$	Power switch ON-resistance			70		mΩ
$R_{DSON-HS}$	Synchronous rectifier ON-resistance			70		mΩ
Control section						
V_{OUT}	Operating output voltage		Vin		40	V
I_{OUT}	Operating output current				9	A
I_{lim}	LX switch current limit		4	4.5	5	A
F_{PWM}	PWM frequency (default value)		70	100	150	kHz
V_{REF}	Constant voltage control loop internal reference voltage		1.18	1.23	1.27	V
Thermal shutdown						
$T_{shutdown}$	Overtemperature threshold for turn-off	Temperature increasing	140	150	160	°C
	Overtemperature hysteresis			-20		°C

5 Detailed description

The SPV1020 is a fully integrated high efficiency DC-DC boost converter with 4-phase interleaved topology operating in the voltage range from 6.5 VDC to 40 VDC. A simplified block diagram showing only one of the four phases is shown in *Figure 3* below.

Figure 3. Simplified block diagram



5.1 Initialization and startup mode

In order to guarantee a correct power-up sequence, the converter initially operates in burst mode. When the input voltage is greater than 6.5 V, the converter sequentially activates each of the four phases.

Initially, only phase 1 starts to work in burst mode, charging the inductor only for one cycle over 15 cycles. Then the duty cycle is progressively increased until phase 1 is switched on at every cycle and at the default switching frequency of 100 kHz.

After phase 1 has reached its steady-state condition, all the other phases are progressively switched on in the following sequence: phase 3, phase 2 and, lastly, phase 4.

All the sequences are running when the power generated by the PV cells is increasing. Otherwise the sequence may go back and then forward again.

5.2 Oscillator

The switching frequency Fswitch is internally fixed at 100 kHz and each phase operates at the frequency fixed by the oscillator. To set the default value of 100 kHz, connect OSC_IN to VREG. The switching frequency can be adjusted from 50 kHz to 200 kHz by connecting an external resistor R6 between OSC and SGND. The relationship between R6 and Fswitch is:

$$R6[k\Omega] = \frac{(100) \times (120)}{Fswitch \quad [kHz]}$$

5.3 Input voltage sensing

The device monitors the input voltage generated by the PV cells through VIN_SNS. This value is used to calculate the power generated by the PV cell string and then to adjust the PWM duty cycle to provide the maximum power point.

The input voltage must be scaled to a reference voltage level of 1.25 V at the input of the ADC integrated in the SPV1020.

Referring to the schematic shown in the application circuit of *Figure 1*, R1 and R2 are the resistors used for partitioning the input voltage.

If Vin_max is the maximum input voltage of the supply source (e.g. the PV panel or the PV string), R1 and R2 must be selected according to the following formula:

Equation 1

$$\frac{R1}{R2} = \frac{V_{inmax}}{1.25} - 1$$

Also, in order to optimize the efficiency of the whole system, when selecting R1 and R2, their power dissipation must be taken into account.

Assuming negligible the current flowing through pin VIN_SNS, maximum power dissipation in the series R1+R2 is:

Equation 2

$$P_{vin\_sns} = \frac{(V_{in\_max})^2}{R1 + R2}$$

As an empirical rule, R1 and R2 should be selected according to:

Equation 3

$$P_{vin\_sns} \ll 0.1x(V_{in\_max} \cdot I_{in\_max})$$

Note: In order to guarantee the proper functionality of pin VIN_SNS, current flowing in the series R1+R2 should be in the range between 20 µA and 200 µA.

5.4 Output voltage sensing and overvoltage protection (OVP)

Another monitoring is carried out on VOUT with the VOUT_SNS pin. This pin is used to monitor the output voltage in order to regulate it's maximum value (which cannot exceed 40 V), preventing damage due to overvoltage.

VOUT_SNS (the partitioned VOUT) is checked against a threshold of 1.0 V, generated by an internal regulated voltage. When VOUT_SNS reaches 1 V, the output feedback loop begins to regulate and limits the output voltage.

The stability of the loop can be externally regulated by connecting a resistor and a capacitor (pole-zero compensation) between the PZ_OUT and SGND.

If VOUT_SNS exceeds 1.04 V a fault signal is generated and transmitted to the fault controller. This stops the drivers and produces a fault signal to an external chip (DIAG = 0).

When VOUT_SNS decreases down to 1.04 V, the boost converter begins to regulate again and the MPPT restarts from the minimum duty cycle of 5%.

Referring to the schematic shown in *Figure 1*, R3 and R4 are the two resistors used to partition the output voltage.

If VOUT_MAX is the maximum output voltage at the load, R3 and R4 must be selected according to the following rule:

Equation 4

$$\frac{R3}{R4} = \frac{V_{outmax}}{1.02} - 1$$

Also, in order to optimize the efficiency of the whole system, when selecting R3 and R4, their power dissipation must be taken into account.

Assuming negligible the current flowing through pin VOUT_SNS, maximum power dissipation in the series R3+R4 is:

Equation 5

$$P_{vout\_sns} = \frac{(V_{out\_max})^2}{R1 + R2}$$

As an empirical rule, R3 and R4 should be selected according to:

Equation 6

$$P_{vout\_sns} \ll 0.1x(V_{out\_max} \cdot I_{out\_max})$$

Note: In order to guarantee the proper functionality of pin V_{out_sns}, current flowing in the series R3+R4 should be in the range between 20 µA and 100 µA.

5.5 Overcurrent protection (OCP)

To guarantee safe operation the low-side power switches have overcurrent protection. If LX is accidentally shorted to VIN or VOUT or when the current flowing through the inductor exceeds the current limit (~4.5 A), the related low-side power switch is immediately turned off and the linked synchronous rectifier is turned on. The low-side power switch is turned on again at the next PWM cycle.

5.6 Overtemperature protection (OTP)

When the temperature sensed at silicon level reaches 150 °C, all low-side power switches are immediately turned off. The device becomes operative again as soon as the silicon temperature drops to 130 °C.

5.7 Shutdown

In shutdown mode, the SHUT command sent to the converter switches the converter off to minimize power consumption. The synchronous rectifier intrinsic body diode causes a parasitic path between the power supply input and output, that cannot be avoided in shutdown.

5.8 Undervoltage lockout (UVLO)

When solar radiation is too low or the PV cells are shaded, the energy generated may be too small to drive the converter. In this case, when the input voltage is lower than the UVLO threshold, all circuitry is in the OFF state, avoiding undesired power consumption. Hysteresis has been implemented to limit undesired switching of the internal reset circuits.

5.9 MPPT

In order to maximize the energy transferred from the PV cell string to the DC bus (connected to the output of the converter) the converter embeds a logic running a *Perturb&Observe MPPT* algorithm based on monitoring the voltage and current supplied by the PV cells. If the operating voltage of the PV array is perturbed in a given direction and the power drawn from the PV array increases, this means that the operating point has moved towards the MPP and, therefore, the operating voltage must be further perturbed in the same direction. Otherwise, if the power drawn from the PV array decreases, the operating point has moved away from the MPP and, therefore, the direction of the operating voltage perturbation must be reversed

5.10 SPI

The SPV1020 embeds a 4-pin compatible SPI interface. The SPI allows full duplex, synchronous, serial communication between a host controller (the master) and the SPV1020 peripheral device (the slave). The SPI master provides the synchronizing clock and starts the communication. The idle state of the serial clock for the SPV1020 is high. Data pins are driven on the falling edges of the serial clock and they are sampled on its rising edges. These features correspond to a clock polarity set to 1 (typical host SPI control

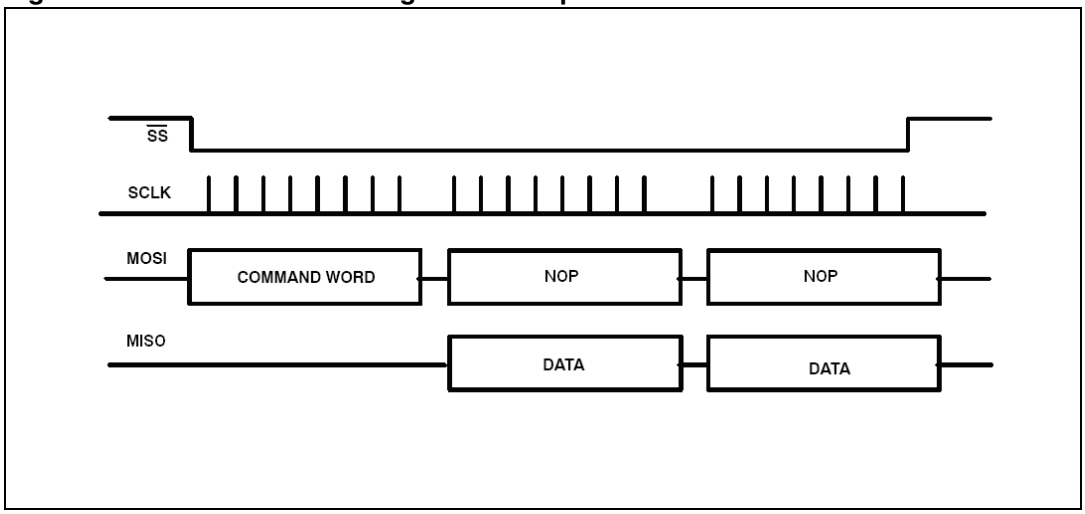
bit CPOL=1) and to a clock phase set to 1 (typical host SPI control bit CPHA=1), respectively. The bit order of each byte is MSB first.

When the master initiates a transmission, a data byte is shifted out through the MOSI pin to the slave, while another data byte is shifted out through the MISO pin to the master. The master controls the serial clock on the SCLK pin. The SS (active low) pin must be driven low by the master during each transmission. The bit order of each byte is MSB first.

The SPV1020 register file is accessible by the host through the SPI bus. Therefore the host can read the SPV1020 control parameter register data. Each data frame includes at least one command byte followed by data bytes whose direction depends on the type of command. If the command byte requires data to be read from the register file, those data are transmitted from the slave to the master through the MISO pin. Therefore the master appends a number of NOPs (0x00) to the command so that the entire data can be transmitted, see *Figure 4*. The master must transmit a byte to receive a byte.

If the SS wire goes high before the completion of a command byte in the data frame, the SPV1020 rejects that byte and the frame is closed. Then the next data frame is considered as a new one, starting with a command byte.

Figure 4. Frame structure: register read operation



The host can insert a short pause between each frame byte, or it can work in burst mode (no pause between frame bytes).

Some data words can be longer than 8 bits, such as ADC results (10 bits). In such cases, data is first extended to the nearest multiple of one byte (right justified). Then it is split into bytes, e.g. the ADC result R is formatted as follows:

Table 6. Data format for words longer than 8 bits

	Bit 7MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
Byte 1	0	0	0	0	0	0	R9 MSB	R8
Byte 2	R7	R6	R5	R4	R3	R2	R1	R0 LSB

Table 7 shows a list of commands. Each command addresses a memory location of a certain width and sets the direction of the related data.

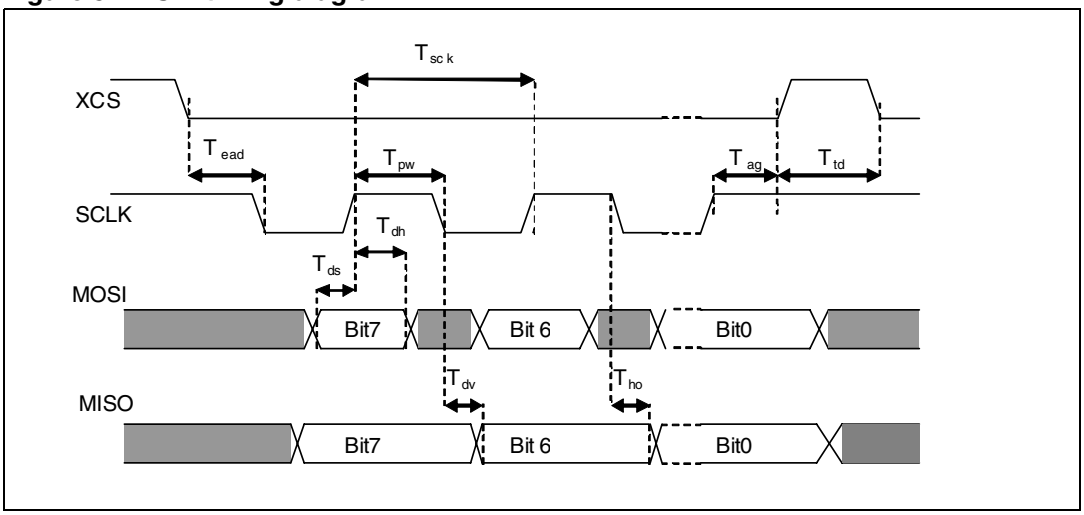
Table 7. Commands list

Code(Hex)	Name	R/W	Comment
00	Not used		RESERVED
01	NOP		No operation
02	SHUT		Shutdown
03	Turn ON		Required only after SHUT command
04	Read current	Read	10-bit
05	Read vin	Read	10-bit
06	Read pwm	Read	9-bit
07	Read status	Read	Read OVC (4-bit) OVV - OVT and CR 7-bit

5.11 SPI timing diagram

Figure 5 shows the SPI timing diagram.

Figure 5. SPI timing diagram



Typical timing requirements are listed in *Table 8* and are based on characterization; these parameters are not tested in production.

Table 8. Typical timing requirements @ 25 °C, V_{DD}=3.3 V

Parameter	Description	Min.	Max.	Units
Fsclk	SCLK frequency		6	MHz
Tsck	SCLK period		167	ns
Tpw	SCLK pulse width	80		ns
Tlead	SS lead time	80		ns
Tlag	SS lag time	80		ns
Ttd	Sequential transfer delay	80		ns
Tds	MOSI data setup time	8		ns
Tdh	MOSI data hold time	8		ns
Tdv	MISO data valid time		20	ns
Tho	MISO data hold time	8		ns

6 Typical curves

Figure 6. Efficiency and power loss vs. input voltage

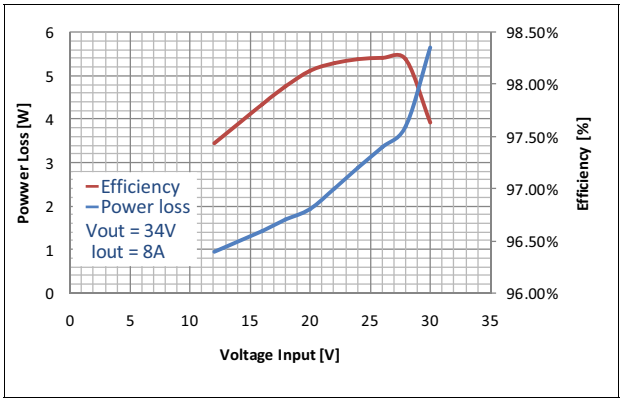


Figure 7. Efficiency vs. output current

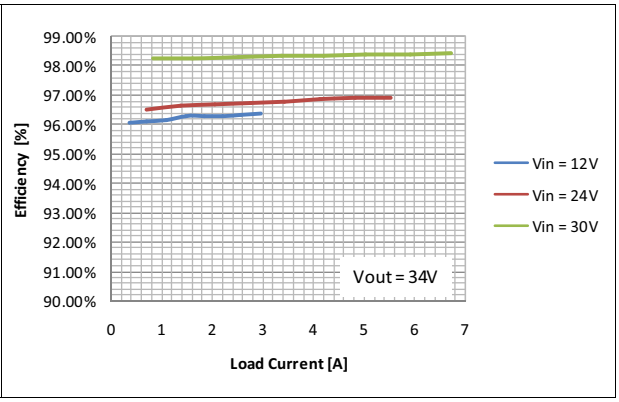


Figure 8. Quiescent current vs. output voltage

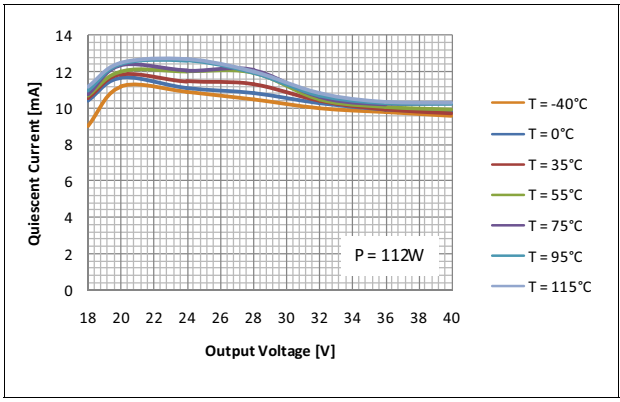


Figure 9. Quiescent current vs. temperature

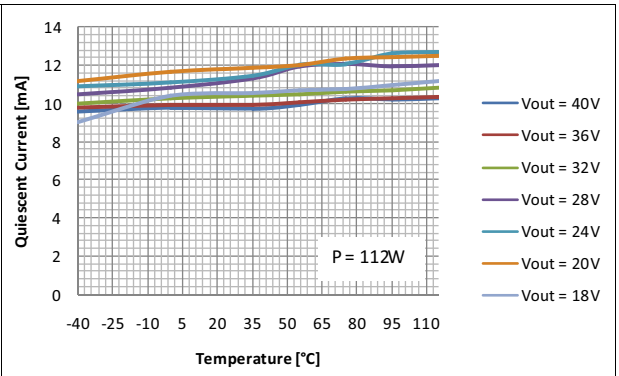
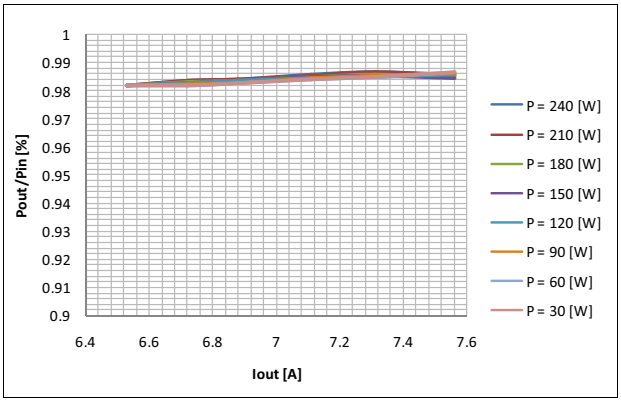


Figure 10. Power efficiency mesured on the board STEVAL-ISV009V1 at T_A=25 °C



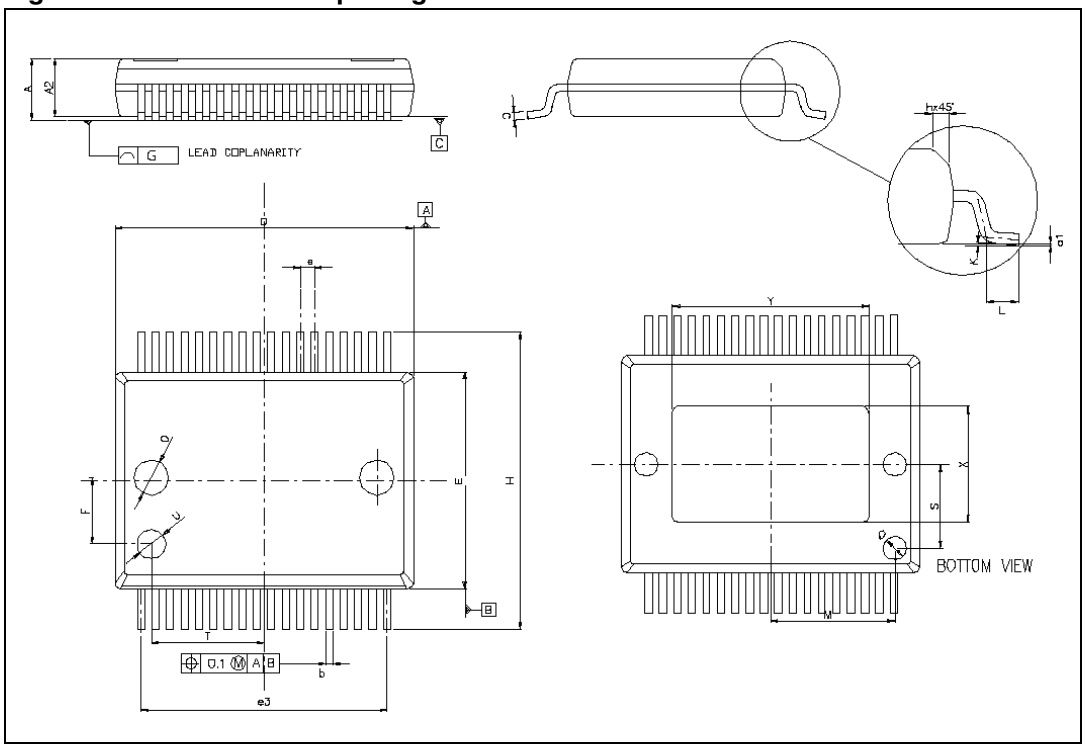
7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 9. PowerSSO-36 mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.18		0.36
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.5	
e3		8.5	
F		2.3	
G			0.075
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
M		4.3	
N			10deg
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
X	4.1		4.7
Y	4.9		5.5

Figure 11. PowerSSO-36 package dimensions



8 Revision history

Table 10. Document revision history

Date	Revision	Changes
07-Jun-2010	1	Initial release
15-Nov-2010	2	Updated Coverpage, *Figure 1*, *Table 5* and *Chapter 5*
16-Jan-2012	3	Added *Chapter 6*, updated *Figure 7* Minor text changes
25-May-2012	4	*Table 4.* added footnote and inserted Tj_{op} min. and max. values. Updated *Figure 3.*