# SCG4001 Synchronous Clock Generators

PLL

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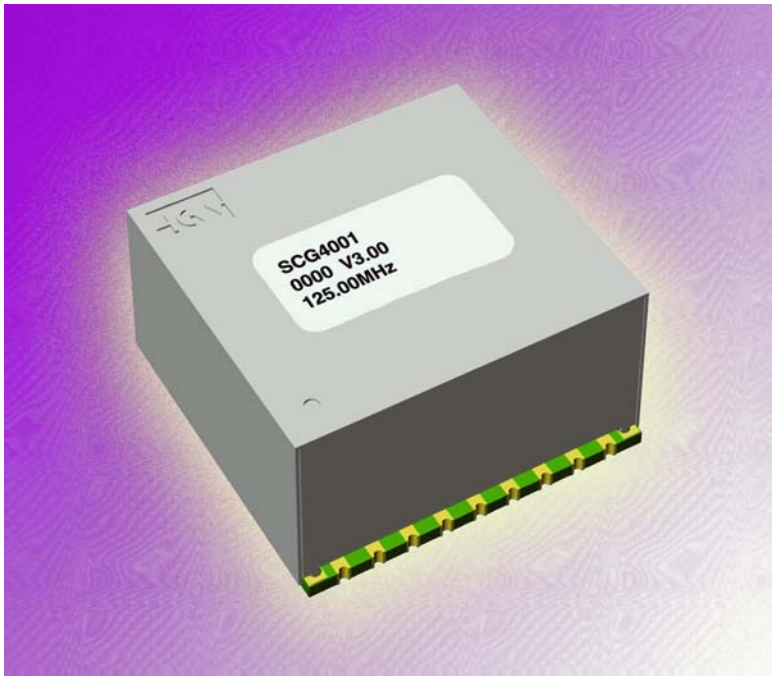


## Application

The Connor-Winfield SCG4001 provides high precision phase lock loop frequency translation for the telecommunication applications.

SCG4001 is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization for TDM, PDH, SONET and SDH network equipment. The SCG4001 provides a jitter filtered, wander following output signal sychronized to a superior Stratum or peer input reference signal.

The SCG4001 is designed to operate with a STRATUM 4 reference

## Features

- ±32 ppm Absolute Pull-in Range
- 3.3V High Precision PLL
- Tri-State Capability
- Active Alarms
- Guaranteed Free Run ±20ppm
- 1 sec. Acquisition Time

| | |
|---|---|
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| Page | 1 of 12 |
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## General Description

The SCG4001 is a digital phase locked loop generating a LVPECL outputs from an intrinsically low jitter voltage controlled crystal oscillator. The LVPECL outputs may be disabled. The jitter attenuated internal reference, divided down from the output frequency, is also output to a pin.

The SCG4001 can only lock to an 8kHz reference. A filtered reference output signal is available at the same frequency. The unit has an acquisition time of about 1 second and it is tolerant of different reference duty cycles.

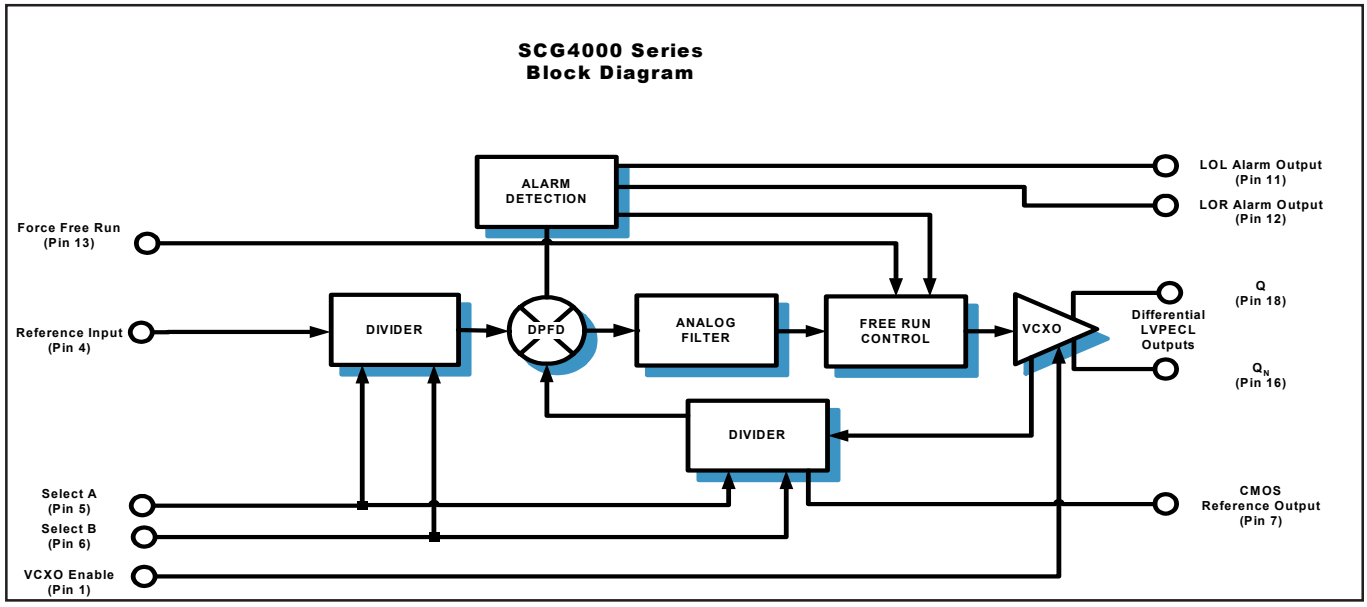
Further features include alarm outputs for Loss-of-Reference (LOR) and Loss-of-Lock (LOL). During the LOR alarm, the SCG4000 will also enter a Free Run state, which will guarantee a 20 ppm accurate output. Additionally the Free Run mode may be entered manually.

The alarms and reference output may be put into the tri-state high impedance condition for external testing purposes.

The package dimensions are 1.025" x 1.0" x 0.429" on a 6 layer FR4 board with castellated pins. Parts are assembled using high temperature solder to withstand 63/37 alloy, 180° C surface mount reflow processes.

## Functional Block Diagram

Figure 1




## Absolute Maximum Rating

Table 1

| Symbol | Parameter | Minimum | Nominal | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| Vcc | Power Supply Voltage | 3.0 | | 3.6 | Volts | |
| V1 | Input Voltage | -0.5 | | 5.5 | Volts | |
| Ts | Storage Temperature | -65 | | 150 | deg. C | |

## Operating Specifications

Table 2

| Symbol | Parameter | Minimum | Nominal | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{cc}$ | Power Supply Voltage | 3.135 | 3.3 | 3.465 | Volts | 1.0 |
| $I_{cc}$ | Power Supply Current | - | 230 | 280 | mA | |
| $T_o$ | Temperature Range | 0 | - | 70 | °C | |
| $F_{fr}$ | Free Run Accuracy | -20 | - | 20 | ppm | |
| $F_{cap}$ | Capture/pull-in range | -32 | - | 32 | ppm | |
| $F_{bw}$ | Jitter Filter Bandwidth | - | - | 10 | Hz | |
| $T_{jtol}$ | Input Jitter Tolerance | - | - | 6.25 | µs | |
| $T_{aq}$ | Acquisition Time | - | 1 | - | s | 2.0 |
| $T_{rf}$ | Output Rise and Fall Time (20% 80%) | 100 | 225 | 350 | ps | 3.0 |

## Features

Table 3

| Parameter | Specifications | Notes |
|---|---|---|
| Alarms | LOR, LOL Status on seperate CMOS Outputs | |
| TDEV | 70 ps (typical) | |
| MTIE | 800 ps (typical) | |
| VCXO Output Logic Type | LVPECL | |
| Reference Output Logic Type | CMOS | |
| Package | FR4 SM 1.025" x 1.0" x 0.429" | |

## CMOS Input And Output Characteristics

Table 4

| Symbol | Parameter | Minimum | Nominal | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | 2 | | 5.5 | V | |
| $V_{IL}$ | Low Level Input Voltage | 0 | | 0.8 | V | |
| $T_{IO}$ | I/O to Output Valid | | | 10 | nS | |
| $C_O$ | Output Capacitance | | | 10 | pF | |
| $V_{HO}$ | High Level Output Voltage Ioh = 04mA | 2.4 | | | | Vcc Min. |
| $V_{IO}$ | Low Level Output Voltage Io1 = 8mA | | | 0.4 | | Vcc Max. |
| $T_{IR}$ | Input Reference Signal Pulse Width | 12.5 | | | nS | |

NOTES: 1.0: Requires external regulation and filter (22uF, 330 pF)
` 2.0: From a 20 ppm offset in reference frequency
3.0: 50Ω load biased to 1.3V

## LVPECL Output Characteristics

Table 5

| Symbol | Parameter | Minimum | Nominal | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High Level PECL Voltage | 2.27 | 2.34 | 2.42 | V | |
| $V_{OL}$ | Low Level PECL Voltage | 1.49 | 1.51 | 1.68 | V | |
| $C_L$ | Output Capacitance | | | 10 | pF | |
| $T_{SKEW}$ | Differential Output Skew | | 50 | | ps | |

## Output Jitter Specifications

Table 6

| | Jitter BW 10 Hz - 1 MHz | | SONET Jitter BW 12 kHz - 20 MHz | |
|---|---|---|---|---|
| Frequency (MHz) | pS (RMS) | m UI | pS (RMS) | m UI |
| 125.0 | 20(typical) | 2.5 (typical) | 1 (max), 0.3 (typical) | 0.125(max) |

## Output Programming

Table 7

| Tristate | Free Run | Output |
|---|---|---|
| 0 | 0 | Locked to reference selected (default) |
| 1 | X | Hi-Z Tristate condition |
| 0 | 1 | Free run at nominal frequency |

## Alarm Status

Table 9

| LOL Output | LOR Output | Alarm Output |
|---|---|---|
| 0 | 0 | No alarm |
| 1 | 0 | Loss-of-Lock |
| X | 1 | Loss-of-Reference |

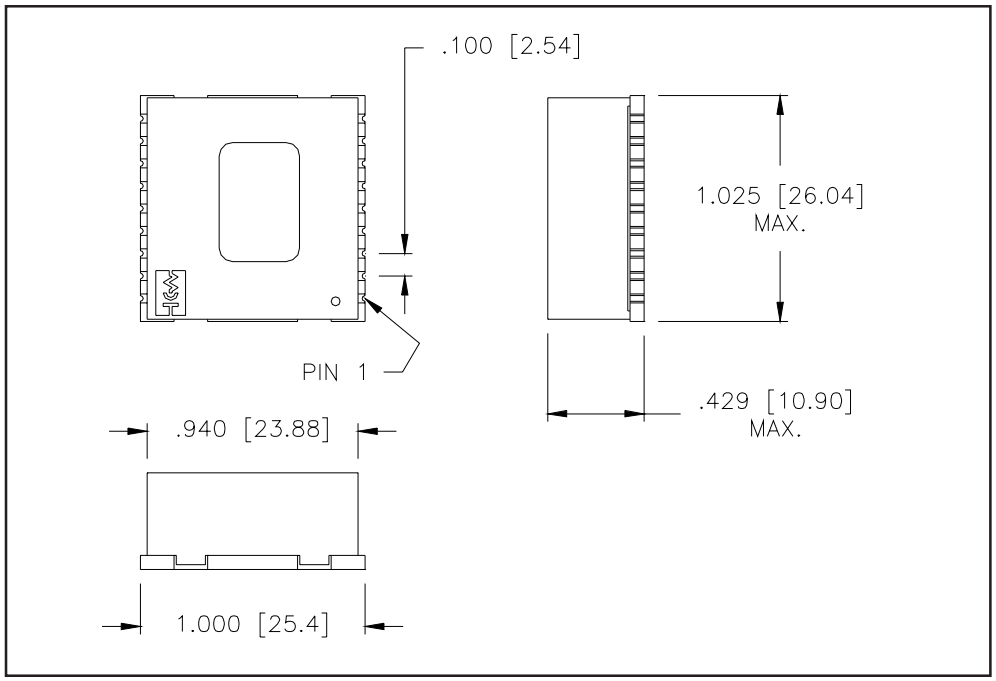
## Pin Description

Table 8

| Pin # | Connection | Description |
|---|---|---|
| 1 | $\overline{\text{Enable}}$/Disable | Enable = 0, Disable = 1 for VCXO Ouputs, Default = 0 (for No Connect) |
| 2 | TCK | JTAG pin that is used only by Connor-Winfield for programming. Do not connect |
| 3 | TDO | JTAG pin that is used only by Connor-Winfield for programming. Do not connect |
| 4 | Reference In | CMOS Reference Frequency Input |
| 5 | Select A | Reference Frequency Select Pin, Default = 0 (for No Connect) |
| 6 | Select B | Reference Frequency Select Pin, Default = 0 (for No Connect) |
| 7 | Reference Out | Filtered Reference Output |
| 8 | Ground | Power Ground |
| 9 | Tri-State Enable | CMOS Output Tri-State enable (Hi-Z =1, Default = 0) |
| 10 | $V_{CC}$ | 3.3V Supply Voltage. |
| 11 | Loss of Lock | LOL Alarm Output |
| 12 | Loss of Reference | LOR Alarm Output |
| 13 | Free Run | Force output frequency to Free Run (FR = 1, Default = 0) |
| 14 | TDI | JTAG pin that is used only by Connor-Winfield for programming. Do not connect |
| 15 | TMS | JTAG pin that is used only by Connor-Winfield for programming. Do not connect |
| 16 | $\overline{\text{VCXO Out}}$ | VCXO differential LVPECL Output |
| 17 | Signal Ground | VCXO output ground (Shield) |
| 18 | VCXO Out | VCXO differential LVPECL Output |

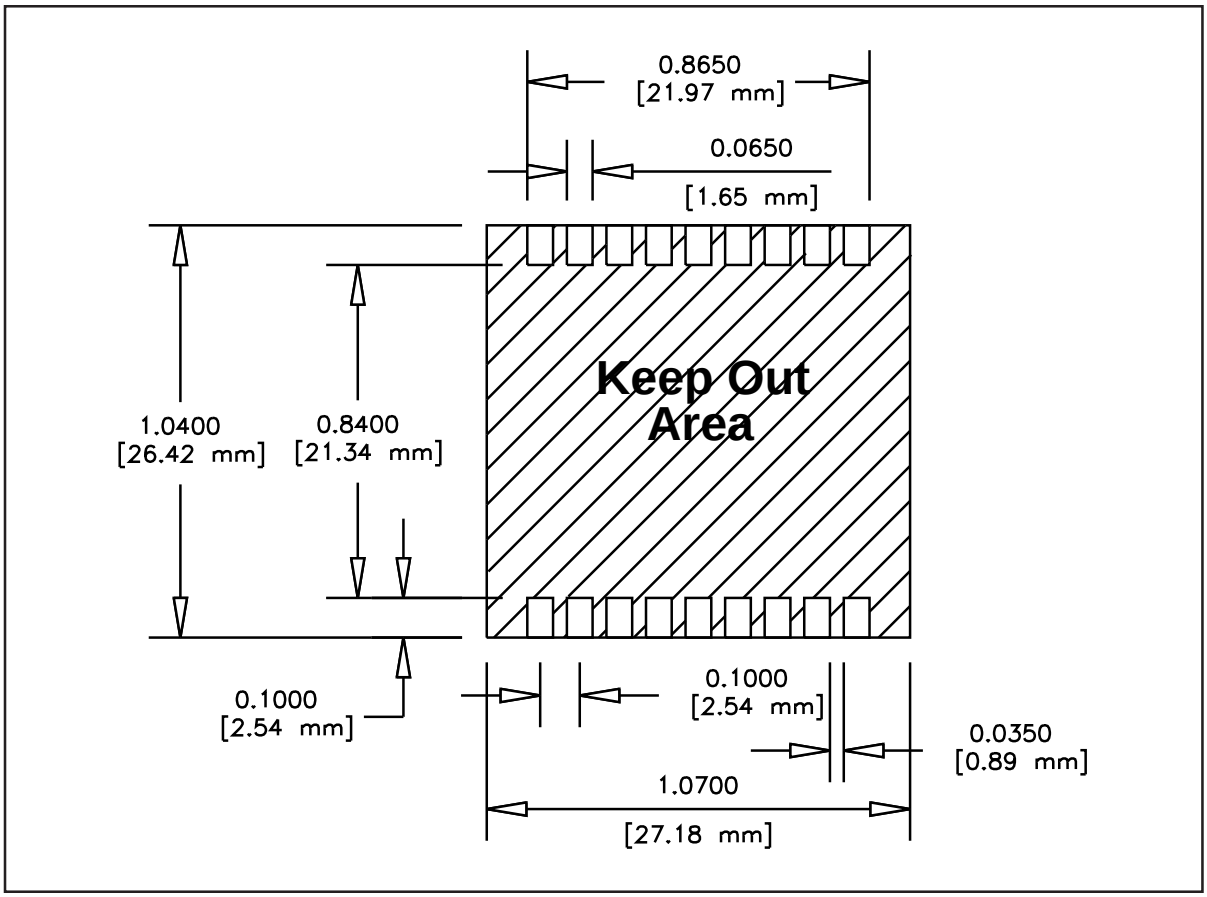
## Package Dimensions

Figure 2



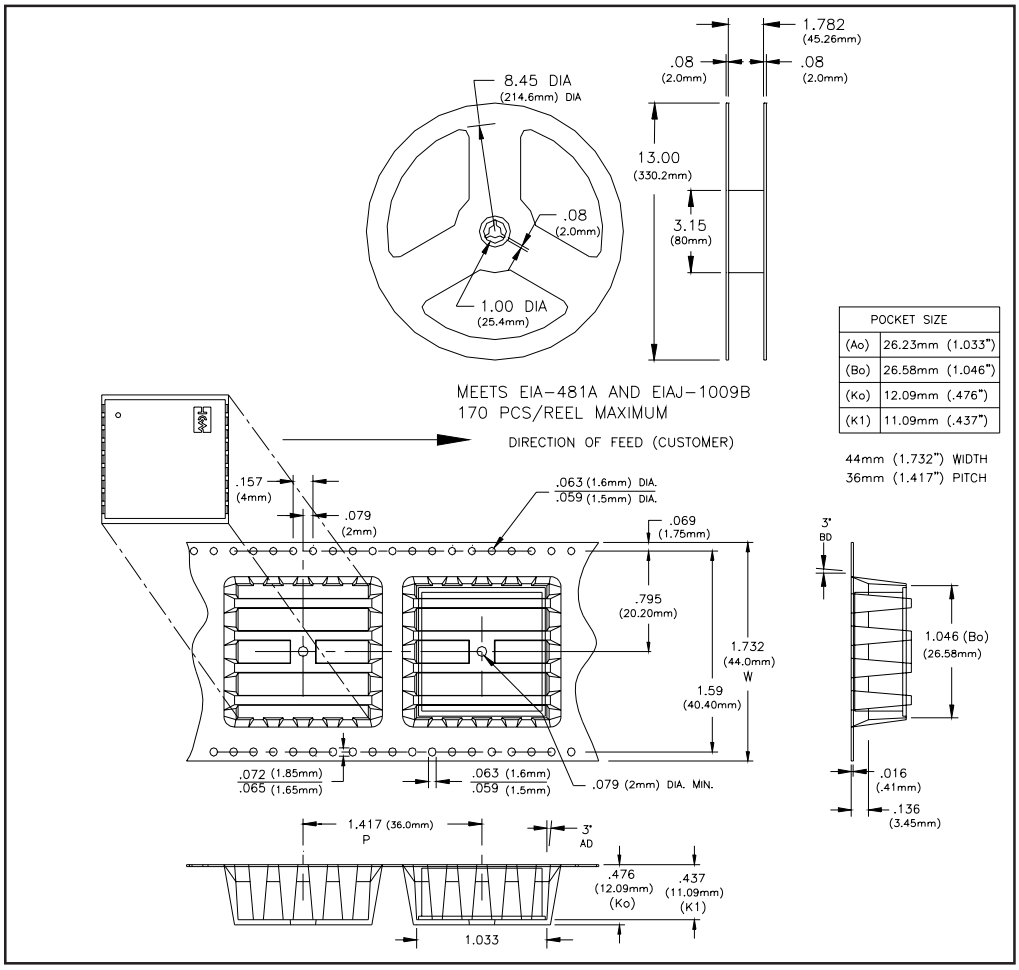

## Recommended Footprint Dimensions

Figure 3



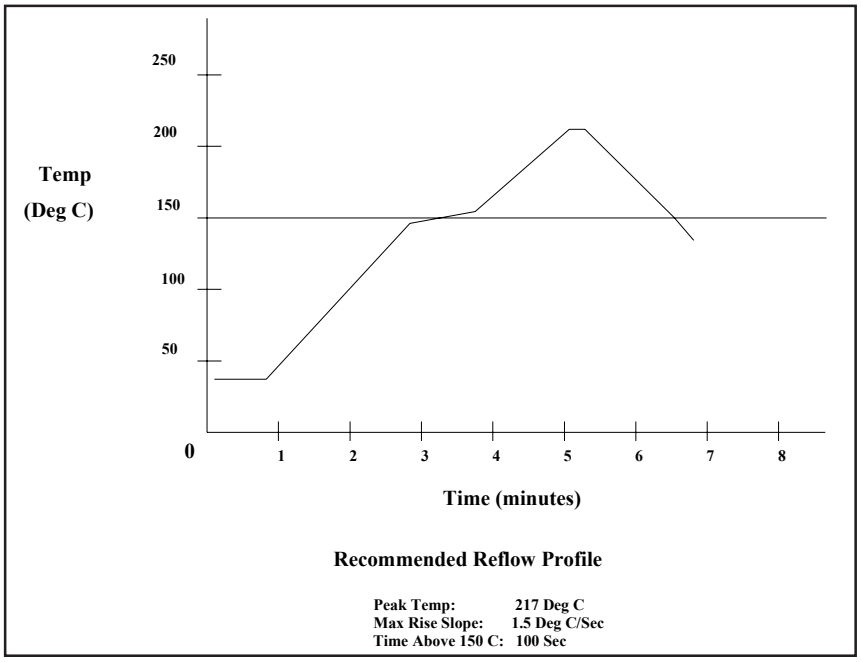
## Tape and Reel Dimensions

Figure 4



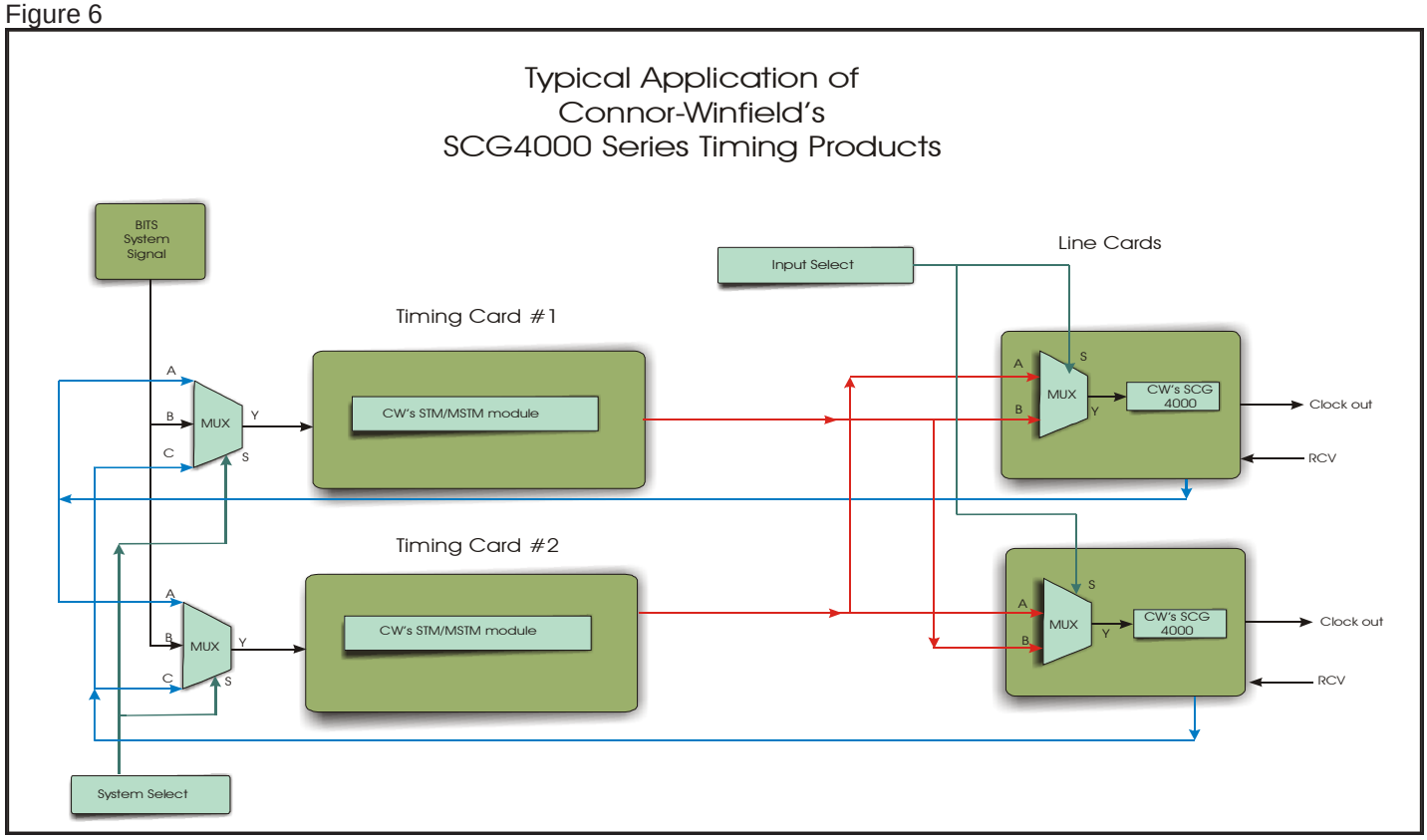

## Solder Profile

Figure 5



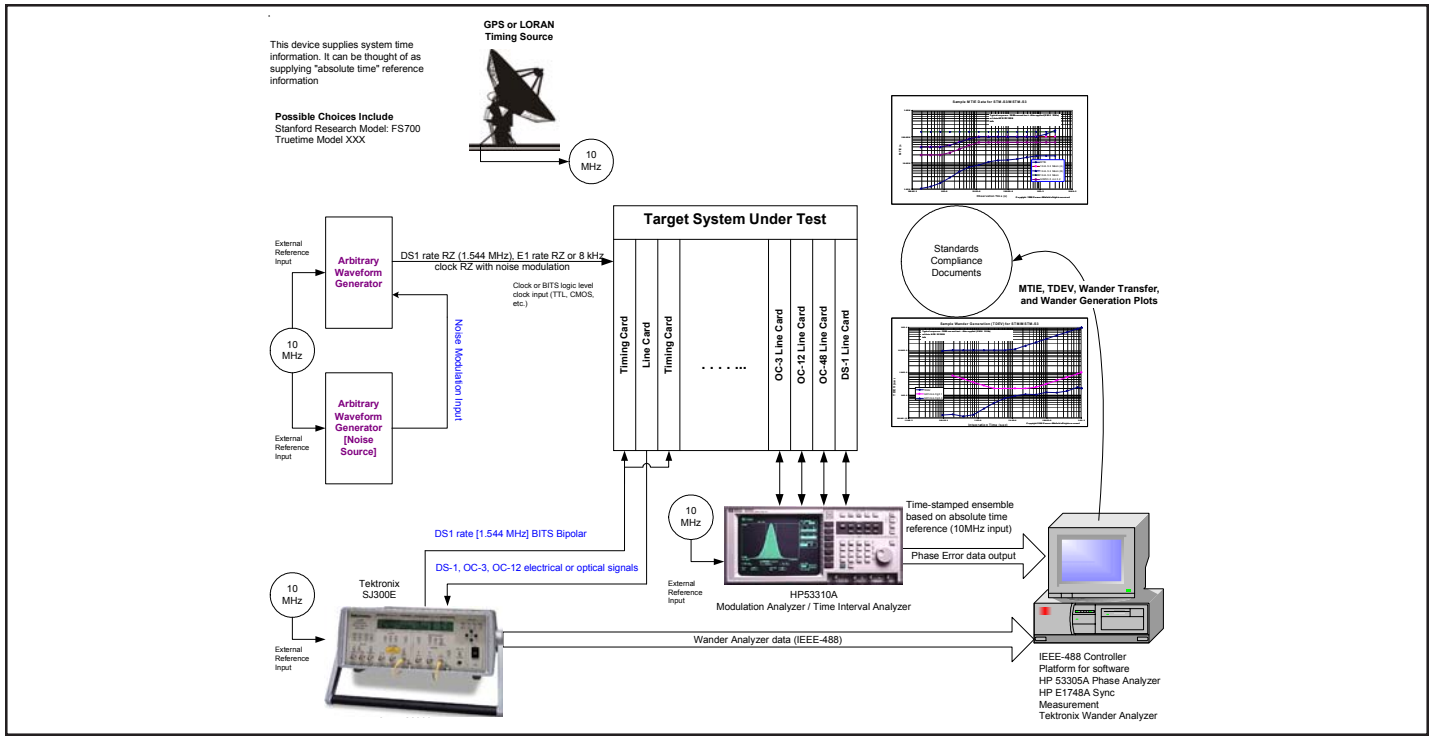
## Typical Application

Figure 6



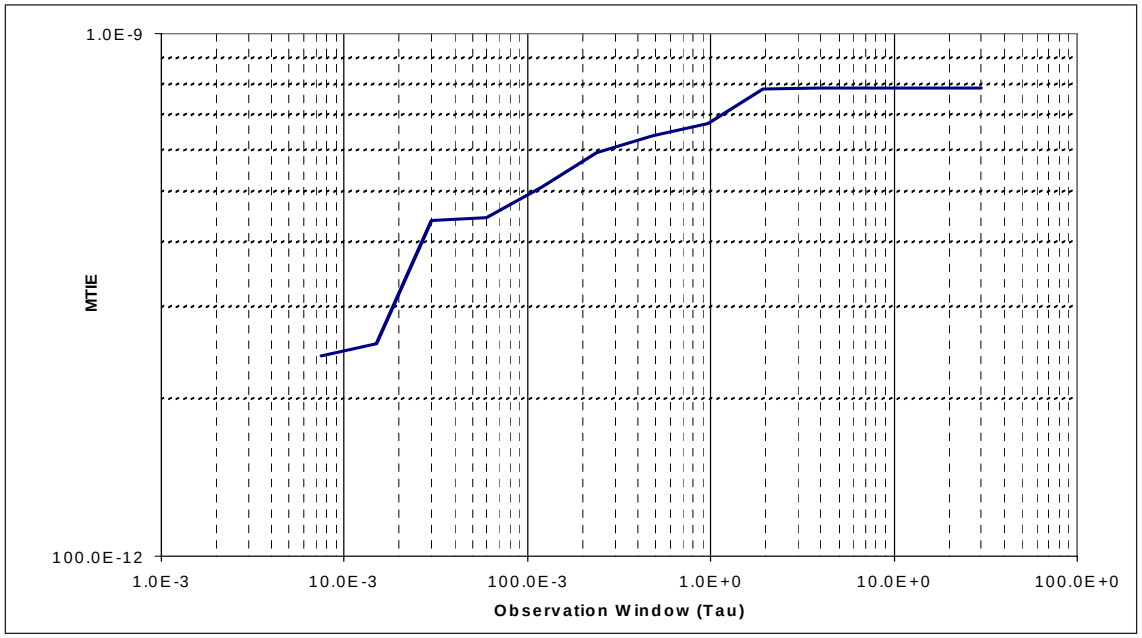

## Typical System Test Set-up

Figure 7



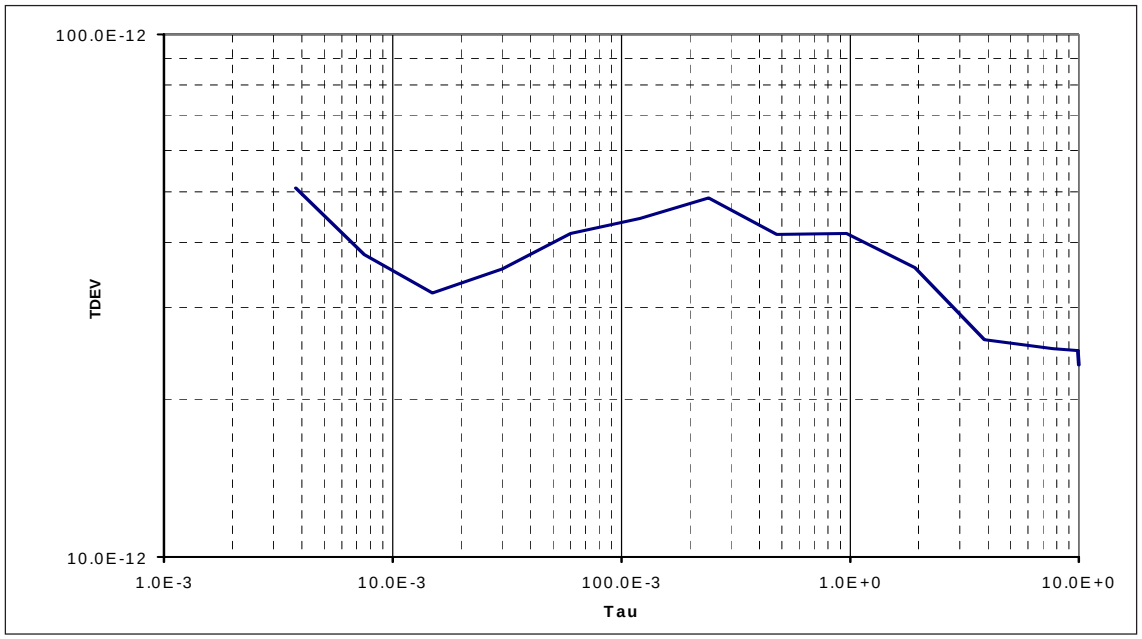
## SCG4000 Series Typical MTIE

Figure 8




## SCG4000 Series Typical TDEV

Figure 9



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| Revision | Revision Date | Note |
|---|---|---|
| P00 | 08/08/02 | Preliminary Release |