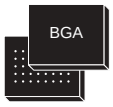
M68AW512D

8 Mbit (512K x16) 3.0V Asynchronous SRAM

FEATURES SUMMARY

- SUPPLY VOLTAGE: 2.7 to 3.6V
- 512K x 16 bits SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 55, 70ns
- LOW STANDBY CURRENT
- LOW V_{CC} DATA RETENTION: 1.5V
- TRI-STATE COMMON I/O
- AUTOMATIC POWER DOWN

Figure 1. Packages



TFBGA48 (ZB)
6 x 7mm

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SUMMARY DESCRIPTION

The M68AW512D is an 8 Mbit (8,388,608 bit) CMOS SRAM, organized as 524,288 words by 16 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 2.7 to 3.6V supply. This device has a Chip Select pin (E2) for easy memory expansion; when it is active (E2 high) the device has an automatic power-down feature, reducing the power consumption by over 99%.

The M68AW512D is available in TFBGA48 (0.75 mm ball pitch) package.

Figure 2. Logic Diagram

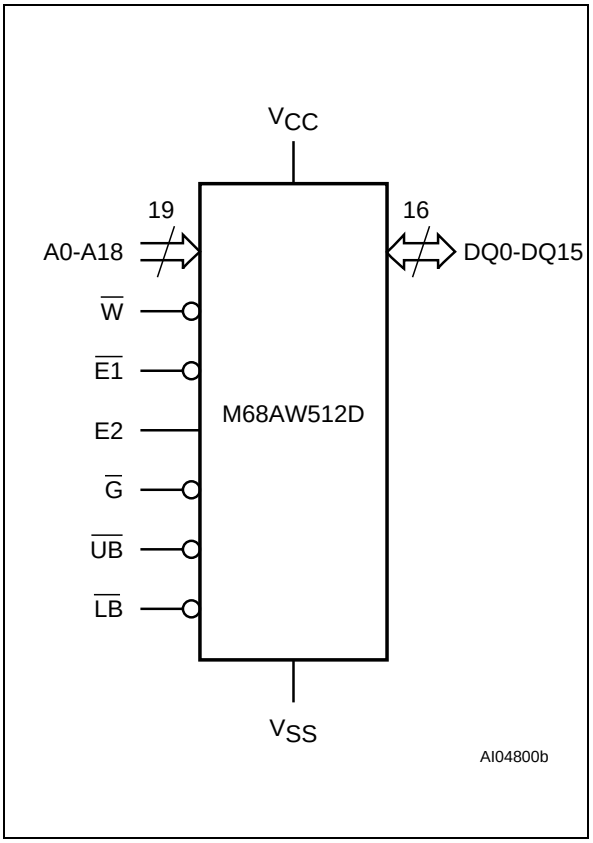


Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ15	Data Input/Output
$\overline{E1}$	Chip Enable
E2	Chip Select
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{UB}$	Upper Byte Enable Input
$\overline{LB}$	Lower Byte Enable Input
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected
DU	Don't Use as Internally Connected

Figure 3. TFBGA Connections (Top view through package)

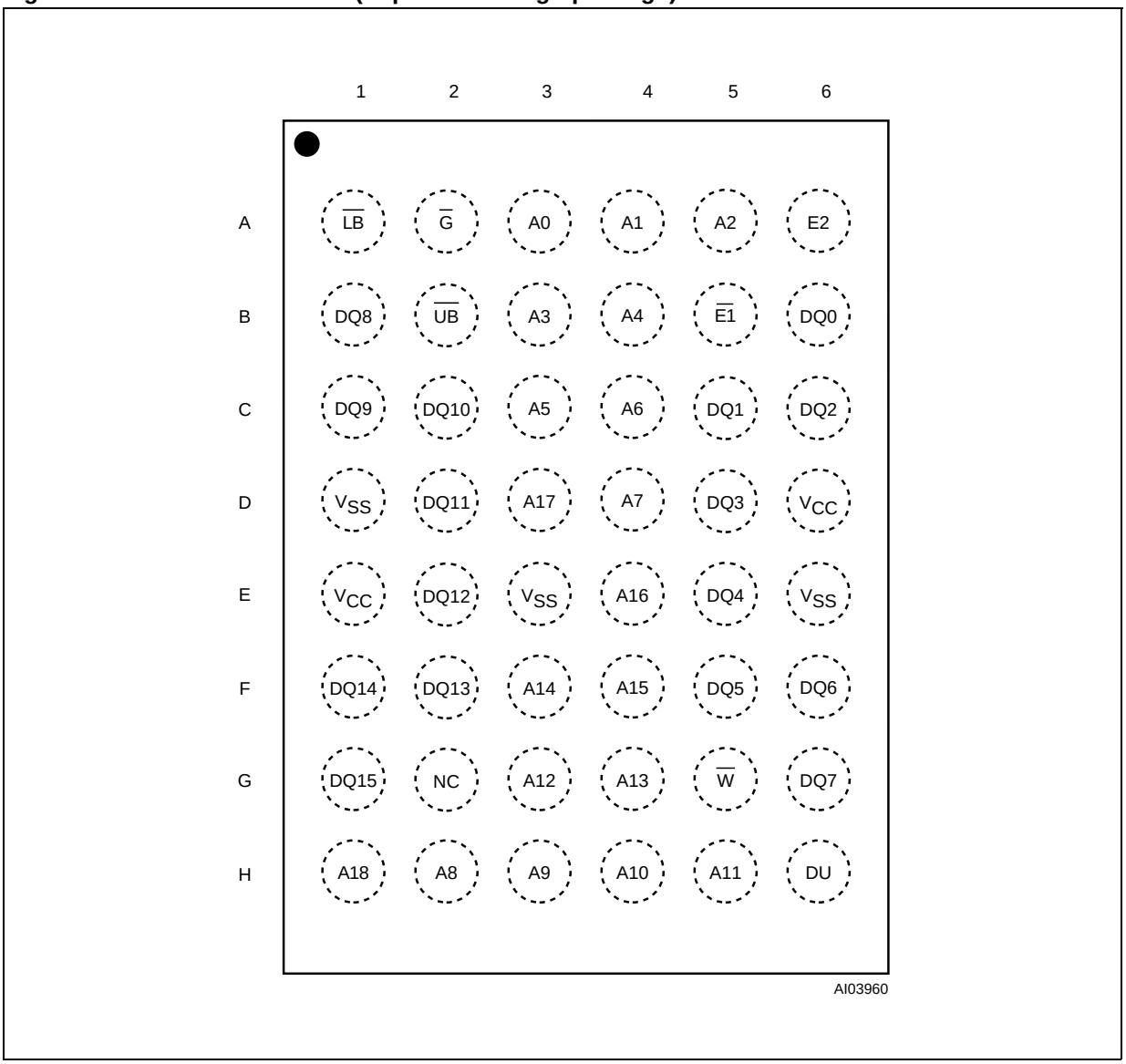
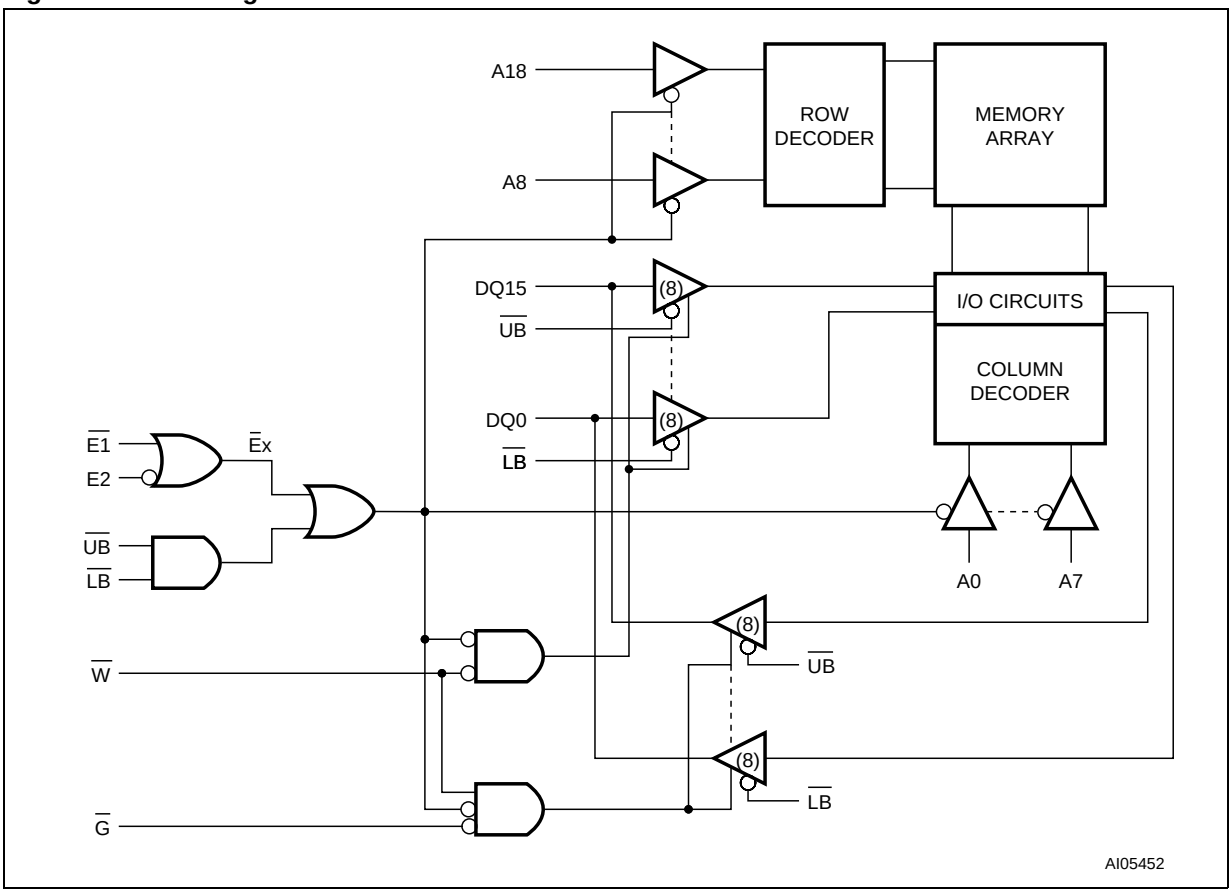


Figure 4. Block Diagram



OPERATION

The device has four standard operating modes: Output Disabled, Read, Write and Standby/Power-Down. These modes are determined by the control inputs $\overline{E1}$, E1, $\overline{W}$, $\overline{G}$, $\overline{LB}$ and $\overline{UB}$ as summarized in Table 2.Operating Modes.

Output Disabled

The Output Enable signal, $\overline{G}$, provides high-speed tri-state control of DQ0-DQ15, allowing fast read/write cycles on the I/O data bus. The device is in Output Disabled mode when Output Enable, $\overline{G}$, is High. In this mode, $\overline{LB}$ and $\overline{UB}$ are Don't care and DQ0-DQ15 are high impedance.

Read Mode

When Chip Select (E2) is High, the Mvvvvv is in the Read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and Chip Enable ($\overline{E1}$) is asserted.

This provides access to data from eight or sixteen, depending on the status of the signal $\overline{UB}$ and $\overline{LB}$, of the 8,388,608 locations in the static memory array, specified by the 19 address inputs. If only one of the Byte Enable inputs is at V_{IL}, the Mvvvvv is in Byte Read mode. If the two Byte Enable inputs are at V_{IL}, the Mvvvvv is in Word Read mode. So depending on the status of the $\overline{UB}$ and $\overline{LB}$ signals, valid data will be available on the lower eight, the upper eight or all sixteen output pins, tAVQV after the last stable address, providing $\overline{G}$ is Low, $\overline{E1}$ is Low and E2 is High.

If either of $\overline{E1}$ or $\overline{G}$ is asserted after t_{AVQV} has elapsed, data access will be measured from the limiting parameter (t_{ELQV}, t_{GLQV} or t_{BLQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, t_{GLQX} and t_{BLQX}, but data lines will always be valid at t_{AVQV}.

Write Mode

The M68AW512D, when Chip Select (E2) is High, is in the Write Mode whenever the $\overline{W}$ and $\overline{E1}$ are Low. Either the Chip Enable Input ($\overline{E1}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. When $\overline{E1}$ or $\overline{W}$ is Low, and $\overline{UB}$ or $\overline{LB}$ is Low, write cycle begins on the $\overline{W}$ or $\overline{E1}$ falling edge. When $\overline{E1}$ and $\overline{W}$ are Low, and $\overline{UB}$ = $\overline{LB}$ = High, write cycle begins on the first falling edge of $\overline{UB}$ or $\overline{LB}$. Therefore, address setup time is referenced to Write Enable, Chip Enables and $\overline{UB}$/$\overline{LB}$ as t_{AVWL}, t_{AVEL} and t_{AVBL} respectively, and is determined by the latter occurring falling edge.

The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$, $\overline{W}$, $\overline{UB}$ and $\overline{LB}$.

If the Output is enabled ($\overline{E1}$ = Low, E2 = High, $\overline{G}$ = Low, $\overline{LB}$ or $\overline{UB}$ = Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E1}$ or for t_{DVBH} before the rising edge of $\overline{UB}$/$\overline{LB}$, whichever occurs first, and remain valid for t_{WHDX}, t_{EHDX} and t_{BHDX} respectively.

Standby/Power-Down

The M68AW512D has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E1}$ = High) or Chip Select is asserted (E2 = Low), or $\overline{UB}$/$\overline{LB}$ are de-asserted ($\overline{UB}$/$\overline{LB}$ = High). An Output Enable ($\overline{G}$) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{E1}$, $\overline{LB}$ and $\overline{UB}$ as summarized in the Operating Modes table (see Table 2).

Table 2. Operating Modes

Operation	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	$\overline{LB}$	$\overline{UB}$	DQ0-DQ7	DQ8-DQ15	Power
Deselected (Standby/Power-Down)	V_{IH}	X	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
	X	V_{IL}	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
	X	X	X	X	V_{IH}	V_{IH}	Hi-Z	Hi-Z	Standby (I_{SB})
Lower Byte Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data Output	Hi-Z	Active (I_{CC})
Lower Byte Write	V_{IL}	V_{IH}	V_{IL}	X	V_{IL}	V_{IH}	Data Input	Hi-Z	Active (I_{CC})
Output Disabled	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z	Hi-Z	Active (I_{CC})
Upper Byte Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Hi-Z	Data Output	Active (I_{CC})
Upper Byte Write	V_{IL}	V_{IH}	V_{IL}	X	V_{IH}	V_{IL}	Hi-Z	Data Input	Active (I_{CC})
Word Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Data Output	Data Output	Active (I_{CC})
Word Write	V_{IL}	V_{IH}	V_{IL}	X	V_{IL}	V_{IL}	Data Input	Data Input	Active (I_{CC})
Output Disabled	V_{IL}	V_{IH}	X	V_{IH}	X	X	Hi-Z	Hi-Z	Active (I_{CC})

Note: 1. X = V_{IH} or V_{IL}.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for periods greater than 1s may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–55 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{CC}	Supply Voltage	–0.5 to 4.6	V
V_{IO} (1)	Input or Output Voltage	–0.5 to V_{CC} +0.5	V
P_D	Power Dissipation	1	W

Note: 1. Up to a maximum operating V_{CC} of 3.6V only.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 4. Operating and AC Measurement Conditions

Parameter		M68AW512D
V_{CC} Supply Voltage		2.7 to 3.6V
Ambient Operating Temperature	Range 1	0 to 70°C
	Range 6	–40 to 85°C
Load Capacitance (C_L)		30pF
Output Circuit Protection Resistance (R_1)		3.0kΩ
Load Resistance (R_2)		3.1kΩ
Input Rise and Fall Times		≤1ns/V
Input Pulse Voltages		0 to V_{CC}
Input and Output Timing Ref. Voltages		$V_{CC}/2$
Output Transition Timing Ref. Voltages		$V_{RL} = 0.3V_{CC}$; $V_{RH} = 0.7V_{CC}$

Figure 5. AC Measurement I/O Waveform

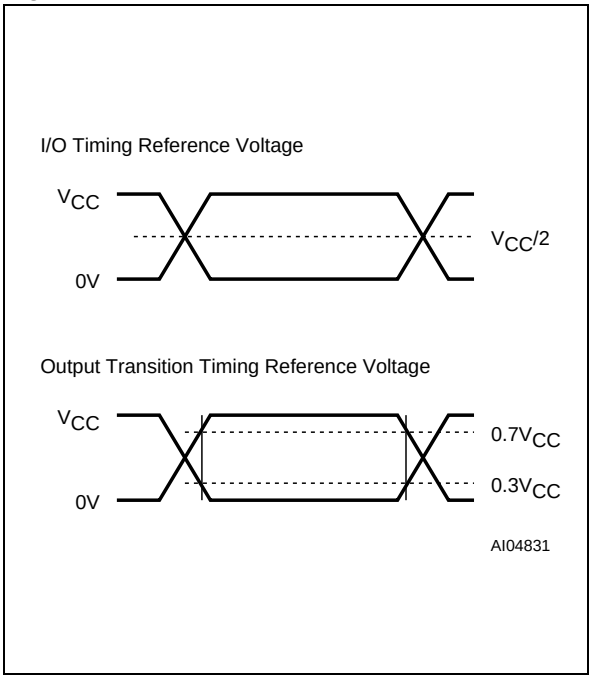


Figure 6. AC Measurement Load Circuit

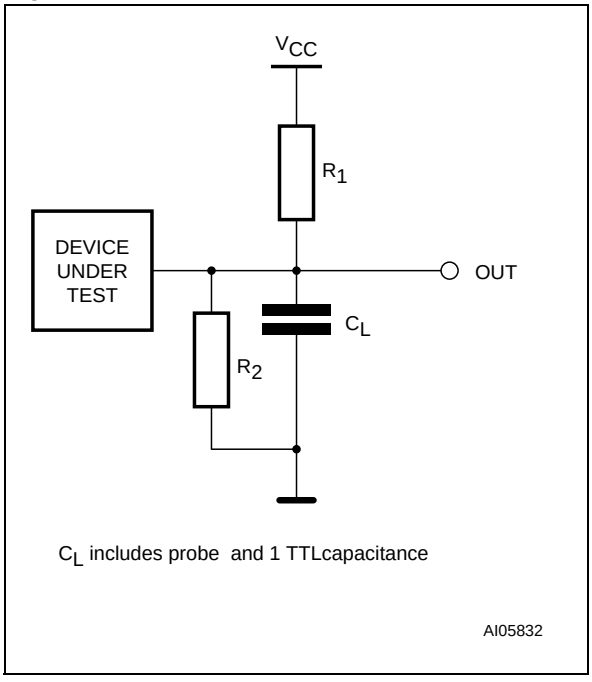


Table 5. Capacitance

Symbol	Parameter[1,2]	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		10	pF

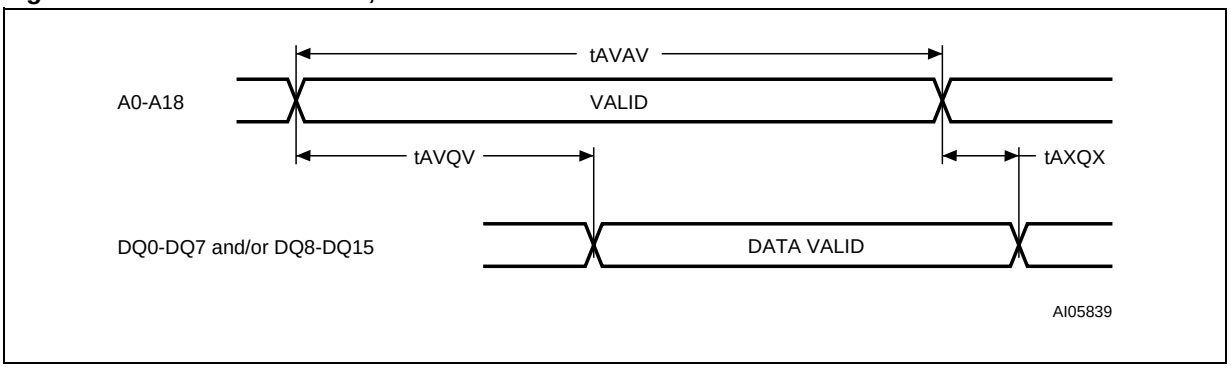
Note: 1. Sampled only, not 100% tested.
2. At T_A = 25°C, f = 1 MHz, V_{CC} = 3.0V.

Table 6. DC Characteristics

Symbol	Parameter	Test Condition		-L		-N		Unit
				Min	Max	Min	Max	
I_{CC1} (1,2)	Operating Supply Current	V_{CC} = 3.6V, f = $1/t_{AVAV}$, I_{OUT} = 0mA	70ns		25		20	mA
			55ns		30		20	mA
I_{CC2}(3)	Operating Supply Current	V_{CC} = 3.6V, f = 1MHz, I_{OUT} = 0mA			4		4	mA
I_{SB}	Standby Supply Current CMOS	V_{CC} = 3.6V, f = 0, $\overline{E1} \geq V_{CC}-0.2V$ or $\overline{E2} \leq 0.2V$ or $\overline{LB}=\overline{UB} \geq V_{CC}-0.2V$			30		30	µA
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		–1	1	–1	1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ (4)		–1	1	–1	1	µA
V_{IH}	Input High Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			–0.3	0.6	–0.3	0.6	V
V_{OH}	Output High Voltage	I_{OH} = –1.0mA		2.4		2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			0.4		0.4	V

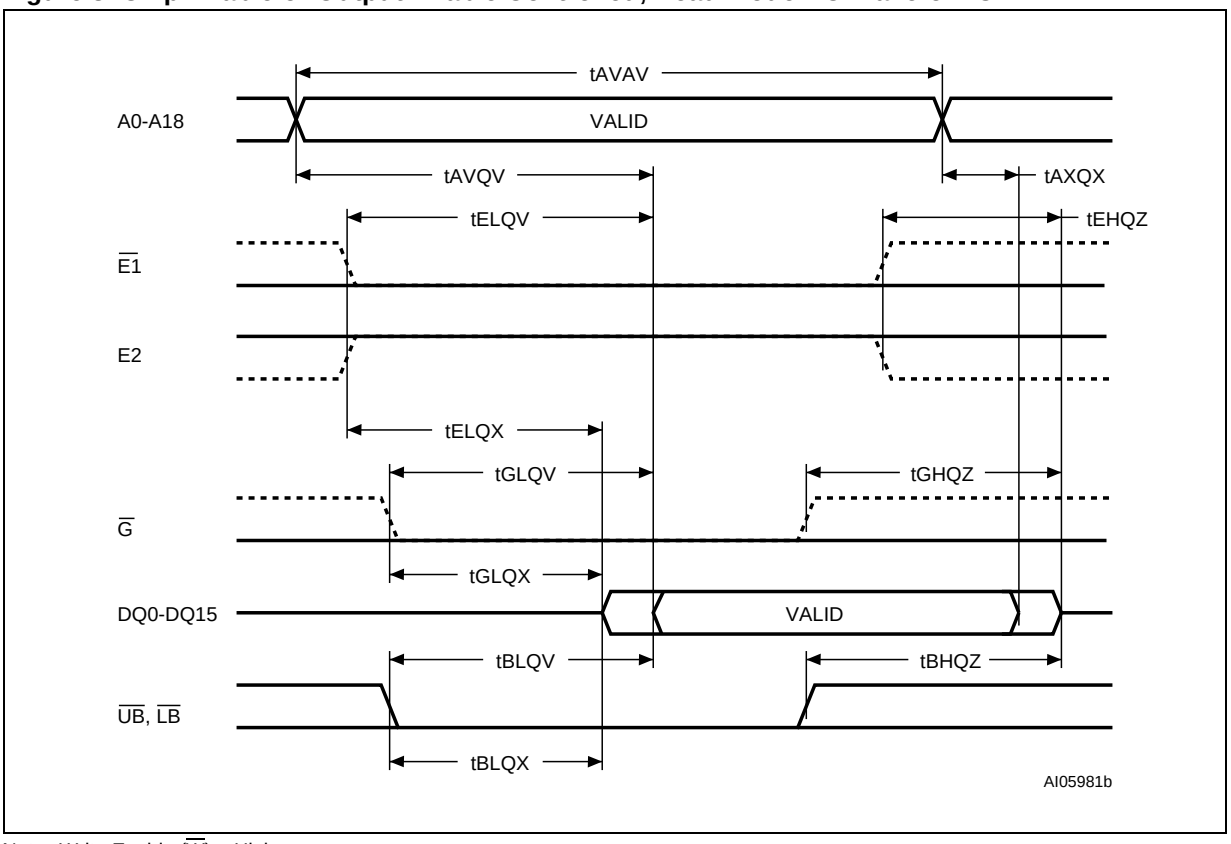
Note: 1. Average AC current, cycling at t_{AVAV} minimum.
2. $\overline{E1}$ = V_{IL} AND E2 = V_{IH}, $\overline{LB}$ OR/AND $\overline{UB}$ = V_{IL}, V_{IN} = V_{IL} OR V_{IH}.
3. $\overline{E1} \leq 0.2V$ AND $E2 \geq V_{CC}-0.2V$, $\overline{LB}$ OR/AND $\overline{UB} \leq 0.2V$, $V_{IN} \leq 0.2V$ OR $V_{IN} \geq V_{CC}-0.2V$.
4. Output disabled.

Figure 7. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E1}$ = Low, E2 = High, $\overline{G}$ = Low, $\overline{W}$ = High, $\overline{UB}$ = Low and/or $\overline{LB}$ = Low.

Figure 8. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High

Figure 9. Chip Enable or $\overline{UB}$/$\overline{LB}$ Controlled, Standby Mode AC Waveforms

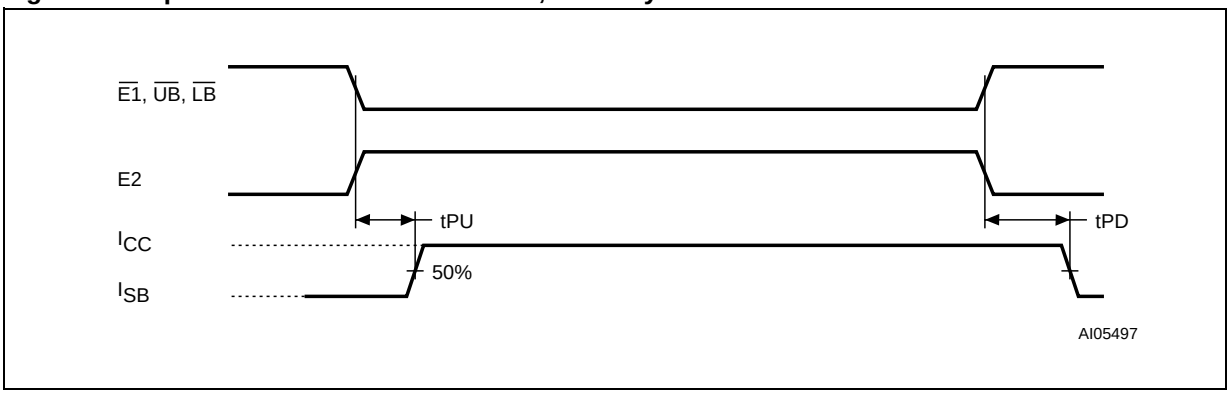
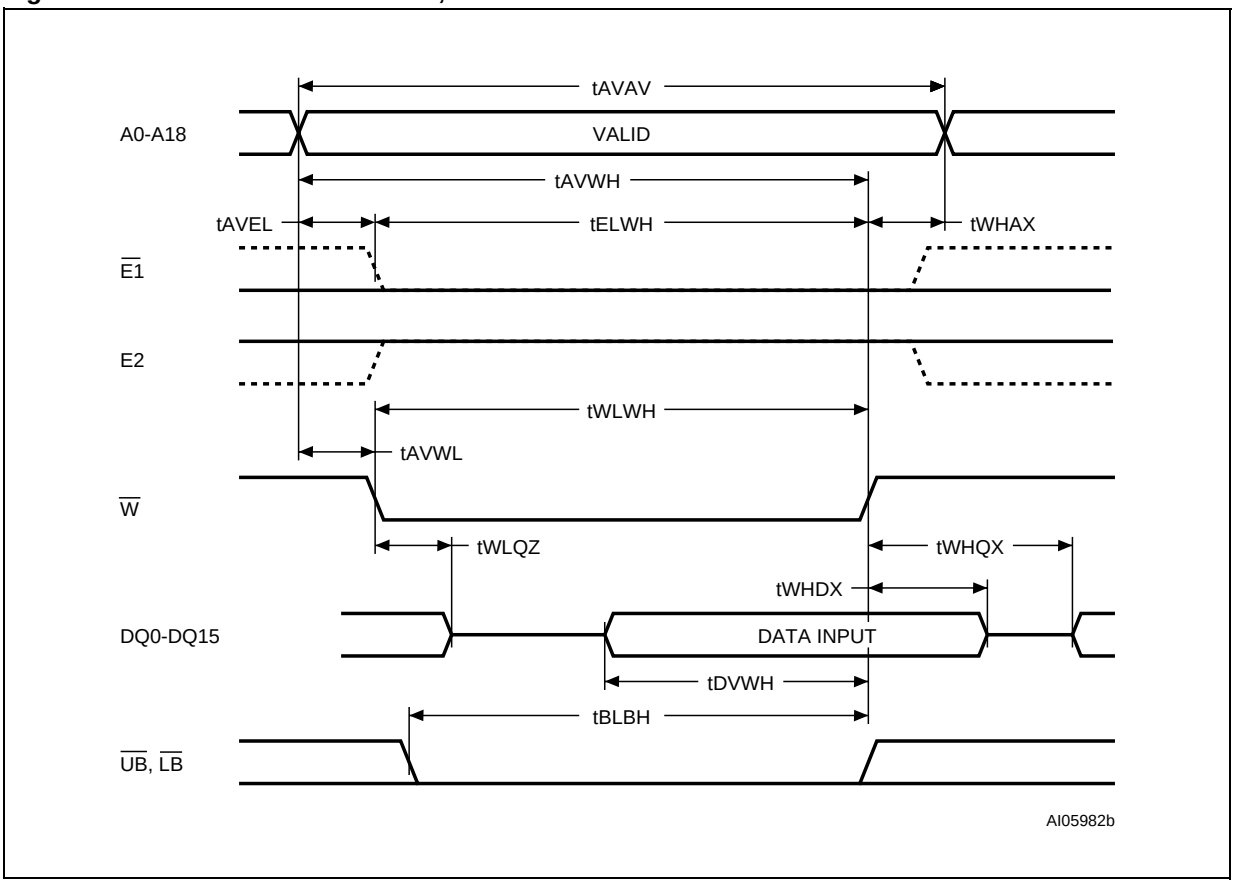


Table 7. Read and Standby Mode AC Characteristics

Symbol	Parameter		M68AW512D		Unit
			55	70	
t_{AVAV}	Read Cycle Time	Min	55	70	ns
t_{AVQV}	Address Valid to Output Valid	Max	55	70	ns
t_{AXQX} (1)	Data hold from address change	Min	5	5	ns
t_{BHQZ} (2,3,4)	Upper/Lower Byte Enable High to Output Hi-Z	Max	20	25	ns
t_{BLQV}	Upper/Lower Byte Enable Low to Output Valid	Max	55	70	ns
t_{BLQX} (1)	Upper/Lower Byte Enable Low to Output Transition	Min	5	5	ns
t_{EHQZ} (2,3,4)	Chip Enable High to Output Hi-Z	Max	20	25	ns
t_{ELQV}	Chip Enable Low to Output Valid	Max	55	70	ns
t_{ELQX} (1)	Chip Enable Low to Output Transition	Min	5	5	ns
t_{GHQZ} (2,3,4)	Output Enable High to Output Hi-Z	Max	20	25	ns
t_{GLQV}	Output Enable Low to Output Valid	Max	25	35	ns
t_{GLQX} (1)	Output Enable Low to Output Transition	Min	5	5	ns
t_{PD}	Chip Enable or $\overline{UB}$/$\overline{LB}$ High to Power Down	Max	55	70	ns
t_{PU}	Chip Enable or $\overline{UB}$/$\overline{LB}$ Low to Power Up	Min	0	0	ns

Note: 1. Test conditions assume transition timing reference level = $0.3V_{CC}$ or $0.7V_{CC}$.
2. At any given temperature and voltage condition, t_{GHQZ} is less than t_{GLQX}, t_{BHQZ} is less than t_{BLQX} and t_{EHQZ} is less than t_{ELQX} for any given device.
3. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Figure 10. Write Enable Controlled, Write AC Waveforms



Note: 1. During this period DQ0-DQ15 are in output state and input signals should not be applied.

Figure 11. Chip Enable Controlled, Write AC Waveforms

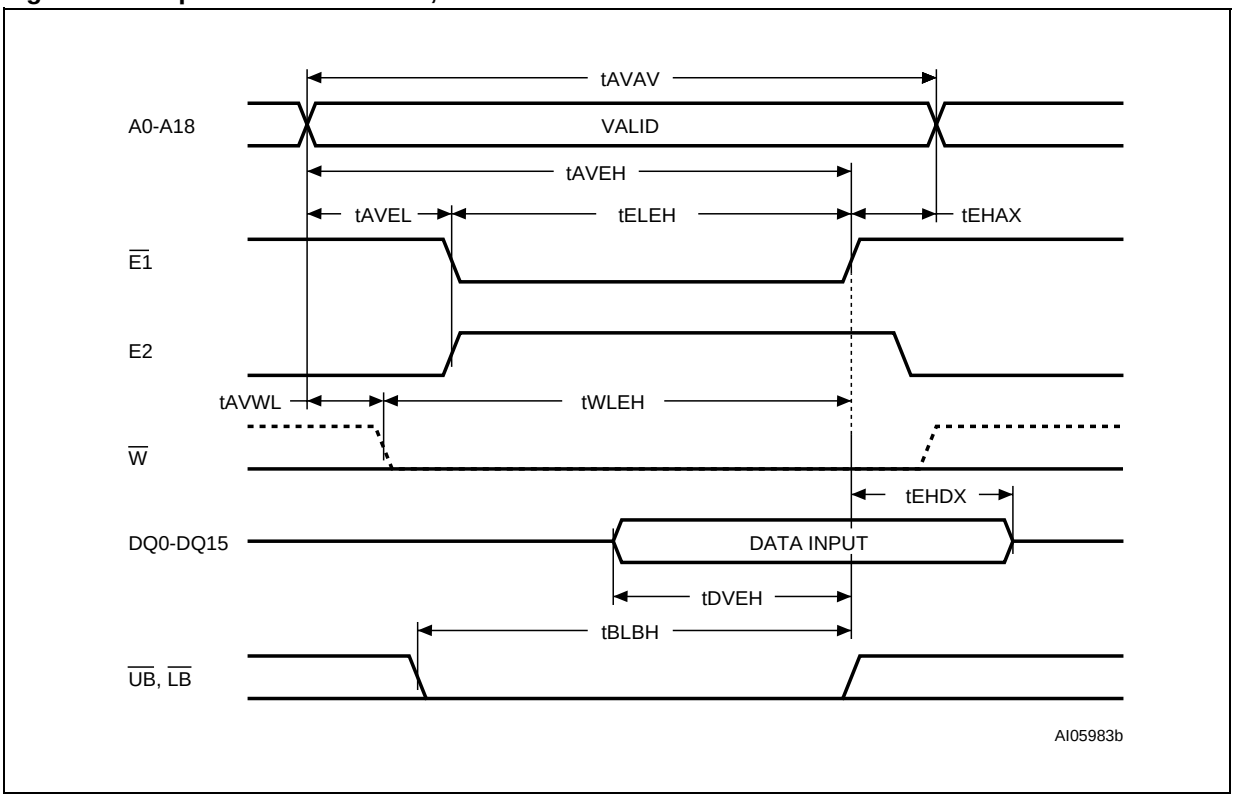
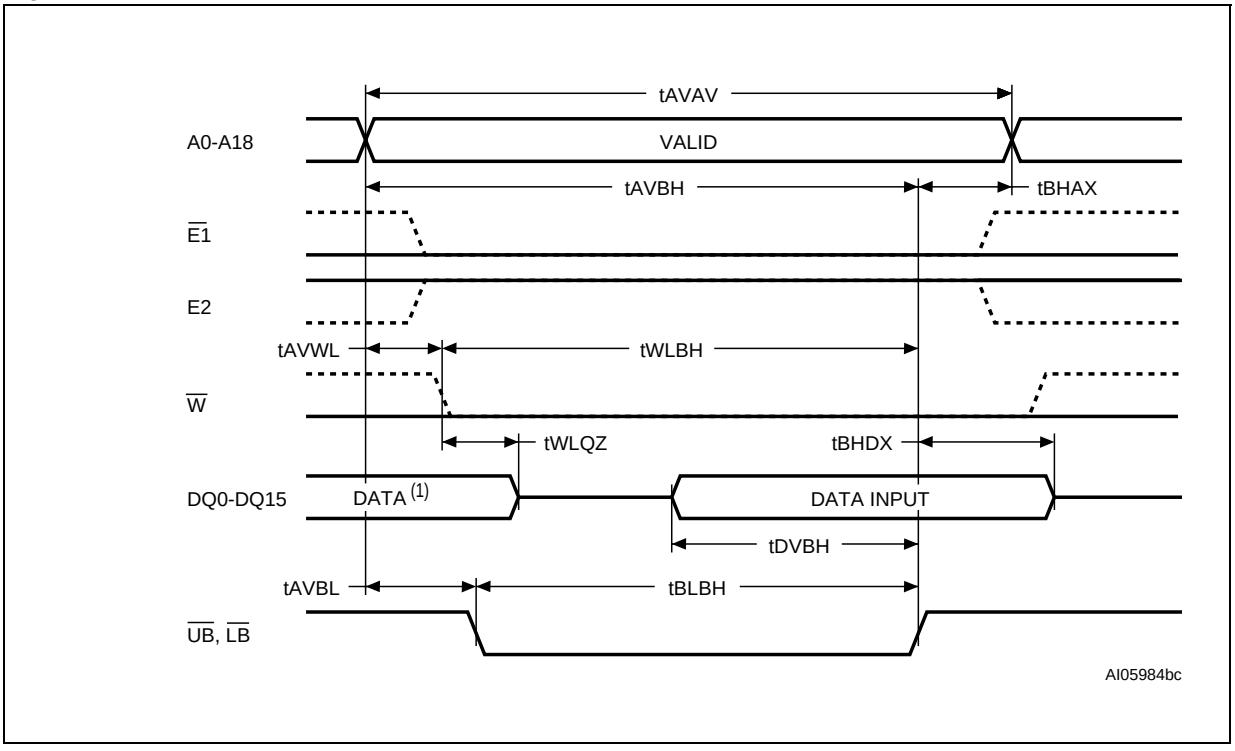


Figure 12. $\overline{UB}$/$\overline{LB}$ Controlled, Write AC Waveforms



Note: 1. During this period DQ0-DQ15 are in output state and input signals should not be applied.

Table 8. Write Mode AC Characteristics

Symbol	Parameter		M68AW512D		Unit
			55	70	
t_{AVAV}	Write Cycle Time	Min	55	70	ns
t_{AVBH}	Address Valid to $\overline{LB}$, $\overline{UB}$ High	Min	45	60	ns
t_{AVBL}	Addess Valid to $\overline{LB}$, $\overline{UB}$ Low	Min	0	0	ns
t_{AVEH}	Address Valid to Chip Enable High	Min	45	60	ns
t_{AVEL}	Address valid to Chip Enable Low	Min	0	0	ns
t_{AVWH}	Address Valid to Write Enable High	Min	45	60	ns
t_{AVWL}	Address Valid to Write Enable Low	Min	0	0	ns
t_{BHAX}	$\overline{LB}$, $\overline{UB}$ High to Address Transition	Min	0	0	ns
t_{BHDX}	$\overline{LB}$, $\overline{UB}$ High to Input Transition	Min	0	0	ns
t_{BLBH}	$\overline{LB}$, $\overline{UB}$ Low to $\overline{LB}$, $\overline{UB}$ High	Min	45	60	ns
t_{BLEH}	$\overline{LB}$, $\overline{UB}$ Low to Chip Enable High	Min	45	60	ns
t_{BLWH}	$\overline{LB}$, $\overline{UB}$ Low to Write Enable High	Min	45	60	ns
t_{DVBH}	Input Valid to $\overline{LB}$, $\overline{UB}$ High	Min	25	30	ns
t_{DVEH}	Input Valid to Chip Enable High	Min	25	30	ns
t_{DVWH}	Input Valid to Write Enable High	Min	25	30	ns
t_{EHAX}	Chip Enable High to Address Transition	Min	0	0	ns
t_{EHDX}	Chip enable High to Input Transition	Min	0	0	ns
t_{ELBH}	Chip Enable Low to $\overline{LB}$, $\overline{UB}$ High	Min	45	60	ns
t_{ELEH}	Chip Enable Low to Chip Enable High	Min	45	60	ns
t_{ELWH}	Chip Enable Low to Write Enable High	Min	45	60	ns
t_{WHAX}	Write Enable High to Address Transition	Min	0	0	ns
t_{WHDX}	Write Enable High to Input Transition	Min	0	0	ns
t_{WHQX} (1)	Write Enable High to Output Transition	Min	5	5	ns
t_{WLBH}	Write Enable Low to $\overline{LB}$, $\overline{UB}$ High	Min	45	60	ns
t_{WLEH}	Write Enable Low to Chip Enable High	Min	45	60	ns
t_{WLQZ} (1,2,3)	Write Enable Low to Output Hi-Z	Max	20	20	ns
t_{WLWH}	Write Enable Low to Write Enable High	Min	40	50	ns

Note: 1. At any given temperature and voltage condition, t_{WLQZ} is less than t_{WHQX} for any given device.
2. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
3. Tested initially and after any design or process changes that may affect these parameters.

Figure 13. $\overline{E1}$ Controlled, Low V_{CC} Data Retention AC Waveforms

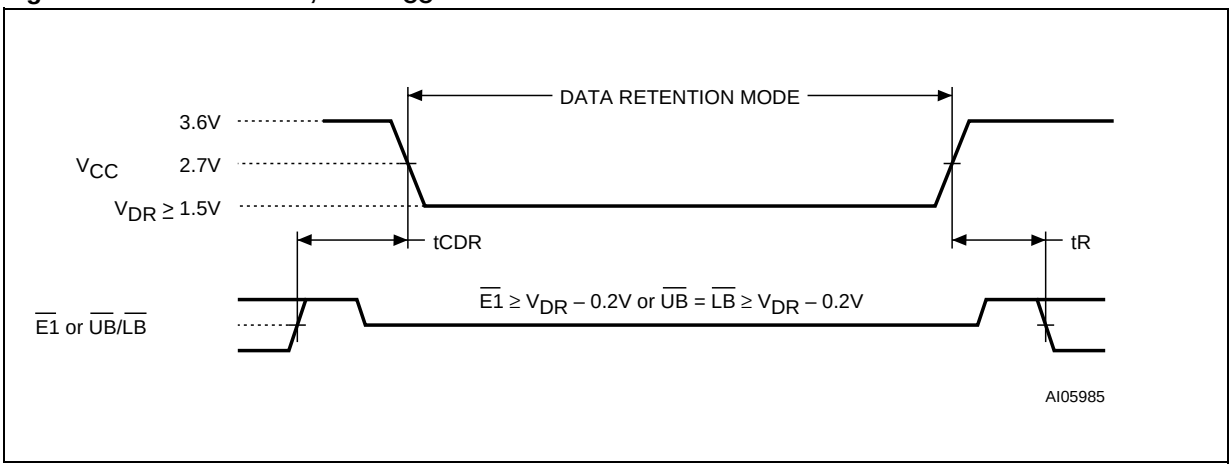


Figure 14. E2 Controlled, Low V_{CC} Data Retention AC Waveforms

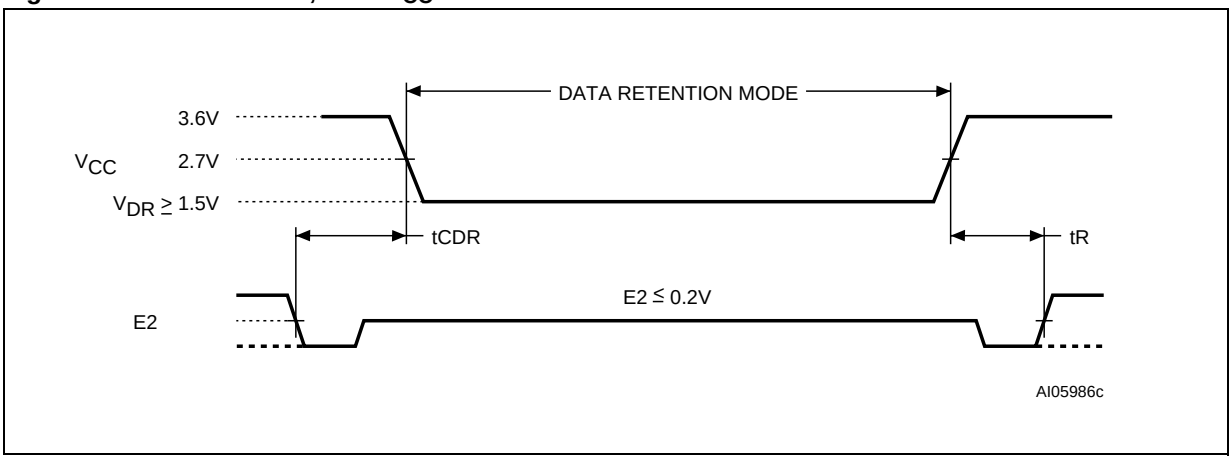


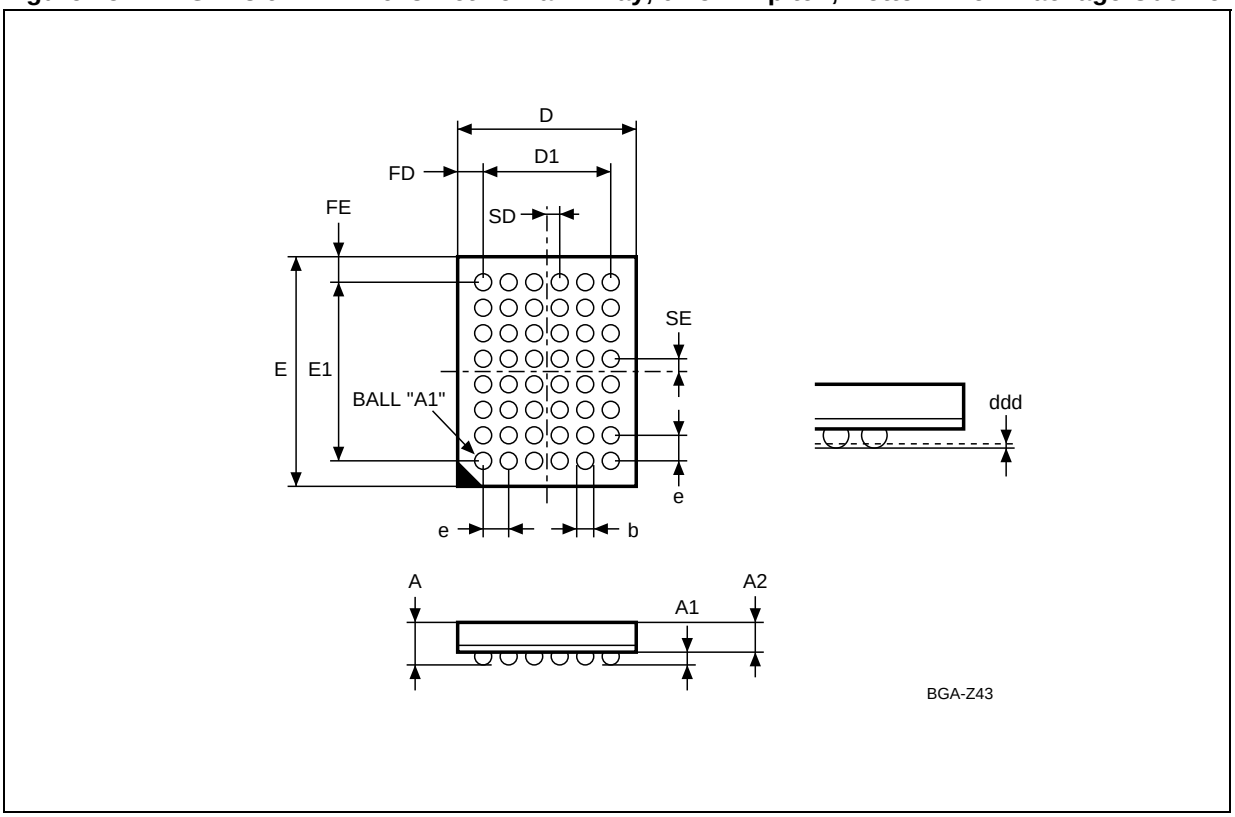
Table 9. Low V_{CC} Data Retention Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CCDR} (1)	Supply Current (Data Retention)	V_{CC} = 1.5V, $\overline{E1} \geq V_{CC}$ –0.2V or E2 ≤0.2V or $\overline{UB} = \overline{LB} \geq V_{CC}$ –0.2V, f = 0		30	µA
t_{CDR} (1,2)	Chip Deselected to Data Retention Time		0		ns
t_R (2)	Operation Recovery Time		t_{AVAV}		ns
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E1} \geq V_{CC}$ –0.2V or E2 ≤0.2V or $\overline{UB} = \overline{LB} \geq V_{CC}$ –0.2V, f = 0	1.5		V

Note: 1. All other Inputs at $V_{IH} \geq V_{CC}$ –0.2V or $V_{IL} \leq$0.2V.
2. Tested initially and after any design or process that may affect these parameters. t_{AVAV} is Read cycle time.
3. No input may exceed V_{CC} +0.2V.

PACKAGE MECHANICAL

Figure 15. TFBGA48 6x7mm - 6x8 Active Ball Array, 0.75mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 10. TFBGA48 6x7mm - 6x8 Active Ball Array, 0.75mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.250	0.400		0.0098	0.0157
A2	0.790			0.0311		
b	0.400	0.350	0.450	0.0157	0.0138	0.0177
D	6.000	5.900	6.100	0.2362	0.2323	0.2402
D1	3.750			0.1476		
ddd			0.100			0.0039
E	7.000	6.900	7.100	0.2756	0.2717	0.2795
E1	5.250			0.2067		
e	0.750	–	–	0.0295	–	–
FD	1.125			0.0443		
FE	0.875			0.0344		
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

PART NUMBERING

Table 11. Ordering Information Scheme

Example: M68AW512 D L 55 ZB 6 T

Device Type
M68

Mode
A = Asynchronous

Operating Voltage
W = 2.7 to 3.6V

Array Organization
512 = 8 Mbit (512K x16)

Option 1
D = 2 Chip Enable; Write and Standby from $\overline{UB}$ and $\overline{LB}$

Option 2
L = L-Die
N = N-Die

Speed Class
55 = 55ns
70 = 70ns

Package
ZB = TFBGA48: 0.75mm pitch

Operative Temperature
1 = 0 to 70°C
6 = –40 to 85°C

Shipping
T = Tape & Reel Packing

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 12. Document Revision History

Date	Version	Revision Details
July 2001	-01	First Issue
06-Feb-2002	-02	70ns Speed Class added, Commercial Temperature Range added
14-Mar-2002	-03	Document status moved to Datasheet Tables 2, 7 and 9 clarified Figures 8, 9, 10, 11 and 12 clarified
17-Jun-2002	-04	Block Diagram clarified (Figure 4) I_{SB} clarified (Table 6) I_{CCDR} clarified (Table 9)
09-Oct-2002	4.1	Revision numbering modified: a minor revision will be indicated by incrementing the digit after the dot, and a major revision, by incrementing the digit before the dot (revision version 04 equals 4.0). Part number modified.
25-Nov-2002	4.2	Figure 14, E2 Controlled, Low VCC Data Retention AC Waveforms, corrected.
01-Jul-2003	4.3	TFBGA package changed to 6x7mm on page 1 (but not on page 15) Values of I_{CC1}, I_{SB} and I_{CCDR} changed.
16-Feb-2004	5.0	Datasheet Status changed to “Preliminary Data”. I_{CC1} and I_{SB} updated in Table 6.DC Characteristics.
23-Sep-2004	6.0	t_{PU} ad t_{PD} updated in Table 7.