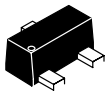
Dual transil array for ESD protection

The LESD6V8T1G is a dual monolithic voltage suppressor designed to protect components which are connected to data and transmission lines against ESD. It clamps the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transients. It can also work as bidirectionnal suppressor by connecting only pin1 and 2.

LESD6V8T1G



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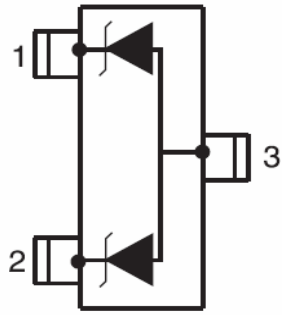


Specification Features

- Low Leakage < 1 μA @ 5 Volt
- Breakdown Voltage: 6.4 – 7.2 Volt @ 5 mA
- Low Capacitance (40 pF typical)
- ESD Protection Meeting 61000–4–2 Level 4 and 16 kV Human Body Model
- We declare that the material of product compliance with RoHS requirements.

Mechanical Characteristics

- Void Free, Transfer–Molded, Thermosetting Plastic Case
- Corrosion Resistant Finish, Easily Solderable
- Package Designed for Optimal Automated Board Assembly
- Small Package Size for High Density Applications

ORDERING INFORMATION

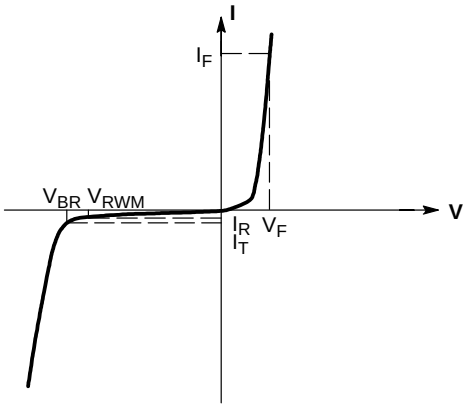
Device	Marking	Shipping
LESD6V8T1G	68	3000/Tape & Reel

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Power Dissipation @ 8 x 20 μs (Note 1)	P_{pk}	75	Watts
Steady State Power Dissipation (Note 2)	P_D	385	mW
Thermal Resistance – Junction to Ambient Derate Above 25°C	$R_{\theta JA}$	328 3.0	°C/W mW/°C
Maximum Junction Temperature	T_{Jmax}	150	°C
Operating Junction and Storage Temperature Range	T_J, T_{stg}	–55 to +150	°C
ESD Discharge MIL STD 883C – Method 3015–6 IEC61000–4–2, Air Discharge IEC61000–4–2, Contact Discharge	V_{PP}	 16 16 8	kV
Lead Solder Temperature (10 seconds duration)	T_L	260	°C

1. Per Waveform Figure 1
2. Mounted on FR–5 Board = 1.0 X 0.75 X 0.062 in.

LESD6V8T1G



V–I Curve

ELECTRICAL CHARACTERISTICS

Device	Breakdown Voltage V_{BR} @ 5 mA (Volts)			Leakage Current I_{RM} @ V_{RWM} = 5 V	Typical Capacitance @ 0 V Bias	Max V_F @ I_F = 10 mA	Max Z_Z @ 5 mA	Max Z_{ZK} @ 0.5 mA
	Min	Nom	Max	(μA)	(pF)	(V)	(Ω)	(Ω)
LESD6V8T1G	6.4	6.8	7.2	1.0	40	1.25	30	300

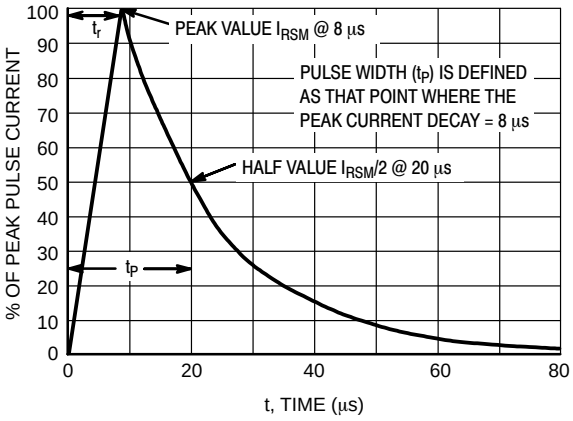


Figure 1. 8 × 20 μs Pulse Waveform

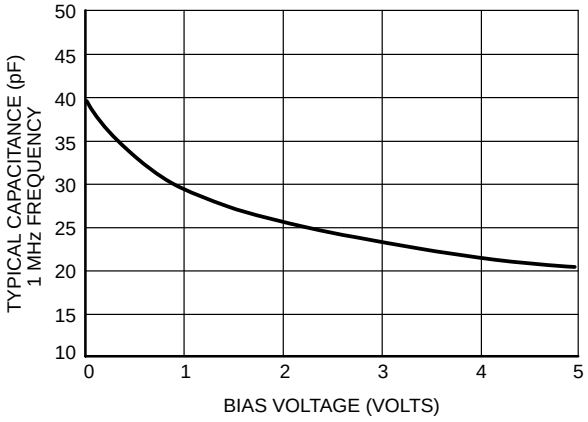


Figure 2. Capacitance

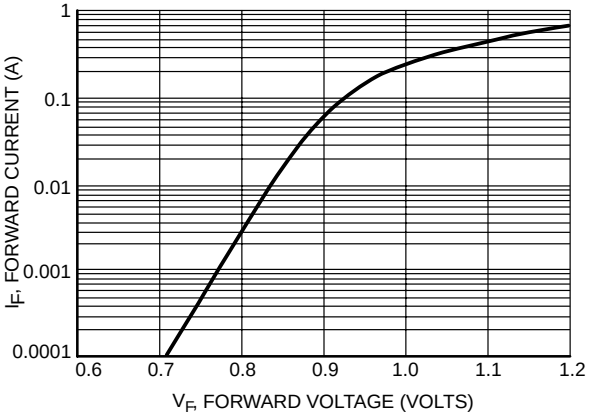


Figure 3. Forward Voltage

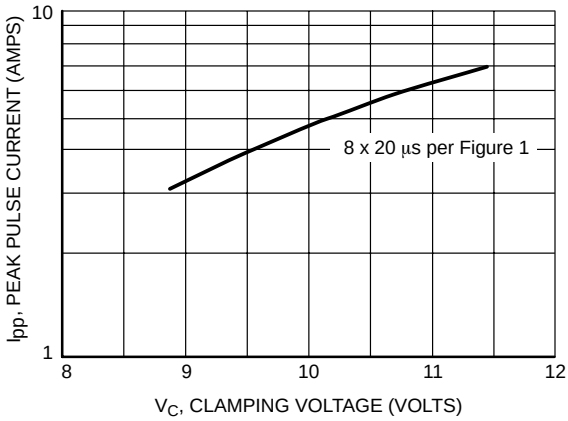


Figure 4. Clamping Voltage versus Peak Pulse Current

LESD6V8T1G

PACKAGE DIMENSIONS

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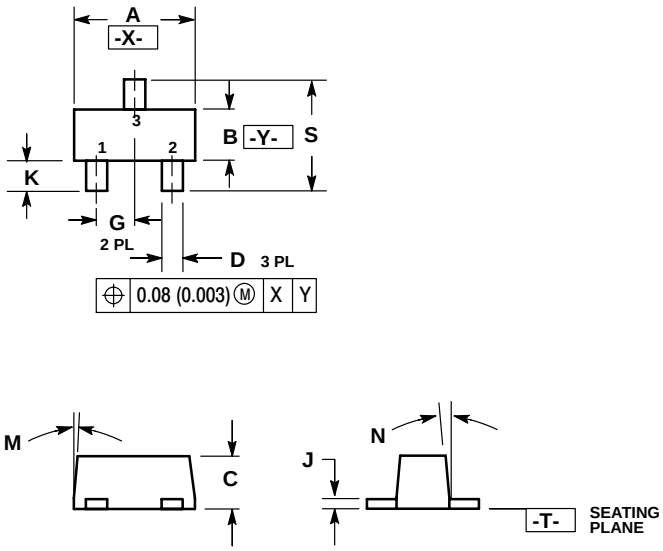
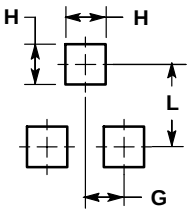


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C-01 OBSOLETE, NEW STANDARD 463C-02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067



RECOMMENDED PATTERN OF SOLDER PADS