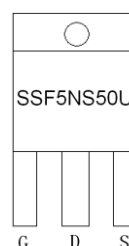
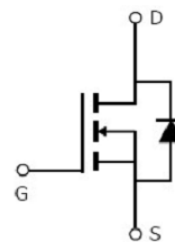


Main Product Characteristics:

V_{DSS}	500V
$R_{DS(on)}$	0.55 Ω (typ.)
I_D	5A ①


TO-220

Marking and pin Assignment

Schematic diagram
Features and Benefits:

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance


Description:

The SSF5NS50U series MOSFETs is a new technology, which combines an innovative super junction technology and advance process. This new technology achieves low Rdson, energy saving, high reliability and uniformity, superior power density and space saving.

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V	5 ①	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V	3.2 ①	
I_{DM}	Pulsed Drain Current ②	15	
P_D @TC = 25°C	Power Dissipation ③	62	W
	Linear Derating Factor	0.5	W/°C
V_{DS}	Drain-Source Voltage	500	V
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy @ L=38.6mH	111	mJ
I_{AS}	Avalanche Current @ L=38.6mH	2.4	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

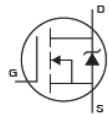
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	2.0	$^{\circ}C/W$
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ④	—	62	$^{\circ}C/W$

Electrical Characterizes @ $T_A=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	0.55	0.65	Ω	$V_{GS}=10V, I_D = 1A$ $T_J = 125^{\circ}C$
		—	1.16	—		
		—	0.58	0.75	Ω	$V_{GS}=10V, I_D = 2.8A$ $T_J = 125^{\circ}C$
		—	1.26	—		
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$ $T_J = 125^{\circ}C$
		—	2.4	—		
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 500V, V_{GS} = 0V$ $T_J = 125^{\circ}C$
		—	—	50		
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 30V$ $V_{GS} = -30V$
		—	—	-100		
Q_g	Total gate charge	—	15	—	nC	$I_D = 2.3A,$ $V_{DS}=400V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge	—	1.8	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	8.1	—		
$t_{d(on)}$	Turn-on delay time	—	8.7	—	ns	$V_{GS}=10V, V_{DS} =400V,$ $R_{GEN}=5.3\Omega, I_D =2.$
t_r	Rise time	—	5.4	—		
$t_{d(off)}$	Turn-Off delay time	—	22	—		
t_f	Fall time	—	10	—		
C_{iss}	Input capacitance	—	332	—	pF	$V_{GS} = 0V$ $V_{DS} = 100V$ $f = 1MHz$
C_{oss}	Output capacitance	—	21	—		
C_{rss}	Reverse transfer capacitance	—	3.5	—		

Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	15	A	
V_{SD}	Diode Forward Voltage	—	0.83	1.2	V	$I_S=2.8A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	130	—	nS	$T_J = 25^{\circ}C, I_F = 2.3A,$
Q_{rr}	Reverse Recovery Charge	—	706	—	nC	$di/dt = 100A/\mu s$

Test circuits and Waveforms

EAS Test Circuit:

Gate charge test circuit:

Switching Time Test Circuit:

Switching Waveforms:


Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Typical electrical and thermal characteristics

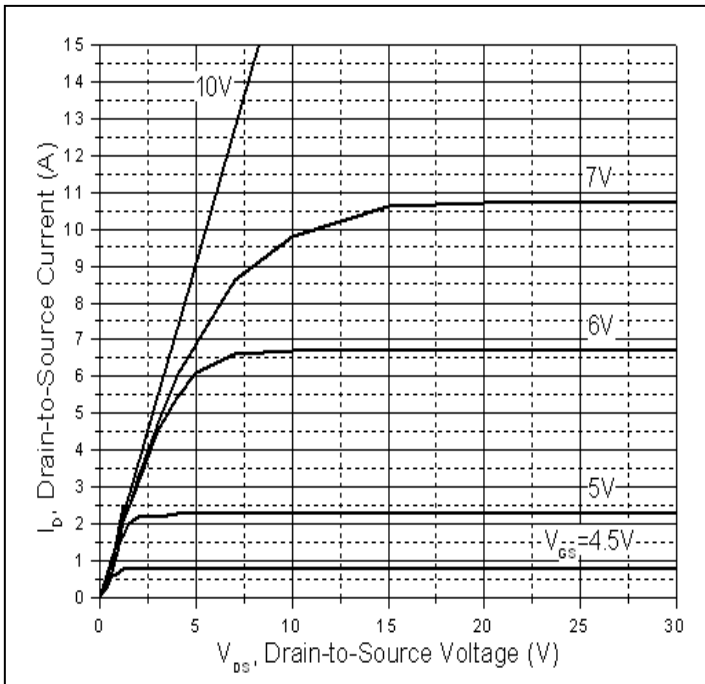


Figure 1: Typical Output Characteristics

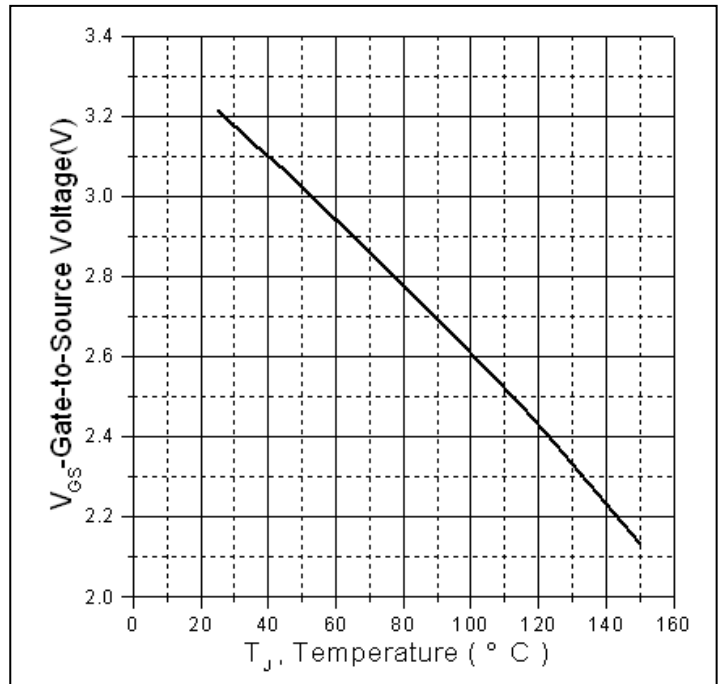


Figure 2. Gate to source cut-off voltage

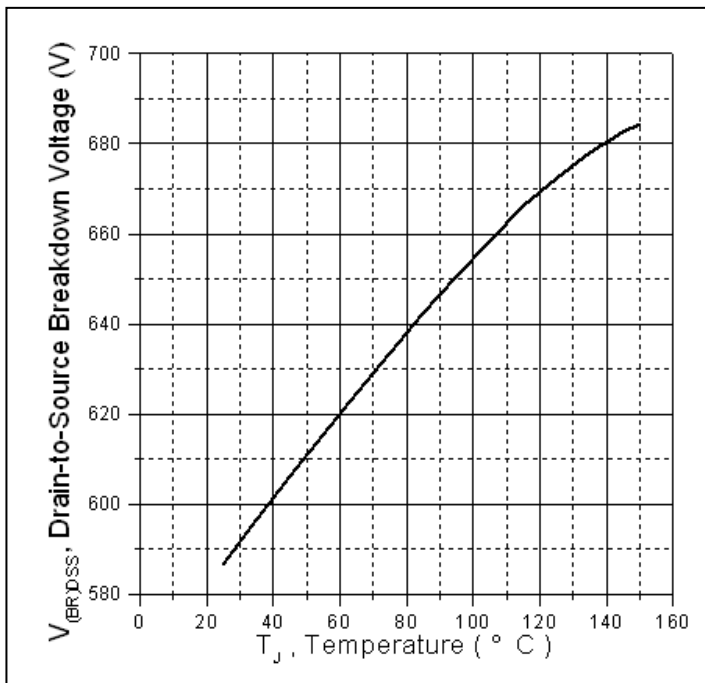


Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature

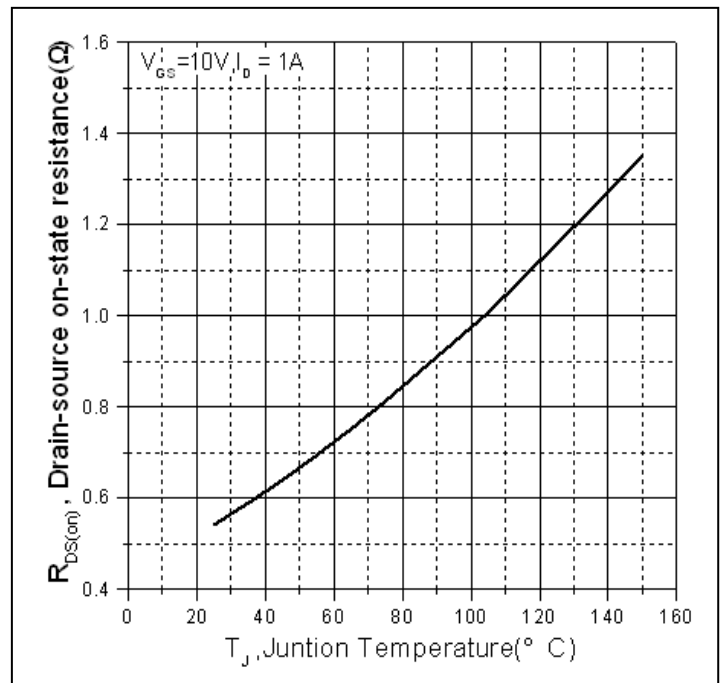


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

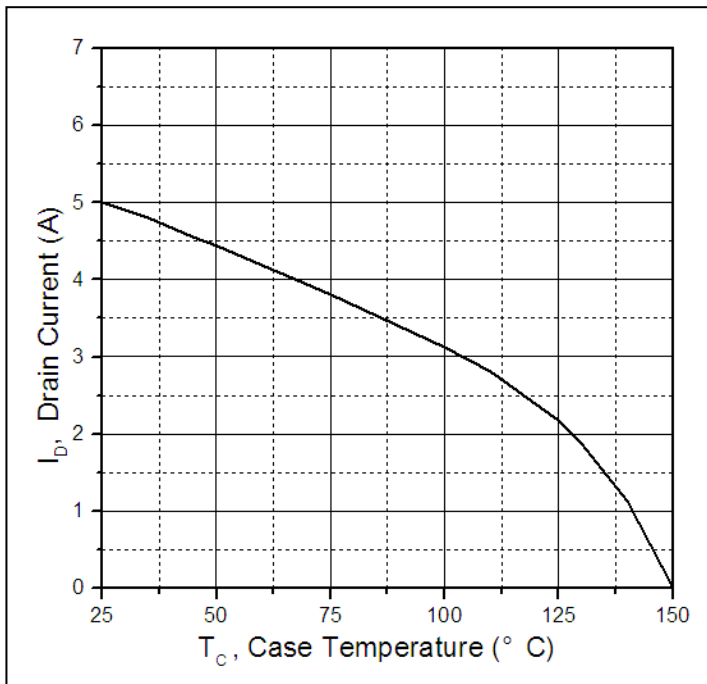


Figure 5. Maximum Drain Current Vs. Case Temperature

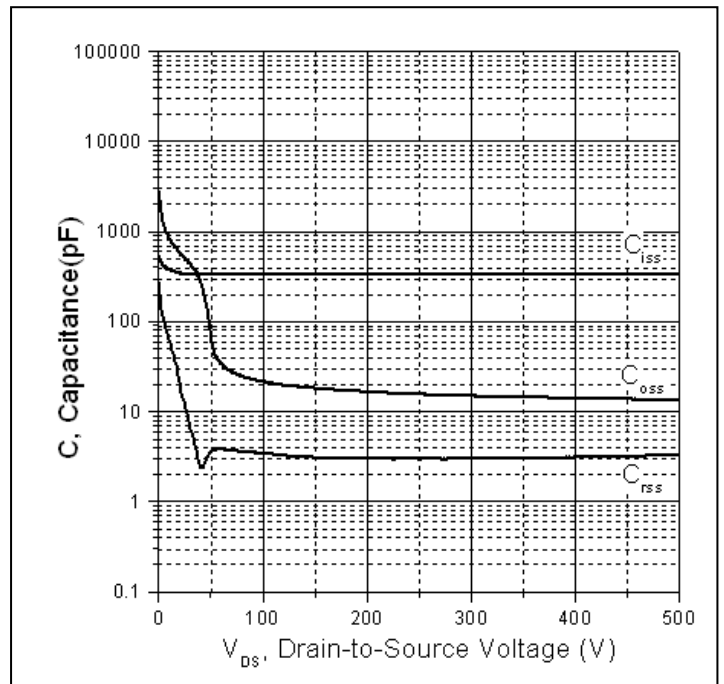


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

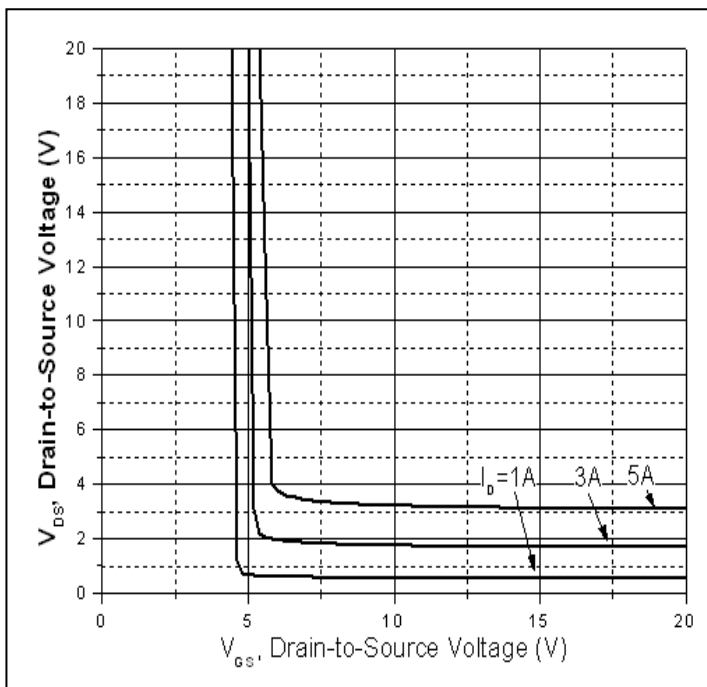


Figure 7. Drain-to-Source Voltage Vs. Gate-to-Source Voltage

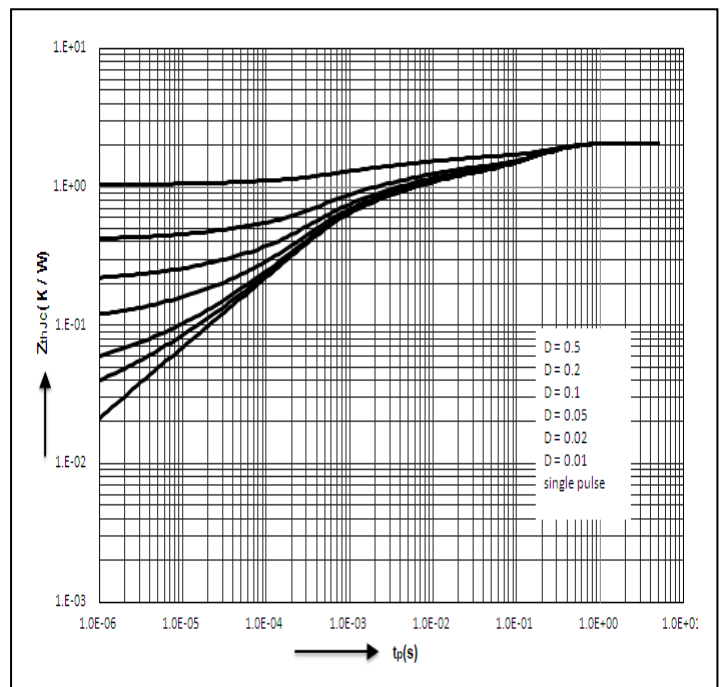
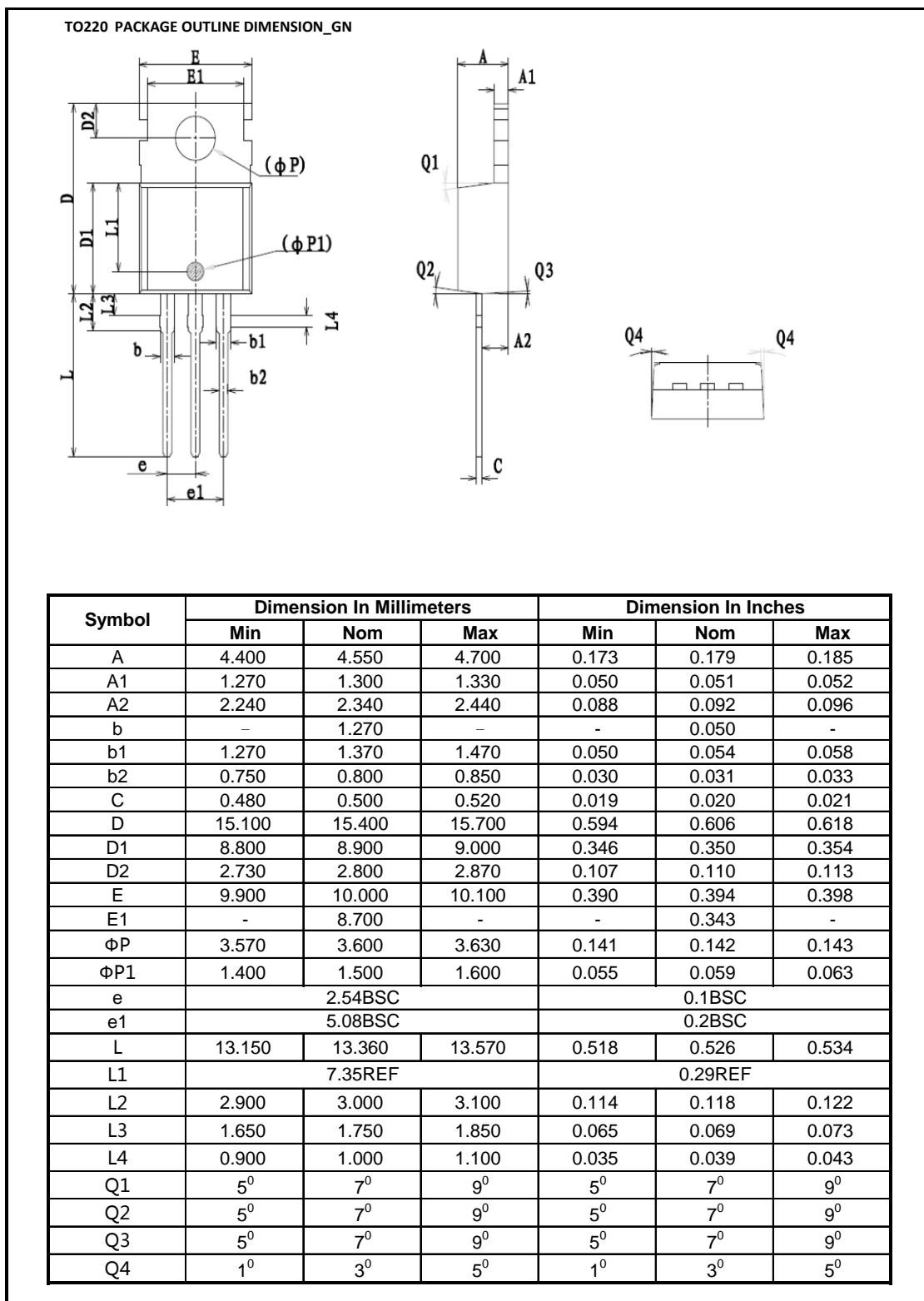


Figure 8. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data:


Ordering and Marking Information
Device Marking: SSF5NS50U

Package (Available)
TO-220
Operating Temperature Range
C : -55 to 150 °C

Devices per Unit

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-220	50	20	1000	6	6000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T _j =125°C to 150°C @ 80% of Max V _{DSS} /V _{CES} /VR	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T _j =150°C @ 100% of Max V _{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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