

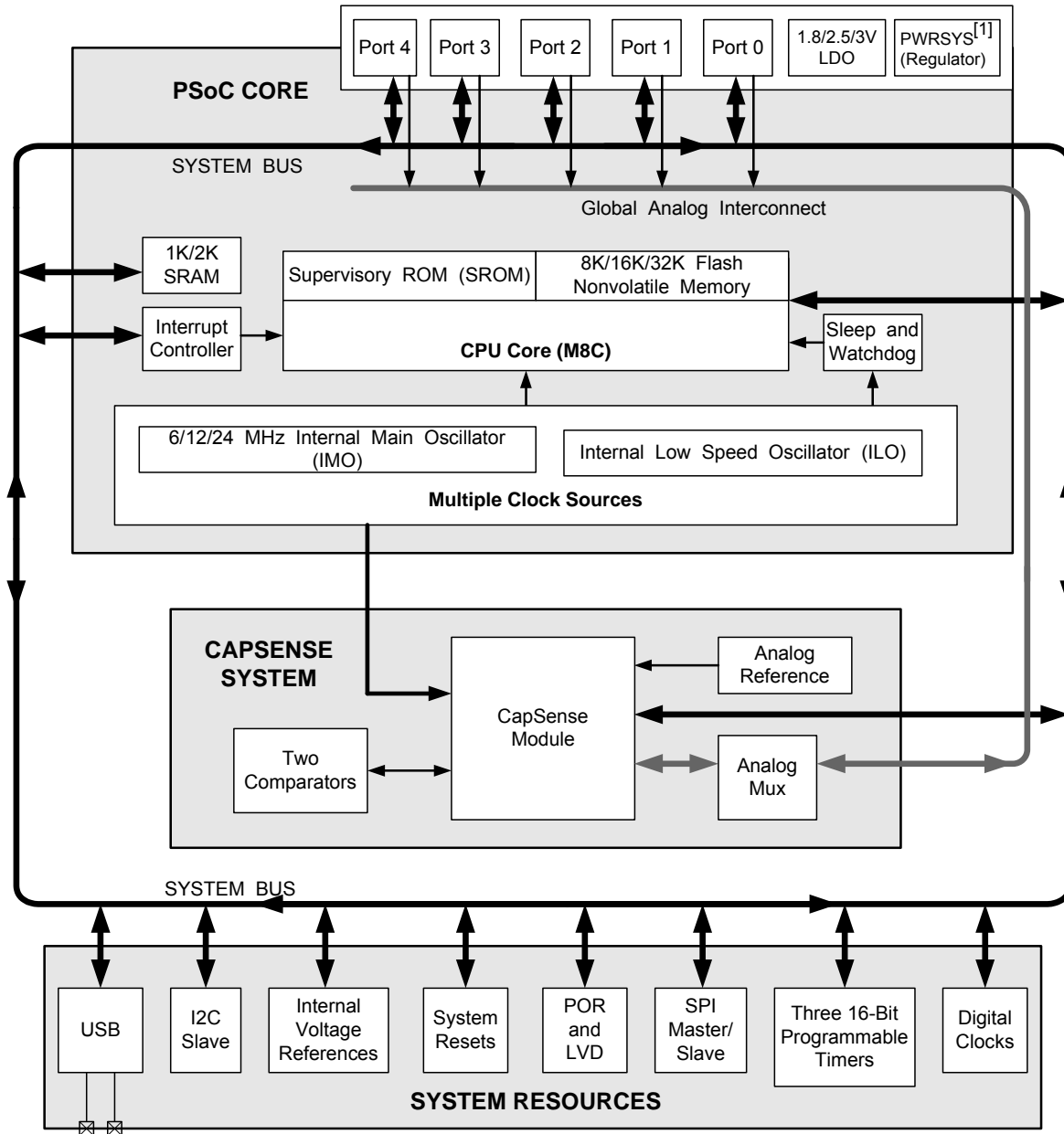
1.8 V Programmable CapSense[®] Controller with SmartSense[™] Auto-tuning 1–33 Buttons, 0–6 Sliders

Features

- Low power CapSense[®] block with SmartSense Auto-tuning
 - Patented CSA_EMC, CSD sensing algorithms
 - SmartSense_EMC Auto-Tuning
 - Sets and maintains optimal sensor performance during run time
 - Eliminates system tuning during development and production
 - Compensates for variations in manufacturing process Low average power consumption – 28 μ A/sensor in run time (wake-up and scan once every 125 ms)
- Powerful Harvard-architecture processor
 - M8C CPU with a max speed of 24 MHz
- Operating Range: 1.71 V to 5.5 V
 - Standby Mode 1.1 μ A (Typ)
 - Deep Sleep 0.1 μ A (Typ)
- Operating Temperature range: –40 °C to +85 °C
- Flexible on-chip memory
 - 8 KB flash, 1 KB SRAM
 - 16 KB flash, 2 KB SRAM
 - 32 KB flash, 2 KB SRAM
 - Read while Write with EEPROM emulation
 - 50,000 flash erase/write cycles
 - In-system programming simplifies manufacturing process
- Four Clock Sources
 - Internal main oscillator (IMO): 6/12/24 MHz
 - Internal low-speed oscillator (ILO) at 32 kHz for watchdog and sleep timers
 - External 32 KHz Crystal Oscillator
 - External Clock Input
- Programmable pin configurations
 - Up to 36 general-purpose I/Os (GPIOs) configurable as buttons or sliders
 - Dual mode GPIO (Analog inputs and Digital I/O supported)
 - High sink current of 25 mA per GPIO
 - Max sink current 120 mA for all GPIOs
 - Source Current
 - 5 mA on ports 0 and 1
 - 1 mA on ports 2,3 and 4
 - Configurable internal pull-up, high-Z and open drain modes
 - Selectable, regulated digital I/O on port 1
 - Configurable input threshold on port 1
- Versatile Analog functions
 - Internal analog bus supports connection of multiple sensors to form ganged proximity sensor
 - Internal Low-Dropout voltage regulator for high power supply rejection ratio (PSRR)
- Full-Speed USB
 - 12 Mbps USB 2.0 compliant
- Additional system resources
 - I2C Slave:
 - Selectable to 50 kHz, 100 kHz, or 400 kHz
 - Configurable up to 12 MHz SPI master and slave
 - Three 16-bit timers
 - Watchdog and sleep timers
 - Integrated supervisory circuit
 - 10-bit incremental analog-to-digital converter (ADC) with internal voltage reference
 - Two general-purpose high speed, low power analog comparators
- Complete development tools
 - Free development tool (PSoC Designer[™])
- Sensor and Package options
 - 10 Sensors – QFN 16, 24
 - 16 Sensors – QFN 24
 - 22 / 25 Sensors – QFN 32
 - 24 Sensors - WLCSP 30
 - 31 Sensors – SSOP 48
 - 33 Sensors – QFN 48

Errata: For information on silicon errata, see “Errata” on page 45. Details include trigger conditions, devices affected, and proposed workaround

Logic Block Diagram



Note

1. Internal voltage regulator for internal circuitry

Contents

| | | | |
|--|-----------|--|-----------|
| PSoC® Functional Overview | 4 | DC I2C Specifications | 26 |
| PSoC Core | 4 | DC Reference Buffer Specifications | 26 |
| CapSense System | 4 | DC IDAC Specifications | 26 |
| Additional System Resources | 5 | AC Chip-Level Specifications | 27 |
| Getting Started | 6 | AC GPIO Specifications | 28 |
| CapSense Design Guides | 6 | AC Comparator Specifications | 29 |
| Silicon Errata | 6 | AC External Clock Specifications | 29 |
| Development Kits | 6 | AC Programming Specifications | 30 |
| Training | 6 | AC I2C Specifications | 31 |
| CYPros Consultants | 6 | Packaging Information | 34 |
| Solutions Library | 6 | Thermal Impedances | 37 |
| Technical Support | 6 | Capacitance on Crystal Pins | 37 |
| Development Tools | 7 | Solder Reflow Specifications | 37 |
| PSoC Designer Software Subsystems | 7 | Development Tool Selection | 38 |
| Designing with PSoC Designer | 8 | Software | 38 |
| Select User Modules | 8 | Development Kits | 38 |
| Configure User Modules | 8 | Evaluation Tools | 38 |
| Organize and Connect | 8 | Device Programmers | 38 |
| Generate, Verify, and Debug | 8 | Accessories (Emulation and Programming) | 39 |
| Pinouts | 9 | Third Party Tools | 39 |
| 16-pin QFN (10 Sensing Inputs) | 9 | Build a PSoC Emulator into Your Board | 39 |
| 24-pin QFN (17 Sensing Inputs) | 10 | Ordering Information | 40 |
| 24-pin QFN (15 Sensing Inputs (With USB)) | 11 | Ordering Code Definitions | 42 |
| 30-ball WLCSP (24 Sensing Inputs) | 12 | Acronyms | 43 |
| 32-pin QFN (25 Sensing Inputs) | 13 | Reference Documents | 43 |
| 32-pin QFN (22 Sensing Inputs (With USB)) | 14 | Document Conventions | 43 |
| 48-pin SSOP (31 Sensing Inputs) | 15 | Units of Measure | 43 |
| 48-pin QFN (33 Sensing Inputs) | 16 | Numeric Naming | 44 |
| 48-pin QFN (33 Sensing Inputs (With USB)) | 17 | Glossary | 44 |
| 48-pin QFN (OCD) (33 Sensing Inputs) | 18 | Errata | 45 |
| Electrical Specifications | 19 | Qualification Status | 45 |
| Absolute Maximum Ratings | 19 | Errata Summary | 45 |
| Operating Temperature | 19 | Document History Page | 48 |
| DC Chip-Level Specifications | 20 | Sales, Solutions, and Legal Information | 51 |
| DC GPIO Specifications | 21 | Worldwide Sales and Design Support | 51 |
| DC Analog Mux Bus Specifications | 23 | Products | 51 |
| DC Low Power Comparator Specifications | 23 | PSoC® Solutions | 51 |
| Comparator User Module Electrical Specifications | 24 | Cypress Developer Community | 51 |
| ADC Electrical Specifications | 24 | Technical Support | 51 |
| DC POR and LVD Specifications | 25 | | |
| DC Programming Specifications | 25 | | |

PSoC[®] Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the [Logic Block Diagram on page 2](#), consists of three main areas:

- The Core
- CapSense Analog System
- System Resources (including a full-speed USB port).

A common, versatile bus allows connection between I/O and the analog system.

Each CY8C20XX6A/S PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 36 GPIO are also included. The GPIO provides access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1 V or 1.2 V analog reference, which together support capacitive sensing of up to 33 inputs [2]. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

SmartSense

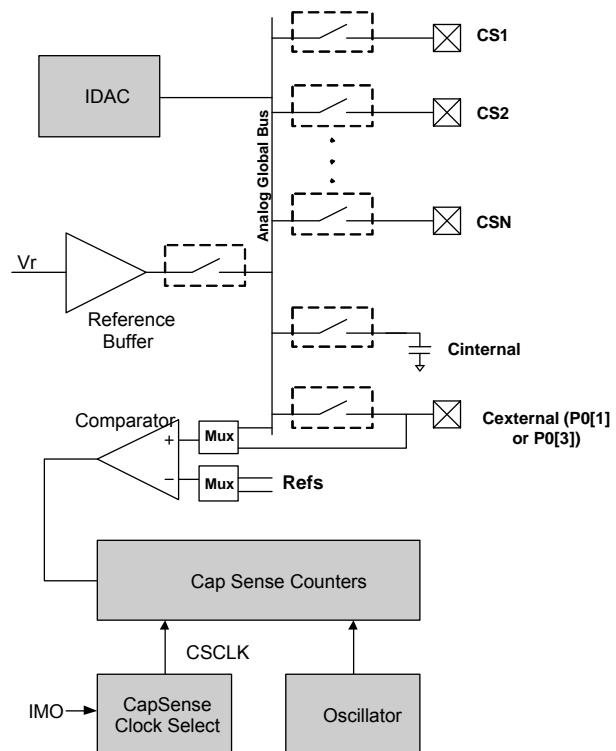
SmartSense is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easy to use and provides a robust noise immunity. It is the only auto-tuning solution that establishes, monitors, and maintains all

required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.

SmartSense_EMC

In addition to the SmartSense auto tuning algorithm to remove manual tuning of CapSense applications, SmartSense_EMC user module incorporates a unique algorithm to improve robustness of capacitive sensing algorithm/circuit against high frequency conducted and radiated noise. Every electronic device must comply with specific limits for radiated and conducted external noise and these limits are specified by regulatory bodies (for example, FCC, CE, U/L and so on). A very good PCB layout design, power supply design and system design is a mandatory for a product to pass the conducted and radiated noise tests. An ideal PCB layout, power supply design or system design is not often possible because of cost and form factor limitations of the product. SmartSense_EMC with superior noise immunity is well suited and handy for such applications to pass radiated and conducted noise test.

Figure 1. CapSense System Block Diagram



Note

2. 36 GPIOs = 33 pins for capacitive sensing + 2 pins for I²C + 1 pin for modulator capacitor.

Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

Additional System Resources

System resources provide additional capability, such as configurable USB and I²C slave, SPI master/slave

communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

These system resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I²C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on-reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the [Technical Reference Manual](#) for the CY8C20XX6A/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

CapSense Design Guides

Design Guides are an excellent introduction to the wide variety of possible CapSense designs. They are located at www.cypress.com/go/CapSenseDesignGuides.

Refer Getting Started with CapSense design guide for information on CapSense design and CY8C20XX6A/H/AS CapSense® Design Guide for specific information on CY8C20XX6A/AS CapSense controllers.

Silicon Errata

Errata documents known issues with silicon including errata trigger conditions, scope of impact, available workarounds and silicon revision applicability. Refer to Silicon Errata for the PSoC® CY8C20x36A/46A/66A/96A/46AS/66AS/36H/46H families available at <http://www.cypress.com/?rID=56239> for errata information on CY8C20xx6A/AS/H family of device. Compare

errata document with datasheet for a complete functional description of device.

Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
 - Hardware and software I²C slaves and masters
 - Full-speed USB 2.0
 - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select [user modules](#).
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the

internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pinouts

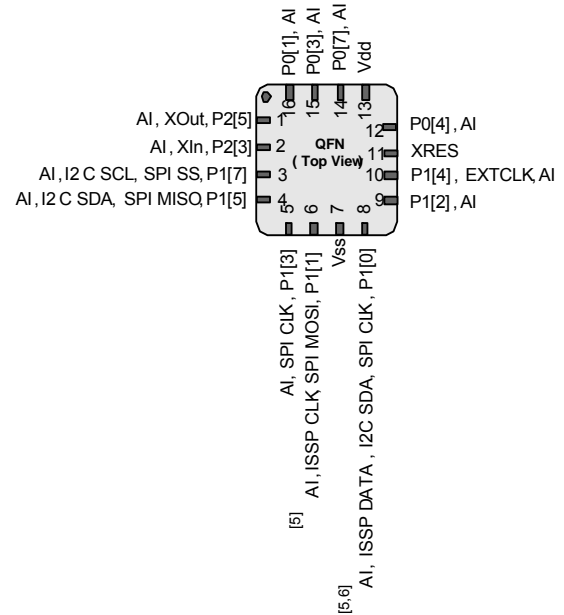
The CY8C20XX6A/S PSoC device is available in a variety of packages, which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

16-pin QFN (10 Sensing Inputs)^[3, 4]

Table 1. Pin Definitions – CY8C20236A, CY8C20246A, CY8C20246AS PSoC Device

| Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|---|
| | Digital | Analog | | |
| 1 | I/O | I | P2[5] | Crystal output (XOut) |
| 2 | I/O | I | P2[3] | Crystal input (XIn) |
| 3 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 4 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 5 | IOHR | I | P1[3] | SPI CLK |
| 6 | IOHR | I | P1[1] | ISSP CLK ^[5] , I ² C SCL, SPI MOSI |
| 7 | Power | | V _{SS} | Ground connection |
| 8 | IOHR | I | P1[0] | ISSP DATA ^[5] , I ² C SDA, SPI CLK ^[6] |
| 9 | IOHR | I | P1[2] | |
| 10 | IOHR | I | P1[4] | Optional external clock (EXTCLK) |
| 11 | Input | | XRES | Active high external reset with internal pull-down |
| 12 | IOH | I | P0[4] | |
| 13 | Power | | V _{DD} | Supply voltage |
| 14 | IOH | I | P0[7] | |
| 15 | IOH | I | P0[3] | Integrating input |
| 16 | IOH | I | P0[1] | Integrating input |

Figure 2. CY8C20236A, CY8C20246A, CY8C20246AS



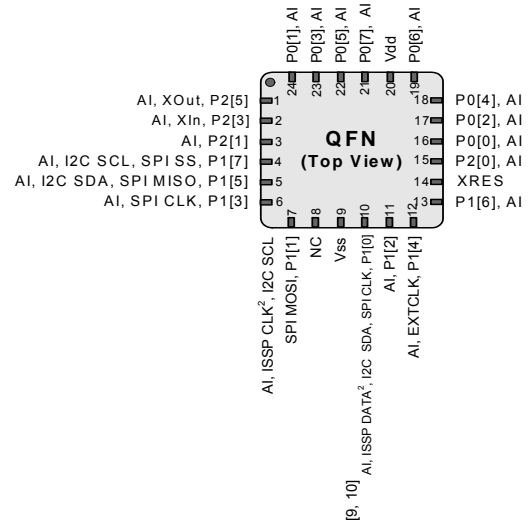
LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Notes

- 13 GPIOs = 10 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
- No Center Pad.
- On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- Alternate SPI clock.

24-pin QFN (17 Sensing Inputs) [7]
Table 2. Pin Definitions – CY8C20336A, CY8C20346A, CY8C20346AS [8]

| Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|--|
| | Digital | Analog | | |
| 1 | I/O | I | P2[5] | Crystal output (XOut) |
| 2 | I/O | I | P2[3] | Crystal input (XIn) |
| 3 | I/O | I | P2[1] | |
| 4 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 5 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 6 | IOHR | I | P1[3] | SPI CLK |
| 7 | IOHR | I | P1[1] | ISSP CLK ^[9] , I ² C SCL, SPI MOSI |
| 8 | | | NC | No connection |
| 9 | Power | | V _{SS} | Ground connection |
| 10 | IOHR | I | P1[0] | ISSP DATA ^[9] , I ² C SDA, SPI CLK ^[10] |
| 11 | IOHR | I | P1[2] | |
| 12 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 13 | IOHR | I | P1[6] | |
| 14 | Input | | XRES | Active high external reset with internal pull-down |
| 15 | I/O | I | P2[0] | |
| 16 | IOH | I | P0[0] | |
| 17 | IOH | I | P0[2] | |
| 18 | IOH | I | P0[4] | |
| 19 | IOH | I | P0[6] | |
| 20 | Power | | V _{DD} | Supply voltage |
| 21 | IOH | I | P0[7] | |
| 22 | IOH | I | P0[5] | |
| 23 | IOH | I | P0[3] | Integrating input |
| 24 | IOH | I | P0[1] | Integrating input |
| CP | Power | | V _{SS} | Center pad must be connected to ground |

Figure 3. CY8C20336A, CY8C20346A, CY8C20346AS


LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Notes

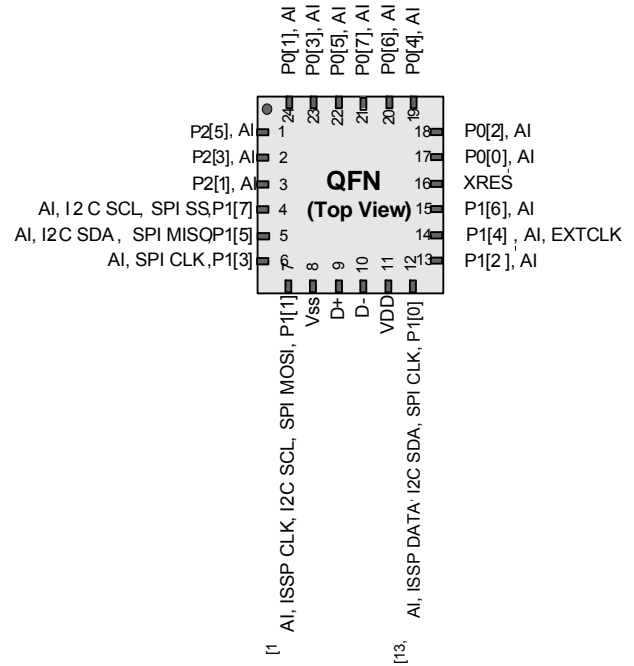
- 20 GPIOs = 17 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
- The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- Alternate SPI clock.

24-pin QFN (15 Sensing Inputs (With USB)) ^[11]

Table 3. Pin Definitions – CY8C20396A ^[12]

| Pin No. | Type | | Name | Description |
|---------|-------------|--------|-----------------|---|
| | Digital | Analog | | |
| 1 | I/O | I | P2[5] | |
| 2 | I/O | I | P2[3] | |
| 3 | I/O | I | P2[1] | |
| 4 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 5 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 6 | IOHR | I | P1[3] | SPI CLK |
| 7 | IOHR | I | P1[1] | ISSP CLK ^[13] , I ² C SCL, SPI MOSI |
| 8 | Power | | V _{SS} | Ground |
| 9 | I/O | I | D+ | USB D+ |
| 10 | I/O | I | D- | USB D- |
| 11 | Power | | V _{DD} | Supply |
| 12 | IOHR | I | P1[0] | ISSP DATA ^[13] , I ² C SDA, SPI CLK ^[14] |
| 13 | IOHR | I | P1[2] | |
| 14 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 15 | IOHR | I | P1[6] | |
| 16 | RESET INPUT | | XRES | Active high external reset with internal pull-down |
| 17 | IOH | I | P0[0] | |
| 18 | IOH | I | P0[2] | |
| 19 | IOH | I | P0[4] | |
| 20 | IOH | I | P0[6] | |
| 21 | IOH | I | P0[7] | |
| 22 | IOH | I | P0[5] | |
| 23 | IOH | I | P0[3] | Integrating input |
| 24 | IOH | I | P0[1] | Integrating input |
| CP | Power | | V _{SS} | Center pad must be connected to Ground |

Figure 4. CY8C20396A



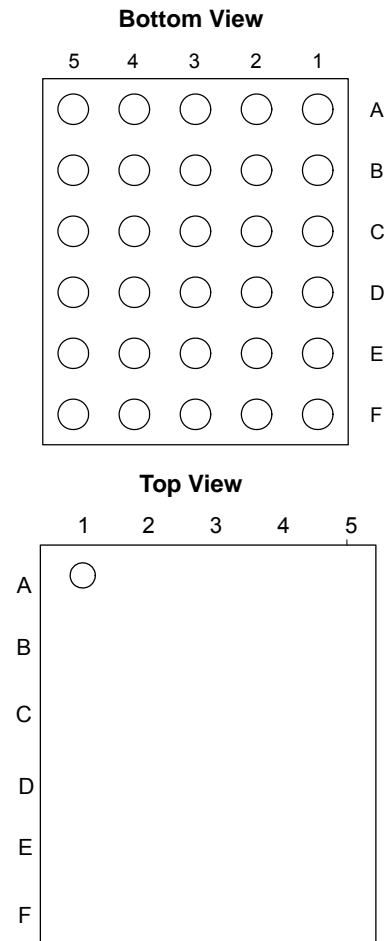
LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Notes

- 11. 20 GPIOs = 15 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
- 12. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- 13. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- 14. Alternate SPI clock.

30-ball WLCSP (24 Sensing Inputs) ^[15]
Table 4. Pin Definitions – CY8C20766A, CY8C20746A 30-ball WLCSP

| Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|---|
| | Digital | Analog | | |
| A1 | IOH | I | P0[2] | |
| A2 | IOH | I | P0[6] | |
| A3 | Power | | V _{DD} | Supply voltage |
| A4 | IOH | I | P0[1] | Integrating Input |
| A5 | I/O | I | P2[7] | |
| B1 | I/O | I | P2[6] | |
| B2 | IOH | I | P0[0] | |
| B3 | IOH | I | P0[4] | |
| B4 | IOH | I | P0[3] | Integrating Input |
| B5 | I/O | I | P2[5] | Crystal Output (Xout) |
| C1 | I/O | I | P2[2] | |
| C2 | I/O | I | P2[4] | |
| C3 | IOH | I | P0[7] | |
| C4 | IOH | I | P0[5] | |
| C5 | I/O | I | P2[3] | Crystal Input (Xin) |
| D1 | I/O | I | P2[0] | |
| D2 | I/O | I | P3[0] | |
| D3 | I/O | I | P3[1] | |
| D4 | I/O | I | P3[3] | |
| D5 | I/O | I | P2[1] | |
| E1 | Input | | XRES | Active high external reset with internal pull-down |
| E2 | IOHR | I | P1[6] | |
| E3 | IOHR | I | P1[4] | Optional external clock input (EXT CLK) |
| E4 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| E5 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| F1 | IOHR | I | P1[2] | |
| F2 | IOHR | I | P1[0] | ISSP DATA ^[16] , I ² C SDA, SPI CLK ^[17] |
| F3 | Power | | V _{SS} | Supply ground |
| F4 | IOHR | I | P1[1] | ISSP CLK ^[16] , I ² C SCL, SPI MOSI |
| F5 | IOHR | I | P1[3] | SPI CLK |

Figure 5. CY8C20766A 30-ball WLCSP

Notes

15. 27 GPIOs = 24 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.

16. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.

17. Alternate SPI clock.

32-pin QFN (25 Sensing Inputs) [18]

Table 5. Pin Definitions – CY8C20436A, CY8C20446A, CY8C20446AS, CY8C20466A, CY8C20466AS [19]

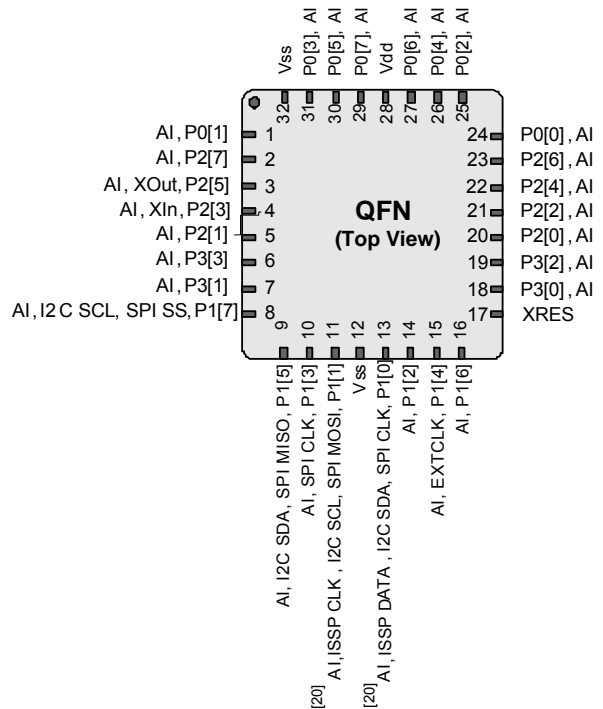
| Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|---|
| | Digital | Analog | | |
| 1 | IOH | I | P0[1] | Integrating input |
| 2 | I/O | I | P2[7] | |
| 3 | I/O | I | P2[5] | Crystal output (XOut) |
| 4 | I/O | I | P2[3] | Crystal input (XIn) |
| 5 | I/O | I | P2[1] | |
| 6 | I/O | I | P3[3] | |
| 7 | I/O | I | P3[1] | |
| 8 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 9 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 10 | IOHR | I | P1[3] | SPI CLK. |
| 11 | IOHR | I | P1[1] | ISSP CLK ^[20] , I ² C SCL, SPI MOSI. |
| 12 | Power | | V _{SS} | Ground connection. |
| 13 | IOHR | I | P1[0] | ISSP DATA ^[20] , I ² C SDA, SPI CLK ^[21] |
| 14 | IOHR | I | P1[2] | |
| 15 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 16 | IOHR | I | P1[6] | |
| 17 | Input | | XRES | Active high external reset with internal pull-down |
| 18 | I/O | I | P3[0] | |
| 19 | I/O | I | P3[2] | |
| 20 | I/O | I | P2[0] | |
| 21 | I/O | I | P2[2] | |
| 22 | I/O | I | P2[4] | |
| 23 | I/O | I | P2[6] | |
| 24 | IOH | I | P0[0] | |
| 25 | IOH | I | P0[2] | |
| 26 | IOH | I | P0[4] | |
| 27 | IOH | I | P0[6] | |
| 28 | Power | | V _{DD} | Supply voltage |
| 29 | IOH | I | P0[7] | |
| 30 | IOH | I | P0[5] | |
| 31 | IOH | I | P0[3] | Integrating input |
| 32 | Power | | V _{SS} | Ground connection |
| CP | Power | | V _{SS} | Center pad must be connected to ground |

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Notes

- 18. 28 GPIOs = 25 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
- 19. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- 20. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- 21. Alternate SPI clock.

Figure 6. CY8C20436A, CY8C20446A, CY8C20446AS, CY8C20466A, CY8C20466AS

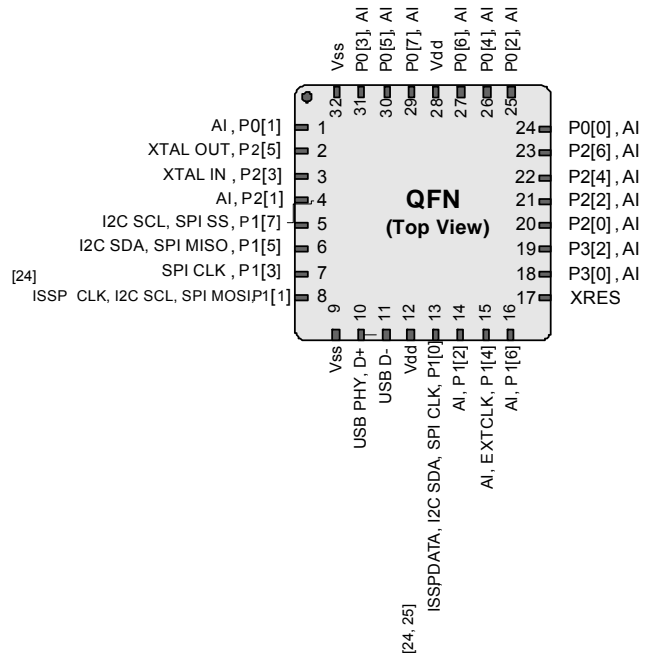


32-pin QFN (22 Sensing Inputs (With USB)) [22]

Table 6. Pin Definitions – CY8C20496A [23]

| Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|---|
| | Digital | Analog | | |
| 1 | IOH | I | P0[1] | Integrating Input |
| 2 | I/O | I | P2[5] | XTAL Out |
| 3 | I/O | I | P2[3] | XTAL In |
| 4 | I/O | I | P2[1] | |
| 5 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 6 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 7 | IOHR | I | P1[3] | SPI CLK |
| 8 | IOHR | I | P1[1] | ISSP CLK ^[24] , I ² C SCL, SPI MOSI |
| 9 | Power | | V _{SS} | Ground Pin |
| 10 | I | | D+ | USB D+ |
| 11 | | | D- | USB D- |
| 12 | Power | | V _{DD} | Power pin |
| 13 | IOHR | I | P1[0] | ISSP DATA ^[24] , I ² C SDA, SPI CLK ^[25] |
| 14 | IOHR | I | P1[2] | |
| 15 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 16 | IOHR | I | P1[6] | |
| 17 | Input | | XRES | Active high external reset with internal pull-down |
| 18 | I/O | I | P3[0] | |
| 19 | I/O | I | P3[2] | |
| 20 | I/O | I | P2[0] | |
| 21 | I/O | I | P2[2] | |
| 22 | I/O | I | P2[4] | |
| 23 | I/O | I | P2[6] | |
| 24 | IOH | I | P0[0] | |
| 25 | IOH | I | P0[2] | |
| 26 | IOH | I | P0[4] | |
| 27 | IOH | I | P0[6] | |
| 28 | Power | | V _{DD} | Power Pin |
| 29 | IOH | I | P0[7] | |
| 30 | IOH | I | P0[5] | |
| 31 | IOH | I | P0[3] | Integrating Input |
| 32 | Power | | V _{SS} | Ground Pin |

Figure 7. CY8C20496A



LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Notes

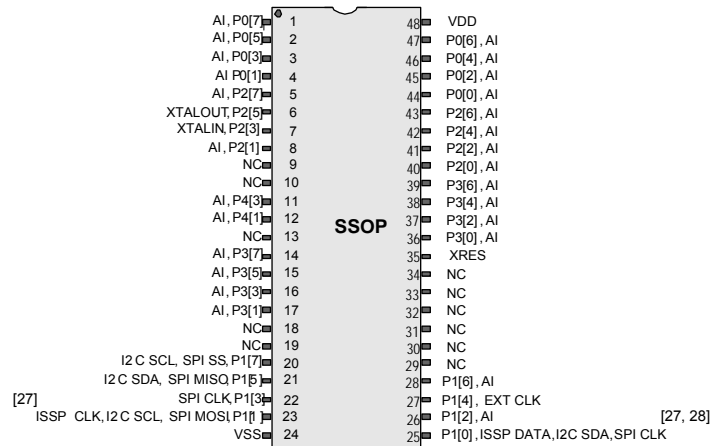
- 22. 27 GPIOs = 22 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
- 23. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- 24. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- 25. Alternate SPI clock.

48-pin SSOP (31 Sensing Inputs) [26]

Table 7. Pin Definitions – CY8C20536A, CY8C20546A, and CY8C20566A [27]

| Pin No. | Digital | Analog | Name | Description |
|---------|---------|--------|-----------------|---|
| 1 | IOH | I | P0[7] | |
| 2 | IOH | I | P0[5] | |
| 3 | IOH | I | P0[3] | Integrating Input |
| 4 | IOH | I | P0[1] | Integrating Input |
| 5 | I/O | I | P2[7] | |
| 6 | I/O | I | P2[5] | XTAL Out |
| 7 | I/O | I | P2[3] | XTAL In |
| 8 | I/O | I | P2[1] | |
| 9 | | | NC | No connection |
| 10 | | | NC | No connection |
| 11 | I/O | I | P4[3] | |
| 12 | I/O | I | P4[1] | |
| 13 | | | NC | No connection |
| 14 | I/O | I | P3[7] | |
| 15 | I/O | I | P3[5] | |
| 16 | I/O | I | P3[3] | |
| 17 | I/O | I | P3[1] | |
| 18 | | | NC | No connection |
| 19 | | | NC | No connection |
| 20 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 21 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 22 | IOHR | I | P1[3] | SPI CLK |
| 23 | IOHR | I | P1[1] | ISSP CLK ^[27] , I ² C SCL, SPI MOSI |
| 24 | | | V _{SS} | Ground Pin |
| 25 | IOHR | I | P1[0] | ISSP DATA ^[27] , I ² C SDA, SPI CLK ^[28] |
| 26 | IOHR | I | P1[2] | |
| 27 | IOHR | I | P1[4] | Optional external clock input (EXT CLK) |
| 28 | IOHR | I | P1[6] | |
| 29 | | | NC | No connection |
| 30 | | | NC | No connection |
| 31 | | | NC | No connection |
| 32 | | | NC | No connection |
| 33 | | | NC | No connection |
| 34 | | | NC | No connection |
| 35 | | | XRES | Active high external reset with internal pull-down |
| 36 | I/O | I | P3[0] | |
| 37 | I/O | I | P3[2] | |
| 38 | I/O | I | P3[4] | |
| 39 | I/O | I | P3[6] | |
| 40 | I/O | I | P2[0] | |
| 41 | I/O | I | P2[2] | |
| 42 | I/O | I | P2[4] | |
| 43 | I/O | I | P2[6] | |
| 44 | IOH | I | P0[0] | |
| 45 | IOH | I | P0[2] | |
| 46 | IOH | I | P0[4] | VREF |
| 47 | IOH | I | P0[6] | |
| 48 | Power | | V _{DD} | Power Pin |

Figure 8. CY8C20536A, CY8C20546A, and CY8C20566A



LEGEND A = Analog, I = Input, O = Output, NC = No Connection, H = 5 mA High Output Drive, R = Regulated Output Option.

Notes

- 26. 34 GPIOs = 31 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
- 27. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- 28. Alternate SPI clock.

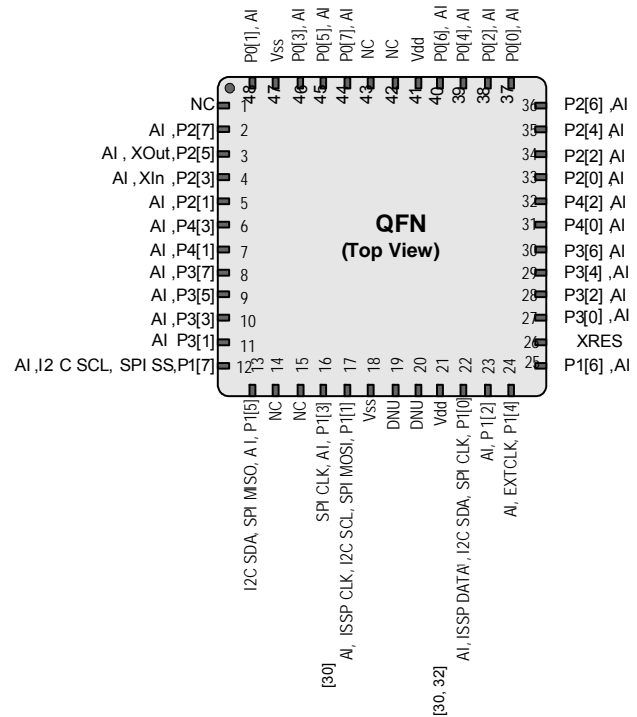
48-pin QFN (33 Sensing Inputs) [29]

Table 8. Pin Definitions – CY8C20636A^[30, 31]

| Pin No. | Digital | Analog | Name | Description |
|---------|---------|--------|-----------------|---|
| 1 | | | NC | No connection |
| 2 | I/O | I | P2[7] | |
| 3 | I/O | I | P2[5] | Crystal output (XOut) |
| 4 | I/O | I | P2[3] | Crystal input (XIn) |
| 5 | I/O | I | P2[1] | |
| 6 | I/O | I | P4[3] | |
| 7 | I/O | I | P4[1] | |
| 8 | I/O | I | P3[7] | |
| 9 | I/O | I | P3[5] | |
| 10 | I/O | I | P3[3] | |
| 11 | I/O | I | P3[1] | |
| 12 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 13 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 14 | | | NC | No connection |
| 15 | | | NC | No connection |
| 16 | IOHR | I | P1[3] | SPI CLK |
| 17 | IOHR | I | P1[1] | ISSP CLK ^[30] , I ² C SCL, SPI MOSI |
| 18 | Power | | V _{SS} | Ground connection |
| 19 | | | DNU | |
| 20 | | | DNU | |
| 21 | Power | | V _{DD} | Supply voltage |
| 22 | IOHR | I | P1[0] | ISSP DATA ^[30] , I ² C SDA, SPI CLK ^[32] |
| 23 | IOHR | I | P1[2] | |
| 24 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 25 | IOHR | I | P1[6] | |
| 26 | Input | | XRES | Active high external reset with internal pull-down |
| 27 | I/O | I | P3[0] | |
| 28 | I/O | I | P3[2] | |
| 29 | I/O | I | P3[4] | |
| 30 | I/O | I | P3[6] | |
| 31 | I/O | I | P4[0] | |
| 32 | I/O | I | P4[2] | |
| 33 | I/O | I | P2[0] | |
| 34 | I/O | I | P2[2] | |
| 35 | I/O | I | P2[4] | |
| 36 | I/O | I | P2[6] | |
| 37 | IOH | I | P0[0] | |
| 38 | IOH | I | P0[2] | |
| 39 | IOH | I | P0[4] | |
| Pin No. | Digital | Analog | Name | Description |
| 40 | IOH | I | P0[6] | |
| 41 | Power | | V _{DD} | Supply voltage |
| 42 | | | NC | No connection |
| 43 | | | NC | No connection |
| 44 | IOH | I | P0[7] | |
| 45 | IOH | I | P0[5] | |
| 46 | IOH | I | P0[3] | Integrating input |
| 47 | Power | | V _{SS} | Ground connection |
| 48 | IOH | I | P0[1] | |
| CP | Power | | V _{SS} | Center pad must be connected to ground |

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Figure 9. CY8C20636A



Notes

- 29. 36 GPIOs = 33 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
- 30. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- 31. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal
- 32. Alternate SPI clock.

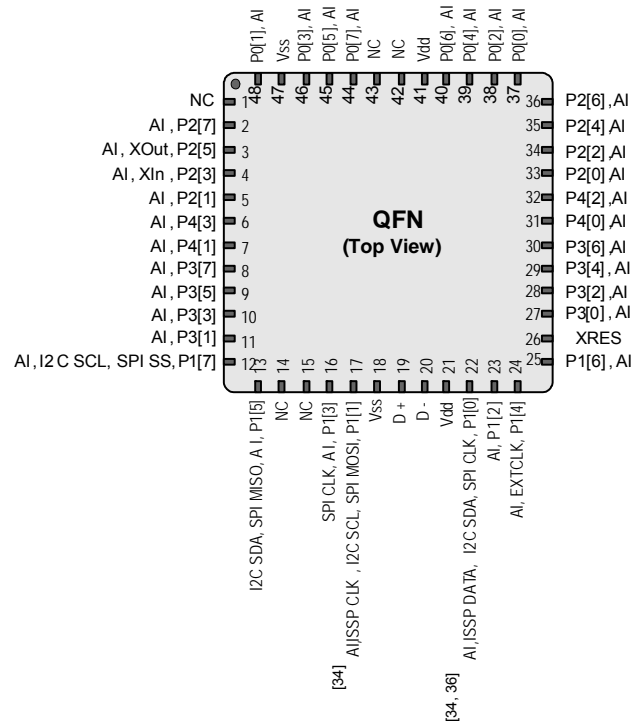
48-pin QFN (33 Sensing Inputs (With USB)) [33]

Table 9. Pin Definitions – CY8C20646A, CY8C20646AS, CY8C20666A, CY8C20666AS [34, 35]

| Pin No. | Digital | Analog | Name | Description |
|---------|---------|--------|-----------------|---|
| 1 | | | NC | No connection |
| 2 | I/O | I | P2[7] | |
| 3 | I/O | I | P2[5] | Crystal output (XOut) |
| 4 | I/O | I | P2[3] | Crystal input (XIn) |
| 5 | I/O | I | P2[1] | |
| 6 | I/O | I | P4[3] | |
| 7 | I/O | I | P4[1] | |
| 8 | I/O | I | P3[7] | |
| 9 | I/O | I | P3[5] | |
| 10 | I/O | I | P3[3] | |
| 11 | I/O | I | P3[1] | |
| 12 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 13 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 14 | | | NC | No connection |
| 15 | | | NC | No connection |
| 16 | IOHR | I | P1[3] | SPI CLK |
| 17 | IOHR | I | P1[1] | ISSP CLK ^[34] , I ² C SCL, SPI MOSI |
| 18 | | Power | V _{SS} | Ground connection |
| 19 | I/O | | D+ | USB D+ |
| 20 | I/O | | D- | USB D- |
| 21 | | Power | V _{DD} | Supply voltage |
| 22 | IOHR | I | P1[0] | ISSP DATA ^[34] , I ² C SDA, SPI CLK ^[36] |
| 23 | IOHR | I | P1[2] | |
| 24 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 25 | IOHR | I | P1[6] | |
| 26 | | Input | XRES | Active high external reset with internal pull-down |
| 27 | I/O | I | P3[0] | |
| 28 | I/O | I | P3[2] | |
| 29 | I/O | I | P3[4] | |
| 30 | I/O | I | P3[6] | |
| 31 | I/O | I | P4[0] | |
| 32 | I/O | I | P4[2] | |
| 33 | I/O | I | P2[0] | |
| 34 | I/O | I | P2[2] | |
| 35 | I/O | I | P2[4] | |
| 36 | I/O | I | P2[6] | |
| 37 | IOH | I | P0[0] | |
| 38 | IOH | I | P0[2] | |
| 39 | IOH | I | P0[4] | |
| Pin No. | Digital | Analog | Name | Description |
| 40 | IOH | I | P0[6] | |
| 41 | | Power | V _{DD} | Supply voltage |
| 42 | | | NC | No connection |
| 43 | | | NC | No connection |
| 44 | IOH | I | P0[7] | |
| 45 | IOH | I | P0[5] | |
| 46 | IOH | I | P0[3] | Integrating input |
| 47 | | Power | V _{SS} | Ground connection |
| 48 | IOH | I | P0[1] | |
| CP | | Power | V _{SS} | Center pad must be connected to ground |

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Figure 10. CY8C20646A, CY8C20646AS, CY8C20666A, CY8C20666AS



Notes

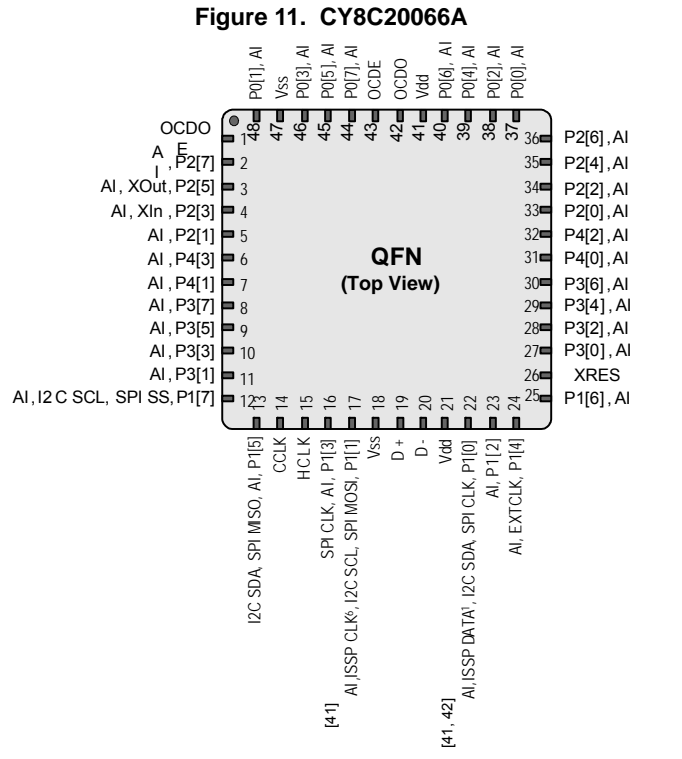
- 33. 38 GPIOs = 33 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
- 34. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- 35. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- 36. Alternate SPI clock.

48-pin QFN (OCD) (33 Sensing Inputs) [37]

The 48-pin QFN part is for the CY8C20066A On-Chip Debug (OCD). Note that this part is only used for in-circuit debugging.

Table 10. Pin Definitions – CY8C20066A [38, 39]

| Pin No. | Digital | Analog | Name | Description |
|--------------------|---------|--------|-----------------|---|
| 1 ^[40] | | | OCDOE | OCD mode direction pin |
| 2 | I/O | I | P2[7] | |
| 3 | I/O | I | P2[5] | Crystal output (XOut) |
| 4 | I/O | I | P2[3] | Crystal input (XIn) |
| 5 | I/O | I | P2[1] | |
| 6 | I/O | I | P4[3] | |
| 7 | I/O | I | P4[1] | |
| 8 | I/O | I | P3[7] | |
| 9 | I/O | I | P3[5] | |
| 10 | I/O | I | P3[3] | |
| 11 | I/O | I | P3[1] | |
| 12 | IOHR | I | P1[7] | I ² C SCL, SPI SS |
| 13 | IOHR | I | P1[5] | I ² C SDA, SPI MISO |
| 14 ^[40] | | | CCLK | OCD CPU clock output |
| 15 ^[40] | | | HCLK | OCD high speed clock output |
| 16 | IOHR | I | P1[3] | SPI CLK. |
| 17 | IOHR | I | P1[1] | ISSP CLK ^[41] , I ² C SCL, SPI MOSI |
| 18 | Power | | V _{SS} | Ground connection |
| 19 | I/O | | D+ | USB D+ |
| 20 | I/O | | D- | USB D- |
| 21 | Power | | V _{DD} | Supply voltage |
| 22 | IOHR | I | P1[0] | ISSP DATA ^[41] , I ² C SDA, SPI CLK ^[42] |
| 23 | IOHR | I | P1[2] | |
| 24 | IOHR | I | P1[4] | Optional external clock input (EXTCLK) |
| 25 | IOHR | I | P1[6] | |
| 26 | Input | | XRES | Active high external reset with internal pull-down |
| 27 | I/O | I | P3[0] | |
| 28 | I/O | I | P3[2] | |
| 29 | I/O | I | P3[4] | |
| 30 | I/O | I | P3[6] | |
| 31 | I/O | I | P4[0] | |
| 32 | I/O | I | P4[2] | |
| 33 | I/O | I | P2[0] | |
| 34 | I/O | I | P2[2] | |
| 35 | I/O | I | P2[4] | |
| 36 | I/O | I | P2[6] | |



LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

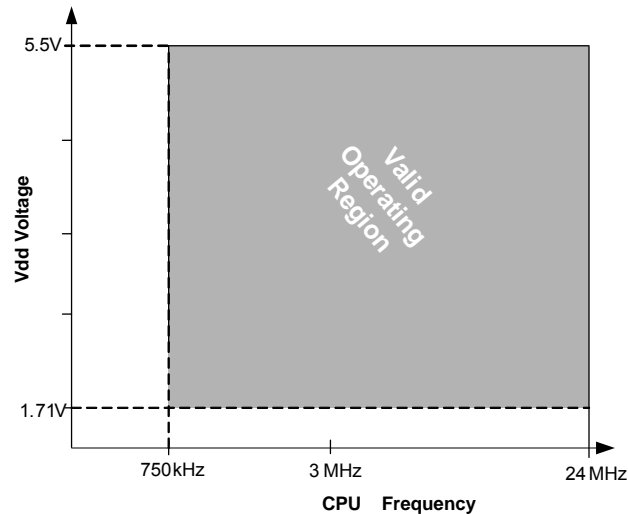
Notes

- 37. 38 GPIOs = 33 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
- 38. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.
- 39. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- 40. This pin (associated with OCD part only) is required for connecting the device to ICE-Cube In-Circuit Emulator for firmware debugging purpose. To know more about the usage of ICE-Cube, refer to [CY3215-DK PSoC® IN-CIRCUIT EMULATOR KIT GUIDE](#).
- 41. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- 42. Alternate SPI clock.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20XX6A/S PSoC devices. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at <http://www.cypress.com/psoc>.

Figure 12. Voltage versus CPU Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 11. Absolute Maximum Ratings

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------------------------|--|---|-----------------------|-----|-----------------------|-------|
| T _{STG} | Storage temperature | Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability. | -55 | +25 | +125 | °C |
| V _{DD} | Supply voltage relative to V _{SS} | - | -0.5 | - | +6.0 | V |
| V _{IO} | DC input voltage | - | V _{SS} - 0.5 | - | V _{DD} + 0.5 | V |
| V _{IOZ} ^[43] | DC voltage applied to tristate | - | V _{SS} - 0.5 | - | V _{DD} + 0.5 | V |
| I _{MIO} | Maximum current into any port pin | - | -25 | - | +50 | mA |
| ESD | Electrostatic discharge voltage | Human body model ESD | 2000 | - | - | V |
| LU | Latch-up current | In accordance with JEDEC standard | - | - | 200 | mA |

Operating Temperature

Table 12. Operating Temperature

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------|------------------------------|---|-----|-----|------|-------|
| T _A | Ambient temperature | - | -40 | - | +85 | °C |
| T _C | Commercial temperature range | - | 0 | - | 70 | °C |
| T _J | Operational die temperature | The temperature rise from ambient to junction is package specific. Refer the Thermal Impedances on page 37 . The user must limit the power consumption to comply with this requirement. | -40 | - | +100 | °C |

Note

43. Port1 pins are hot-swap capable with I/O configured in High-Z mode, and pin input voltage above V_{DD}.

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 13. DC Chip-Level Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------------------------------------|---|--|------|------|------|---------|
| V_{DD} [44, 45, 46, 47] | Supply voltage | No USB activity. Refer the table “DC POR and LVD Specifications” on page 25 | 1.71 | – | 5.50 | V |
| V_{DDUSB} [44, 45, 46, 47] | Operating voltage | USB activity, USB regulator enabled | 4.35 | – | 5.25 | V |
| | | USB activity, USB regulator bypassed | 3.15 | 3.3 | 3.60 | V |
| I_{DD24} | Supply current, IMO = 24 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current | – | 2.88 | 4.00 | mA |
| I_{DD12} | Supply current, IMO = 12 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current | – | 1.71 | 2.60 | mA |
| I_{DD6} | Supply current, IMO = 6 MHz | Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current | – | 1.16 | 1.80 | mA |
| $I_{DDAVG10}$ | Average supply current per sensor | One sensor scanned at 10 mS rate | – | 250 | – | μ A |
| $I_{DDAVG100}$ | Average supply current per sensor | One sensor scanned at 100 mS rate | – | 25 | – | μ A |
| $I_{DDAVG500}$ | Average supply current per sensor | One sensor scanned at 500 mS rate | – | 7 | – | μ A |
| I_{SBO} [48, 49, 50, 51, 52, 53] | Deep sleep current | $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off | – | 0.10 | 1.05 | μ A |
| I_{SB1} [48, 49, 50, 51, 52, 53] | Standby current with POR, LVD and sleep timer | $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off | – | 1.07 | 1.50 | μ A |
| I_{SB12C} [48, 49, 50, 51, 52, 53] | Standby current with I ² C enabled | Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz | – | 1.64 | – | μ A |

Notes

44. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 μ s, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 μ s to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
45. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
 - a. Bring the device out of sleep before powering down.
 - b. Assure that V_{DD} falls below 100 mV before powering back up.
 - c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
 - d. Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register.
 For the referenced registers, refer to the *CY8C20X36 Technical Reference Manual*. In deep sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected for edge rates slower than 1V/ms.
46. For USB mode, the V_{DD} supply for bus-powered application should be limited to 4.35 V–5.35 V. For self-powered application, V_{DD} should be 3.15 V–3.45 V.
47. For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD} , the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.
48. **Errata:** When the device is put to sleep in Standby or I²C_USB Mode and the bandgap circuit is refreshed less frequently than every 8 ms (default), the device may not come out of sleep when a sleep-ending input is received. For more information, see the “Errata” on page 45.
49. **Errata:** The I²C block exhibits occasional data and bus corruption errors when the I²C master initiates transactions while the device is in or out of transition of sleep mode. For more information, see the “Errata” on page 45.
50. **Errata:** When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice. For more information, see the “Errata” on page 46.
51. **Errata:** When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run. For more information, see the “Errata” on page 46.
52. **Errata:** If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed. For more information, see the “Errata” on page 47.
53. **Errata:** Device wakes up from sleep when an analog interrupt is trigger. For more information, see the “Errata” on page 47.

DC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 1.71 V to 2.4 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 C and are for design guidance only.

Table 14. 3.0 V to 5.5 V DC GPIO Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-----------------------|--|---|------------------------|-------|------|-------|
| R _{PU} | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| V _{OH1} | High output voltage Port 2 or 3 or 4 pins | I _{OH} ≤ 10 μA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.20 | – | – | V |
| V _{OH2} | High output voltage Port 2 or 3 or 4 pins | I _{OH} = 1 mA, maximum of 20 mA source current in all I/Os | V _{DD} – 0.90 | – | – | V |
| V _{OH3} | High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1 | I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.20 | – | – | V |
| V _{OH4} | High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1 | I _{OH} = 5 mA, maximum of 20 mA source current in all I/Os | V _{DD} – 0.90 | – | – | V |
| V _{OH5} | High output voltage Port 1 Pins with LDO Regulator Enabled for 3 V out | I _{OH} < 10 μA, V _{DD} > 3.1 V, maximum of 4 I/Os all sourcing 5 mA | 2.85 | 3.00 | 3.30 | V |
| V _{OH6} | High output voltage Port 1 pins with LDO regulator enabled for 3 V out | I _{OH} = 5 mA, V _{DD} > 3.1 V, maximum of 20 mA source current in all I/Os | 2.20 | – | – | V |
| V _{OH7} | High output voltage Port 1 pins with LDO enabled for 2.5 V out | I _{OH} < 10 μA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os | 2.35 | 2.50 | 2.75 | V |
| V _{OH8} | High output voltage Port 1 pins with LDO enabled for 2.5 V out | I _{OH} = 2 mA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os | 1.90 | – | – | V |
| V _{OH9} | High output voltage Port 1 pins with LDO enabled for 1.8 V out | I _{OH} < 10 μA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os | 1.60 | 1.80 | 2.10 | V |
| V _{OH10} | High output voltage Port 1 pins with LDO enabled for 1.8 V out | I _{OH} = 1 mA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os | 1.20 | – | – | V |
| V _{OL} | Low output voltage | I _{OL} = 25 mA, V _{DD} > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.75 | V |
| V _{IL} | Input low voltage | – | – | – | 0.80 | V |
| V _{IH} | Input high voltage | – | 2.00 | – | – | V |
| V _H | Input hysteresis voltage | – | – | 80 | – | mV |
| I _{IL} | Input leakage (Absolute Value) | – | – | 0.001 | 1 | μA |
| C _{PIN} | Pin capacitance | Package and pin dependent Temp = 25 °C | 0.50 | 1.70 | 7 | pF |
| V _{ILLVT3.3} | Input Low Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 0.8 | V | – | – |
| V _{IHLVT3.3} | Input High Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 1.4 | – | – | V |
| V _{ILLVT5.5} | Input Low Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 0.8 | V | – | – |
| V _{IHLVT5.5} | Input High Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 1.7 | – | – | V |

Table 15. 2.4 V to 3.0 V DC GPIO Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-----------------------|---|--|------------------------|------|------|-------|
| R _{PU} | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| V _{OH1} | High output voltage Port 2 or 3 or 4 pins | I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.20 | – | – | V |
| V _{OH2} | High output voltage Port 2 or 3 or 4 pins | I _{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.40 | – | – | V |
| V _{OH3} | High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1 | I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.20 | – | – | V |
| V _{OH4} | High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1 | I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.50 | – | – | V |
| V _{OH5A} | High output voltage Port 1 pins with LDO enabled for 1.8 V out | I _{OH} < 10 μA, V _{DD} > 2.4 V, maximum of 20 mA source current in all I/Os | 1.50 | 1.80 | 2.10 | V |
| V _{OH6A} | High output voltage Port 1 pins with LDO enabled for 1.8 V out | I _{OH} = 1 mA, V _{DD} > 2.4 V, maximum of 20 mA source current in all I/Os | 1.20 | – | – | V |
| V _{OL} | Low output voltage | I _{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.75 | V |
| V _{IL} | Input low voltage | – | – | – | 0.72 | V |
| V _{IH} | Input high voltage | – | 1.40 | – | – | V |
| V _H | Input hysteresis voltage | – | – | 80 | – | mV |
| I _{IL} | Input leakage (absolute value) | – | – | 1 | 1000 | nA |
| C _{PIN} | Capacitive load on pins | Package and pin dependent Temp = 25 °C | 0.50 | 1.70 | 7 | pF |
| V _{ILLVT2.5} | Input Low Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 0.7 | V | – | |
| V _{IHLVT2.5} | Input High Voltage with low threshold enable set, Enable for Port1 | Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input | 1.2 | – | – | V |

Table 16. 1.71 V to 2.4 V DC GPIO Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|------------------|---|---|------------------------|------|------|-------|
| R _{PU} | Pull-up resistor | – | 4 | 5.60 | 8 | kΩ |
| V _{OH1} | High output voltage Port 2 or 3 or 4 pins | I _{OH} = 10 μA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.20 | – | – | V |
| V _{OH2} | High output voltage Port 2 or 3 or 4 pins | I _{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.50 | – | – | V |
| V _{OH3} | High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1 | I _{OH} = 100 μA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.20 | – | – | V |
| V _{OH4} | High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1 | I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os | V _{DD} – 0.50 | – | – | V |
| V _{OL} | Low output voltage | I _{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]) | – | – | 0.40 | V |

Table 16. 1.71 V to 2.4 V DC GPIO Specifications (continued)

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|------------------|--------------------------------|---|------------------------|------|------------------------|-------|
| V _{IL} | Input low voltage | – | – | – | 0.30 × V _{DD} | V |
| V _{IH} | Input high voltage | – | 0.65 × V _{DD} | – | – | V |
| V _H | Input hysteresis voltage | – | – | 80 | – | mV |
| I _{IL} | Input leakage (absolute value) | – | – | 1 | 1000 | nA |
| C _{PIN} | Capacitive load on pins | Package and pin dependent temp = 25 °C | 0.50 | 1.70 | 7 | pF |

Table 17. DC Characteristics – USB Interface

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------------------|--------------------------------------|-----------------------------|-------|------|-------|-------|
| R _{USBI} | USB D+ pull-up resistance | With idle bus | 900 | – | 1575 | Ω |
| R _{USBA} | USB D+ pull-up resistance | While receiving traffic | 1425 | – | 3090 | Ω |
| V _{OHUSB} | Static output high | – | 2.8 | – | 3.6 | V |
| V _{OLUSB} | Static output low | – | – | – | 0.3 | V |
| V _{DI} | Differential input sensitivity | – | 0.2 | – | – | V |
| V _{CM} | Differential input common mode range | – | 0.8 | – | 2.5 | V |
| V _{SE} | Single ended receiver threshold | – | 0.8 | – | 2.0 | V |
| C _{IN} | Transceiver capacitance | – | – | – | 50 | pF |
| I _{IO} | High Z state data line leakage | On D+ or D- line | –10 | – | +10 | μA |
| R _{PS2} | PS/2 pull-up resistance | – | 3000 | 5000 | 7000 | Ω |
| R _{EXT} | External USB series resistor | In series with each USB pin | 21.78 | 22.0 | 22.22 | Ω |

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. DC Analog Mux Bus Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|------------------|--|------------|-----|-----|-----|-------|
| R _{SW} | Switch resistance to common analog bus | – | – | – | 800 | Ω |
| R _{GND} | Resistance of initialization switch to V _{SS} | – | – | – | 800 | Ω |

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC Comparator Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------------------|--|--|-----|-----|-----|-------|
| V _{LPC} | Low power comparator (LPC) common mode | Maximum voltage limited to V _{DD} | 0.0 | – | 1.8 | V |
| I _{LPC} | LPC supply current | – | – | 10 | 40 | μA |
| V _{OSLPC} | LPC voltage offset | – | – | 3 | 30 | mV |

Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$.

Table 20. Comparator User Module Electrical Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-------------------|--------------------------|---|-----|-----|-----|---------------|
| t_{COMP} | Comparator response time | 50 mV overdrive | – | 70 | 100 | ns |
| Offset | | Valid from 0.2 V to $V_{DD} - 0.2\text{ V}$ | – | 2.5 | 30 | mV |
| Current | | Average DC current, 50 mV overdrive | – | 20 | 80 | μA |
| PSRR | Supply voltage > 2 V | Power supply rejection ratio | – | 80 | – | dB |
| | Supply voltage < 2 V | Power supply rejection ratio | – | 40 | – | dB |
| Input range | | – | 0 | | 1.5 | V |

ADC Electrical Specifications
Table 21. ADC User Module Electrical Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|------------------------|------------------------------|--|---|---|---|----------|
| Input | | | | | | |
| V_{IN} | Input voltage range | – | 0 | – | V_{REFADC} | V |
| C_{IIN} | Input capacitance | – | – | – | 5 | pF |
| R_{IN} | Input resistance | Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution | $1/(500\text{fF} \times \text{data clock})$ | $1/(400\text{fF} \times \text{data clock})$ | $1/(300\text{fF} \times \text{data clock})$ | Ω |
| Reference | | | | | | |
| V_{REFADC} | ADC reference voltage | – | 1.14 | – | 1.26 | V |
| Conversion Rate | | | | | | |
| F_{CLK} | Data clock | Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy | 2.25 | – | 6 | MHz |
| S8 | 8-bit sample rate | Data clock set to 6 MHz. sample rate = $0.001 / (2^{\text{Resolution}} / \text{Data Clock})$ | – | 23.43 | – | ksp/s |
| S10 | 10-bit sample rate | Data clock set to 6 MHz. sample rate = $0.001 / (2^{\text{resolution}} / \text{data clock})$ | – | 5.85 | – | ksp/s |
| DC Accuracy | | | | | | |
| RES | Resolution | Can be set to 8-, 9-, or 10-bit | 8 | – | 10 | bits |
| DNL | Differential nonlinearity | – | –1 | – | +2 | LSB |
| INL | Integral nonlinearity | – | –2 | – | +2 | LSB |
| E_{OFFSET} | Offset error | 8-bit resolution | 0 | 3.20 | 19.20 | LSB |
| | | 10-bit resolution | 0 | 12.80 | 76.80 | LSB |
| E_{GAIN} | Gain error | For any resolution | –5 | – | +5 | %FSR |
| Power | | | | | | |
| I_{ADC} | Operating current | – | – | 2.10 | 2.60 | mA |
| PSRR | Power supply rejection ratio | PSRR ($V_{DD} > 3.0\text{ V}$) | – | 24 | – | dB |
| | | PSRR ($V_{DD} < 3.0\text{ V}$) | – | 30 | – | dB |

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 22. DC POR and LVD Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-------------------|----------------------------------|--|----------------------|------|------|-------|
| V _{POR0} | 1.66 V selected in PSoC Designer | V _{DD} must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog. | 1.61 | 1.66 | 1.71 | V |
| V _{POR1} | 2.36 V selected in PSoC Designer | | – | 2.36 | 2.41 | |
| V _{POR2} | 2.60 V selected in PSoC Designer | | – | 2.60 | 2.66 | |
| V _{POR3} | 2.82 V selected in PSoC Designer | | – | 2.82 | 2.95 | |
| V _{LVD0} | 2.45 V selected in PSoC Designer | – | 2.40 | 2.45 | 2.51 | V |
| V _{LVD1} | 2.71 V selected in PSoC Designer | | 2.64 ^[54] | 2.71 | 2.78 | |
| V _{LVD2} | 2.92 V selected in PSoC Designer | | 2.85 ^[55] | 2.92 | 2.99 | |
| V _{LVD3} | 3.02 V selected in PSoC Designer | | 2.95 ^[56] | 3.02 | 3.09 | |
| V _{LVD4} | 3.13 V selected in PSoC Designer | | 3.06 | 3.13 | 3.20 | |
| V _{LVD5} | 1.90 V selected in PSoC Designer | | 1.84 | 1.90 | 2.32 | |
| V _{LVD6} | 1.80 V selected in PSoC Designer | | 1.75 ^[57] | 1.80 | 1.84 | |
| V _{LVD7} | 4.73 V selected in PSoC Designer | | 4.62 | 4.73 | 4.83 | |

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 23. DC Programming Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-----------------------|---|---|-----------------|-----|------------------------|-------|
| V _{DDIWRITE} | Supply voltage for flash write operations | – | 1.71 | – | 5.25 | V |
| I _{DDP} | Supply current during programming or verify | – | – | 5 | 25 | mA |
| V _{ILP} | Input low voltage during programming or verify | See the appropriate DC GPIO Specifications on page 21 | – | – | V _{IL} | V |
| V _{IHP} | Input high voltage during programming or verify | See the appropriate “ DC GPIO Specifications ” on page 21 | V _{IH} | – | – | V |
| I _{ILP} | Input current when Applying V _{ILP} to P1[0] or P1[1] during programming or verify | Driving internal pull-down resistor | – | – | 0.2 | mA |
| I _{IHP} | Input current when applying V _{IHP} to P1[0] or P1[1] during programming or verify | Driving internal pull-down resistor | – | – | 1.5 | mA |
| V _{OLP} | Output low voltage during programming or verify | | – | – | V _{SS} + 0.75 | V |
| V _{OHP} | Output high voltage during programming or verify | See appropriate DC GPIO Specifications on page 21 . For V _{DD} > 3 V use V _{OH4} in Table 12 on page 19 . | V _{OH} | – | V _{DD} | V |
| Flash _{ENPB} | Flash write endurance | Erase/write cycles per block | 50,000 | – | – | – |
| Flash _{DR} | Flash data retention | Following maximum Flash write cycles; ambient temperature of 55 °C | 20 | – | – | Years |

Notes

- 54. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
- 55. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
- 56. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
- 57. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

DC I²C Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 1.71 V to 2.4 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 24. DC I²C Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------------------|------------------|---|----------------------|-----|----------------------|-------|
| V _{ILi2C} | Input low level | $3.1\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | – | – | $0.25 \times V_{DD}$ | V |
| | | $2.5\text{ V} \leq V_{DD} \leq 3.0\text{ V}$ | – | – | $0.3 \times V_{DD}$ | V |
| | | $1.71\text{ V} \leq V_{DD} \leq 2.4\text{ V}$ | – | – | $0.3 \times V_{DD}$ | V |
| V _{IHi2C} | Input high level | $1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | $0.65 \times V_{DD}$ | – | – | V |

DC Reference Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 1.71 V to 2.4 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. DC Reference Buffer Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------------------|-------------------------|--|-----|-----|------|-------|
| V _{Ref} | Reference buffer output | $1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1 | – | 1.05 | V |
| V _{RefHi} | Reference buffer output | $1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1.2 | – | 1.25 | V |

DC IDAC Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 26. DC IDAC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------------|---------------------------|-------|-----|-------|-------|--|
| IDAC_DNL | Differential nonlinearity | –4.5 | – | +4.5 | LSB | |
| IDAC_INL | Integral nonlinearity | –5 | – | +5 | LSB | |
| IDAC_Gain (Source) | Range = 0.5x | 6.64 | – | 22.46 | μA | DAC setting = 128 dec. Not recommended for CapSense applications. |
| | Range = 1x | 14.5 | – | 47.8 | μA | |
| | Range = 2x | 42.7 | – | 92.3 | μA | |
| | Range = 4x | 91.1 | – | 170 | μA | |
| | Range = 8x | 184.5 | – | 426.9 | μA | |

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 27. AC Chip-Level Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------------------------------------|---|---|------|-----|-------|-------|
| F _{IMO24} | IMO frequency at 24 MHz Setting | – | 22.8 | 24 | 25.2 | MHz |
| F _{IMO12} | IMO frequency at 12 MHz setting | – | 11.4 | 12 | 12.6 | MHz |
| F _{IMO6} | IMO frequency at 6 MHz setting | – | 5.7 | 6.0 | 6.3 | MHz |
| F _{CPU} | CPU frequency | – | 0.75 | – | 25.20 | MHz |
| F _{32K1} | ILO frequency | – | 15 | 32 | 50 | kHz |
| F _{32K_U} | ILO untrimmed frequency | – | 13 | 32 | 82 | kHz |
| DC _{IMO} | Duty cycle of IMO | – | 40 | 50 | 60 | % |
| DC _{ILO} | ILO duty cycle | – | 40 | 50 | 60 | % |
| SR _{POWER_UP} | Power supply slew rate | V _{DD} slew rate during power-up | – | – | 250 | V/ms |
| t _{XRST} | External reset pulse width at power-up | After supply voltage is valid | 1 | – | – | ms |
| t _{XRST2} | External reset pulse width after power-up ^[58] | Applies after part has booted | 10 | – | – | μs |
| t _{OS} | Startup time of ECO | – | – | 1 | – | s |
| t _{JIT_IMO} ^[59] | N=32 | 6 MHz IMO cycle-to-cycle jitter (RMS) | – | 0.7 | 6.7 | ns |
| | | 6 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS) | – | 4.3 | 29.3 | ns |
| | | 6 MHz IMO period jitter (RMS) | – | 0.7 | 3.3 | ns |
| | | 12 MHz IMO cycle-to-cycle jitter (RMS) | – | 0.5 | 5.2 | ns |
| | | 12 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS) | – | 2.3 | 5.6 | ns |
| | | 12 MHz IMO period jitter (RMS) | – | 0.4 | 2.6 | ns |
| | | 24 MHz IMO cycle-to-cycle jitter (RMS) | – | 1.0 | 8.7 | ns |
| | | 24 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS) | – | 1.4 | 6.0 | ns |
| | | 24 MHz IMO period jitter (RMS) | – | 0.6 | 4.0 | ns |

Notes

58. The minimum required XRES pulse length is longer when programming the device (see Table 33 on page 30).

59. Refer to Cypress Jitter Specifications application note, [Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054](#) for more information.

AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 28. AC GPIO Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---------------|--|---|-----|-----|---|----------------|
| F_{GPIO} | GPIO operating frequency | Normal strong mode Port 0, 1 | 0 | – | 6 MHz for 1.71 V < V_{DD} < 2.40 V 12 MHz for 2.40 V < V_{DD} < 5.50 V | MHz MHz |
| t_{RISE23} | Rise time, strong mode, Cload = 50 pF Port 2 or 3 or 4 pins | $V_{DD} = 3.0$ to 3.6 V, 10% to 90% | 15 | – | 80 | ns |
| $t_{RISE23L}$ | Rise time, strong mode low supply, Cload = 50 pF, Port 2 or 3 or 4 pins | $V_{DD} = 1.71$ to 3.0 V, 10% to 90% | 15 | – | 80 | ns |
| t_{RISE01} | Rise time, strong mode, Cload = 50 pF Ports 0 or 1 | $V_{DD} = 3.0$ to 3.6 V, 10% to 90% LDO enabled or disabled | 10 | – | 50 | ns |
| $t_{RISE01L}$ | Rise time, strong mode low supply, Cload = 50 pF, Ports 0 or 1 | $V_{DD} = 1.71$ to 3.0 V, 10% to 90% LDO enabled or disabled | 10 | – | 80 | ns |
| t_{FALL} | Fall time, strong mode, Cload = 50 pF all ports | $V_{DD} = 3.0$ to 3.6 V, 10% to 90% | 10 | – | 50 | ns |
| t_{FALLL} | Fall time, strong mode low supply, Cload = 50 pF, all ports | $V_{DD} = 1.71$ to 3.0 V, 10% to 90% | 10 | – | 70 | ns |

Figure 13. GPIO Timing Diagram

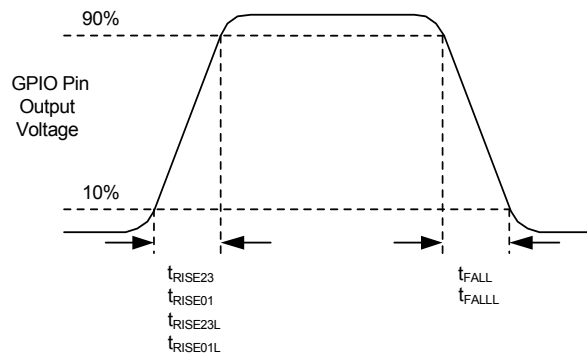


Table 29. AC Characteristics – USB Data Timings

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|--------------------|--|--------------------|------------|-----|------------|-------|
| t _{DRATE} | Full speed data rate | Average bit rate | 12 – 0.25% | 12 | 12 + 0.25% | MHz |
| t _{JR1} | Receiver jitter tolerance | To next transition | –18.5 | – | 18.5 | ns |
| t _{JR2} | Receiver jitter tolerance | To pair transition | –9.0 | – | 9 | ns |
| t _{DJ1} | FS Driver jitter | To next transition | –3.5 | – | 3.5 | ns |
| t _{DJ2} | FS Driver jitter | To pair transition | –4.0 | – | 4.0 | ns |
| t _{FDEOP} | Source jitter for differential transition | To SE0 transition | –2.0 | – | 5 | ns |
| t _{FEOPT} | Source SE0 interval of EOP | – | 160.0 | – | 175 | ns |
| t _{FEOPR} | Receiver SE0 interval of EOP | – | 82.0 | – | – | ns |
| t _{FST} | Width of SE0 interval during differential transition | – | – | – | 14 | ns |

Table 30. AC Characteristics – USB Driver

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|-----------------------------------|---------------------------------|------------|------|-----|------|-------|
| t _{FR} | Transition rise time | 50 pF | 4 | – | 20 | ns |
| t _{FF} | Transition fall time | 50 pF | 4 | – | 20 | ns |
| t _{FRFM} ^[60] | Rise/fall time matching | – | 90 | – | 111 | % |
| V _{CRS} | Output signal crossover voltage | – | 1.30 | – | 2.00 | V |

AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 31. AC Low Power Comparator Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|------------------|---|--|-----|-----|-----|-------|
| t _{LPC} | Comparator response time, 50 mV overdrive | 50 mV overdrive does not include offset voltage. | – | – | 100 | ns |

AC External Clock Specifications

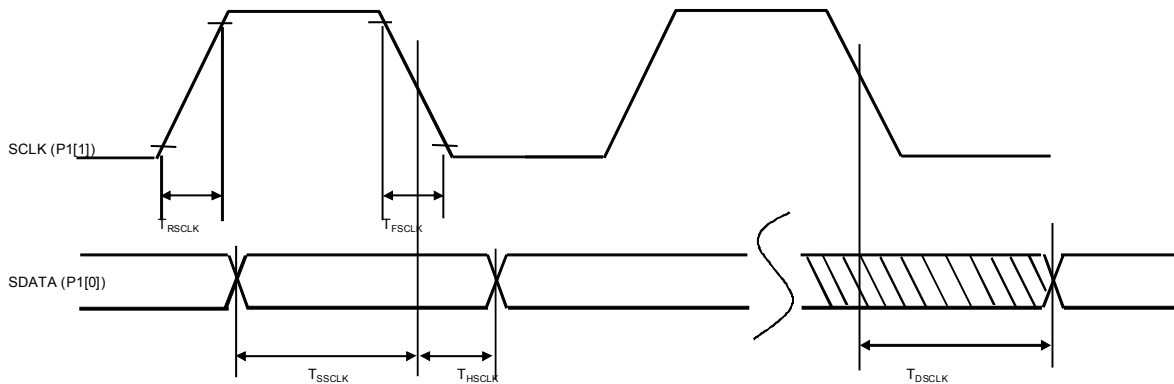
The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 32. AC External Clock Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---------------------|---|------------|-------|-----|-------|-------|
| F _{OSCEXT} | Frequency (external oscillator frequency) | – | 0.75 | – | 25.20 | MHz |
| | High period | – | 20.60 | – | 5300 | ns |
| | Low period | – | 20.60 | – | – | ns |
| | Power-up IMO to switch | – | 150 | – | – | μs |

Note

60. T_{FRFM} is not met under all conditions. There is a corner case at lower supply voltages, such as those under 3.3 V. This condition does not affect USB communications. Signal integrity tests show an excellent eye diagram at 3.15 V.

AC Programming Specifications
Figure 14. AC Waveform


The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 33. AC Programming Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------------|---|---|-------|-----|-------|---------|
| t_{RSCLK} | Rise time of SCLK | – | 1 | – | 20 | ns |
| t_{FSCLK} | Fall time of SCLK | – | 1 | – | 20 | ns |
| t_{SSCLK} | Data setup time to falling edge of SCLK | – | 40 | – | – | ns |
| t_{HSCLK} | Data hold time from falling edge of SCLK | – | 40 | – | – | ns |
| F_{SCLK} | Frequency of SCLK | – | 0 | – | 8 | MHz |
| t_{ERASEB} | Flash erase time (block) | – | – | – | 18 | ms |
| t_{WRITE} | Flash block write time | – | – | – | 25 | ms |
| t_{DSCLK} | Data out delay from falling edge of SCLK | $3.6 < V_{DD}$ | – | – | 60 | ns |
| t_{DSCLK3} | Data out delay from falling edge of SCLK | $3.0 \leq V_{DD} \leq 3.6$ | – | – | 85 | ns |
| t_{DSCLK2} | Data out delay from falling edge of SCLK | $1.71 \leq V_{DD} \leq 3.0$ | – | – | 130 | ns |
| t_{XRST3} | External reset pulse width after power-up | Required to enter programming mode when coming out of sleep | 300 | – | – | μ s |
| t_{XRES} | XRES pulse length | – | 300 | – | – | μ s |
| $t_{VDDWAIT}^{[61]}$ | V_{DD} stable to wait-and-poll hold off | – | 0.1 | – | 1 | ms |
| $t_{VDDXRES}^{[61]}$ | V_{DD} stable to XRES assertion delay | – | 14.27 | – | – | ms |
| t_{POLL} | SDATA high pulse time | – | 0.01 | – | 200 | ms |
| $t_{ACQ}^{[61]}$ | “Key window” time after a V_{DD} ramp acquire event, based on 256 ILO clocks. | – | 3.20 | – | 19.60 | ms |
| $t_{XRESINI}^{[61]}$ | “Key window” time after an XRES event, based on 8 ILO clocks | – | 98 | – | 615 | μ s |

Note

61. Valid from 5 to 50 °C. See the spec, CY8C20X66, CY8C20X46, CY8C20X36, CY7C643XX, CY7C604XX, CY8CTST2XX, CY8CTMG2XX, CY8C20X67, CY8C20X47, CY8C20X37, Programming Spec for more details.

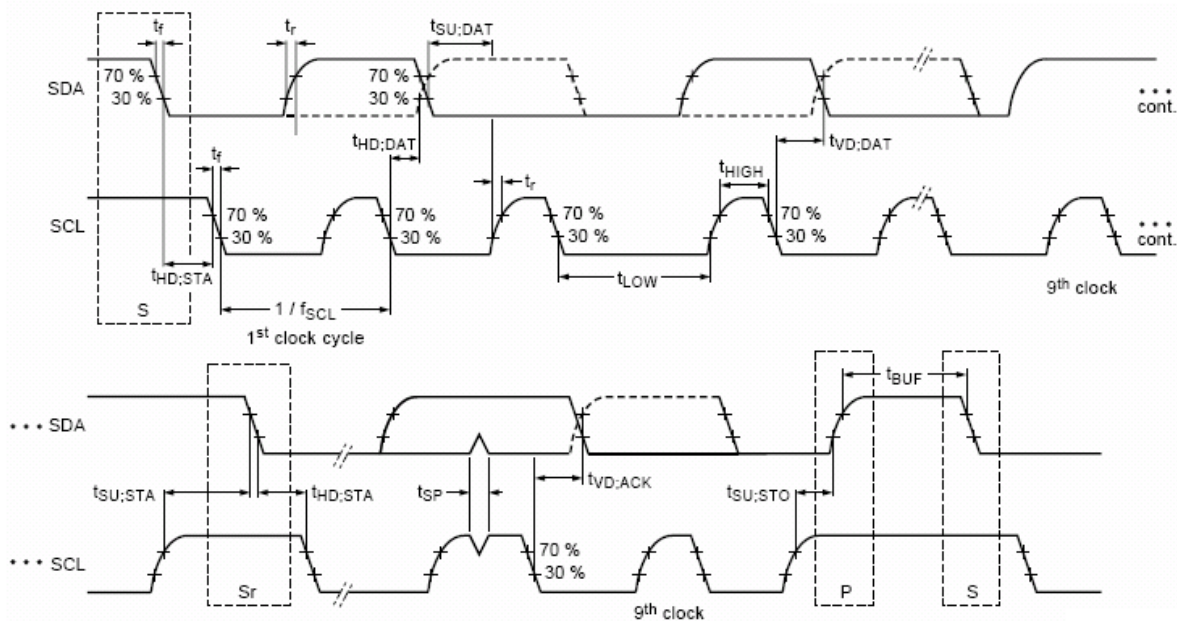
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 34. AC Characteristics of the I²C SDA and SCL Pins

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|---------------------|---|---------------|------|---------------------|------|-------|
| | | Min | Max | Min | Max | |
| f _{SCL} | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| t _{HD;STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated | 4.0 | – | 0.6 | – | µs |
| t _{LOW} | LOW period of the SCL clock | 4.7 | – | 1.3 | – | µs |
| t _{HIGH} | HIGH Period of the SCL clock | 4.0 | – | 0.6 | – | µs |
| t _{SU;STA} | Setup time for a repeated START condition | 4.7 | – | 0.6 | – | µs |
| t _{HD;DAT} | Data hold time | 0 | 3.45 | 0 | 0.90 | µs |
| t _{SU;DAT} | Data setup time | 250 | – | 100 ^[62] | – | ns |
| t _{SU;STO} | Setup time for STOP condition | 4.0 | – | 0.6 | – | µs |
| t _{BUF} | Bus free time between a STOP and START condition | 4.7 | – | 1.3 | – | µs |
| t _{SP} | Pulse width of spikes are suppressed by the input filter | – | – | 0 | 50 | ns |

Figure 15. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

62. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement t_{SU;DAT} ≥ 250 ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250 ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Table 35. SPI Master AC Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|----------------|-------------------------|---|-----------|--------|--------|------------|
| F_{SCLK} | SCLK clock frequency | $V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$ | – – | – – | 6 3 | MHz MHz |
| DC | SCLK duty cycle | – | – | 50 | – | % |
| t_{SETUP} | MISO to SCLK setup time | $V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$ | 60 100 | – – | – – | ns ns |
| t_{HOLD} | SCLK to MISO hold time | – | 40 | – | – | ns |
| t_{OUT_VAL} | SCLK to MOSI valid time | – | – | – | 40 | ns |
| t_{OUT_H} | MOSI high time | – | 40 | – | – | ns |

Figure 16. SPI Master Mode 0 and 2

SPI Master, modes 0 and 2

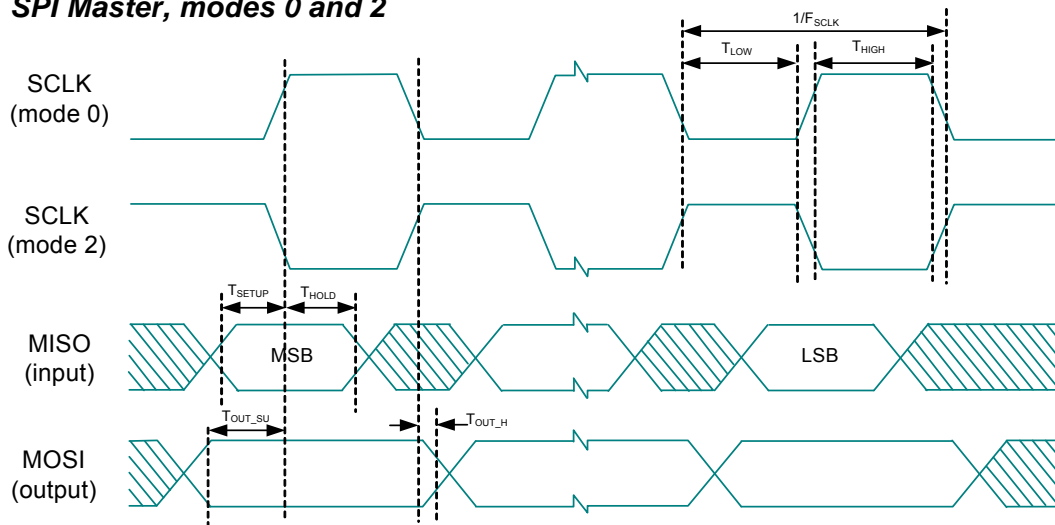


Figure 17. SPI Master Mode 1 and 3

SPI Master, modes 1 and 3

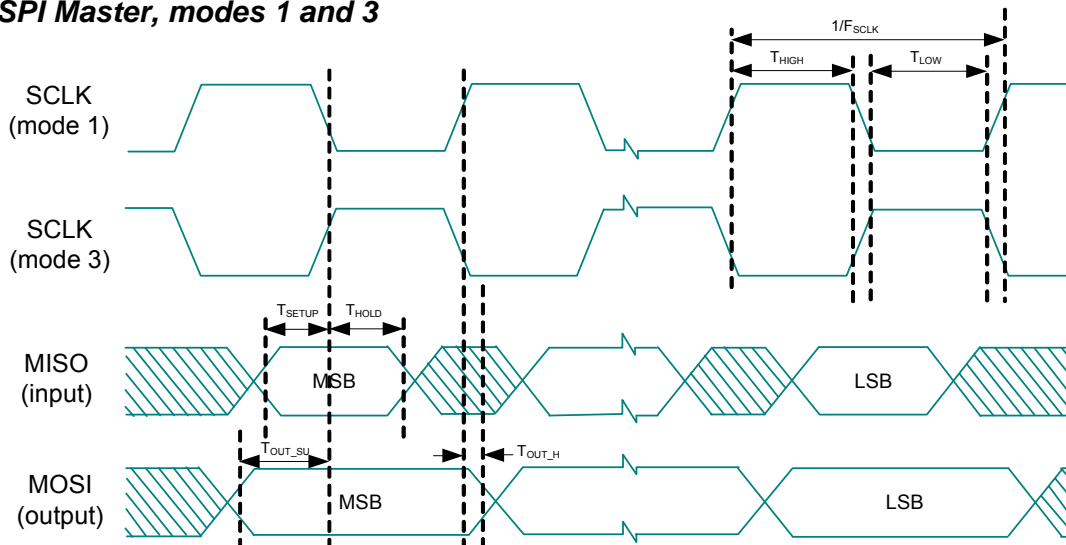


Table 36. SPI Slave AC Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|------------------|--------------------------------|------------|--------|-----|-----|-------|
| F_{SCLK} | SCLK clock frequency | – | – | – | 4 | MHz |
| t_{LOW} | SCLK low time | – | 42 | – | – | ns |
| t_{HIGH} | SCLK high time | – | 42 | – | – | ns |
| t_{SETUP} | MOSI to SCLK setup time | – | 30 | – | – | ns |
| t_{HOLD} | SCLK to MOSI hold time | – | 50 | – | – | ns |
| t_{SS_MISO} | SS high to MISO valid | – | – | – | 153 | ns |
| t_{SCLK_MISO} | SCLK to MISO valid | – | – | – | 125 | ns |
| t_{SS_HIGH} | SS high time | – | 50 | – | – | ns |
| t_{SS_CLK} | Time from SS low to first SCLK | – | 2/SCLK | – | – | ns |
| t_{CLK_SS} | Time from last SCLK to SS high | – | 2/SCLK | – | – | ns |

Figure 18. SPI Slave Mode 0 and 2

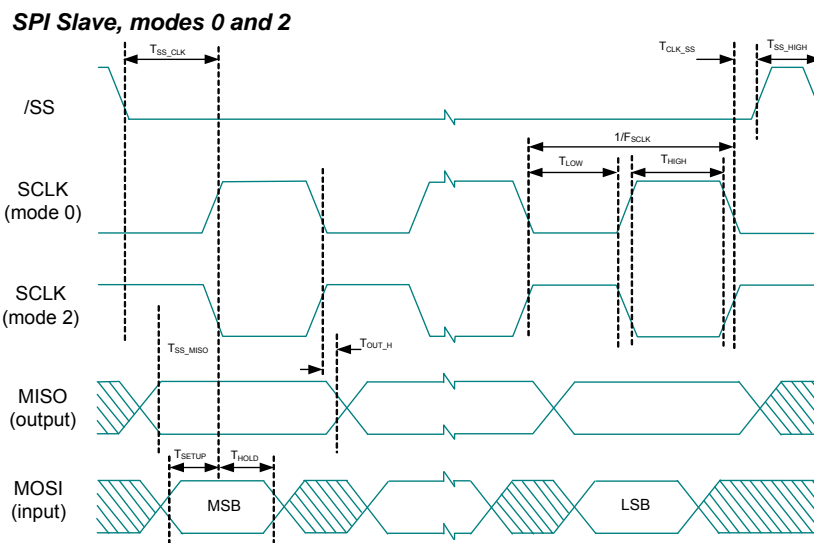
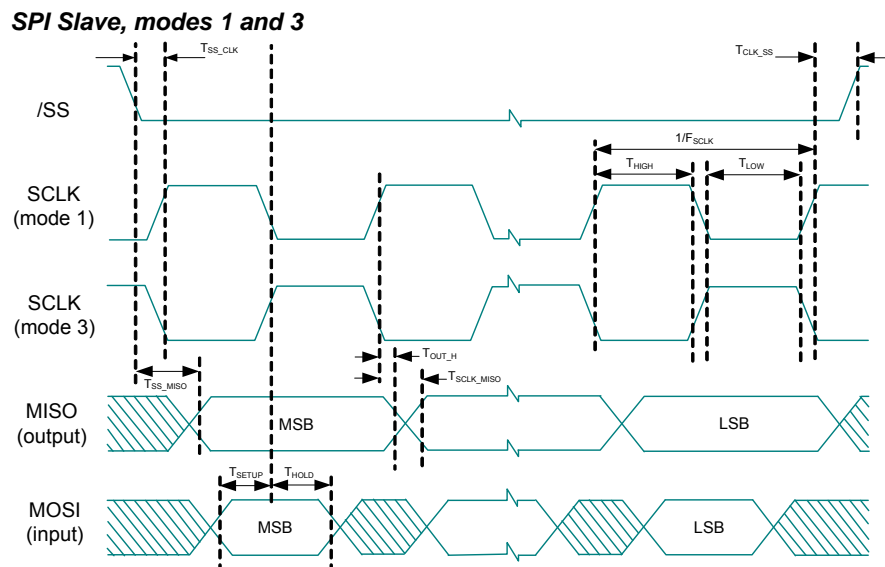


Figure 19. SPI Slave Mode 1 and 3

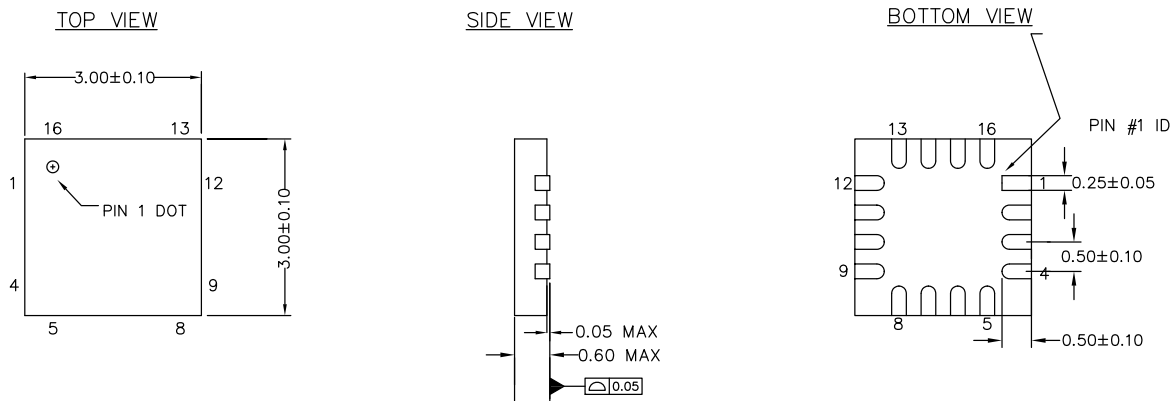


Packaging Information

This section illustrates the packaging specifications for the CY8C20XX6A/S PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at <http://www.cypress.com/design/MR10161>.

Figure 20. 16-pin QFN (No E-Pad) (3 × 3 × 0.6 mm) LG16A (Sawn) Package Outline, 001-09116

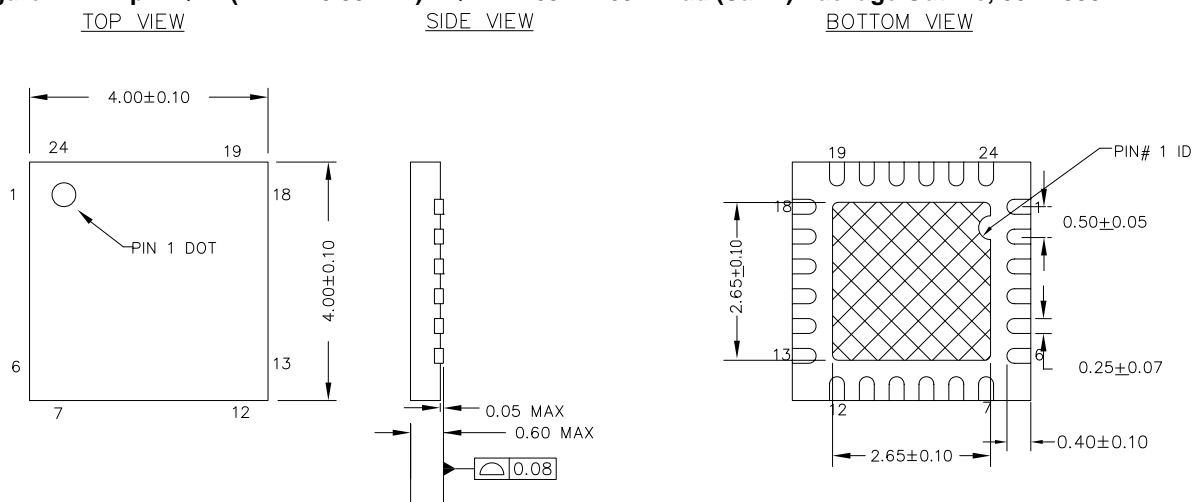


NOTES


1. REFERENCE JEDEC # MO-220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *1

Figure 21. 24-pin QFN (4 × 4 × 0.55 mm) LQ24A 2.65 × 2.65 E-Pad (Sawn) Package Outline, 001-13937

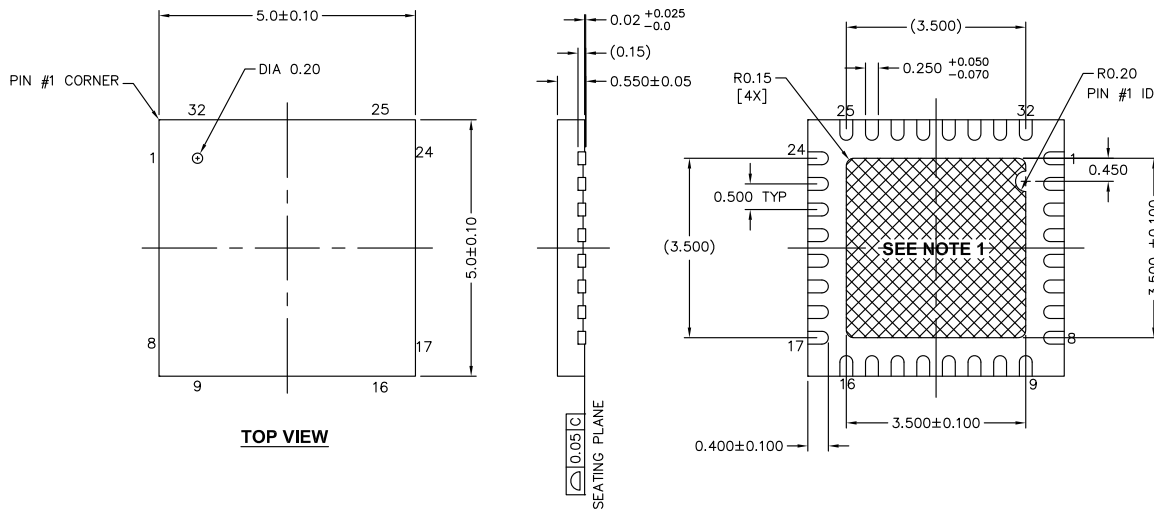


NOTES :


1.  HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *E

Figure 22. 32-pin QFN (5 x 5 x 0.55 mm) LQ32 3.5 x 3.5 E-Pad (Sawn) Package Outline, 001-42168



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

Figure 23. 48-pin SSOP (300 Mils) O483 Package Outline, 51-85061

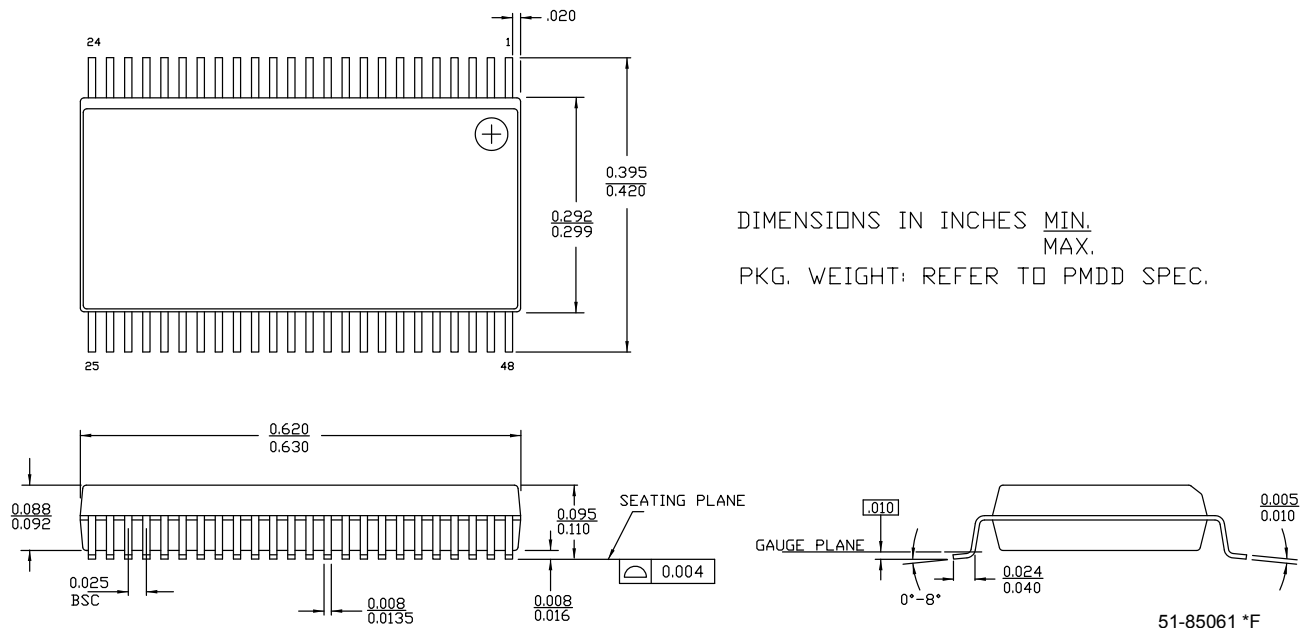
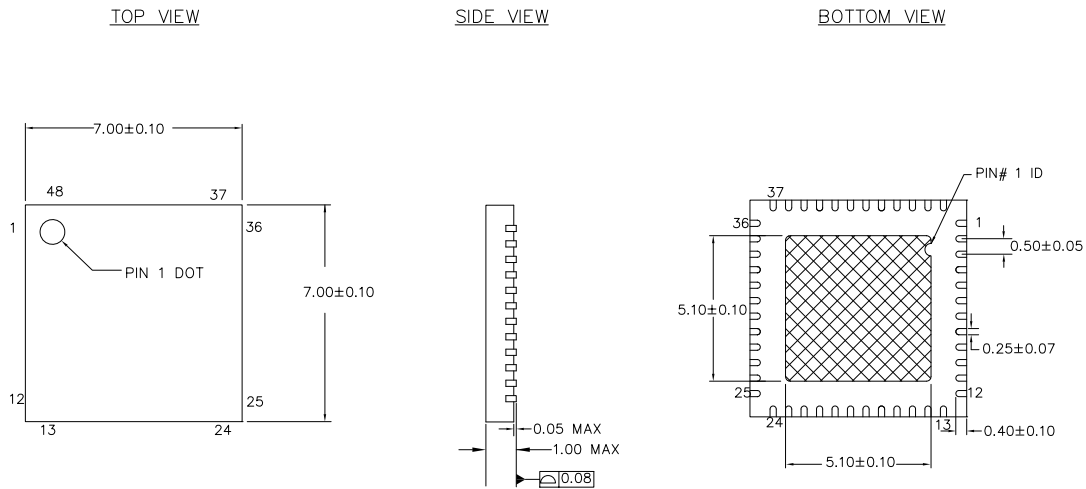



Figure 24. 48-pin QFN (7 x 7 x 1.0 mm) LT48A 5.1 x 5.1 E-Pad (Sawn) Package Outline, 001-13191

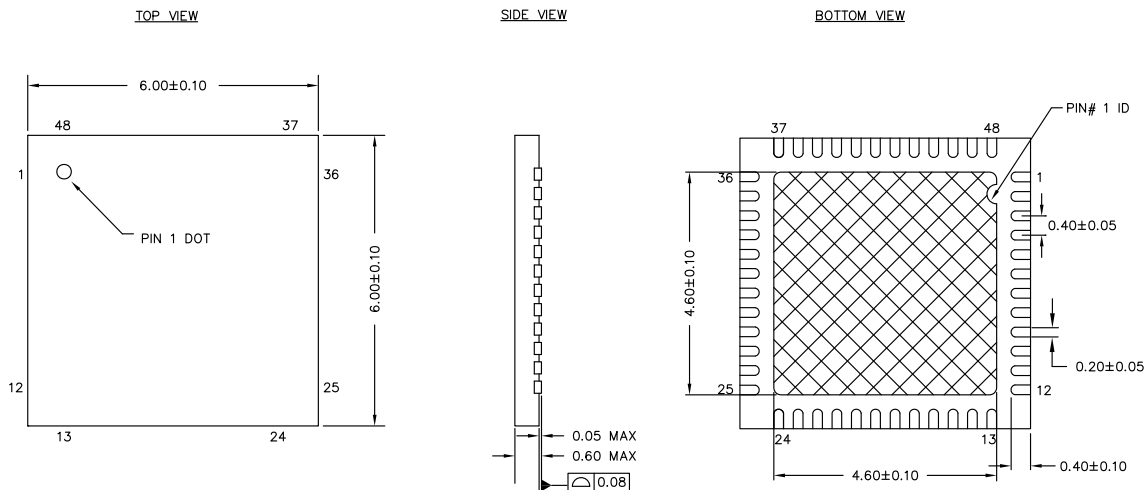


NOTES:


1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *G

Figure 25. 48-pin QFN (6 x 6 x 0.6 mm) LQ48A 4.6 x 4.6 E-Pad (Sawn) Package Outline, 001-57280



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ± 7 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-57280 *E

Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Thermal Impedances
Table 37. Thermal Impedances per Package

| Package | Typical θ_{JA} ^[63] | Typical θ_{JC} |
|---|---------------------------------------|-----------------------|
| 16-pin QFN (No Center Pad) | 33 °C/W | – |
| 24-pin QFN ^[64] | 21 °C/W | – |
| 32-pin QFN ^[64] | 20 °C/W | – |
| 48-pin SSOP | 69 °C/W | – |
| 48-pin QFN (6 × 6 × 0.6 mm) ^[64] | 25.20 °C/W | 3.04 °C/W |
| 48-pin QFN (7 × 7 × 1.0 mm) ^[64] | 18 °C/W | – |
| 30-ball WLCSP | 54 °C/W | – |

Capacitance on Crystal Pins
Table 38. Typical Package Capacitance on Crystal Pins

| Package | Package Capacitance |
|------------|---------------------|
| 32-pin QFN | 3.2 pF |
| 48-pin QFN | 3.3 pF |

Solder Reflow Specifications

Table 39 shows the solder reflow temperature limits that must not be exceeded.

Table 39. Solder Reflow Specifications

| Package | Maximum Peak Temperature (T_C) | Maximum Time above $T_C - 5$ °C |
|-----------------------------|------------------------------------|---------------------------------|
| 16-pin QFN | 260 °C | 30 seconds |
| 24-pin QFN | 260 °C | 30 seconds |
| 32-pin QFN | 260 °C | 30 seconds |
| 48-pin SSOP | 260 °C | 30 seconds |
| 48-pin QFN (6 × 6 × 0.6 mm) | 260 °C | 30 seconds |
| 48-pin QFN (7 × 7 × 1.0 mm) | 260 °C | 30 seconds |
| 30-ball WLCSP | 260 °C | 30 seconds |

Notes

63. $T_J = T_A + \text{Power} \times \theta_{JA}$.

64. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at <http://www.cypress.com>.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at <http://www.cypress.com>.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29X66A Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466A-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board

- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample
- 28-pin CY8C27443A-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466A-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3280-20X66 Universal CapSense Controller

The CY3280-20X66 CapSense Controller Kit is designed for easy prototyping and debug of CY8C20XX6A CapSense Family designs with pre-defined control circuitry and plug-in hardware. Programming hardware and an I2C-to-USB bridge are included for tuning and data acquisition.

The kit includes:

- CY3280-20X66 CapSense Controller Board
- CY3240-I2USB Bridge
- CY3210 MiniProg1 Programmer
- USB 2.0 Retractable Cable
- CY3280-20X66 Kit CD

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.

Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)
Table 40. Emulation and Programming Accessories

| Part Number | Pin Package | Flex-Pod Kit ^[65] | Foot Kit ^[66] | Adapter ^[67] |
|--------------------|-----------------------|------------------------------|--------------------------|-------------------------|
| CY8C20236A-24LKXI | 16-pin QFN (No E-Pad) | CY3250-20246QFN | CY3250-20246QFN-POD | See note 64 |
| CY8C20246A-24LKXI | 16-pin QFN (No E-Pad) | CY3250-20246QFN | CY3250-20246QFN-POD | See note 67 |
| CY8C20246AS-24LKXI | 16-pin QFN (No E-Pad) | Not Supported | | |
| CY8C20336A-24LQXI | 24-pin QFN | CY3250-20346QFN | CY3250-20346QFN-POD | See note 64 |
| CY8C20346A-24LQXI | 24-pin QFN | CY3250-20346QFN | CY3250-20346QFN-POD | See note 67 |
| CY8C20346AS-24LQXI | 24-pin QFN | Not Supported | | |
| CY8C20396A-24LQXI | 24-pin QFN | Not Supported | | |
| CY8C20436A-24LQXI | 32-pin QFN | CY3250-20466QFN | CY3250-20466QFN-POD | See note 64 |
| CY8C20446A-24LQXI | 32-pin QFN | CY3250-20466QFN | CY3250-20466QFN-POD | See note 67 |
| CY8C20446AS-24LQXI | 32-pin QFN | Not Supported | | |
| CY8C20466A-24LQXI | 32-pin QFN | CY3250-20466QFN | CY3250-20466QFN-POD | See note 67 |
| CY8C20466AS-24LQXI | 32-pin QFN | Not Supported | | |
| CY8C20496A-24LQXI | 32-pin QFN | Not Supported | | |
| CY8C20536A-24PVXI | 48-pin SSOP | CY3250-20566 | CY3250-20566-POD | See note 67 |
| CY8C20546A-24PVXI | 48-pin SSOP | CY3250-20566 | CY3250-20566-POD | See note 67 |
| CY8C20566A-24PVXI | 48-pin SSOP | CY3250-20566 | CY3250-20566-POD | See note 67 |

Third Party Tools

Several tools have been specially designed by third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at <http://www.cypress.com> under Documentation > Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note [Debugging - Build a PSoC Emulator into Your Board – AN2323](#).

Notes

65. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.

66. Foot kit includes surface mount feet that can be soldered to the target PCB.

67. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at <http://www.emulation.com>.

Ordering Information

The following table lists the CY8C20XX6A/S PSoC devices' key package features and ordering codes.

Table 41. PSoC Device Key Features and Ordering Information

| Package | Ordering Code | Flash (Bytes) | SRAM (Bytes) | CapSense Blocks | Digital I/O Pins | Analog Inputs ^[68] | XRES Pin | USB | ADC |
|--|---------------------|---------------|--------------|-----------------|------------------|-------------------------------|----------|-----|-----|
| 16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) | CY8C20236A-24LKXI | 8 K | 1 K | 1 | 13 | 13 | Yes | No | Yes |
| 16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) (Tape and Reel) | CY8C20236A-24LKXIT | 8 K | 1 K | 1 | 13 | 13 | Yes | No | Yes |
| 16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) | CY8C20246A-24LKXI | 16 K | 2 K | 1 | 13 | 13 | Yes | No | Yes |
| 16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) | CY8C20246AS-24LKXI | 16 K | 2 K | 1 | 13 | 13 | Yes | No | Yes |
| 16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) (Tape and Reel) | CY8C20246A-24LKXIT | 16 K | 2 K | 1 | 13 | 13 | Yes | No | Yes |
| 16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) (Tape and Reel) | CY8C20246AS-24LKXIT | 16 K | 2 K | 1 | 13 | 13 | Yes | No | Yes |
| 24-pin (4 × 4 × 0.6 mm) QFN | CY8C20336A-24LQXI | 8 K | 1 K | 1 | 20 | 20 | Yes | No | Yes |
| 24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel) | CY8C20336A-24LQXIT | 8 K | 1 K | 1 | 20 | 20 | Yes | No | Yes |
| 24-pin (4 × 4 × 0.6 mm) QFN | CY8C20346A-24LQXI | 16 K | 2 K | 1 | 20 | 20 | Yes | No | Yes |
| 24-pin (4 × 4 × 0.6 mm) QFN | CY8C20346AS-24LQXI | 16 K | 2 K | 1 | 20 | 20 | Yes | No | Yes |
| 24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel) | CY8C20346A-24LQXIT | 16 K | 2 K | 1 | 20 | 20 | Yes | No | Yes |
| 24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel) | CY8C20346AS-24LQXIT | 16 K | 2 K | 1 | 20 | 20 | Yes | No | Yes |
| 24-pin (4 × 4 × 0.6 mm) QFN | CY8C20396A-24LQXI | 16 K | 2 K | 1 | 19 | 19 | Yes | Yes | Yes |
| 24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel) | CY8C20396A-24LQXIT | 16 K | 2 K | 1 | 19 | 19 | Yes | Yes | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN | CY8C20436A-24LQXI | 8 K | 1 K | 1 | 28 | 28 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel) | CY8C20436A-24LQXIT | 8 K | 1 K | 1 | 28 | 28 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN | CY8C20446A-24LQXI | 16 K | 2 K | 1 | 28 | 28 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN | CY8C20446AS-24LQXI | 16 K | 2 K | 1 | 28 | 28 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel) | CY8C20446A-24LQXIT | 16 K | 2 K | 1 | 28 | 28 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel) | CY8C20446AS-24LQXIT | 16 K | 2 K | 1 | 28 | 28 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN | CY8C20466A-24LQXI | 32 K | 2 K | 1 | 28 | 28 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN | CY8C20466AS-24LQXI | 32 K | 2 K | 1 | 28 | 28 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel) | CY8C20466A-24LQXIT | 32 K | 2 K | 1 | 28 | 28 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel) | CY8C20466AS-24LQXIT | 32 K | 2 K | 1 | 28 | 28 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN | CY8C20496A-24LQXI | 16 K | 2 K | 1 | 25 | 25 | Yes | Yes | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel) | CY8C20496A-24LQXIT | 16 K | 2 K | 1 | 25 | 25 | Yes | Yes | Yes |

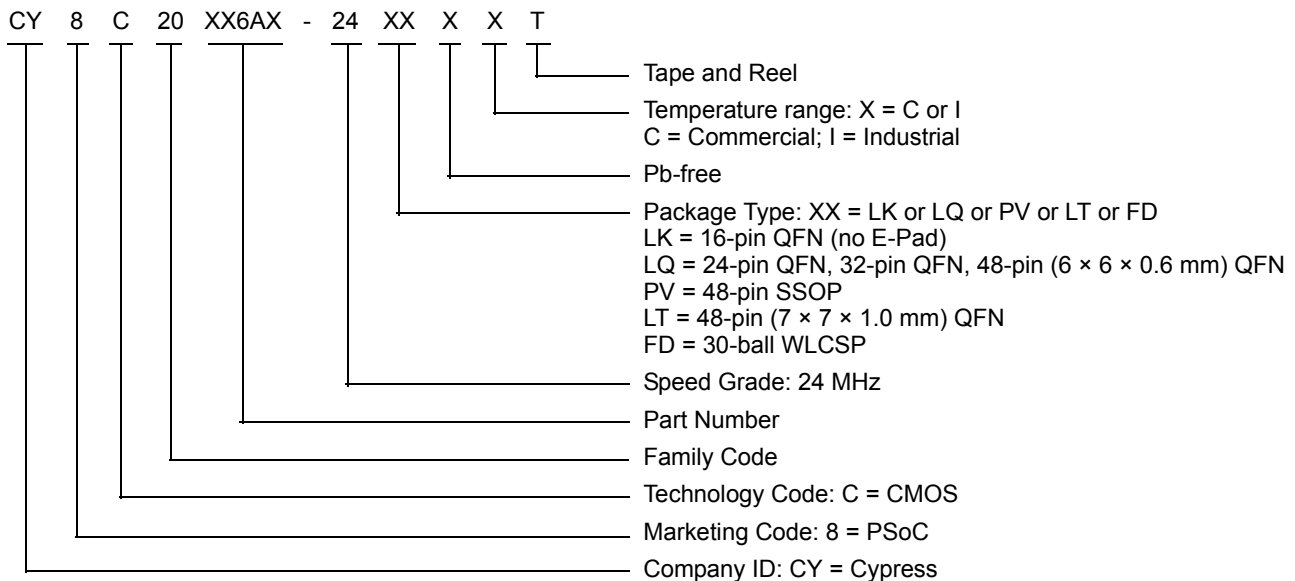
Table 41. PSoC Device Key Features and Ordering Information (continued)

| Package | Ordering Code | Flash (Bytes) | SRAM (Bytes) | CapSense Blocks | Digital I/O Pins | Analog Inputs ^[68] | XRES Pin | USB | ADC |
|---|-------------------------------------|---------------|--------------|-----------------|------------------|-------------------------------|----------|-----|-----|
| 48-pin SSOP ^[69] | CY8C20536A-24PVXI ^[69] | 8 K | 1 K | 1 | 34 | 34 | Yes | No | Yes |
| 48-pin SSOP (Tape and Reel) ^[69] | CY8C20536A-24PVXIT ^[69] | 8 K | 1 K | 1 | 34 | 34 | Yes | No | Yes |
| 48-pin SSOP ^[69] | CY8C20546A-24PVXI ^[69] | 16 K | 2 K | 1 | 34 | 34 | Yes | No | Yes |
| 48-pin SSOP (Tape and Reel) ^[69] | CY8C20546A-24PVXIT ^[69] | 16 K | 2 K | 1 | 34 | 34 | Yes | No | Yes |
| 48-pin SSOP ^[69] | CY8C20566A-24PVXI ^[69] | 32 K | 2 K | 1 | 34 | 34 | Yes | No | Yes |
| 48-pin SSOP (Tape and Reel) ^[69] | CY8C20566A-24PVXIT ^[69] | 32 K | 2 K | 1 | 34 | 34 | Yes | No | Yes |
| 48-pin (6 × 6 × 0.6 mm) QFN | CY8C20636A-24LQXI | 8 K | 1 K | 1 | 36 | 36 | Yes | No | Yes |
| 48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel) | CY8C20636A-24LQXIT | 8 K | 1 K | 1 | 36 | 36 | Yes | No | Yes |
| 48-pin (7 × 7 × 1.0 mm) QFN ^[69] | CY8C20636A-24LTXI ^[69] | 8 K | 1 K | 1 | 36 | 36 | Yes | No | Yes |
| 48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) ^[69] | CY8C20636A-24LTXIT ^[69] | 8 K | 1 K | 1 | 36 | 36 | Yes | No | Yes |
| 48-pin (6 × 6 × 0.6 mm) QFN | CY8C20646A-24LQXI | 16 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel) | CY8C20646A-24LQXIT | 16 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (7 × 7 × 1.0 mm) QFN ^[69] | CY8C20646A-24LTXI ^[69] | 16 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) ^[69] | CY8C20646A-24LTXIT ^[69] | 16 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (6 × 6 × 0.6 mm) QFN | CY8C20666A-24LQXI | 32 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel) | CY8C20666A-24LQXIT | 32 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (7 × 7 × 1.0 mm) QFN ^[69] | CY8C20666A-24LTXI ^[69] | 32 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (7 × 7 × 1.0 mm) QFN ^[69] | CY8C20666AS-24LTXI ^[69] | 32 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) ^[69] | CY8C20666A-24LTXIT ^[69] | 32 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) ^[69] | CY8C20666AS-24LTXIT ^[69] | 32 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (7 × 7 × 1.0 mm) QFN (OCD) ^[68] | CY8C20066A-24LTXI ^[68] | 32 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 30-ball WLCSP | CY8C20746A-24FDXC | 16 K | 1 K | 1 | 27 | 27 | Yes | No | Yes |
| 30-ball WLCSP (Tape and Reel) | CY8C20746A-24FDXCT | 16 K | 1 K | 1 | 27 | 27 | Yes | No | Yes |
| 30-ball WLCSP | CY8C20766A-24FDXC | 32 K | 2 K | 1 | 27 | 27 | Yes | No | Yes |
| 30-ball WLCSP (Tape and Reel) | CY8C20766A-24FDXCT | 32 K | 2 K | 1 | 27 | 27 | Yes | No | Yes |
| 24-pin (4 × 4 × 0.6 mm) QFN | CY8C20336AN-24LQXI | 8 K | 1 K | 1 | 20 | 20 | Yes | No | No |
| 24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel) | CY8C20336AN-24LQXIT | 8 K | 1 K | 1 | 20 | 20 | Yes | No | No |
| 32-pin (5 × 5 × 0.6 mm) QFN | CY8C20436AN-24LQXI | 8 K | 1 K | 1 | 28 | 28 | Yes | No | No |
| 32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel) | CY8C20436AN-24LQXIT | 8 K | 1 K | 1 | 28 | 28 | Yes | No | No |
| 48-pin (7 × 7 × 1.0 mm) QFN ^[69] | CY8C20636AN-24LTXI ^[69] | 8 K | 1 K | 1 | 36 | 36 | Yes | No | No |
| 48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) ^[69] | CY8C20636AN-24LTXIT ^[69] | 8 K | 1 K | 1 | 36 | 36 | Yes | No | No |

Table 41. PSoC Device Key Features and Ordering Information (continued)

| Package | Ordering Code | Flash (Bytes) | SRAM (Bytes) | CapSense Blocks | Digital I/O Pins | Analog Inputs ^[68] | XRES Pin | USB | ADC |
|---|-------------------------------------|---------------|--------------|-----------------|------------------|-------------------------------|----------|-----|-----|
| 16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) | CY8C20246AS-24LKXI | 16 K | 2 K | 1 | 13 | 13 | Yes | No | Yes |
| 16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad, Tape and Reel) | CY8C20246AS-24LKXIT | 16 K | 2 K | 1 | 13 | 13 | Yes | No | Yes |
| 24-pin (4 × 4 × 0.6 mm) QFN | CY8C20346AS-24LQXI | 16 K | 2 K | 1 | 20 | 20 | Yes | No | Yes |
| 24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel) | CY8C20346AS-24LQXIT | 16 K | 2 K | 1 | 20 | 20 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN | CY8C20446AS-24LQXI | 16 K | 2 K | 1 | 28 | 28 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel) | CY8C20446AS-24LQXIT | 16 K | 2 K | 1 | 28 | 28 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN | CY8C20466AS-24LQXI | 32 K | 2 K | 1 | 28 | 28 | Yes | No | Yes |
| 32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel) | CY8C20466AS-24LQXIT | 32 K | 2 K | 1 | 28 | 28 | Yes | No | Yes |
| 48-pin (6 × 6 × 0.6 mm) QFN | CY8C20666AS-24LQXI | 32 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel) | CY8C20666AS-24LQXIT | 32 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (7 × 7 × 1.0 mm) QFN ^[69] | CY8C20666AS-24LTXI ^[69] | 32 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) ^[69] | CY8C20666AS-24LTXIT ^[69] | 32 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (6 × 6 × 0.6 mm) QFN | CY8C20646AS-24LQXI | 16 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel) | CY8C20646AS-24LQXIT | 16 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (7 × 7 × 1.0 mm) QFN ^[69] | CY8C20646AS-24LTXI ^[69] | 16 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |
| 48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) ^[69] | CY8C20646AS-24LTXIT ^[69] | 16 K | 2 K | 1 | 36 | 36 | Yes | Yes | Yes |

Ordering Code Definitions



Notes

- 68. Dual-function Digital I/O Pins also connect to the common analog mux.
- 69. Not Recommended for New Designs.

Acronyms

Table 42. Acronyms Used in this Document

| Acronym | Description |
|-------------------|---|
| AC | alternating current |
| ADC | analog-to-digital converter |
| API | application programming interface |
| CMOS | complementary metal oxide semiconductor |
| CPU | central processing unit |
| DAC | digital-to-analog converter |
| DC | direct current |
| EOP | end of packet |
| FSR | full scale range |
| GPIO | general purpose input/output |
| GUI | graphical user interface |
| I ² C | inter-integrated circuit |
| ICE | in-circuit emulator |
| IDAC | digital analog converter current |
| ILO | internal low speed oscillator |
| IMO | internal main oscillator |
| I/O | input/output |
| ISSP | in-system serial programming |
| LCD | liquid crystal display |
| LDO | low dropout (regulator) |
| LSB | least-significant bit |
| LVD | low voltage detect |
| MCU | micro-controller unit |
| MIPS | mega instructions per second |
| MISO | master in slave out |
| MOSI | master out slave in |
| MSB | most-significant bit |
| OCD | on-chip debugger |
| POR | power on reset |
| PPOR | precision power on reset |
| PSRR | power supply rejection ratio |
| PWRSYS | power system |
| PSoC [®] | Programmable System-on-Chip |
| SLIMO | slow internal main oscillator |
| SRAM | static random access memory |
| SNR | signal to noise ratio |
| QFN | quad flat no-lead |
| SCL | serial I2C clock |
| SDA | serial I2C data |
| SDATA | serial ISSP data |
| SPI | serial peripheral interface |
| SS | slave select |
| SSOP | shrink small outline package |
| TC | test controller |
| USB | universal serial bus |
| USB D+ | USB Data+ |
| USB D- | USB Data- |
| WLCSP | wafer level chip scale package |
| XTAL | crystal |

Reference Documents

- *Technical reference manual for CY8C20xx6 devices*
- *In-system Serial Programming (ISSP) protocol for 20xx6 (AN2026C)*
- *Host Sourced Serial Programming for 20xx6 devices (AN59389)*

Document Conventions

Units of Measure

Table 43. Units of Measure

| Symbol | Unit of Measure |
|--------|-------------------------------|
| °C | degree Celsius |
| dB | decibels |
| fF | femtofarad |
| g | gram |
| Hz | hertz |
| KB | 1024 bytes |
| Kbit | 1024 bits |
| KHz | kilohertz |
| Ksps | kilo samples per second |
| kΩ | kilohm |
| MHz | megahertz |
| MΩ | megaohm |
| μA | microampere |
| μF | microfarad |
| μH | microhenry |
| μs | microsecond |
| μW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| nF | nanofarad |
| ns | nanosecond |
| nV | nanovolt |
| W | ohm |
| pA | picoampere |
| pF | picofarad |
| pp | peak-to-peak |
| ppm | parts per million |
| ps | picosecond |
| sps | samples per second |
| s | sigma: one standard deviation |
| V | volt |
| W | watt |

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

Glossary

| | |
|-------------------------------------|---|
| Crosspoint connection | Connection between any GPIO combination via analog multiplexer bus. |
| Differential non-linearity | Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step. |
| Hold time | Hold time is the time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct. |
| I ² C | It is a serial multi-master bus used to connect low speed peripherals to MCU. |
| Integral nonlinearity | It is a term describing the maximum deviation between the ideal output of a DAC/ADC and the actual output level. |
| Latch-up current | Current at which the latch-up test is conducted according to JESD78 standard (at 125 degree Celsius) |
| Power supply rejection ratio (PSRR) | The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage of the device. |
| Scan | The conversion of all sensor capacitances to digital values. |
| Setup time | Period required to prepare a device, machine, process, or system for it to be ready to function. |
| Signal-to-noise ratio | The ratio between a capacitive finger signal and system noise. |
| SPI | Serial peripheral interface is a synchronous serial data link standard. |

Errata

This section describes the errata for the PSoC[®] CY8C20x36A/46A/66A/96A/46AS/66AS/36H/46H families. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Qualification Status

Product Status: Production released.

Errata Summary

The following Errata items apply to CY8C20x36A/46A/66A/96A/46AS/66AS/36H/46H families.

1. Wakeup from sleep may intermittently fail

■ Problem Definition

When the device is put to sleep in Standby or I2C_USB Mode and the bandgap circuit is refreshed less frequently than every 8 ms (default), the device may not come out of sleep when a sleep-ending input is received.

■ Parameters Affected

None

■ Trigger Condition(S)

By default, when the device is in the Standby or I2C_USB sleep modes, the bandgap circuit is powered-up approximately every 8 ms to facilitate detection of POR or LVD events. This interval can be lengthened or the periodic power-up disabled to reduce sleep current by setting the ALT_BUZZ bits in the SLP_CFG2 register or the Disable Buzz bit in the OSC_CR0 register respectively. If the bandgap circuit refresh interval is set longer than the default 8 ms, the device may fail to wakeup from sleep and enter a locked up state that can only be recovered by Watchdog Reset, XRES, or POR.

■ Scope of Impact

The trigger conditions outlined above may cause the device to never wakeup.

■ Workaround

Prior to entering Standby or I2C_USB sleep modes, do not lengthen or disable the bandgap refresh interval by manipulating the ALT_BUZZ bits in the SLP_CFG2 register or the Disable Buzz bit in the OSC_CR0 register respectively.

■ Fix Status

This issue will not be corrected in the next silicon revision.

2. I²C Errors

■ Problem Definition

The I²C block exhibits occasional data and bus corruption errors when the I²C master initiates transactions while the device is transitioning in to or out of sleep mode.

■ Parameters Affected

Affects reliability of I²C communication to device, and between I²C master and third party I²C slaves.

■ Trigger Condition(S)

Triggered by transitions into and out of the device's sleep mode.

■ Scope of Impact

Data errors result in incorrect data reported to the I²C master, or incorrect data received from the master by the device. Bus corruption errors can corrupt data in transactions between the I²C master and third party I²C slaves.

■ Workaround

Firmware workarounds are available in firmware. Generally the workaround consists of disconnecting the I²C block from the bus prior to going to sleep modes. I²C transactions during sleep are supported by a protocol in which the master wakes the device prior to the I²C transaction.

■ Fix Status

To be fixed in future silicon.

■ **Changes**

None

3. DoubleTimer0 ISR

■ **Problem Definition**

When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice.

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling one-shot mode in the timer, and using the timer to wake from sleep mode.

■ **Scope of Impact**

The ISR may be executed twice.

■ **Workaround**

In the ISR, firmware should clear the one-shot bit with a statement such as “and reg[B0h], FDh”

■ **Fix Status**

Will not be fixed

■ **Changes**

None

4. Missed GPIO Interrupt

■ **Problem Definition**

When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run.

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling sleep mode, then having GPIO interrupt occur simultaneously with a Timer 0 or Sleep Timer interrupt.

■ **Scope of Impact**

The GPIO interrupt service routine will not be run.

■ **Workaround**

The system should be architected such that a missed GPIO interrupt may be detected. For example, if a GPIO is used to wake the system to perform some function, the system should detect if the function is not performed, and re-issue the GPIO interrupt.

Alternatively, if a GPIO interrupt is required to wake the system, then firmware should disable the Sleep Timer and Timer0.

Alternatively, the ISR's for Sleep Timer and Timer0 should manually check the state of the GPIO to determine if the host system has attempted to generate a GPIO interrupt.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

5. Missed Interrupt During Transition to Sleep

■ Problem Definition

If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed.

■ Parameters Affected

No datasheet parameters are affected.

■ Trigger Condition(S)

Triggered by enabling sleep mode just prior to an interrupt.

■ Scope of Impact

The relevant interrupt service routine will not be run.

■ Workaround

None.

■ Fix Status

Will not be fixed

■ Changes

None

6. Wakeup from sleep with analog interrupt

■ Problem Definition

Device wakes up from sleep when an analog interrupt is trigger

■ Parameters Affected

No datasheet parameters are affected.

■ Trigger Condition(S)

Triggered by enabling analog interrupt during sleep mode when device operating temperature is 50 °C or above

■ Scope of Impact

Device unexpectedly wakes up from sleep

■ Workaround

Disable the analog interrupt before entering sleep and turn it back on upon wakeup.

■ Fix Status

Will not be fixed

■ Changes

None

Document History Page

| Document Title: CY8C20XX6A/S, 1.8 V Programmable CapSense® Controller with SmartSense™ Auto-tuning 1–33 Buttons, 0–6 Sliders | | | | |
|--|---------|-----------------|-----------------|---|
| Document Number: 001-54459 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 2737924 | SNV | 07/14/09 | New silicon and document |
| *A | 2764528 | MATT | 09/16/2009 | Updated AC Chip Level Specifications Updated ADC User Module Electrical Specifications table Added Note 5. Added SR _{POWER_UP} parameter. Updated Ordering information. Updated Capacitance on Crystal Pins |
| *B | 2803229 | VZD | 11/10/09 | Added “Contents” on page 3. Added Note 6 on page 20. Edited Features section to include reference to Incremental ADC. |
| *C | 2846083 | DST / KEJO | 01/12/2010 | Updated “AC Programming Specifications” on page 30 per CDT 56531. Updated Idd typical values in “DC Chip-Level Specifications” on page 20. Added 30-pin WLCSP pin and package details. Added Contents on page 2. |
| *D | 2935141 | KEJO/ISW / SSSH | 03/05/2010 | Updated “Features” on page 1. Added “SmartSense” on page 4. Updated “PSoC® Functional Overview” on page 4. Removed SNR statement regarding on page 4 (Analog Multiplexer section). Updated “” on page 7 with the I2C enhanced slave interface point. Removed references to “system level” in “Designing with PSoC Designer” on page 8. Changed TC CLK and TC DATA to ISSP CLK and ISSP DATA respectively in all the pinouts. Modified notes in Pinouts. Updated 30-ball pin diagram. Removed IMO frequency trim options diagram in “Electrical Specifications” on page 19. Updated and formatted values in DC and AC specifications. Updated Ordering information table. Updated 48-pin SSOP package diagram. Added 30-Ball WLCSP package spec 001-50669. Removed AC Analog Mux Bus Specifications section. Added SPI Master and Slave mode diagrams. Modified Definition for Timing for Fast/Standard Mode on the I2C Bus on page 28 . Updated “Thermal Impedances” on page 37. Combined Development Tools with “Development Tool Selection” on page 38. Removed references to “system level”. Updated “Evaluation Tools” on page 38. Added “Ordering Code Definitions” on page 42. Updated “Acronyms” on page 43. Added Glossary and “Reference Documents” on page 43. Changed datasheet status from Preliminary to Final |
| *E | 3043291 | SAAC | 09/30/10 | Change: Added the line “Supports SmartSense” in the “Low power CapSense® block” bullet in the Features section. Impact: Helps to know that this part has the feature of Auto Tuning. Change: Replaced pod MPNs. Areas affected: Foot kit column of table 37. Change: Template and Styles update. Areas affected: Entire datasheet. Impact: Datasheet adheres to Cypress standards. |
| *F | 3071632 | JPX | 10/26/10 | In Table 36 on page 33 , modified t _{LOW} and t _{HIGH} min values to 42. Updated t _{SS_HIGH} min value to 50; removed max value. |

Document History Page *(continued)*

| Document Title: CY8C20XX6A/S, 1.8 V Programmable CapSense® Controller with SmartSense™ Auto-tuning 1–33 Buttons, 0–6 Sliders | | | | |
|--|---------|-------------------------------|-----------------|---|
| Document Number: 001-54459 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *G | 3247491 | TTO / JPM / ARVM / BVI | 06/16/11 | <p>Add 4 new parameters to Table 14 on page 21, and 2 new parameters to Table 15 on page 22.</p> <p>Changed Typ values for the following parameters: I_{DD24}, I_{DD12}, I_{DD6}, V_{OSLPC}.</p> <p>Added footnote # 40 and referred it to pin numbers 1, 14, 15, 42, and 43 under Table 10 on page 18.</p> <p>Added footnote # 43 and referred it to parameter V_{IOZ} under Table 11 on page 19.</p> <p>Added “t_{JIT_IMO}” parameter to Table 27 on page 27.</p> <p>Included footnote # 59 and added reference to t_{JIT_IMO} specification under Table 27 on page 27.</p> <p>Updated Solder Reflow Specifications on page 37 as per specs 25-00090 and 25-00103.</p> <p>I_{SB0} Max value changed from 0.5 μA to 1.1 μA in Table 13 on page 20.</p> <p>Added Table 26 on page 26.</p> <p>Updated part numbers for “SmartSense_EMC” enabled CapSense controller.</p> |
| *H | 3367332 | BTK / SSHH / JPM / TTO / VMAD | 09/09/11 | <p>Added parameter “t_{OS}” to Table 27 on page 27.</p> <p>Added parameter “I_{SB12C}” to Table 13 on page 20.</p> <p>Added Table 24 on page 26.</p> <p>Added Table 25 on page 26.</p> <p>Replaced text “Port 2 or 3 pins” with “Port 2 or 3 or 4 pins” in Table 14, Table 15, Table 16, and Table 28.</p> |
| *I | 3371807 | MATT | 09/30/2011 | <p>Updated Packaging Information (Updated the next revision package outline for Figure 20, Figure 23 and included a new package outline Figure 25).</p> <p>Updated Ordering Information (Added new part numbers CY8C20636A-24LQXI, CY8C20636A-24LQXIT, CY8C20646A-24LQXI, CY8C20646A-24LQXIT, CY8C20666A-24LQXI, CY8C20666A-24LQXIT, CY8C20666AS-24LQXI, CY8C20666AS-24LQXIT, CY8C20646AS-24LQXI and CY8C20646AS-24LQXIT).</p> <p>Updated in new template.</p> |
| *J | 3401666 | MATT | 10/11/2011 | No technical updates. |
| *K | 3414479 | KPOL | 10/19/2011 | <p>Removed clock stretching feature on page 1.</p> <p>Removed I²C enhanced slave interface point from Additional System Resources.</p> |
| *L | 3452591 | BVI / UDYG | 12/01/2011 | <p>Changed document title.</p> <p>Updated DC Chip-Level Specifications table.</p> <p>Updated Solder Reflow Specifications section.</p> <p>Updated Getting Started and Designing with PSoC Designer sections.</p> <p>Included Development Tools section.</p> <p>Updated Software under Development Tool Selection section.</p> |
| *M | 3473330 | ANBA | 12/22/2011 | Updated DC Chip-Level Specifications under Electrical Specifications (updated maximum value of I_{SB0} parameter from 1.1 μ A to 1.05 μ A). |
| *N | 3587003 | DST | 04/16/2012 | <p>Added note for WLCSP package on page 1.</p> <p>Added Sensing inputs to pin table captions.</p> <p>Updated Conditions for DC Reference Buffer Specifications.</p> <p>Updated t_{JIT_IMO} description in AC Chip-Level Specifications.</p> <p>Added note for $t_{VDDWAIT}$, $t_{VDDXRES}$, t_{ACQ}, and $t_{XRESINI}$ specs.</p> <p>Removed WLCSP package outline.</p> |
| *O | 3638569 | BVI | 06/06/2012 | <p>Updated F_{SCLK} parameter in the Table 36, “SPI Slave AC Specifications,” on page 33.</p> <p>Changed t_{OUT_HIGH} to t_{OUT_H} in Table 35, “SPI Master AC Specifications,” on page 32.</p> <p>Updated package diagram 001-57280 to *C revision.</p> |

Document History Page *(continued)*

| Document Title: CY8C20XX6A/S, 1.8 V Programmable CapSense® Controller with SmartSense™ Auto-tuning 1–33 Buttons, 0–6 Sliders Document Number: 001-54459 | | | | |
|--|---------|-----------------|-----------------|--|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *P | 3774062 | UBU | 10/11/2012 | Updated min value of parameter F _{32K1} (from 19 to 15) in the Table 27, “AC Chip-Level Specifications,” on page 27. Updated Packaging Information for 001-09116 (*F to *G), 001-13937 (*D to *E), 51-85061 (*E to *F), 001-13191 (*F to *G), and 001-57280 (*C to *D). |
| *Q | 3807186 | PKS | 15/11/2012 | No content update; appended to EROS document. |
| *R | 3836626 | SRLI | 01/03/2013 | Updated Document Title to read as “CY8C20XX6A/S, 1.8 V Programmable CapSense® Controller with SmartSense™ Auto-tuning 1–33 Buttons, 0–6 Sliders”. Updated Features . Updated PSoC® Functional Overview : Replaced “CY8C20X36A/46A/66A/96A/46AS/66AS” with “CY8C20XX6A/S”. Updated Getting Started : Replaced “CY8C20X36A/46A/66A/96A/46AS/66AS” with “CY8C20XX6A/S”. Updated Pinouts : Updated 16-pin QFN (10 Sensing Inputs)[3, 4] : Replaced “12 Sensing Inputs” with “10 Sensing Inputs” in heading, added Note 3 only. Updated 24-pin QFN (17 Sensing Inputs) [7] : Replaced “12 Sensing Inputs” with “17 Sensing Inputs” in heading, added Note 7 only. Updated 24-pin QFN (15 Sensing Inputs (With USB)) [11] : Replaced “18 Sensing Inputs” with “15 Sensing Inputs” in heading, added Note 11 only. Updated 30-ball WLCSP (24 Sensing Inputs) [15] : Replaced “26 Sensing Inputs” with “24 Sensing Inputs” in heading, added Note 15 only. Updated 32-pin QFN (25 Sensing Inputs) [18] : Replaced “27 Sensing Inputs” with “25 Sensing Inputs” in heading, added Note 18 only. updated 32-pin QFN (22 Sensing Inputs (With USB)) [22] : Replaced “24 Sensing Inputs” with “22 Sensing Inputs” in heading, added Note 22 only. Updated 48-pin SSOP (31 Sensing Inputs) [26] : Replaced “33 Sensing Inputs” with “31 Sensing Inputs” in heading, added Note 26 only. Updated 48-pin QFN (33 Sensing Inputs) [29] : Replaced “35 Sensing Inputs” with “33 Sensing Inputs” in heading, added Note 29 only. Updated 48-pin QFN (33 Sensing Inputs (With USB)) [33] : Replaced “35 Sensing Inputs” with “33 Sensing Inputs” in heading, added Note 33 only. Updated 48-pin QFN (OCD) (33 Sensing Inputs) [37] : Added “33 Sensing Inputs” in heading, added Note 37 only. Updated Packaging Information : spec 001-42168 – Changed revision from *D to *E. spec 001-57280 – Changed revision from *D to *E. |
| *S | 3997568 | BVI | 05/11/2013 | Added Errata . |
| *T | 4044148 | BVI | 06/28/2013 | Added Errata Footnotes. Updated Packaging Information : spec 001-09116 – Changed revision from *G to *H. Updated in new template. |
| *U | 4185313 | BVI | 11/07/2013 | Updated Features . Updated Packaging Information : spec 001-09116 – Changed revision from *H to *I. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|--------------------------|--|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

PSoC[®] Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

cypress.com/go/support

© Cypress Semiconductor Corporation, 2009-2013. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.