

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MB3244CFT, TC7MB3244CFK, TC7MB3244CFTG TC7MB3245CFT, TC7MB3245CFK, TC7MB3245CFTG

Low Capacitance Octal Bus Switch

The TC7MB3244C, TC7MB3245C is a Low ON-resistance / Low Capacitance CMOS 8bit Bus Switch. The low on-resistance of the switch allows connections to be made with minimal propagation delay time.

The TC7MB3244C is organized as two 4-bit low-impedance switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on and data can flow from port A to port B, or vice versa. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

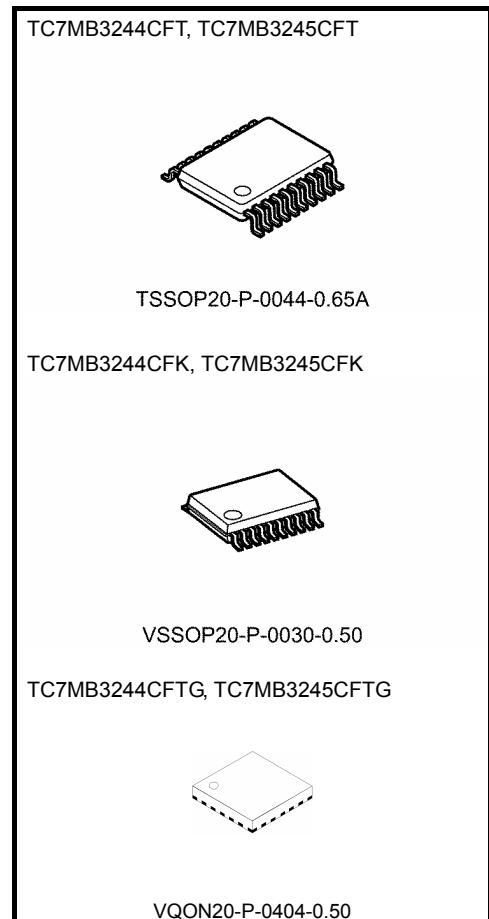
The TC7MB3245C requires the output enable (\overline{OE}) input to be set high to place the output into the high impedance.

All inputs are equipped with protection circuits against static discharge.

Features

- Operating voltage: $V_{CC} = 4.0$ to 5.5 V
- On-capacitance: $C_{I/O} = 7$ pF Switch On (typ.) @ $V_{CC} = 5$ V
- On-resistance: $R_{ON} = 3 \Omega$ (typ.) @ $V_{CC} = 4.5$ V, $V_{IS} = 0$ V
- ESD performance: Machine model $\geq \pm 200$ V
Human body model $\geq \pm 2000$ V
- Compatible with TTL outputs (control inputs)
- Power-down protection for inputs (\overline{OE} and I/O)
- Package: TSSOP20, VSSOP20 (US20), VQON20

Note: When mounting VQON package, the type of recommended flux is RA or RMA.



Weight

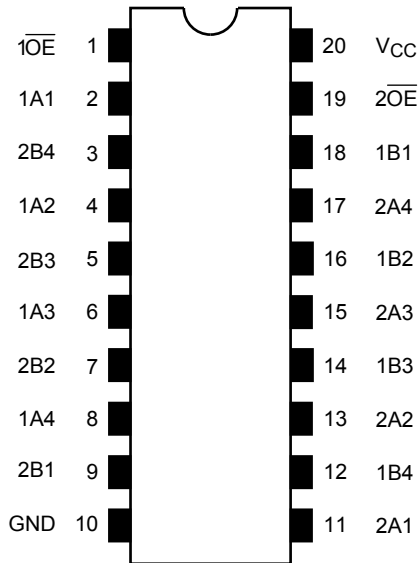
TSSOP20-P-0044-0.65A	: 0.08 g (typ.)
VSSOP20-P-0030-0.50	: 0.03 g (typ.)
VQON20-P-0404-0.50	: 0.0145g (typ.)

Start of commercial production
2011-05

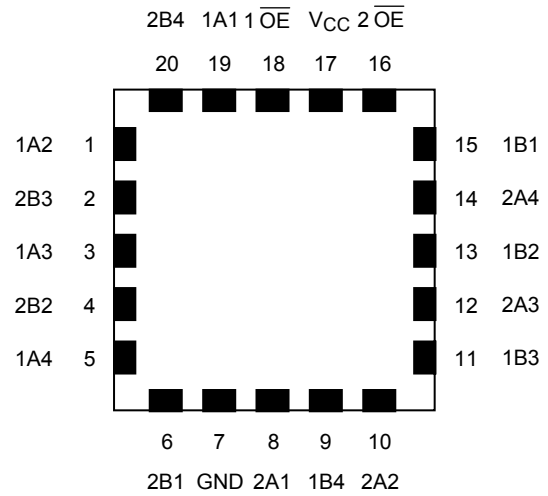
Pin Assignment (top view)

TC7MB3244C

FT (TSSOP20-P-0044-0.65A)
FK (VSSOP20-P-0030-0.50)

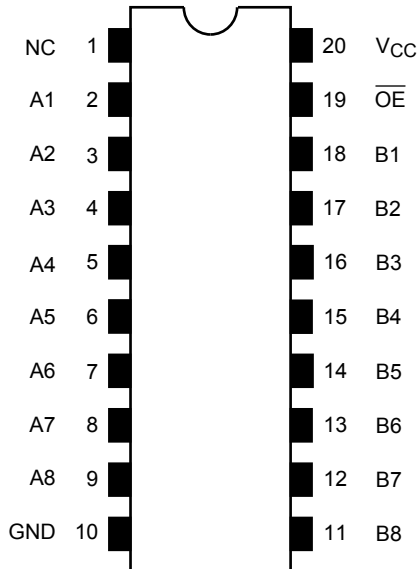


FTG (VQON20-P-0404-0.50)

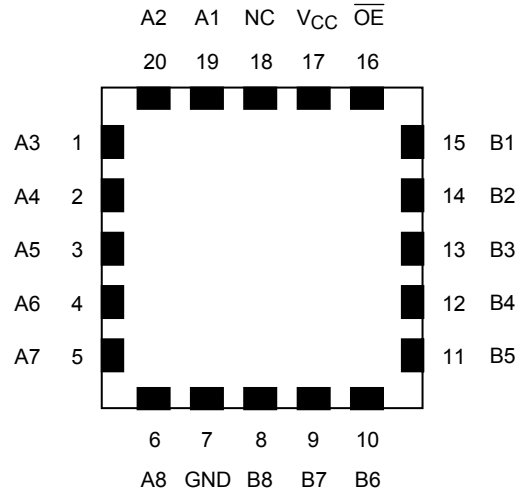


TC7MB3245C

FT (TSSOP20-P-0044-0.65A)
FK (VSSOP20-P-0030-0.50)



FTG (VQON20-P-0404-0.50)



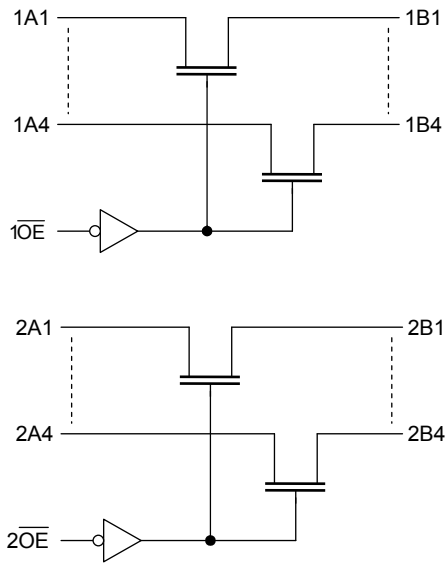
NC-No Internal Connection

Truth Table

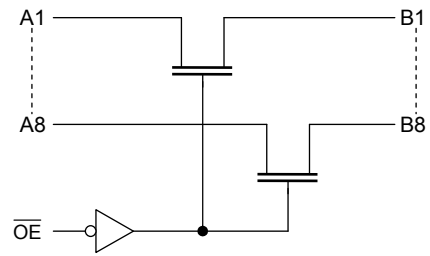
Inputs	Function
\overline{OE}	
L	A port = B port
H	Disconnect

System Diagram

TC7MB3244C



TC7MB3245C



Absolute Maximum Ratings (Note)

Characteristic	Symbol	Rating	Unit
Power supply range	V_{CC}	-0.5 to 7.0	V
Control pin input voltage (\overline{OE})	V_{IN}	-0.5 to 7.0	V
Switch terminal I/O voltage	V_S	-0.5 to 7.0	V
Clump diode current	I_{IK}	-50	mA
Switch I/O current	I_S	50	mA
Power dissipation	P_D	180	mW
DC V_{CC} /GND current	I_{CC}/I_{GND}	± 100	mA
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristic	Symbol	Rating	Unit
Power supply voltage	V_{CC}	4.0 to 5.5	V
Control pin input voltage (\overline{OE})	V_{IN}	0 to 5.5	V
Switch I/O voltage	V_S	0 to 5.5	V
Operating temperature	T_{opr}	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dv	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused control pin inputs must be tied to either V_{CC} or GND.

Leave unused switch I/O pins open.

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Typ.	Max	Unit	
Input voltage (\overline{OE})	"H" level	V _{IH}	—	4.0 to 5.5	2.0	—	—	V
	"L" level	V _{IL}	—	4.0 to 5.5	—	—	0.8	
Input leakage current (\overline{OE})	I _{IN}	V _{IN} = 0 to 5.5 V	4.0 to 5.5	—	—	±1.0	μA	
Power-off leakage current	I _{OFF}	\overline{OE} , A, B = 0 to 5.5 V	0	—	—	10	μA	
Off-state leakage current (switch off)	I _{SZ}	A, B = 0 to 5.5 V, $\overline{OE} = V_{CC}$	4.0 to 5.5	—	—	±1.0	μA	
On resistance (Mote1)(Note2)	R _{ON}	V _{IS} = 0 V, I _{IS} = 30 mA	4.5	—	3	7	Ω	
		V _{IS} = 2.4 V, I _{IS} = 15 mA	4.5	—	5	15		
			4.0	—	9	20		
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND, I _{OUT} = 0 V	5.5	—	—	10	μA	
	ΔI _{CC}	V _{IN} = 3.4 V (one input)	5.5	—	—	500	μA	

Note1: All typical values are at Ta=25°C.

Note2: Measured by the voltage drop between A and B pins at the indicated current through the switch.
On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = -40 to 85°C)

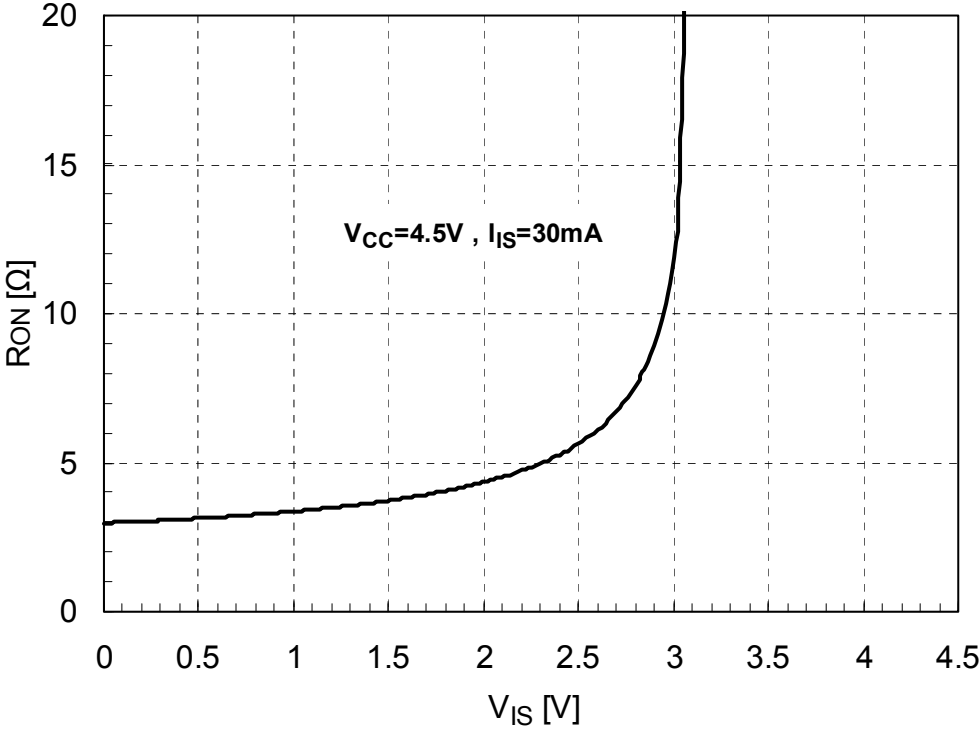
Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Output enable time	t _{pZL}	Figure 1, Figure 2	4.5	—	6	ns
	t _{pZH}					
Output disable time	t _{pLZ}	Figure 1, Figure 2	4.5	—	6	ns
	t _{pHZ}					

Capacitive Characteristics (Ta = 25°C)

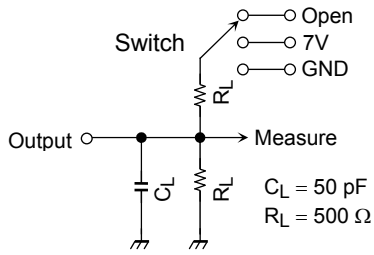
Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit	
Control pin input capacitance	C _{IN}	V _{IN} = 0 V	(Note)	5.0	5	pF
Switch OFF terminal capacitance	C _{I/O}	$\overline{OE} = V_{CC}$, V _{IS} = 0 V	(Note)	5.0	4	pF
Switch ON terminal capacitance	C _{I/O}	$\overline{OE} = GND$, V _{IS} = 0 V	(Note)	5.0	7	pF

Note: This parameter is guaranteed by design.

R_{ON} - V_{IS} Curve (Typ.) Ta = 25°C



AC Test Circuit



Parameter	Switch
t_{pLZ}, t_{pZL}	7V
t_{pHZ}, t_{pZH}	Open

Figure 1

AC Waveform

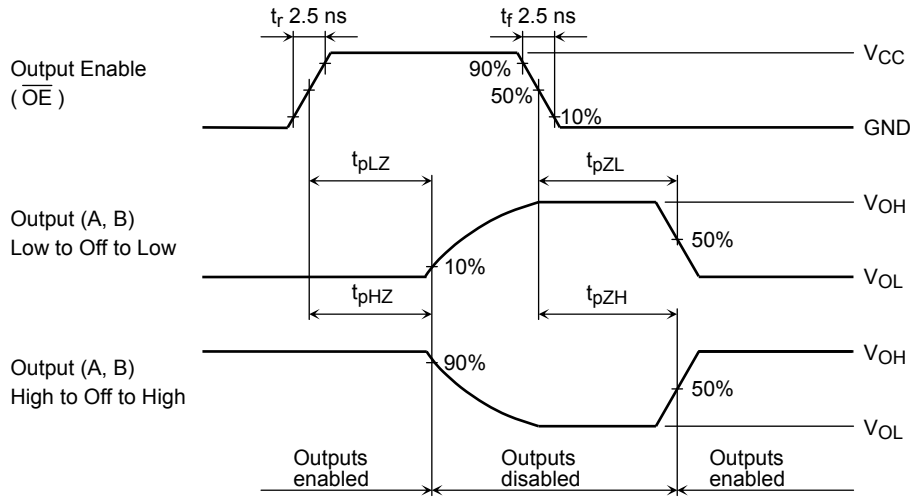


Figure 2 $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$

Rise and Fall Times (tr / tf) of the TC7MB3244C,3245C I/O Signals

The tr(out) and tf(out) values of the output signals are affected by the CR time constant of the input, which consists of the switch terminal capacitance (C_{I/O}) and the on-resistance (R_{ON}) of the input.

In practice, the tr(out) and tf(out) values are also affected by the circuit's capacitance and resistance components other than those of the TC7MB3244C,3245C.

The tr / tf (out) values can be approximated as follows. (Figure 3 shows the test circuit.)

$$tr / tf \text{ out (approx)} = - (C_{I/O} + C_L) \cdot (R_{DRIVE} + R_{ON}) \cdot \ln (((V_{OH} - V_{OL}) - V_M) / (V_{OH} - V_{OL}))$$

where, R_{DRIVE} is the output impedance of the previous-stage circuit.

Calculation example:

$$tr \text{ out (approx)} = - (7 + 15) E-12 \cdot (120 + 3) \cdot \ln (((4.5 - 0) - 2.25) / (4.5 - 0))$$

$$\approx 1.9 \text{ ns}$$

Calculation conditions:

V_{CC} = 4.5V , C_L = 15pF , R_{DRIVE} = 120Ω (output impedance of the previous IC), V_M = 2.25V (V_{CC} / 2)
 Output of the previous IC = digital (i.e., high-level voltage = V_{CC}; low-level voltage = GND)

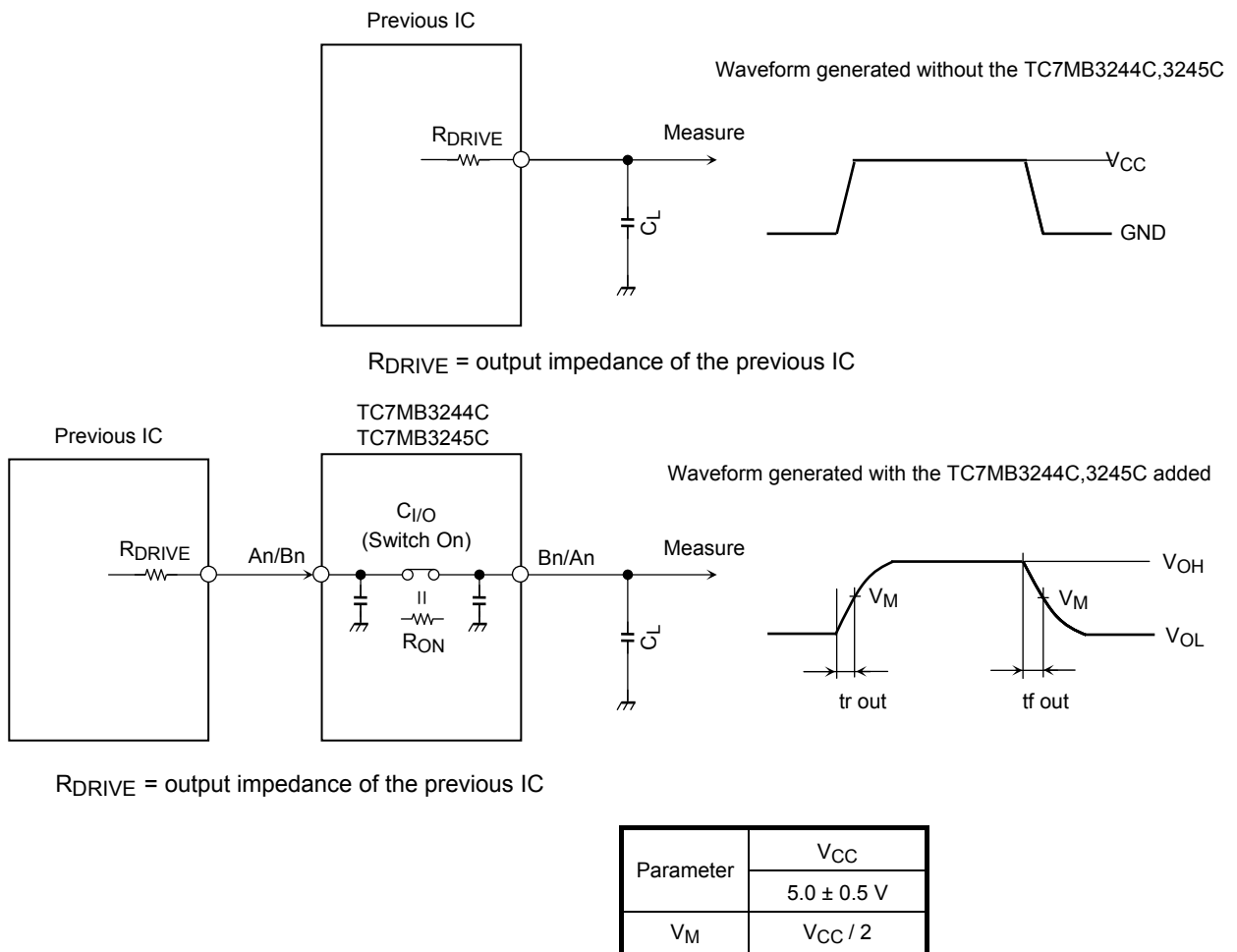
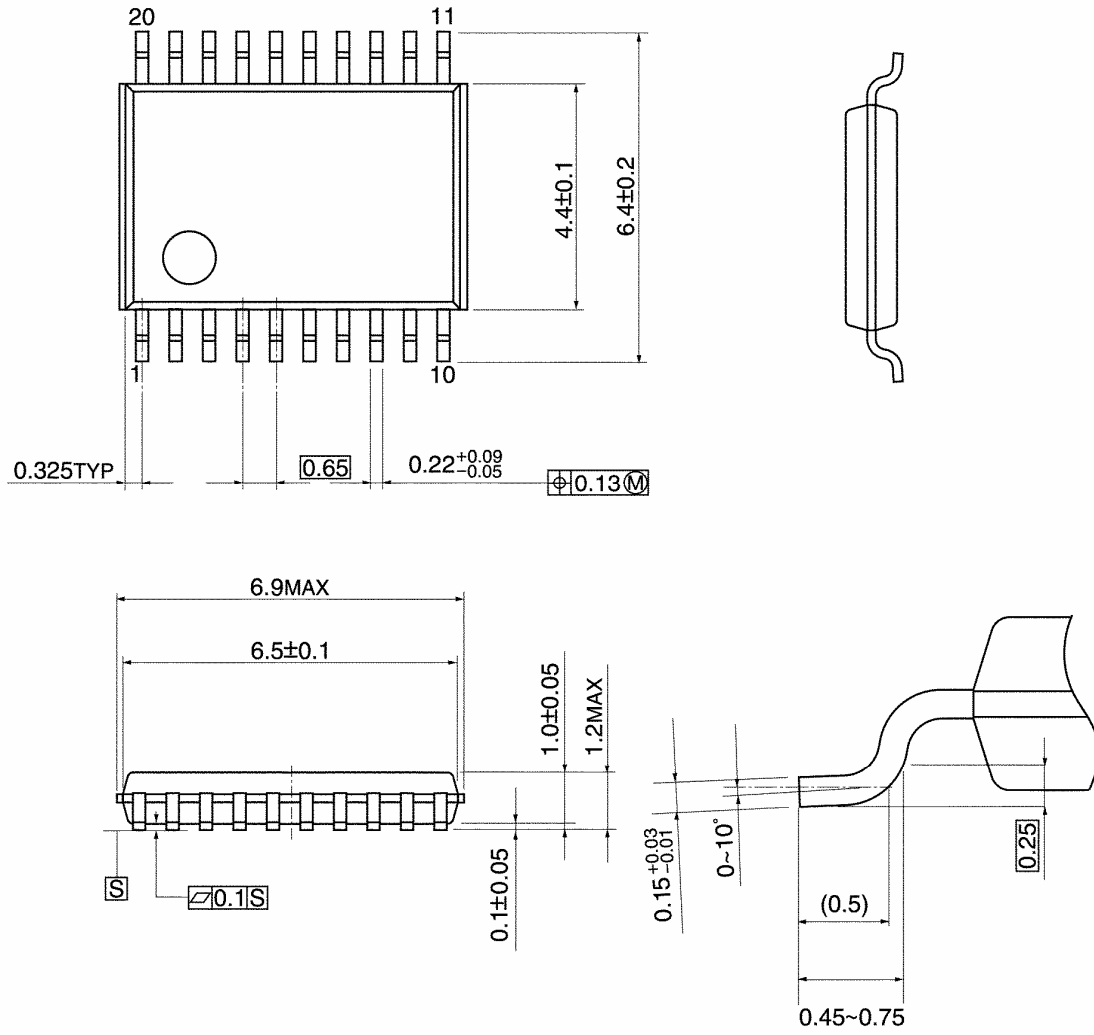


Figure 3 Test Circuit

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm

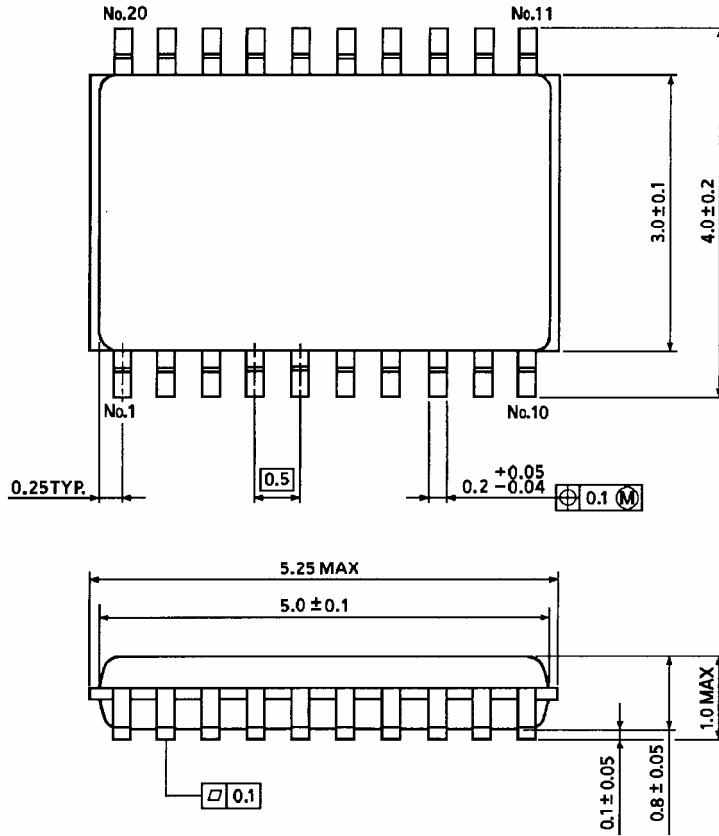


Weight: 0.08 g (typ.)

Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm



Weight: 0.03 g (typ.)

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