



## PA3312

CMOS IC

### DUAL 2.6W AUDIO POWER AMPLIFIER WITH FOUR SELECTABLE GAIN SETTINGS AND INPUT-MUX CONTROL

#### DESCRIPTION

The UTC **PA3312** is a monolithic integrated circuit that stereo bridged audio power amplifiers capable of producing 2.6W into 3Ω with less than 10% THD+N or 1W into 8Ω with less than 0.65% THD+N. This device minimizes the number of external components needed, simplifying the design, and freeing up board space for other features. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in UTC **PA3312**, that reduce pops and clicks noise during power up or shutdown mode operation .

Amplifier gain is internally configured and controlled by way of two terminals (GAIN0 and GAIN1). BTL gain setting of 6 dB, 10 dB, 15.6dB, 21.6dB (inverting) are provided, whereas SE gain is always configured as 4.1dB for headphone drive. A MUX control terminal (HP/LINE) allows selection between the two sets of stereo input signals. To simplify the audio system design, UTC **PA3312** combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/BTL input control pin signal.

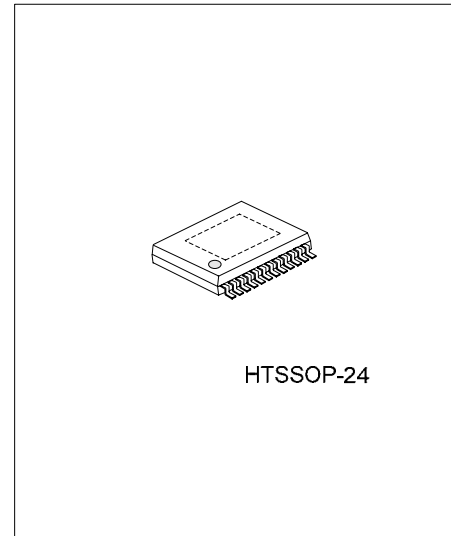
#### FEATURES

- \* Low operating current with 10mA
- \* Compatible with pc 99 desktop line-out into 10KΩ load
- \* Internal gain control ,which eliminates external gain-setting resistors
- \* 2.6w per channel output power into 3Ω at 5V , BTL mode
- \* Input MUX select terminal
- \* Pc-beep input
- \* Improves depop circuitry to eliminate turn-on and turn-off transients in output
- \* Fully differential input

#### ORDERING INFORMATION

Order Number		Package	Packing
Normal	Lead Free Plating		
PA3312-N24-R	PA3312L-N24-R	HTSSOP-24	Tape Reel
PA3312-N24-T	PA3312L-N24-T	HTSSOP-24	Tube

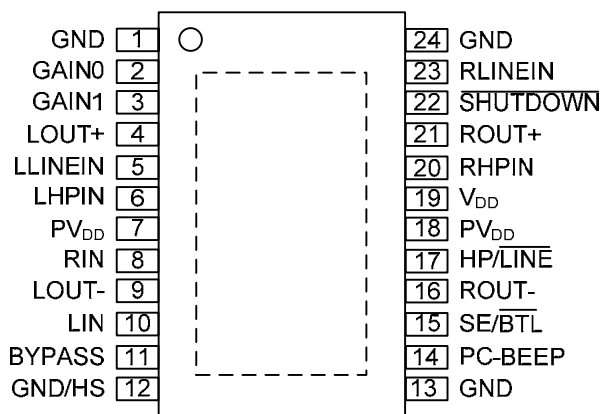
<p>PA3312L-N24-R</p> <p>(1)Packing Type (2)Package Type (3)Lead Plating</p>	<p>(1) R: Tape Reel, T: Tube (2) N24: HTSSOP-24 (3) L: Lead Free Plating, Blank: Pb/Sn</p>
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HTSSOP-24

\*Pb-free plating product number: PA3312L

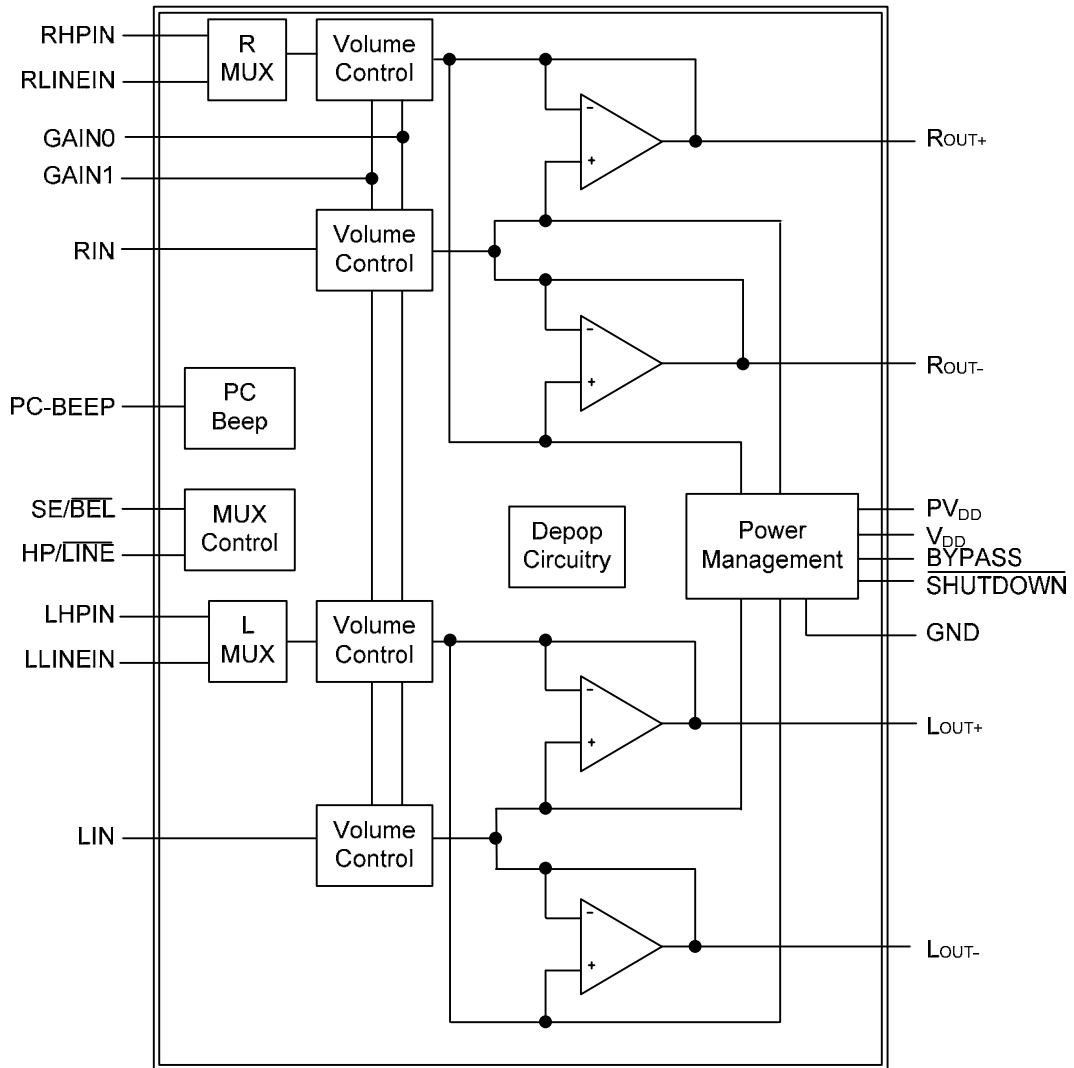
## ■ PIN CONFIGURATION



## ■ PIN DESCRIPTION

PIN NO	PIN NAME	I/O	DESCRIPTION
1, 12, 13, 24	GND		Ground connection for circuitry. Connected to the thermal pad.
11	BYPASS		Tap to voltage divider for internal mid-supply bias generator
2	GAIN0	I	Bit 0 of gain control
3	GAIN1	I	Bit 1 of gain control
5	LLINEIN	I	Left-channel line input, selected when $\overline{\text{SE/BTL}}$ is held low
6	LHPIN	I	Left-channel headphone input, selected when $\overline{\text{SE/BTL}}$ is held high
7, 18	PV <sub>DD</sub>	I	Power supply for output stage
8	RIN	I	Common right input for fully differential input. AC ground for single-ended inputs.
10	LIN	I	Common left input for fully differential input. AC ground for single-ended inputs.
14	PC-BEEP	I	For PC Beep mode. PC-BEEP is enabled when a > 1.5-V (peak-to-peak) square wave is input
17	HP/LINE	I	HP/LINE is the input MUX control input. When the HP/LINE terminal is held high, the headphone inputs (LHPIN or RHPIN [6, 20]) are active. When the HP/LINE terminal is held low, the line inputs (LLINEIN or RLINEIN [5, 23]) are active.
15	SE/BTL	I	Hold SE/BTL low for BTL mode and hold high for SE mode.
19	V <sub>DD</sub>	I	Analog V <sub>DD</sub> input supply. This terminal needs to be isolated from PV <sub>DD</sub> to achieve highest performance.
20	RHPIN	I	Right-channel headphone input, selected when $\overline{\text{SE/BTL}}$ is held high
23	RLINEIN	I	Right-channel line input, selected when $\overline{\text{SE/BTL}}$ is held low
22	SHUTDOWN	I	Places entire IC in shutdown mode when held low, except PC-BEEP remains active
4	L <sub>OUT+</sub>	O	Left-channel positive output in BTL mode and positive output in SE mode
9	L <sub>OUT-</sub>	O	Left-channel negative output in BTL mode and high-impedance in SE mode
21	R <sub>OUT+</sub>	O	Right-channel positive output in BTL mode and positive output in SE mode
16	R <sub>OUT-</sub>	O	Right-channel negative output in BTL mode and high-impedance in SE mode

■ BLOCK DIAGRAM



- ABSOLUTE MAXIMUM RATING over operating free-air temperature range (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{DD}$	6	V
Input Voltage	$V_{IN}$	-0.3~ $V_{DD}$ ~+0.3	V
Power Dissipation	$P_D$	Internally limited	
Operating Junction Temperature	$T_{OPR}$	-40 ~ +85	
Storage Temperature	$T_{STG}$	-65 ~ +85	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	$V_{DD}$	4.5	5.5	V
High-Level Input Voltage	$V_{IH}$	$0.8 \times V_{DD}$		V
Low-Level Input Voltage	$V_{IL}$	SE/BTL, HP/LINE	$0.6 \times V_{DD}$	V
		GAIN0, GAIN1	$0.4 \times V_{DD}$	
		SHUTDOWN	0.8	
Operating Free-Air Temperature	$T_A$	-40	85	

- OPERATING CHARACTERISTICS  $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 8\Omega$ , Gain = 6 dB, BTL mode

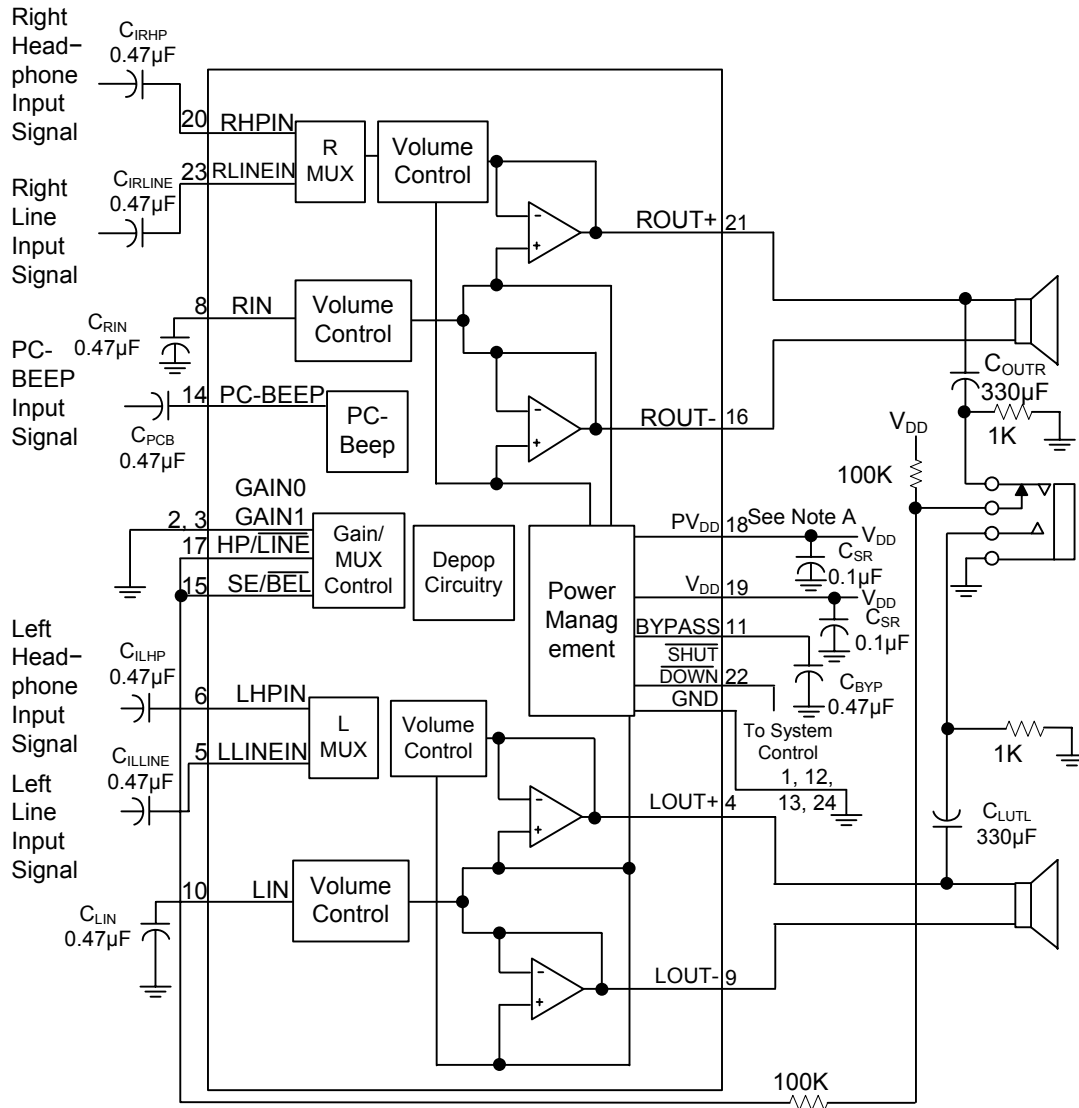
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Power	$P_{OUT}$	$R_L = 3\Omega$	THD+N=10%	2.6		W
			THD+N=1%	2.05		
Total Harmonic Distortion Plus Noise	TDH+N	$P_{OUT} = 1\text{ W}$ , $f = 20\text{ Hz} \sim 15\text{ kHz}$		0.65%		
Maximum Output Power Bandwidth	$B_{OM}$	THD = 5%		>15		KHz
Supply Ripple Rejection Ratio	RR	$f = 1\text{ kHz}$ , $C_B = 0.47\text{ }\mu\text{F}$   BTLmode		72		dB
Signal-to-Noise Ratio	SNR			105		dB
Noise Output Voltage	eN	$C_B = 0.47\text{ }\mu\text{F}$ , $f = 20\text{ Hz} \sim 20\text{ KHz}$	BTLmode	20		$\mu\text{V}_{RMS}$
			SE mode	18		

- ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ , unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Offset Voltage (Measured Differentially)	$ V_{O(OFF)} $	$V_{IN} = 0$ , $A_V = 6\text{ dB}$			25	mV
Power Supply Rejection Ratio	PSRR	$V_{DD} = 4.5\text{ V} \sim 5.5\text{ V}$		77		dB
High-Level Input Current	$ I_{IH} $	$V_{DD} = 5.5\text{ V}$ , $V_{IN} = V_{DD}$			1	$\mu\text{A}$
Low-Level Input Current	$ I_{IL} $	$V_{DD} = 5.5\text{ V}$ , $V_{IN} = 0\text{ V}$			1	$\mu\text{A}$
Supply Current	$I_{DD}$	BTL mode		6	10	mA
		SE mode		3	5	
Supply Current, Shutdown Mode	$I_{DD(SD)}$			150	300	$\mu\text{A}$

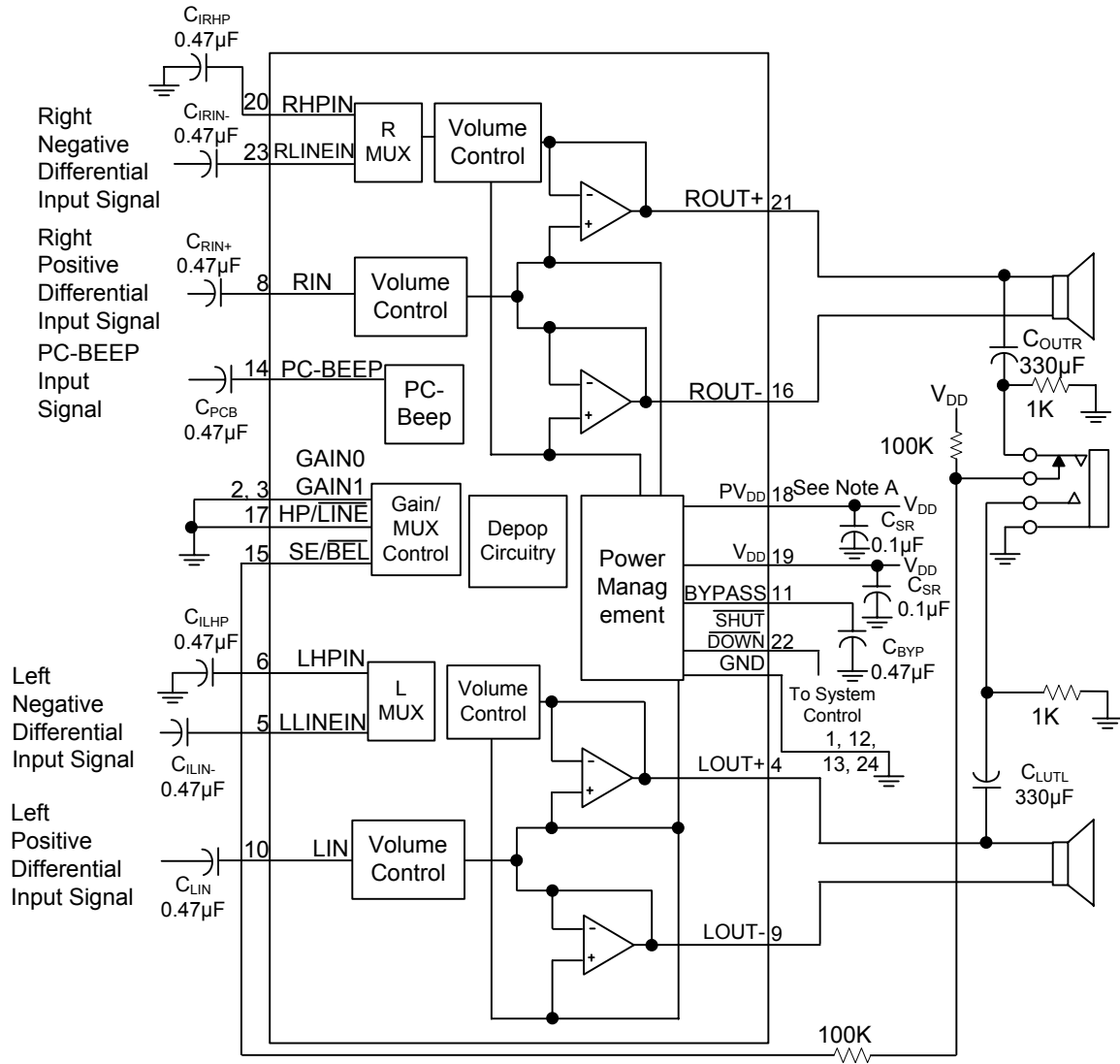
■ TYPICAL APPLICATION CIRCUIT



A. A 0.1- $\mu$ F ceramic capacitor should be placed as close as possible to the IC. For filtering lower frequency noise signals, a larger electrolytic capacitor of 10  $\mu$ F or greater should be placed near the audio power amplifier.

Typical PA3312 Application Circuit Using Single-Ended Inputs and Input MUX

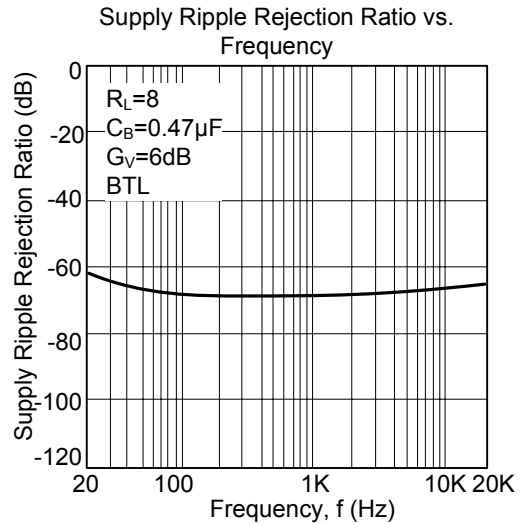
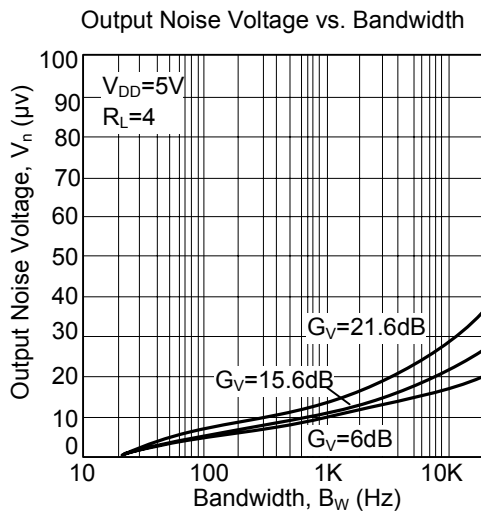
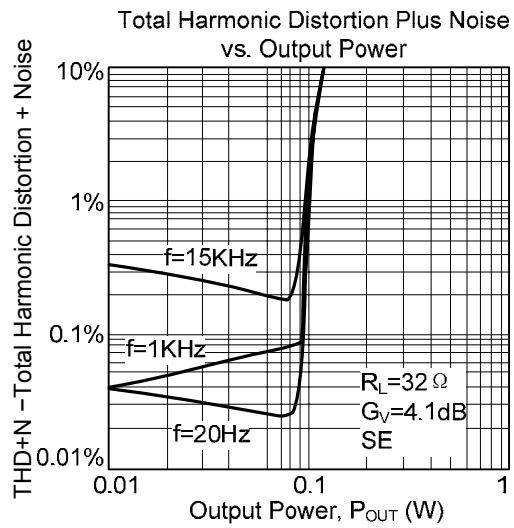
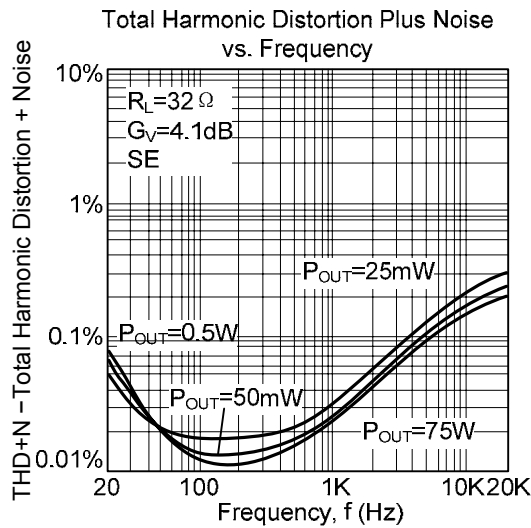
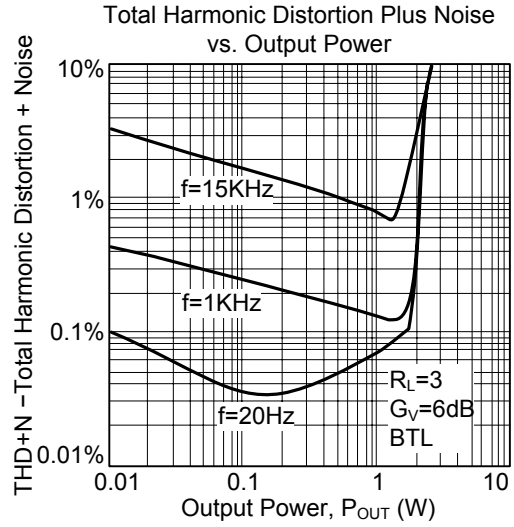
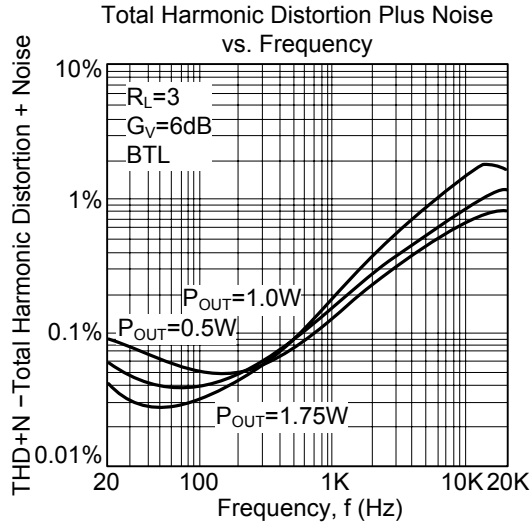
■ TYPICAL APPLICATION CIRCUIT(Cont.)



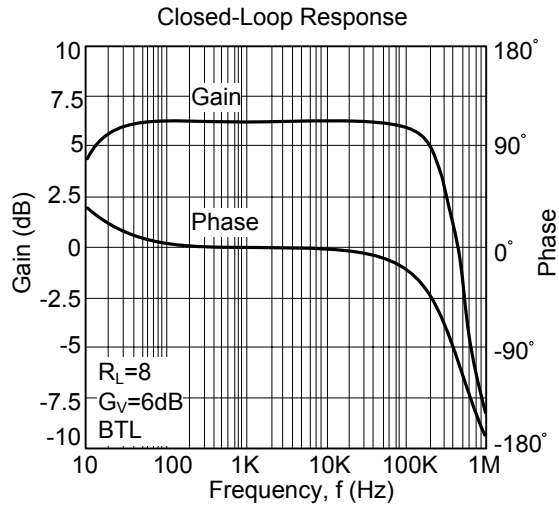
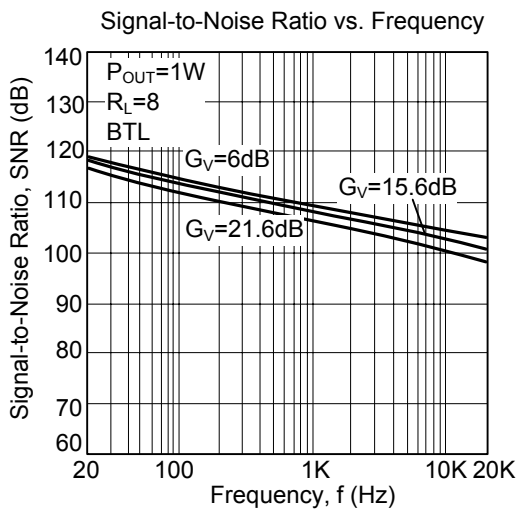
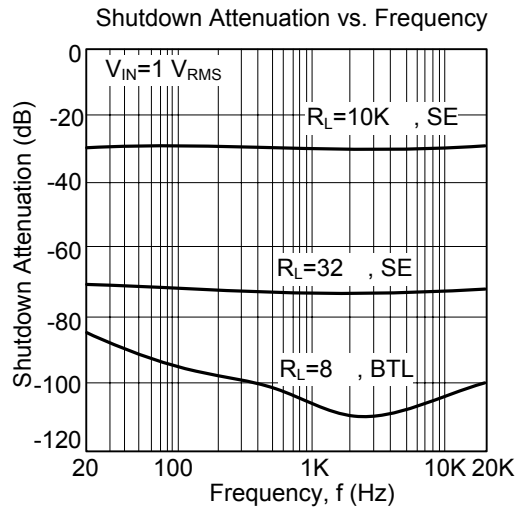
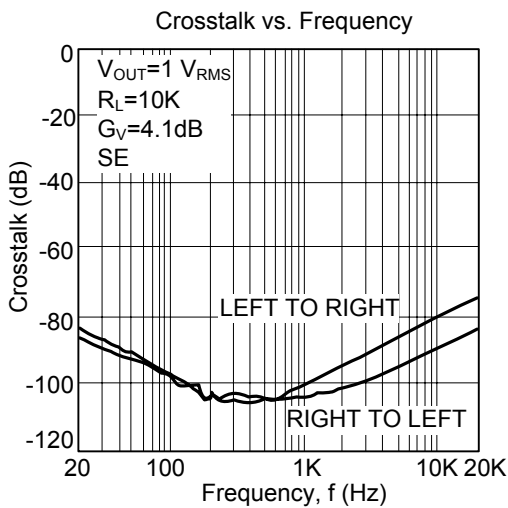
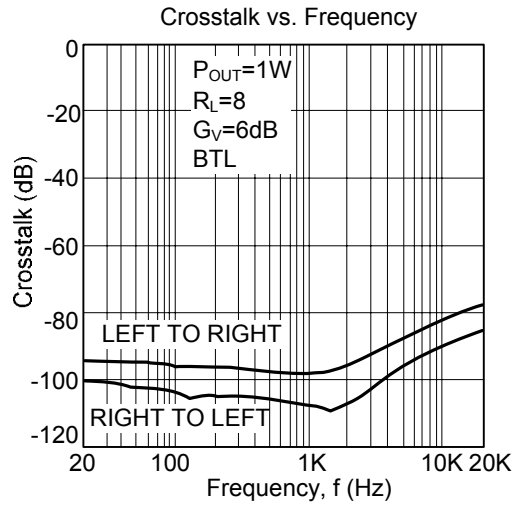
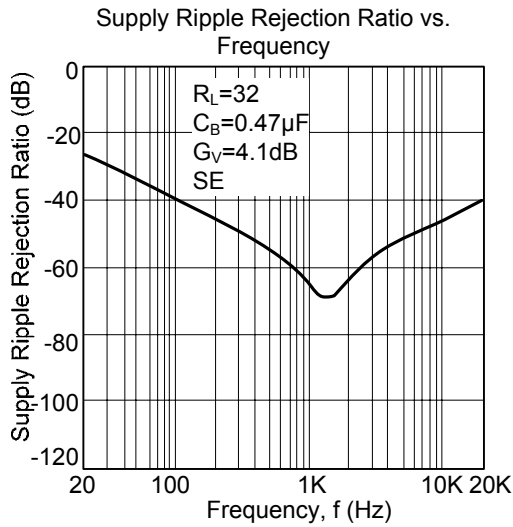
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Typical PA3312 Application Circuit Using Differential Inputs

■ TYPICAL CHARACTERISTICS

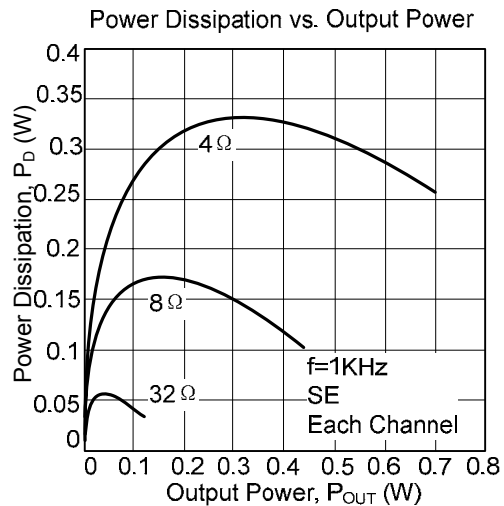
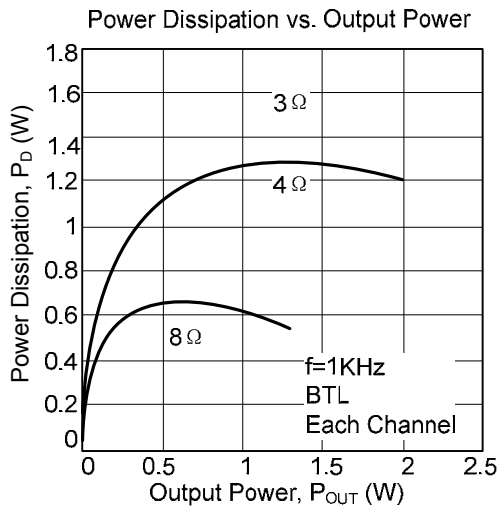
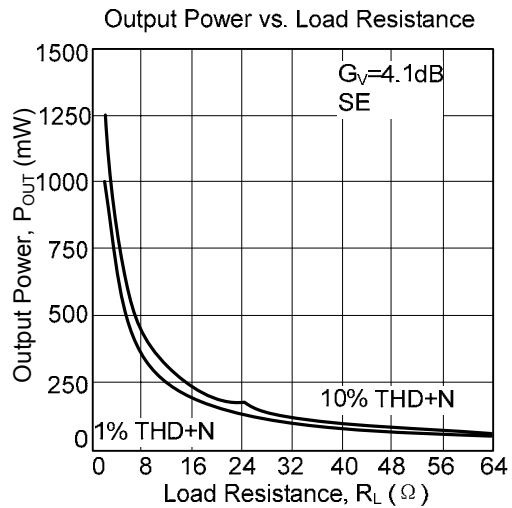
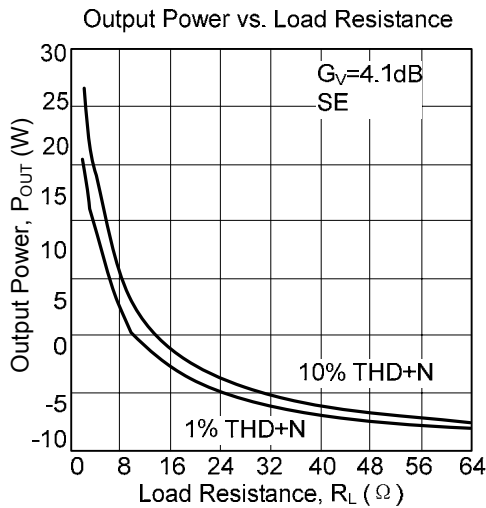
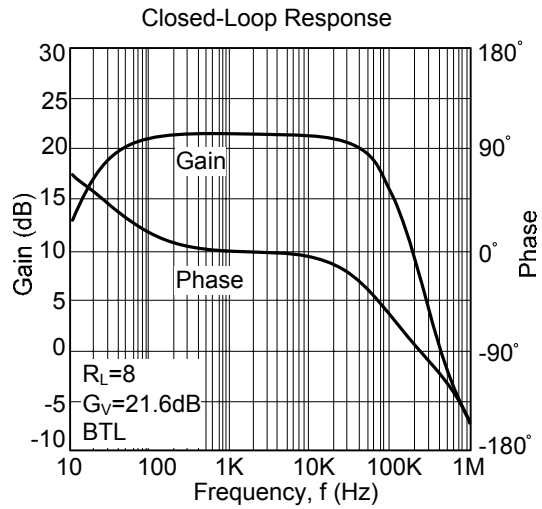
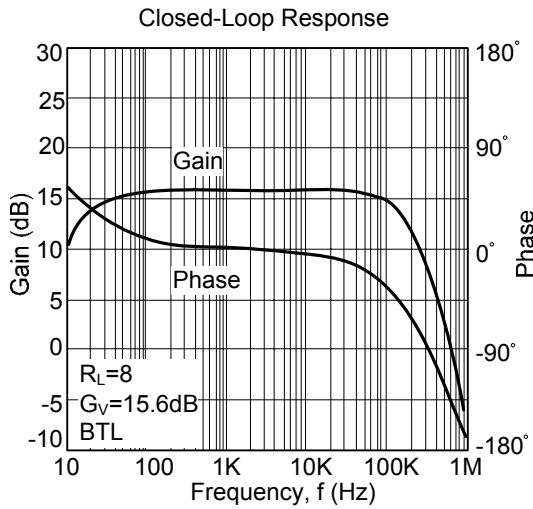


■ TYPICAL CHARACTERISTICS(Cont.)





■ TYPICAL CHARACTERISTICS(Cont.)



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