

# NTD5407N, STD5407N

## Power MOSFET

40 V, 38 A, Single N-Channel, DPAK



ON Semiconductor®

<http://onsemi.com>

### Features

- Low  $R_{DS(on)}$
- High Current Capability
- Low Gate Charge
- AEC-Q101 Qualified and PPAP Capable – STD5407N
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- Electronic Brake Systems
- Electronic Power Steering
- Bridge Circuits

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DS}$	40	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V	
Continuous Drain Current – $R_{\theta JC}$	Steady State	$I_D$	$T_C = 25^\circ\text{C}$	38	A
			$T_C = 100^\circ\text{C}$	27	
Power Dissipation – $R_{\theta JC}$	Steady State	$P_D$	75	W	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	7.6	A
			$T_A = 100^\circ\text{C}$	5.3	
Power Dissipation – $R_{\theta JA}$ (Note 1)	Steady State	$P_D$	2.9	W	
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	75	A	
Operating Junction and Storage Temperature		$T_J$ , $T_{STG}$	-55 to 175	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	36	A	
Single Pulse Drain-to-Source Avalanche Energy – ( $V_{DD} = 50 \text{ V}$ , $V_{GS} = 10 \text{ V}$ , $I_{PK} = 17 \text{ A}$ , $L = 1 \text{ mH}$ , $R_G = 25 \Omega$ )		EAS	150	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

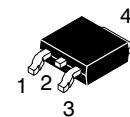
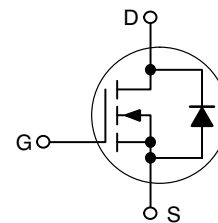
### THERMAL RESISTANCE RATINGS (Note 1)

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	2.0	$^\circ\text{C/W}$
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	52	$^\circ\text{C/W}$

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).

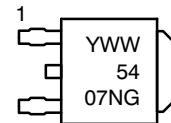
$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	$I_D$ MAX (Note 1)
40 V	21 m $\Omega$ @ 10 V	38 A

### N-Channel



DPAK  
CASE 369C  
STYLE 2

### MARKING DIAGRAM



Y = Year  
WW = Work Week  
5407N = Specific Device Code  
G = Pb-Free Device

### ORDERING INFORMATION

Device	Package	Shipping†
NTD5407NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
STD5407NT4G	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTD5407N, STD5407N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			39		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 100°C		10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±30 V			±100	nA

## ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.5		3.5	V
Gate Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			-6.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		21	26	mΩ
		V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 10 A		32	40	
Forward Transconductance	g <sub>FS</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 18 A		15		S

## CHARGES AND CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 32 V		615	1000	pF
Output Capacitance	C <sub>OSS</sub>			173		
Reverse Transfer Capacitance	C <sub>RSS</sub>			80		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 38 A		20		nC
Gate-to-Source Charge	Q <sub>GS</sub>			2.25		
Gate-to-Drain Charge	Q <sub>GD</sub>			10.5		

## SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 10 V (Note 3)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 32 V, I <sub>D</sub> = 38 A, R <sub>G</sub> = 2.5 Ω		6.8		ns
Rise Time	t <sub>r</sub>			17		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			66		
Fall Time	t <sub>f</sub>			51		

## SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 5 V (Note 3)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 5 V, V <sub>DD</sub> = 20 V, I <sub>D</sub> = 20 A, R <sub>G</sub> = 2.5 Ω		10		ns
Rise Time	t <sub>r</sub>			175		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			13		
Fall Time	t <sub>f</sub>			23		

## DRAIN-SOURCE DIODE CHARACTERISTICS (Note 2)

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 5.0 A	T <sub>J</sub> = 25°C		0.9	1.1	V
			T <sub>J</sub> = 125°C		0.75		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 15 A		38		ns	
Charge Time	t <sub>a</sub>			20.5			
Discharge Time	t <sub>b</sub>			17			
Reverse Recovery Charge	Q <sub>RR</sub>			40			nC

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

# NTD5407N, STD5407N

## TYPICAL PERFORMANCE CURVES

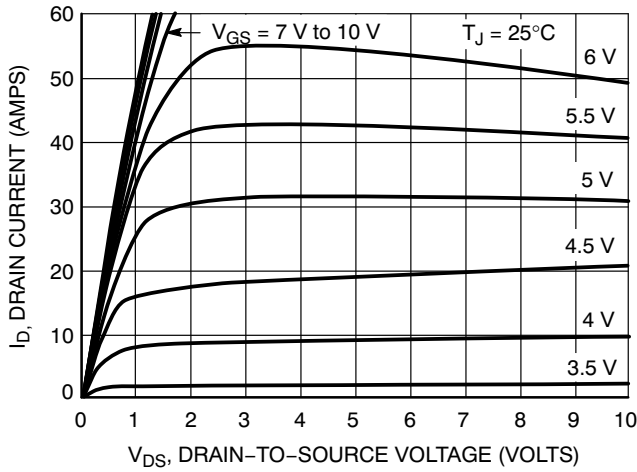


Figure 1. On-Region Characteristics

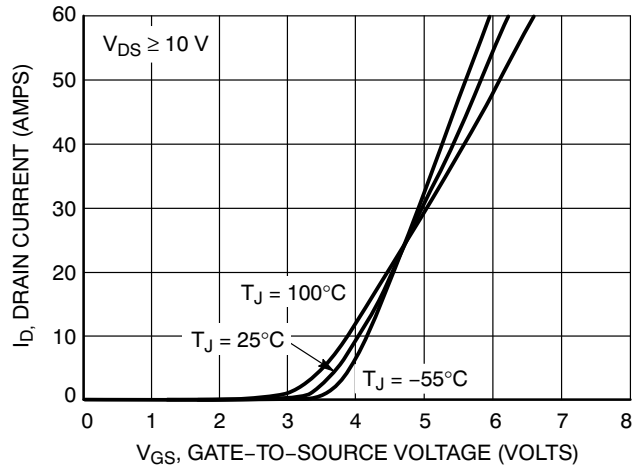


Figure 2. Transfer Characteristics

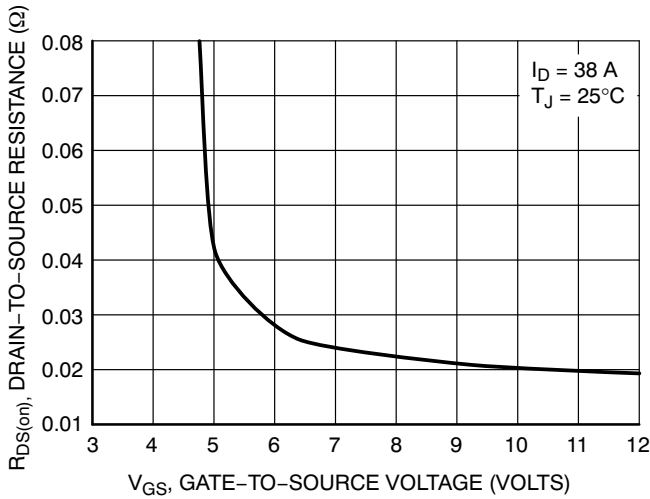


Figure 3. On-Resistance vs. Gate-to-Source Voltage

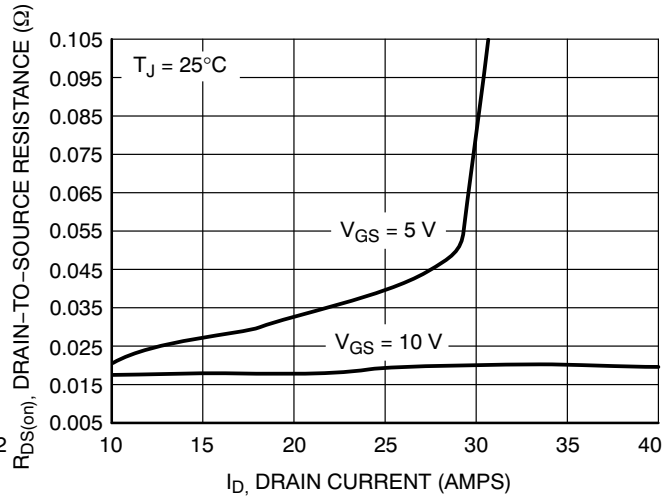


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

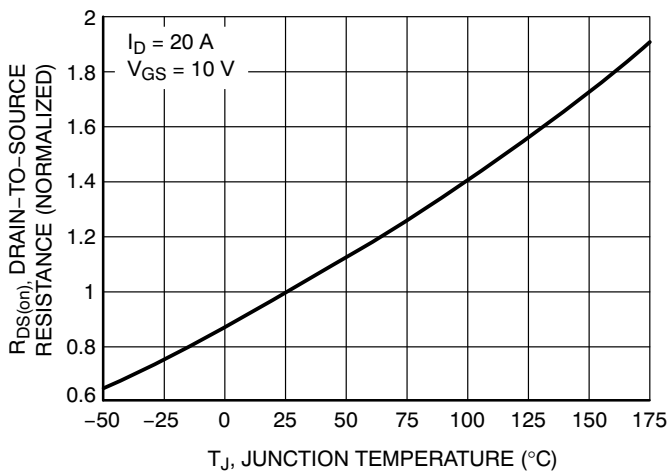


Figure 5. On-Resistance Variation with Temperature

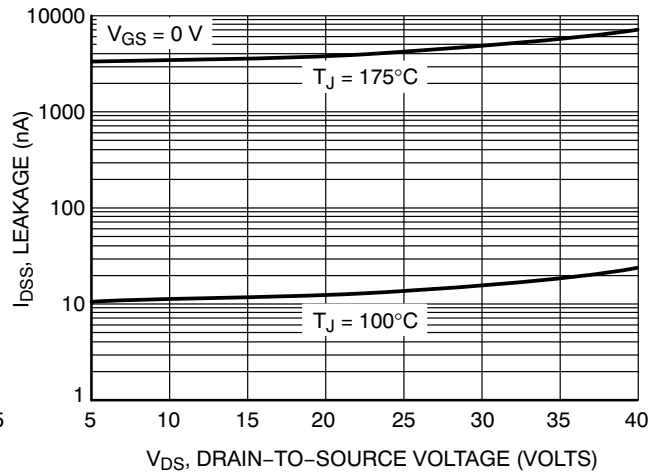


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTD5407N, STD5407N

## TYPICAL PERFORMANCE CURVES

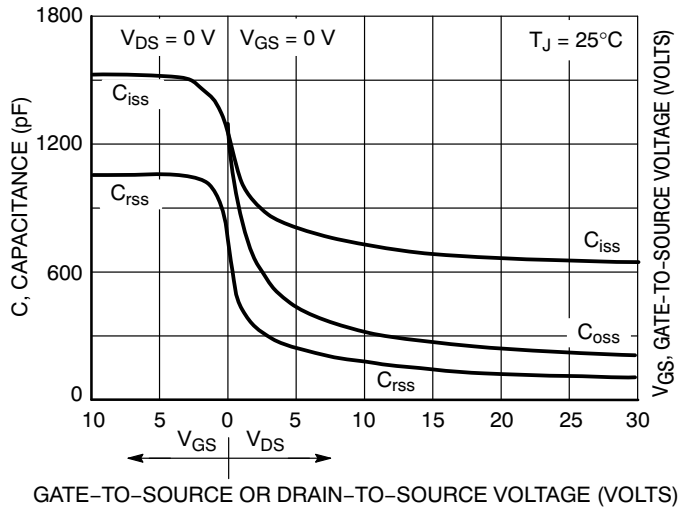


Figure 7. Capacitance Variation

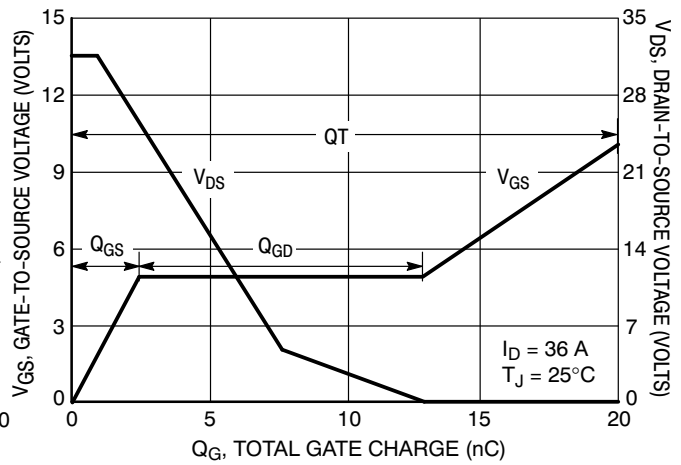


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

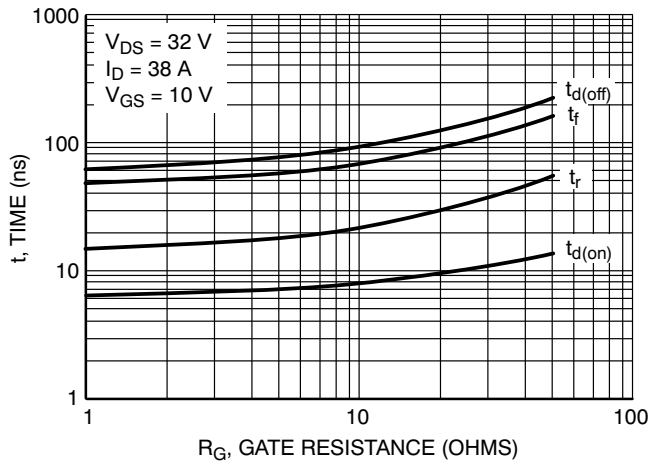


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

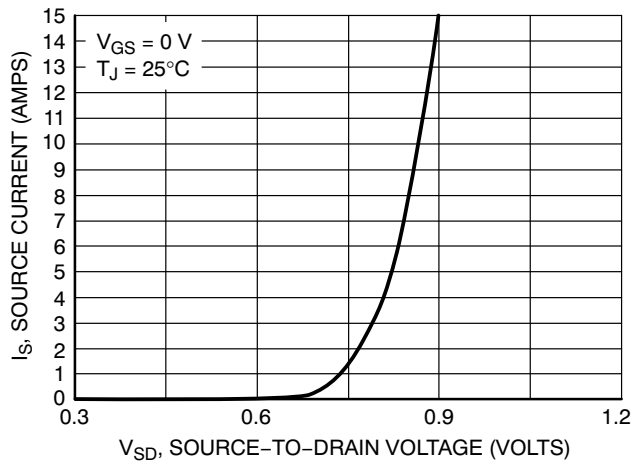


Figure 10. Diode Forward Voltage vs. Current

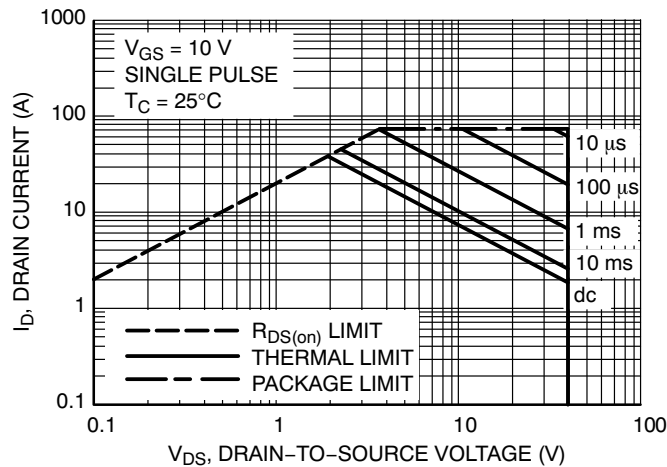
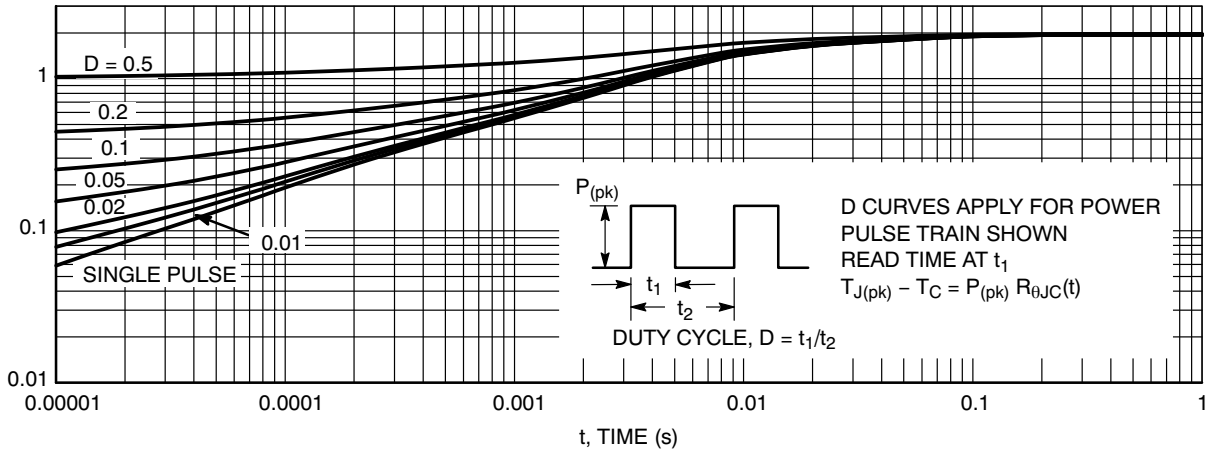


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NTD5407N, STD5407N

## TYPICAL PERFORMANCE CURVES

r(t), EFFECTIVE TRANSIENT THERMAL RESISTANCE

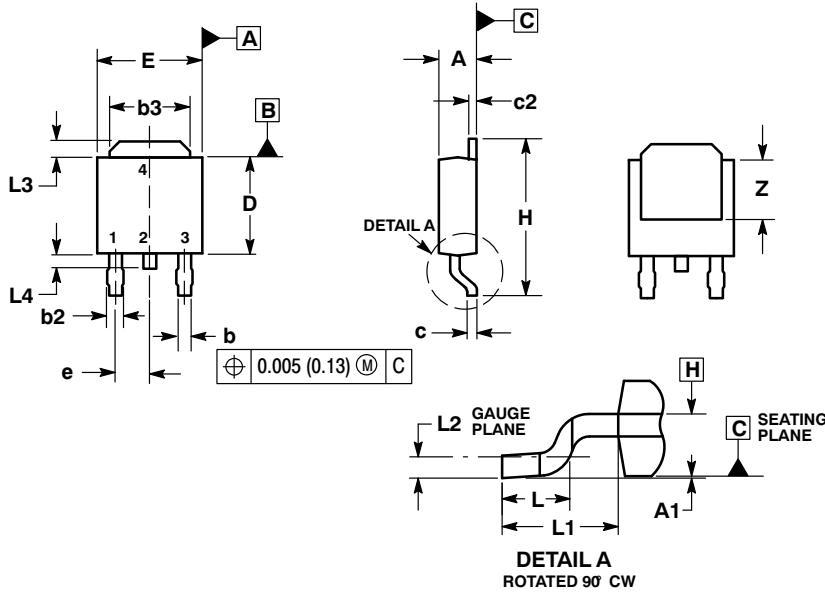


**Figure 12. Thermal Response**

# NTD5407N, STD5407N

## PACKAGE DIMENSIONS

### DPAK (SINGLE GAUGE) CASE 369C ISSUE D



#### NOTES:

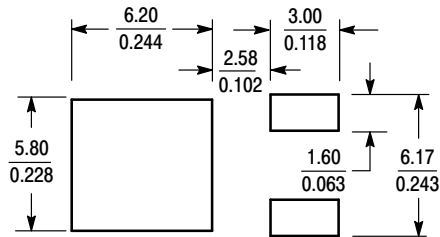
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108	REF	2.74	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

#### STYLE 2:


- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

#### SOLDERING FOOTPRINT\*



SCALE 3:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

##### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative