

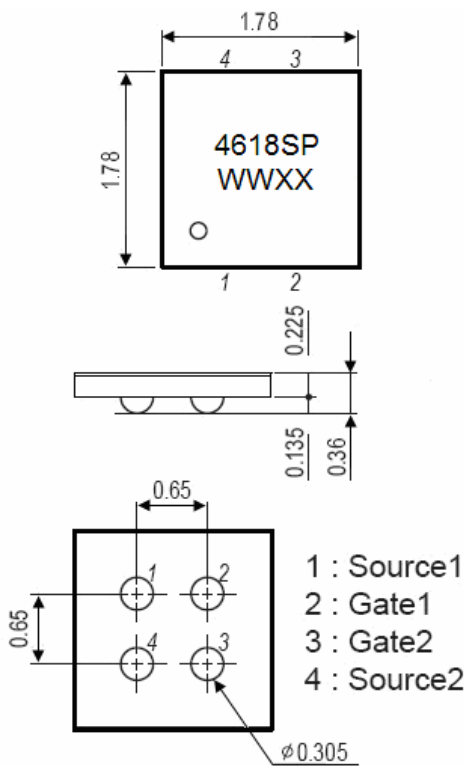
NCE Common-Drain Dual N-Channel Enhancement Mode Field Effect Transistor

Description

The NCE4618SP uses advanced trench technology to provide excellent $R_{SS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V while retaining a 12V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

Package Dimensions

Unit : mm



General Features

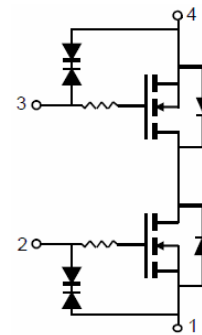
- $V_{SSS} = 24V, I_s = 6A$
- 2.5V drive
- Common-drain type
- 2KV HBM

Package Information

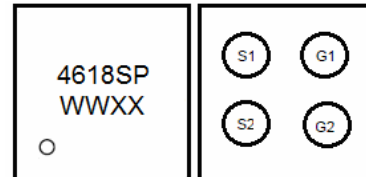
- Minimum Packing Quantity : 5,000 pcs./reel

Application

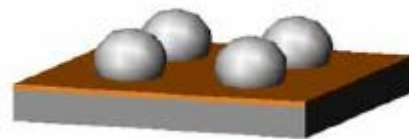
- Lithium-ion battery charging and discharging switch



Equivalent Circuit



Marking and pin assignment



CSP top view

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

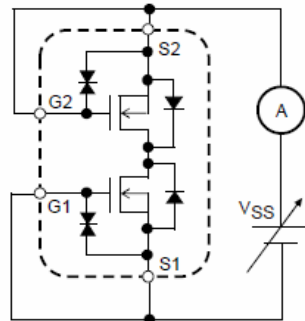
Symbol	Parameter	Limit	Unit
V_{SSS}	Source to Source Voltage	24	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_s	Source Current(DC)	6	A
I_{SP}	Source Current (Pulse)	60	A
P_T	Total Dissipation	1.6	W
T_{ch}	Channel Temperature	150	$^\circ C$
T_{STG}	Storage Temperature	-55 To 150	$^\circ C$

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

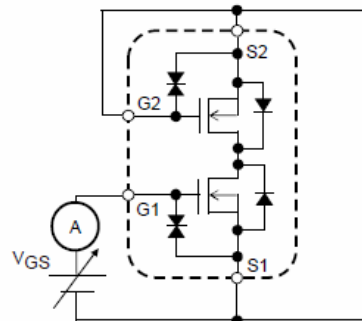
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
BV_{SSS}	Source to Source Breakdown Voltage	$I_S=1\text{mA}, V_{GS}=0\text{V}$, Test Circuit 1	24	-	-	V
I_{SSS}	Zero- Gate Voltage Source Current	$V_{SS}=20\text{V}, V_{GS}=0\text{V}$, Test Circuit 1	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{SS}=0\text{V}, V_{GS}=\pm 8\text{V}$, Test Circuit 2	-	-	± 1	μA
$V_{GS(off)}$	Cutoff Voltage	$V_{SS}=10\text{V}, I_S=1\text{mA}$, Test Circuit 3	0.5	0.83	1.3	V
$ y_{gfs} $	Forward Transfer Admittance	$V_{SS}=10\text{V}, I_S=3\text{A}$, Test Circuit 4	6.5	-	-	S
$R_{SS(on)}$	Static Source to Source On-Resistance	$V_{GS}=4.5\text{V}, I_S=3\text{A}$, Test Circuit 5		18.3	21.5	$\text{m}\Omega$
		$V_{GS}=4.0\text{V}, I_S=3\text{A}$, Test Circuit 5		19	22.5	$\text{m}\Omega$
		$V_{GS}=3.7\text{V}, I_S=3\text{A}$, Test Circuit 5		19.3	24	$\text{m}\Omega$
		$V_{GS}=3.1\text{V}, I_S=3\text{A}$, Test Circuit 5		20.3	27	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_S=3\text{A}$, Test Circuit 5		23.0	32	$\text{m}\Omega$
$t_{d(on)}$	Turn-on Delay Time	$V_{SS}=10\text{V}, I_S=3\text{A}, V_{GS}=4.5\text{V}$ Test Circuit 7	-	15	-	nS
t_r	Turn-on Rise Time		-	50	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	40	-	nS
t_f	Turn-Off Fall Time		-	55	-	nS
Q_g	Total Gate Charge	$V_{SS}=10\text{V}, I_S=6\text{A}, V_{GS}=4.5\text{V}$ Test Circuit 8	-	25.4	-	nC
$V_{F(S-S)}$	Diode Forward Voltage	$V_{GS}=0\text{V}, I_S=6\text{A}$	-	-	1.2	V

Test Circuit

Test Circuit 1
 I_{SS}

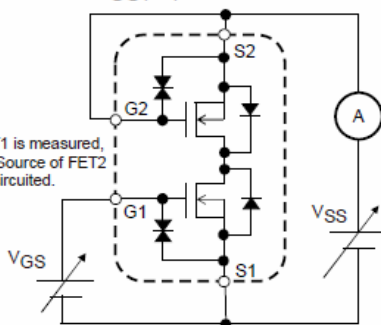


Test Circuit 2
 I_{GSS}



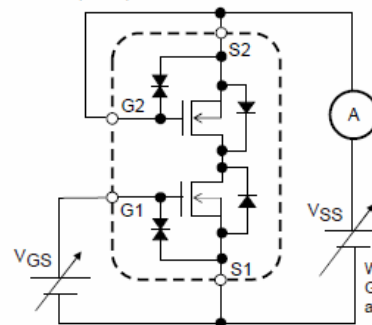
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
 $V_{GS(off)}$



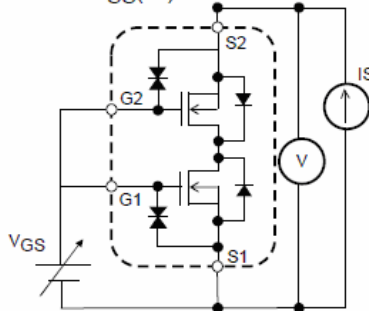
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 4
 $|y_{fs}|$

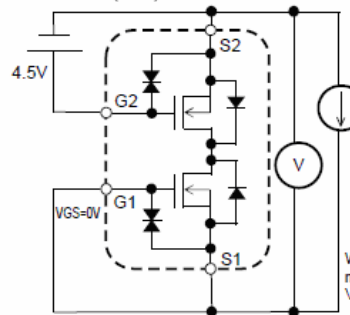


When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 5
 $R_{SS(on)}$

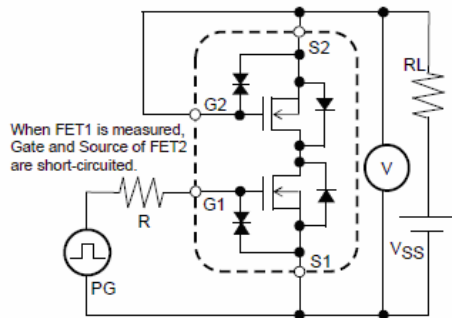


Test Circuit 6
 $V_F(S-S)$



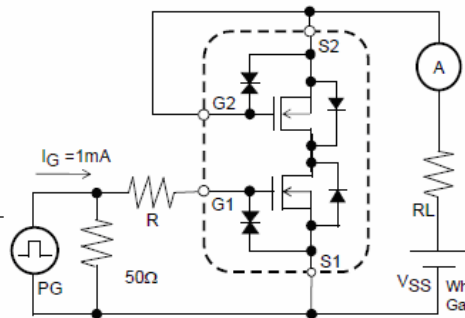
When FET1 is measured, +4.5V is added to V_{GS} of FET2.

Test Circuit 7
 $t_d(on), t_r, t_d(off), t_f$



When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 8
 Q_g



When FET1 is measured, Gate and Source of FET2 are short-circuited.

Typical Electrical and Thermal Characteristics (Curves)

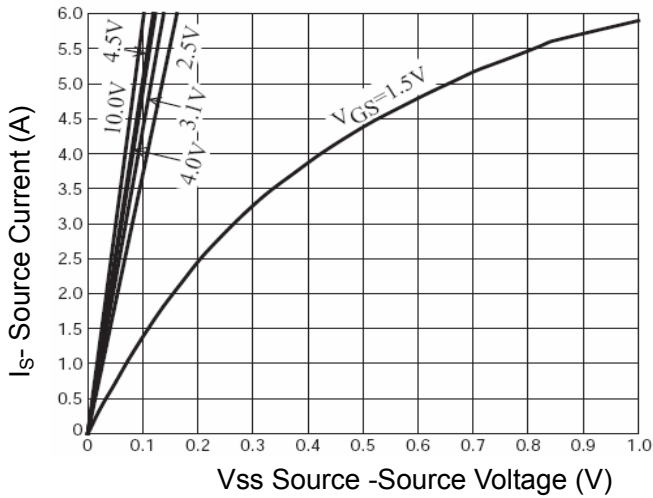


Figure 1 On-Region Characteristics

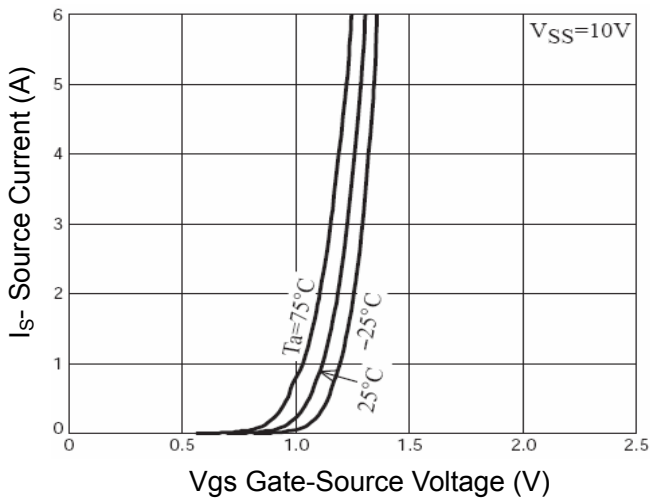


Figure 2 Transfer Characteristics

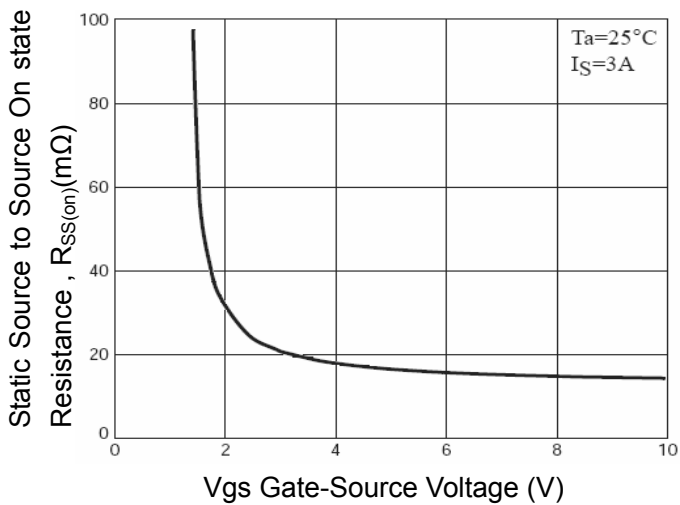


Figure 3 On-Resistance-Gate-Source Voltage

Static Source to Source On state

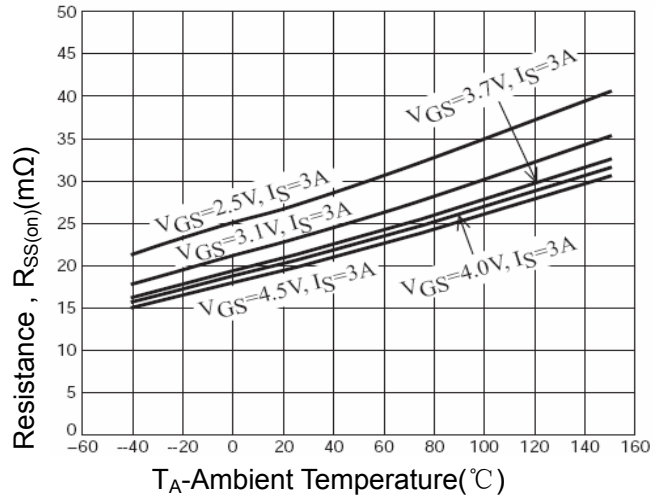


Figure 4 Rss(on)- Ambient Temperature

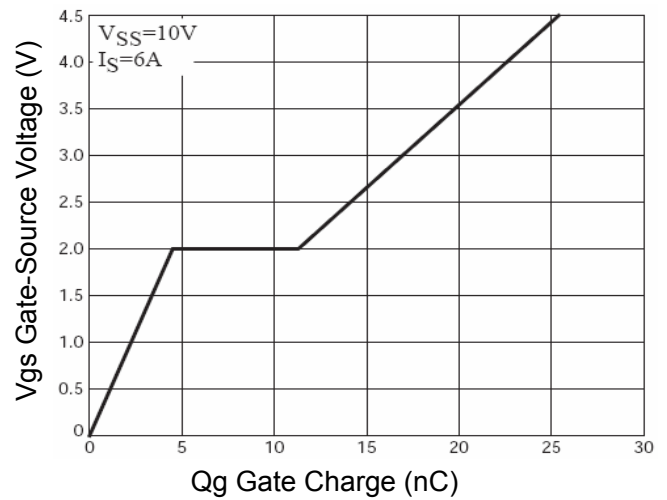


Figure 5 Gate Charge

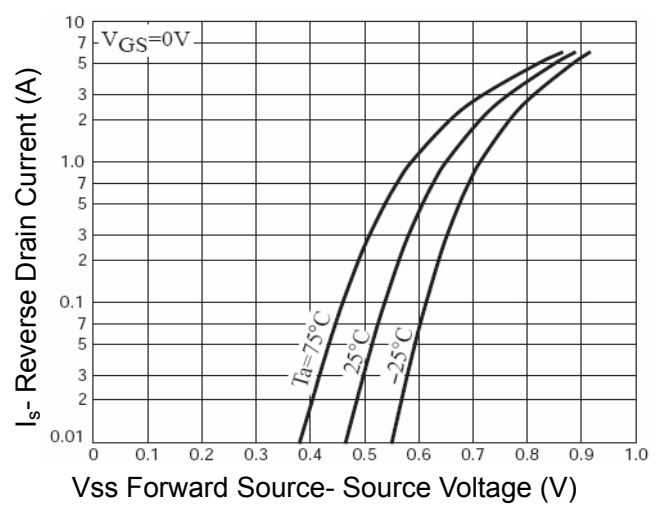


Figure 6 Body-Diode Characteristics

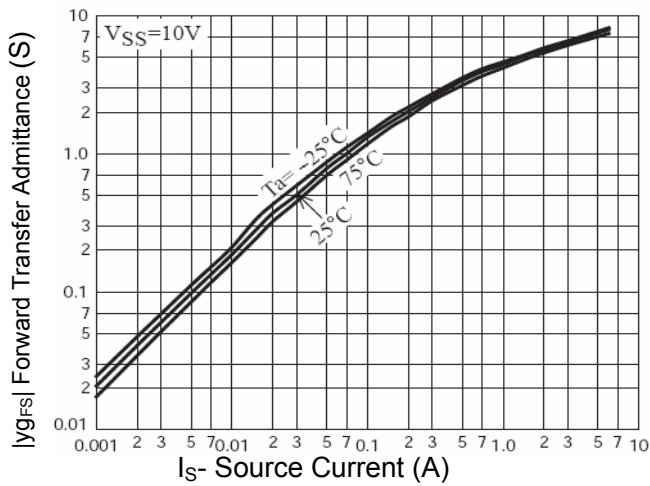


Figure 7 $|y_{fs}|$ vs I_S

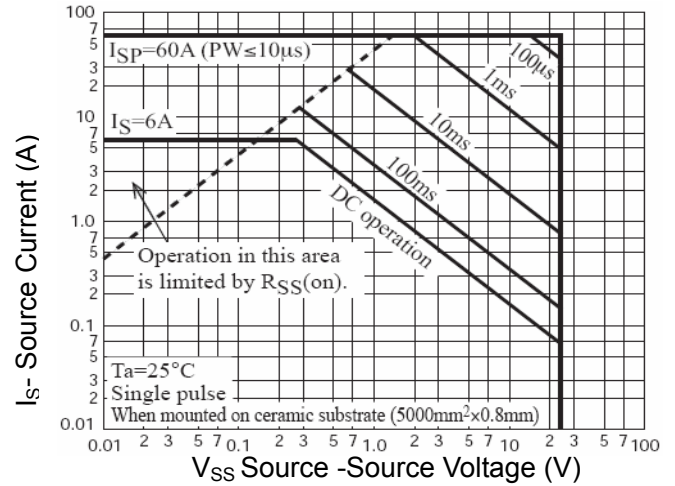


Figure 8 Safe Operation Area

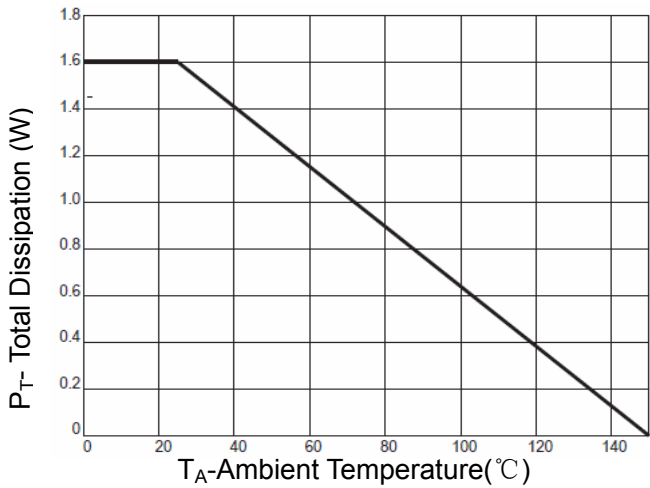


Figure 9 P_T Dissipation De-rating

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