# AN5011

## TV Electronic Channel Selection Circuit

■ Outline

The AN5011 is an integrated circuit designed for electronic tuner circuit by the preset volume method.

■ Features

- Simplifies selection circuit up to 10 channels
- Incorporating clock oscillator, input control, UP – DOWN counter and decoder circuits
- Remote control system available (UP – DOWN bidirectional)
- Clock frequency changeable by external components
- Provided with pulse output
- Channel initialize when power is switched on can be set at any channel
- Selection output breakdown voltage : 40V
- Selection output saturation voltage : <0.15V (5mA)
- Supply voltage : 6.0V
- Channel selection : 10 channels, jump over selection available

Unit : mm

18-Lead DIL Plastic Package
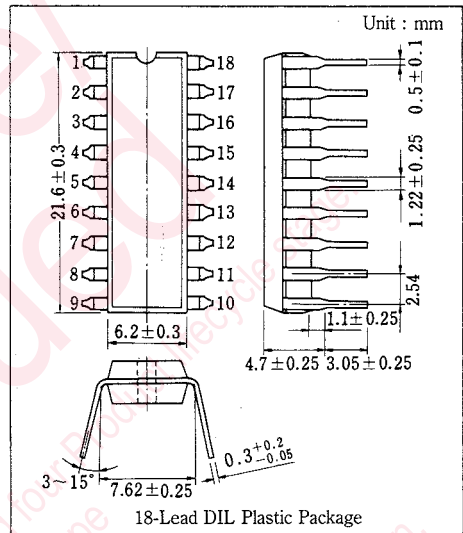
■ Block Diagram
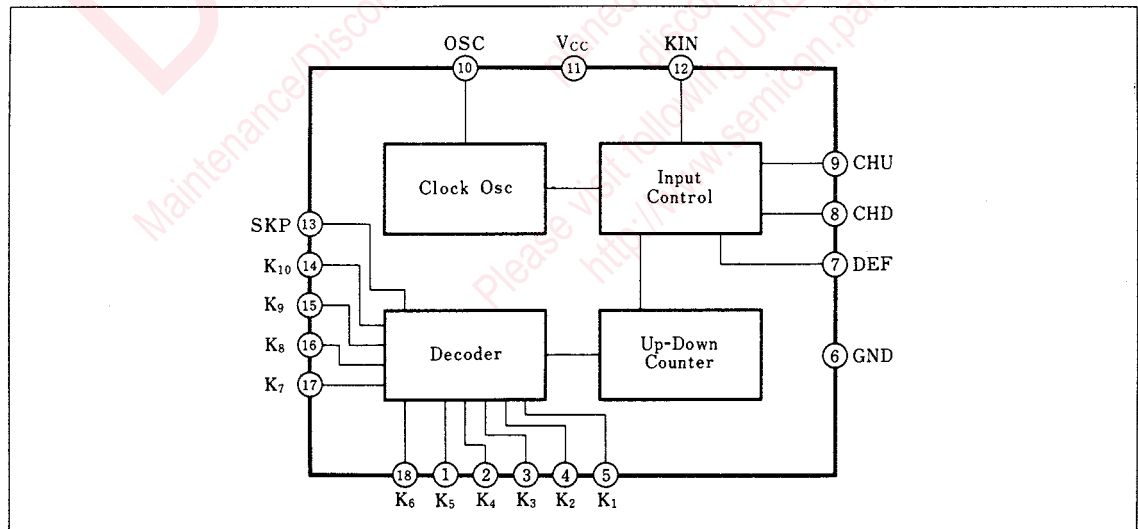
■ Absolute Maximum Ratings (Ta=25℃)

Item		Symbol	Rating		Unit
Voltage	Supply Voltage	V_{cc}	7.2		V
	Circuit Voltage	V_{K-6}*1	−0.5	50	V
		V_{7-6}	−0.5	14.4	V
		V_{11-6}	−0.5	7.2	V
		V_{10-6}	−0.5	7.2	V
Current	Supply Current	I_{tot}	60		mA
	Circuit Current	I_K*2	−5	15	mA
		I_7	−5	15	mA
		I_8	−5	10	mA
		I_9	−5	10	mA
		I_{10}	−5	10	mA
		I_{11}	−5	60	mA
		I_{12}	−5	10	mA
		I_{13}	−5	10	mA
Power Dissipation (Ta=75℃)		P_D	450		mW
Temperature	Operating Ambient Temperature	T_{opr}	−20～+75		℃
	Storage Temperature	T_{stg}	−40～+150		℃

＊1：K of Vk indicates pins ① to ⑤ and ⑭ to ⑰.

＊2：K of Ik indicates pins ① to ⑤ and ⑭ to ⑰ and ratings when output is LOW level.

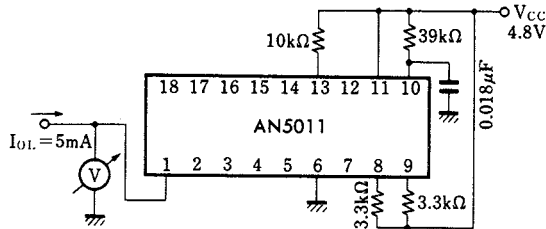## ■ Electrical Characteristics ($V_{cc}=V_{5-3}=12V$, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Output Voltage Low Level (Tuning)	$V_{OL(K)}$	1	$V_{cc}=4.8V$, $I_{OL}=5mA$			0.15	V
Output Current High Level (Tuning)	$I_{OH(K)}$	2	$V_{cc}=7.2V$, $V_{OH}=35V$			5	μA
Output Voltage Low Level (DEF)	$V_{OL(D)}$	3	$V_{cc}=4.8V$, $I_{OL}=5mA$			5	V
Output Current High Level (DEF)	$I_{OH(D)}$	4	$V_{cc}=7.2V$, $V_{OH}=14.4V$			5	μA
Input Current Low Level (CHD)	$I_{IL(CHD)}$	5	$V_{cc}=7.2V$, $V_{IL}=0V$	− 5			μA
Input Current Low Level (CHU)	$I_{IL(CHU)}$	7	$V_{cc}=7.2V$, $V_{IL}=0V$	− 5			μA
Input Current High Level (CHD)	$I_{IH(CHD)}$*1	6	$V_{cc}=4.8V$	50			μA
Input Current High Level (CHU)	$I_{IH(CHU)}$*1	8	$V_{cc}=4.8V$	50			μA
Input Current Low Level (KIN)	$I_{IL(KI)}$	9	$V_{cc}=7.2V$, $V_{IL}=0V$	−10			μA
Input Current High Level (KIN)	$I_{IH(KI)}$*2	10	$V_{cc}=4.8V$	200			μA
Input Current Low Level (SKP)	$I_{IL(SK)}$	11	$V_{cc}=7.2V$, $V_{IL}=0V$	− 5			μA
Input Current High Level (SKP)	$I_{IH(SK)}$*1	12	$V_{cc}=4.8V$	50			μA
Input Current Low Level (OSC)	$I_{IL(OS)}$	13	$V_{cc}=7.2V$, $V_{IL}=1.0V$			5	μA
Input Current High Level (OSC)	$I_{IH(OS)}$	14	$V_{cc}=4.8V$, $V_{IH}=4V$	1.7		3.2	mA
Oscillation Frequency (Clock)	fosc	15	$V_{cc}=6V$	1.5	2.0	2.5	kHz
Total Circuit Current	I_{tot}	16	$V_{cc}=6V$	23	35	50	mA

＊1：DEF Pin (⑦) shall be "H" level (3.0V or more).

＊2：DEF Pin (⑦) shall be "L" level (1.0V or less).

Note: Operating supply voltage is: V_{cc} (opr) = 4.8 ～ 7.2V.

Test Circuit 1 (V_OL(K))

$I_{OL} = 5mA$

10kΩ 39kΩ 0.018μF

V_{CC} 4.8V

AN5011

18 17 16 15 14 13 12 11 10

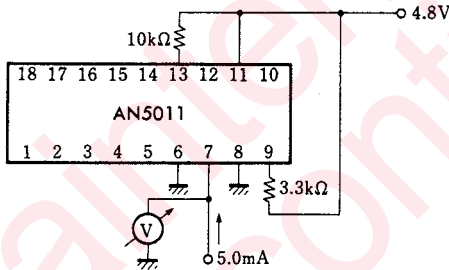1 2 3 4 5 6 7 8 9

3.3kΩ 3.3kΩ

Note: Pins ① to ⑤ and ⑭ to ⑰ are used for measuring pins. First, short-circuit pins ⑫ (KIN) and ⑤ (KI) to set the measuring pin to ⑤. Then, make CHU and CHD pins "L" level to set K1 to K16 sequentially. Pins other than measuring pins are not required for connection.
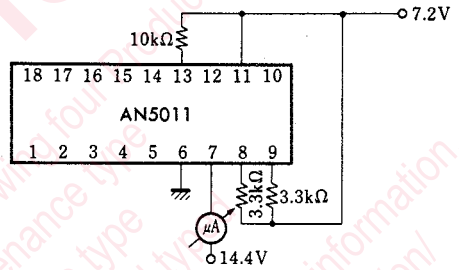
Test Circuit 2 (I_OH(K))

7.2V

10kΩ

+35V

1kΩ

mA

AN5011

18 17 16 15 14 13 12 11 10

1 2 3 4 5 6 7 8 9

3.3kΩ 3.3kΩ
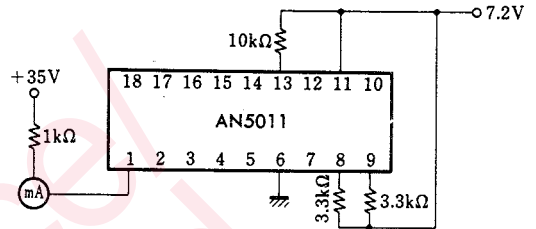
Note: Pins ① to ⑤ and ⑭ to ⑱ are used for measuring pins. Pins other than measuring pins are not required for connection.

Test Circuit 3 (V_OL(D))
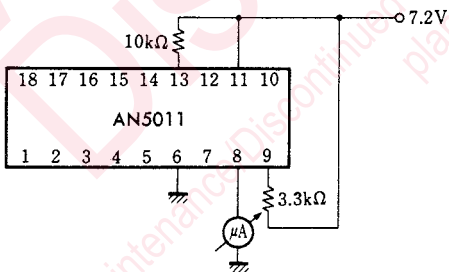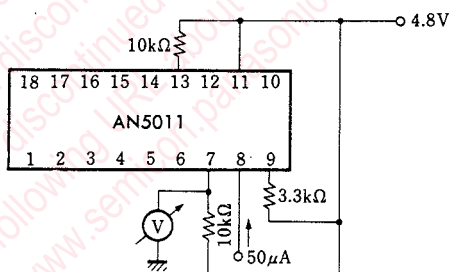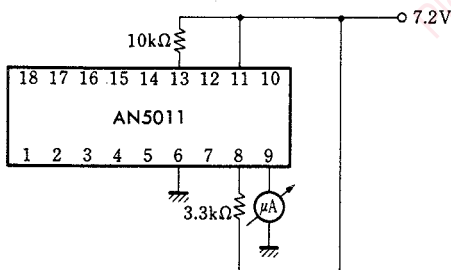
4.8V

10kΩ

AN5011

18 17 16 15 14 13 12 11 10

1 2 3 4 5 6 7 8 9

3.3kΩ

V

5.0mA

Test Circuit 4 (I_OH(D))

7.2V

10kΩ

AN5011

18 17 16 15 14 13 12 11 10

1 2 3 4 5 6 7 8 9

3.3kΩ 3.3kΩ

μA

14.4V

Test Circuit 5 (I_IL(CHD))

7.2V

10kΩ

AN5011

18 17 16 15 14 13 12 11 10

1 2 3 4 5 6 7 8 9

3.3kΩ

μA

Test Circuit 6 (I_IH(CHD))

4.8V

10kΩ

AN5011

18 17 16 15 14 13 12 11 10

1 2 3 4 5 6 7 8 9

10kΩ 3.3kΩ

V

50μA

Test Circuit 7 (I_IL(CHU))

7.2V

10kΩ

AN5011

18 17 16 15 14 13 12 11 10

1 2 3 4 5 6 7 8 9

3.3kΩ μA

Test Circuit 8 (I_IH(CHU))

4.8V

10kΩ

AN5011

18 17 16 15 14 13 12 11 10

1 2 3 4 5 6 7 8 9

V

10kΩ 3.3kΩ

50μA
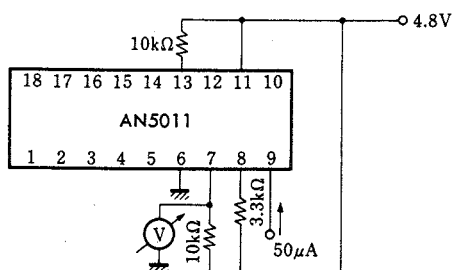
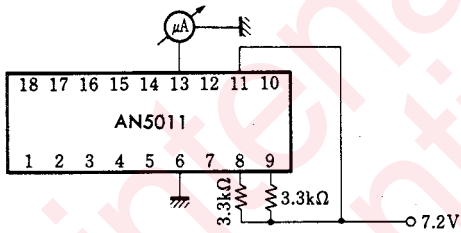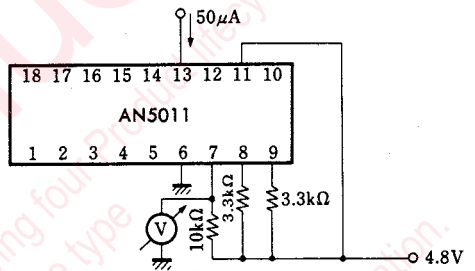**Test Circuit 9** ($I_{IL(KI)}$)
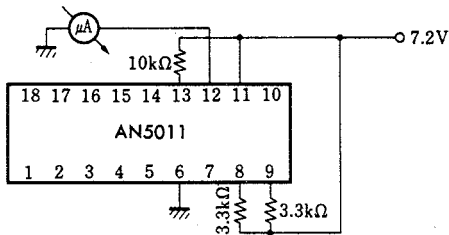
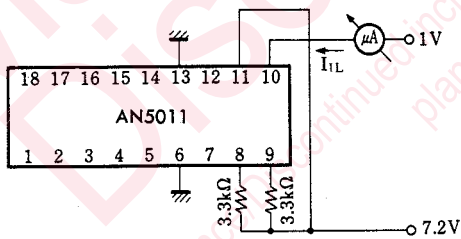**Test Circuit 10** ($I_{IH(KI)}$)
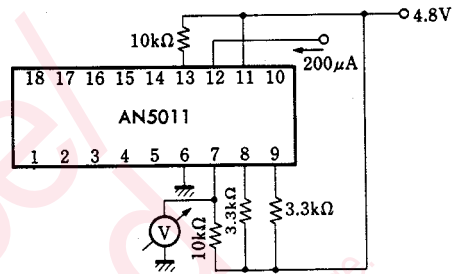
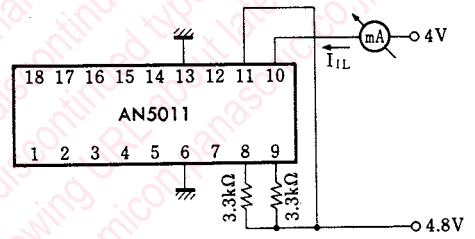**Test Circuit 11** ($I_{IL(SK)}$)
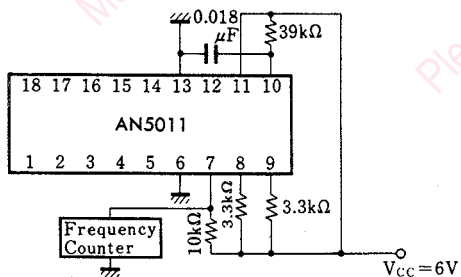

Test Circuit 12 ($I_{IH(SK)}$)

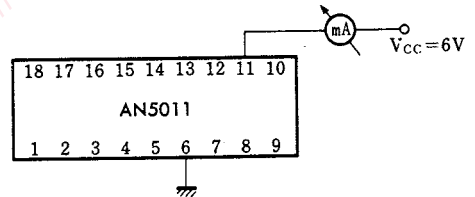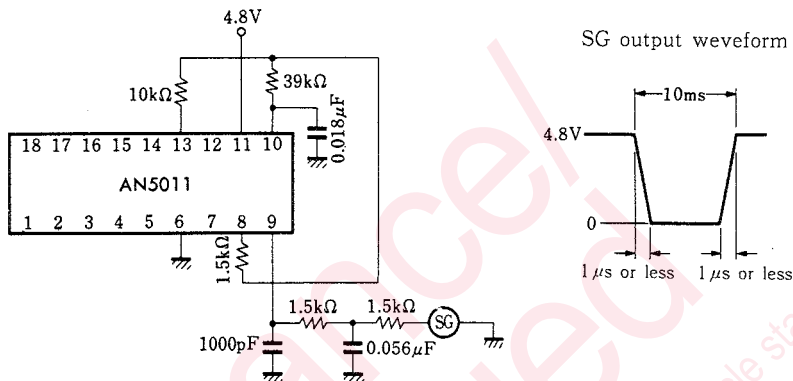**Test Circuit 13** ($I_{IL(OS)}$)

Test Circuit 14 ($I_{IH(OS)}$)

Test Circuit 15 (f_{OSC})

Test Circuit 16 (I_{tot})

Test Circuit 17 (sequential tuning operation by CHU and CHD inputs)

SG output weveform

■ Application Circuit
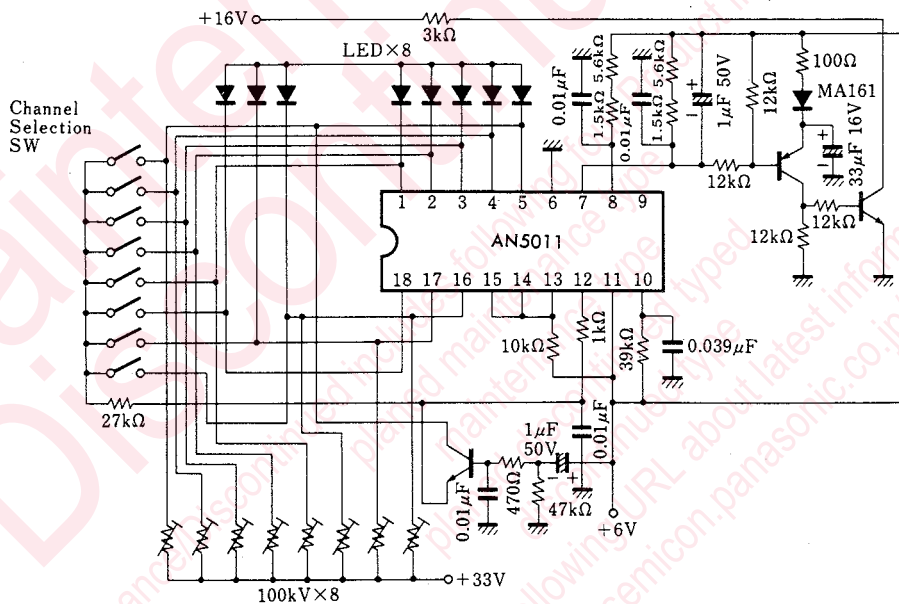
■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Ch.Selection Output(5)	10	VOsc. Filter
2	Ch.Selection Output(4)	11	Vcc
3	Ch.Selection Output(3)	12	Key Input
4	Ch.Selection Output(2)	13	Skip Input
5	Ch.Selection Output(1)	14	Ch.Selection Output(10)
6	GND	15	Ch.Selection Output(9)
7	AFT Defeat Input	16	Ch.Selection Output(8)
8	Ch.Down Input	17	Ch.Selection Output(7)
9	Ch.Up Input	18	Ch.Selection Output(6)

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