

N-channel 100 V, 0.02 Ω typ., 10 A, STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet – production data

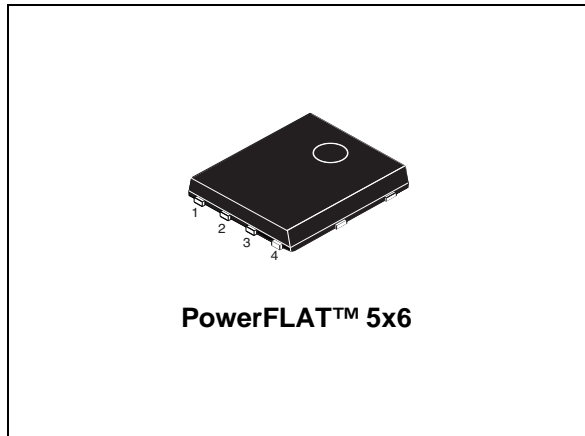
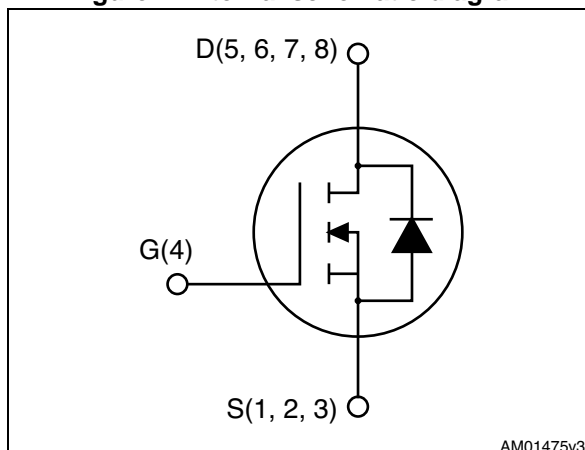


Figure 1. Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STL40N10F7	100 V	0.024 Ω	10 A	5 W

- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the 7th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL40N10F7	40N10F7	PowerFLAT™ 5x6	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	40	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	28	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	10	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb}=100\text{ }^\circ\text{C}$	7	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	40	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	5	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. This value is rated according to R_{thj-c} .
2. This value is rated according to $R_{thj-pcb}$.
3. Pulse width limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.08	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	31	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1 inch², 2oz Cu, $t < 10$ sec

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\ \mu A$	100			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 100\ V$			10	μA
		$V_{GS} = 0, V_{DS} = 100\ V, T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = +20\ V$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\ V, I_D = 10\ A$		0.02	0.024	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\ V, f = 1\ MHz, V_{GS} = 0$	-	1270	-	pF
C_{oss}	Output capacitance		-	290	-	pF
C_{riss}	Reverse transfer capacitance		-	24	-	pF
Q_g	Total gate charge	$V_{DD} = 50\ V, I_D = 32\ A, V_{GS} = 10\ V$ (see Figure 14)	-	19	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain charge		-	4.5	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ V, I_D = 16\ A, R_G = 4.7\ \Omega, V_{GS} = 10\ V$ (see Figure 13)	-	12	-	ns
t_r	Rise time		-	17.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	22	-	ns
t_f	Fall time		-	5.6	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	32	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	128	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 32 \text{ A}$, $V_{GS} = 0$	-	-	1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 32 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 80 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$	-	41		ns
Q_{rr}	Reverse recovery charge		-	47		nC
I_{RRM}	Reverse recovery current		-	2.3		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

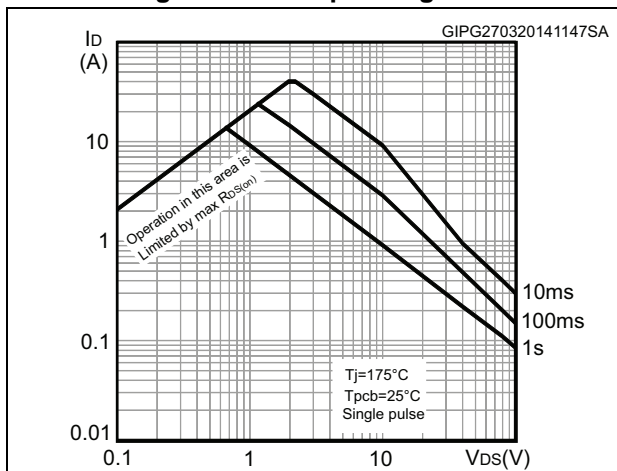


Figure 3. Thermal impedance

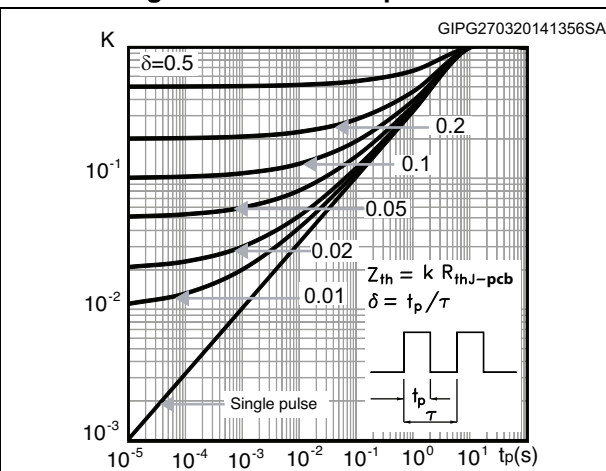


Figure 4. Output characteristics

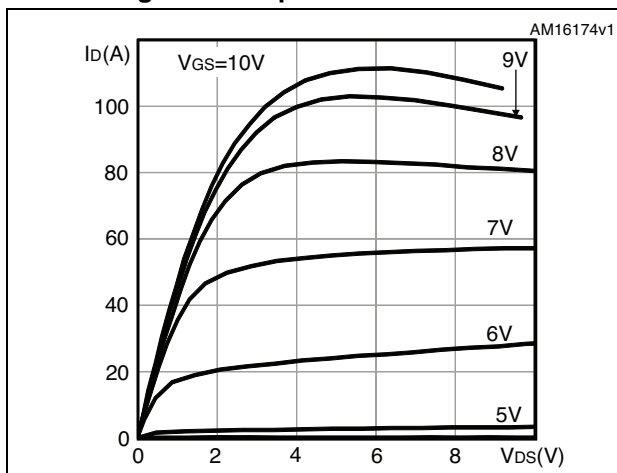


Figure 5. Transfer characteristics

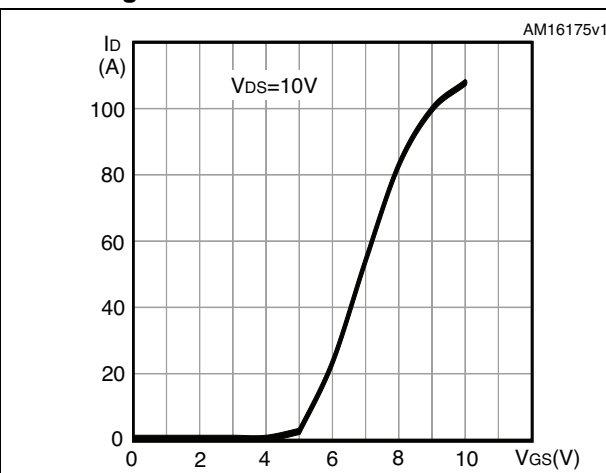


Figure 6. Gate charge vs gate-source voltage

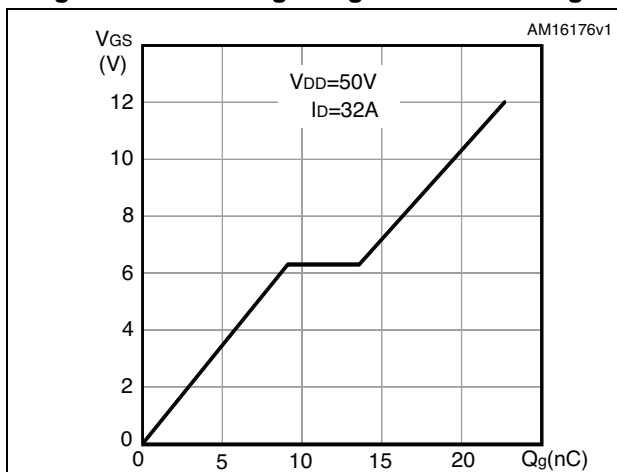


Figure 7. Static drain-source on-resistance

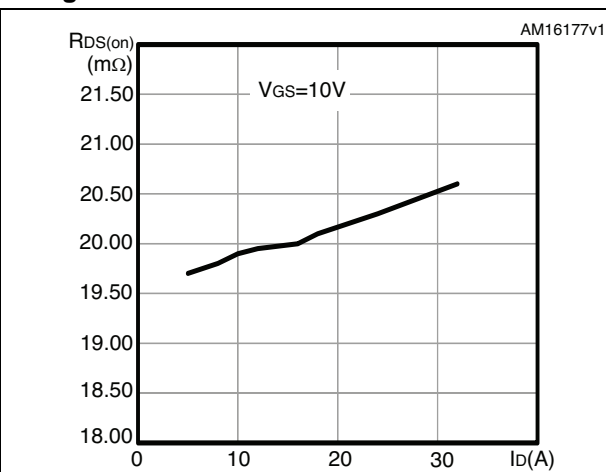


Figure 8. Capacitance variations

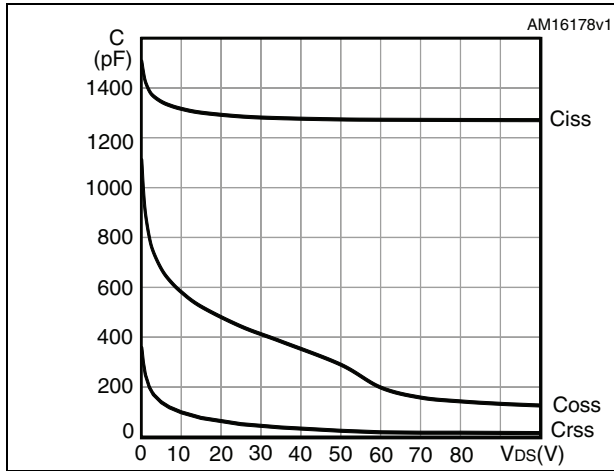


Figure 9. Normalized gate threshold voltage vs temperature

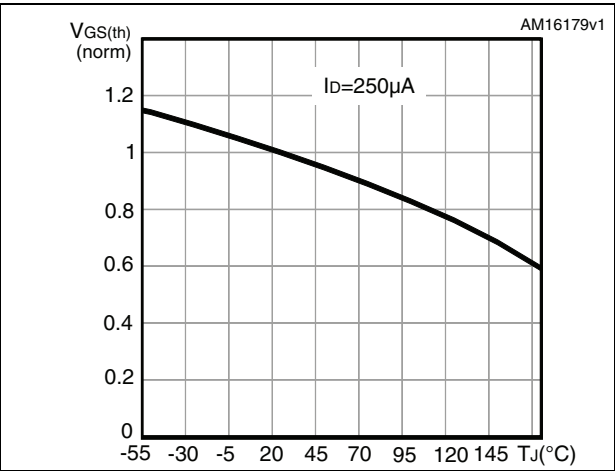


Figure 10. Normalized on-resistance vs temperature

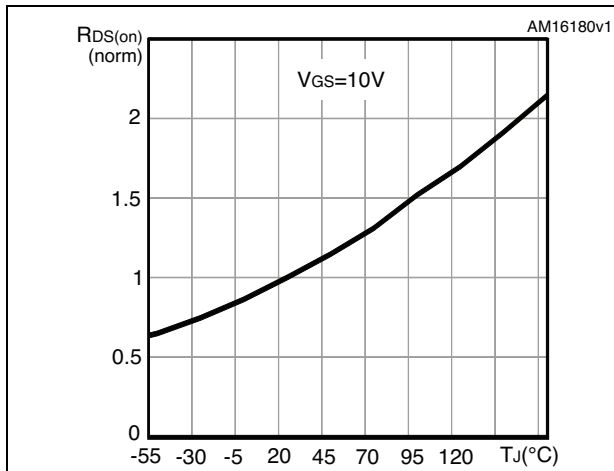


Figure 11. Normalized V(BR)DSS vs temperature

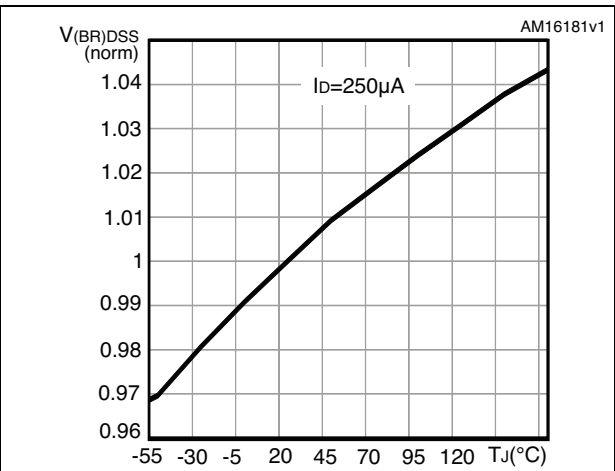
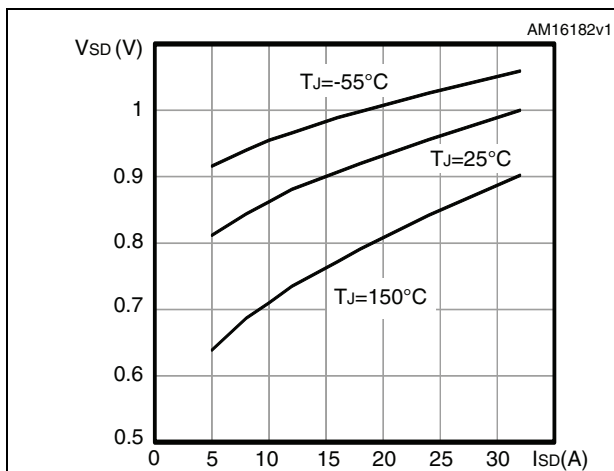


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load



Figure 14. Gate charge test circuit

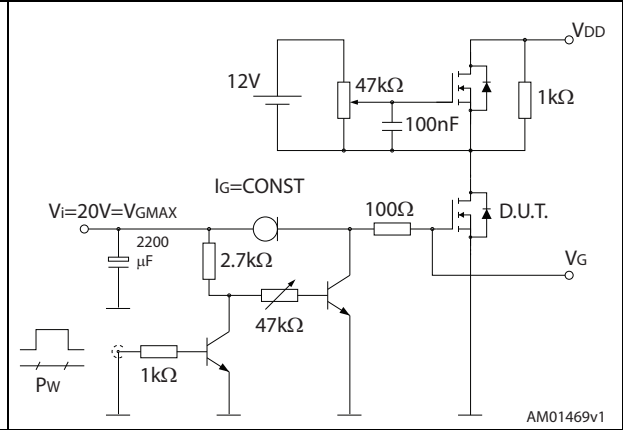


Figure 15. Test circuit for inductive load switching and diode recovery times



Figure 16. Unclamped inductive load test circuit

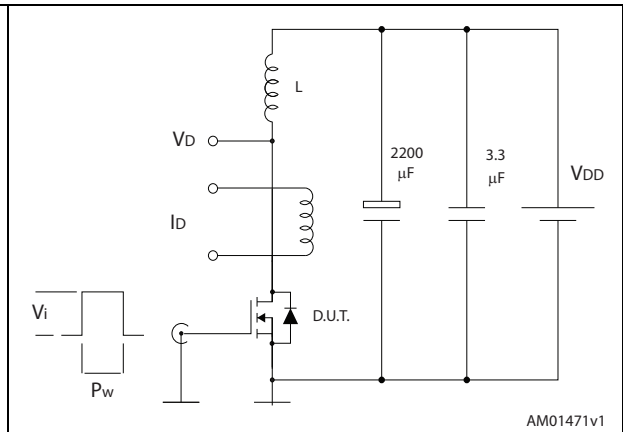
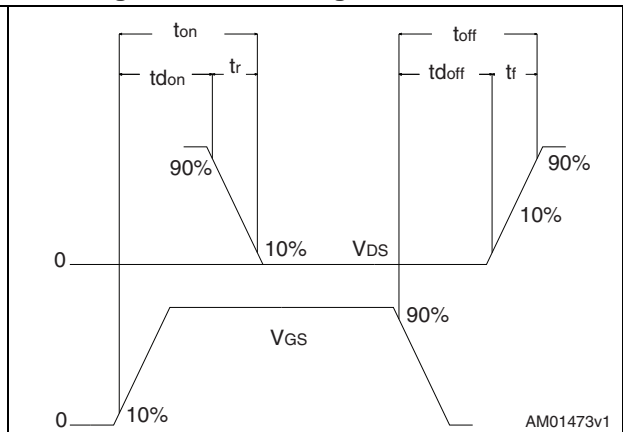


Figure 17. Unclamped inductive waveform



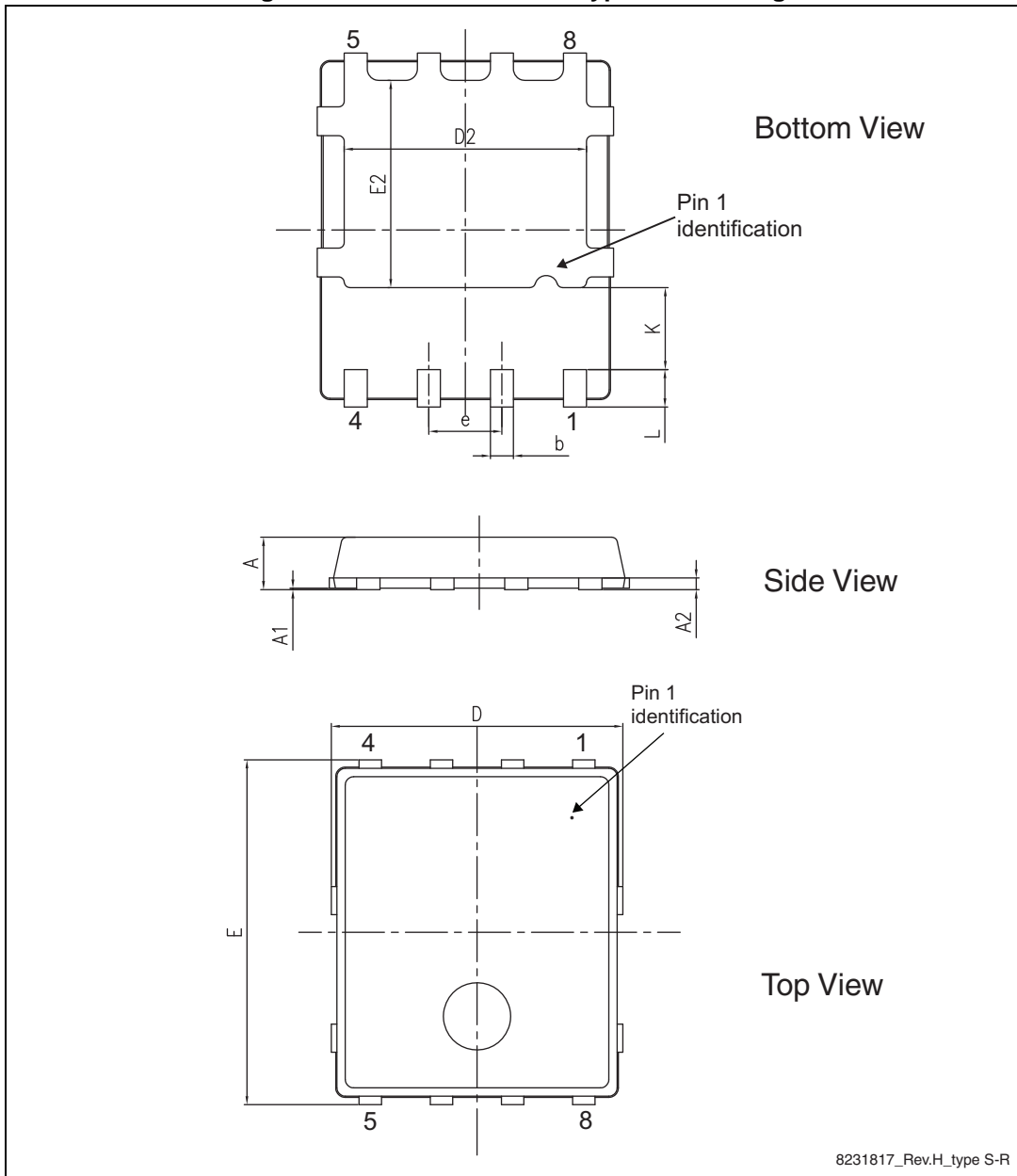
Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 19. PowerFLAT™ 5x6 type S-R drawing



5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape^(a)

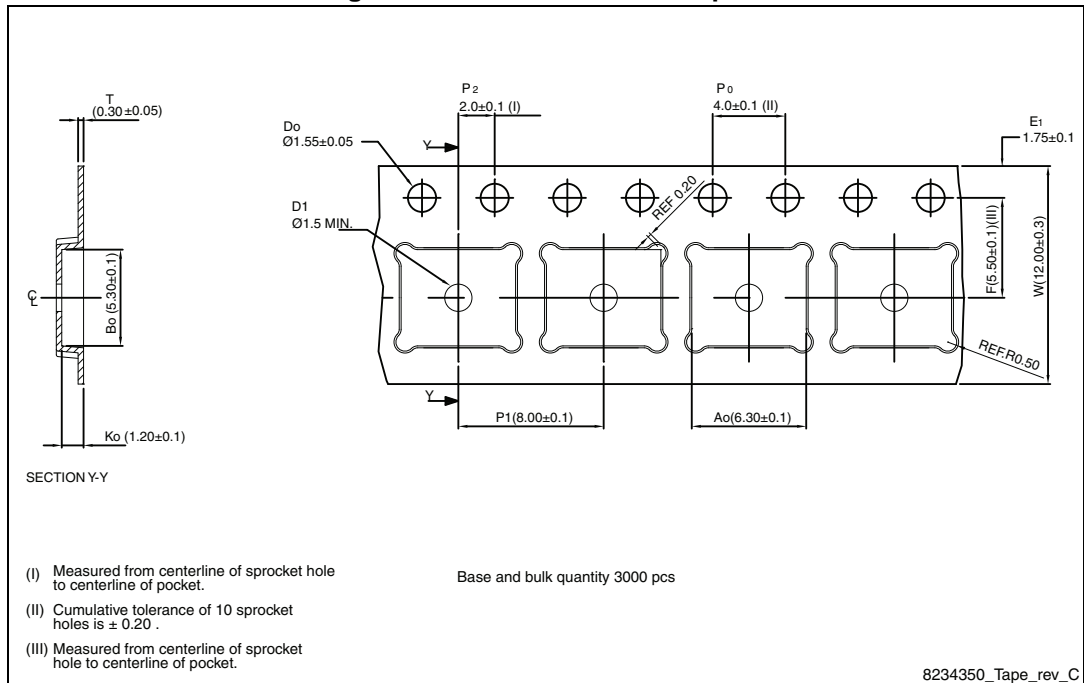
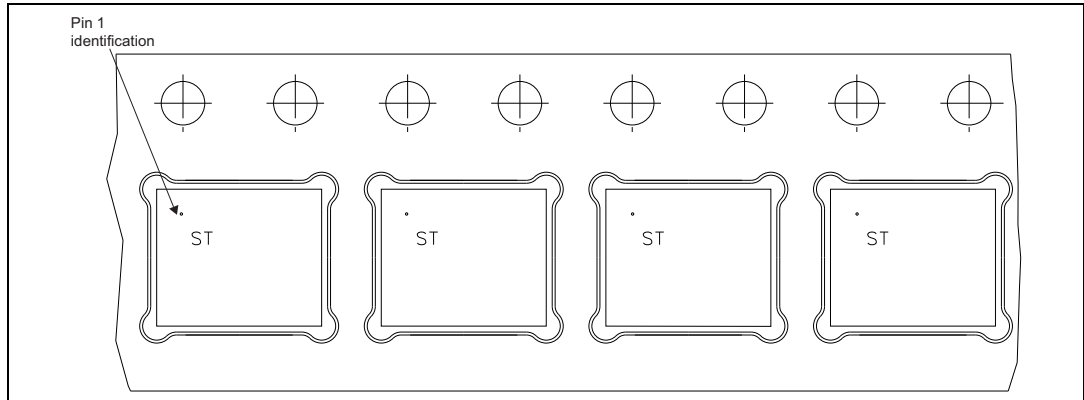
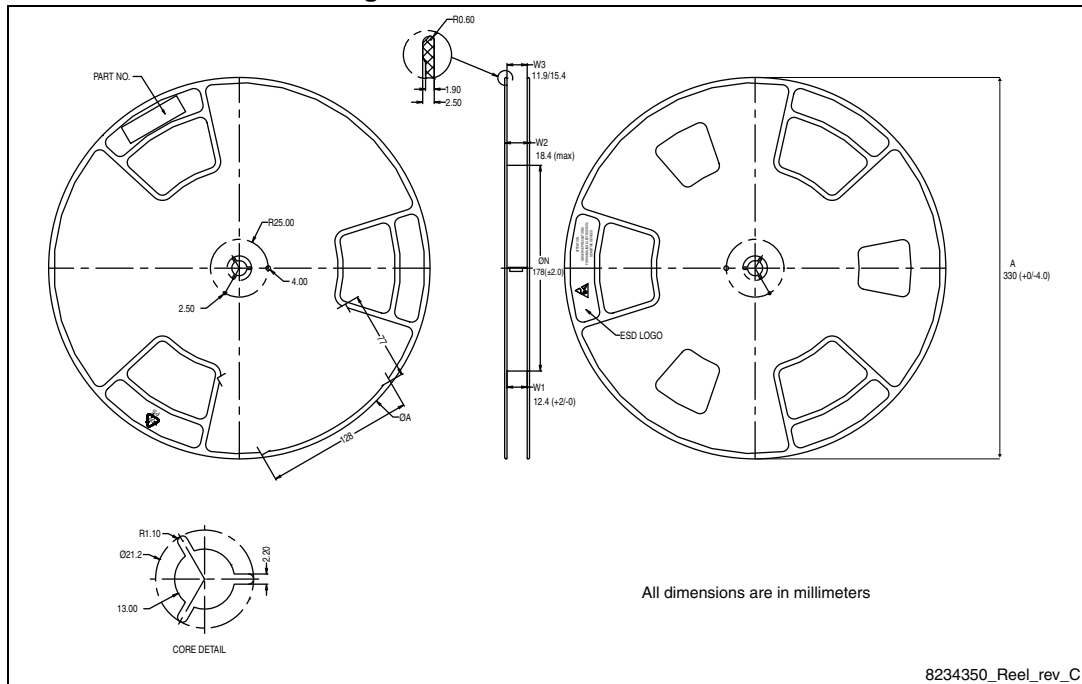


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
20-May-2013	1	First release.
02-Apr-2014	2	<ul style="list-style-type: none">– Document status promoted from preliminary data to production data– Modified: $V_{GS(th)}$ values in Table 4– Modified: the entire typical values in Table 5, 6 and 7– Added: Section 2.1: Electrical characteristics (curves)– Updated: Figure 13, 14, 15 and 16– Minor text changes

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