P-Channel Logic Level Enhancement Mode Power MOSFET

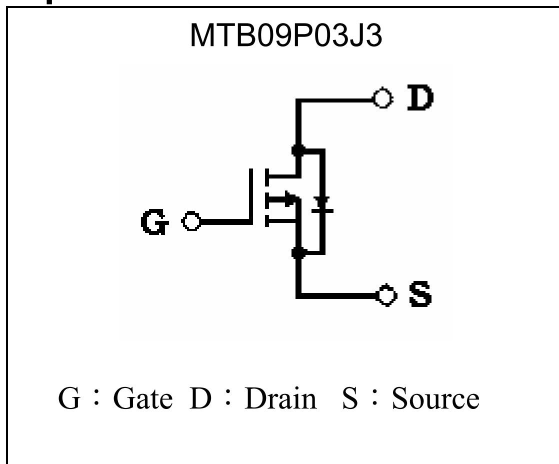
MTB09P03J3

BV_{DSS}	-30V
I_D	-75A
R_{DSON}@V_{GS}=-10V, I_D=-25A	8mΩ(typ.)
R_{DSON}@V_{GS}=-4.5V, I_D=-10A	11mΩ(typ.)

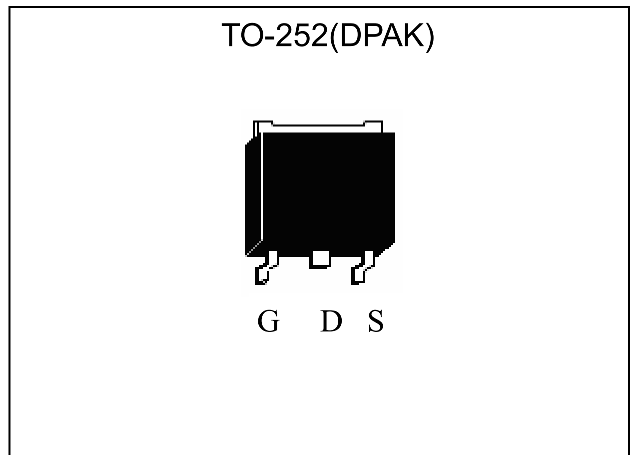
Features

- Low Gate Charge
- Simple Drive Requirement
- Pb-free lead plating & Halogen-free package

Equivalent Circuit

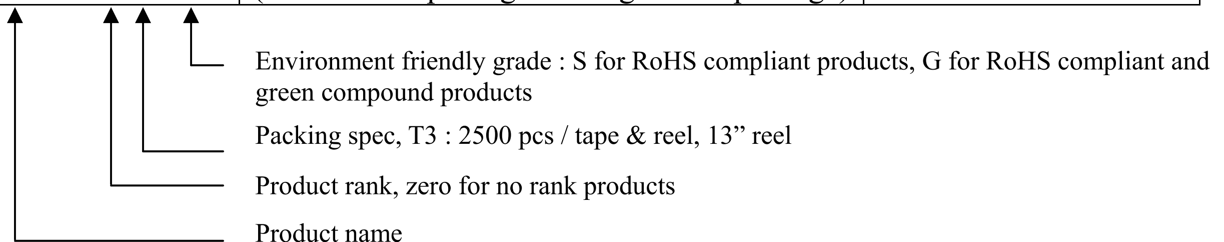


Outline



Ordering Information

Device	Package	Shipping
MTB09P03J3-0-T3-G	TO-252 (Pb-free lead plating & Halogen-free package)	2500 pcs / Tape & Reel



Absolute Maximum Ratings (Tc=25°C, unless otherwise noted)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	
Continuous Drain Current @ Tc=25°C	I_D	-75	A
Continuous Drain Current @ Tc=100°C	I_D	-48	
Pulsed Drain Current *1	I_{DM}	-160	
Avalanche Current	I_{AS}	-20	
Avalanche Energy @ L=0.1mH, I_D=-20A, R_G=25Ω	E_{AS}	20	mJ
Total Power Dissipation @Tc=25℃	Pd	93	W
Total Power Dissipation @Tc=100℃		50	
Operating Junction and Storage Temperature Range	Tj, Tstg	-55~+150	°C

100% UIS testing in condition of V_D=-15V, L=0.1mH, V_G=-10V, I_L=-15A, Rated V_{DS}=-30V P-Channel

Note : *1. Pulse width limited by maximum junction temperature
*2. Duty cycle ≤ 1%

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	1.34	°C/W
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	50 (Note)	°C/W
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	110	°C/W

Note : When mounted on the minimum pad size recommended (PCB mount).

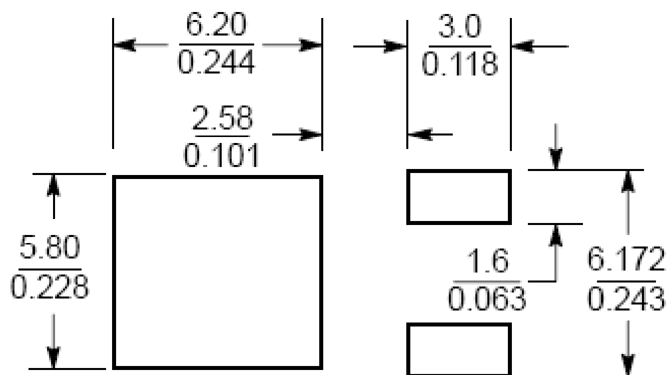
Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	-30	-	-	V	V_{GS}=0V, I_D=-250μA
$V_{GS(th)}$	-1	-1.5	-3	V	V_{DS} =V_{GS}, I_D=-250μA
G_{FS} *1	-	37	-	S	V_{DS} =-5V, I_D=-25A
I_{GSS}	-	-	±100	nA	V_{GS}=±20, V_{DS}=0V
I_{DSS}	-	-	-1	μA	V_{DS} =-24V, V_{GS} =0V
	-	-	-10		V_{DS} =-24V, V_{GS} =0V, Tj=125°C
$R_{DS(ON)}$ *1	-	8	9	mΩ	V_{GS} =-10V, I_D=-25A
	-	11	15		V_{GS} =-4.5V, I_D=-10A
Dynamic					
Qg *1, 2	-	56	-	nC	I_D=-25A, V_{DS}=-15V, V_{GS}=-10V
Qgs *1, 2	-	7.9	-		
Qgd *1, 2	-	11.5	-		
$t_{d(ON)}$ *1, 2	-	22	-	ns	V_{DS}=-15V, I_D=-1A, V_{GS}=-10V, R_G=2.7Ω
tr *1, 2	-	20	-		
$t_{d(OFF)}$ *1, 2	-	65	-		
t_f *1, 2	-	12	-		

Ciss	-	4400	-	pF	V_{GS}=0V, V_{DS}=-15V, f=1MHz
Coss	-	486	-		
Crss	-	405	-		
Rg	-	3	-	Ω	V_{GS}=15mV, V_{DS}=0, f=1MHz
Source-Drain Diode					
I_S *1	-	-	-75	A	
I_{SM} *3	-	-	-160		
V_{SD} *1	-	-	-1.2	V	I_F=-24A, V_{GS}=0V
trr	-	47	-	ns	I_F=I_S, dI_F/dt=100A/μs
Qrr	-	43	-	nC	

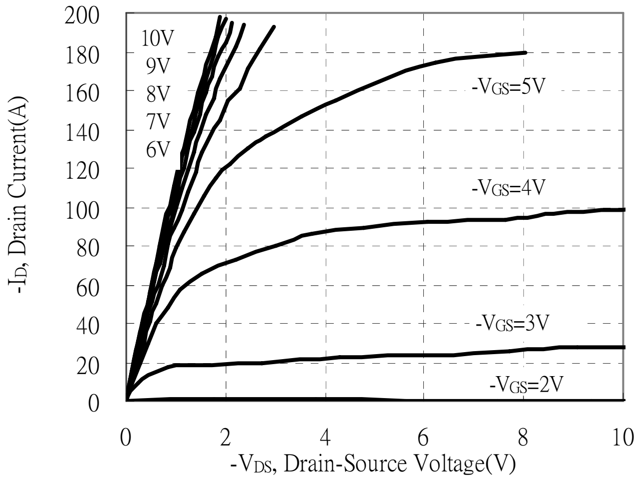
Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
*2.Independent of operating temperature
*3.Pulse width limited by maximum junction temperature.

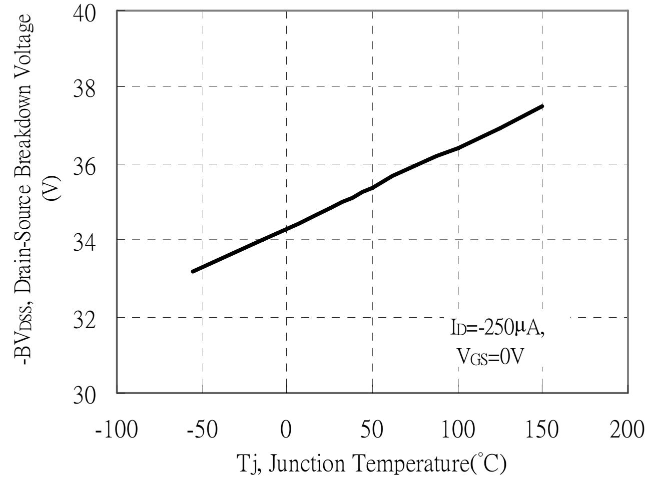
Recommended soldering footprint

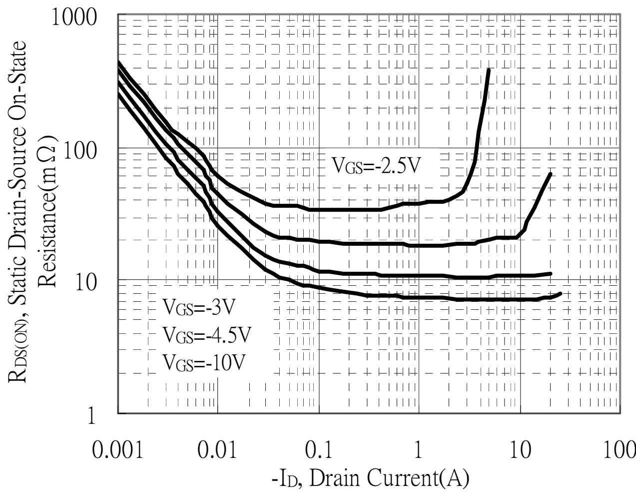


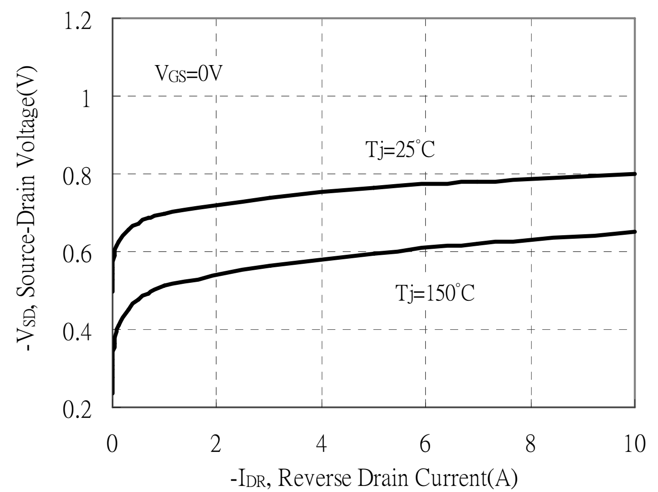
Unit (mm / inch)

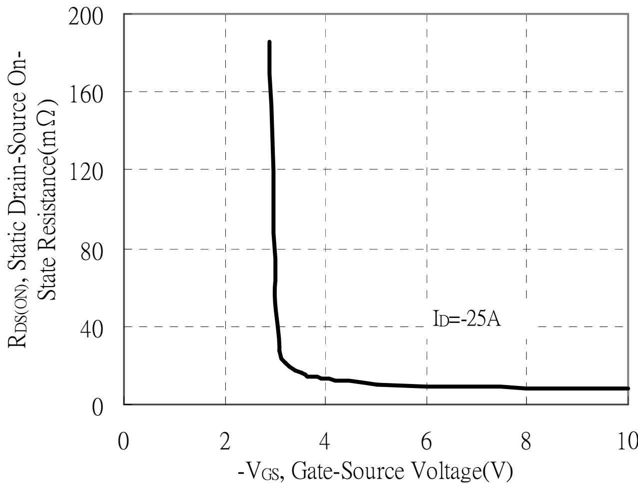
Typical Characteristics

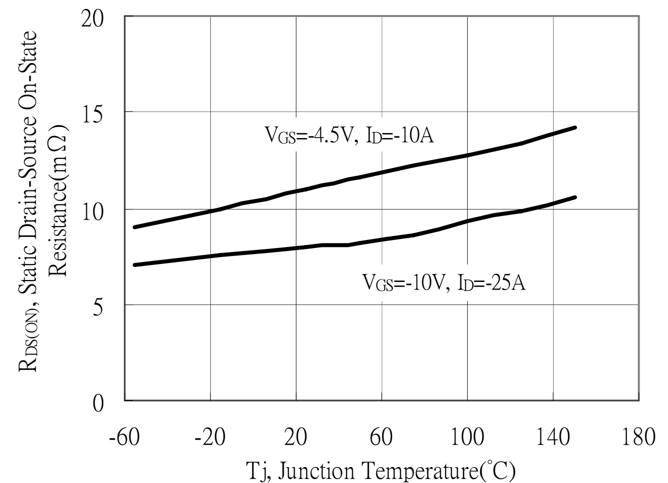




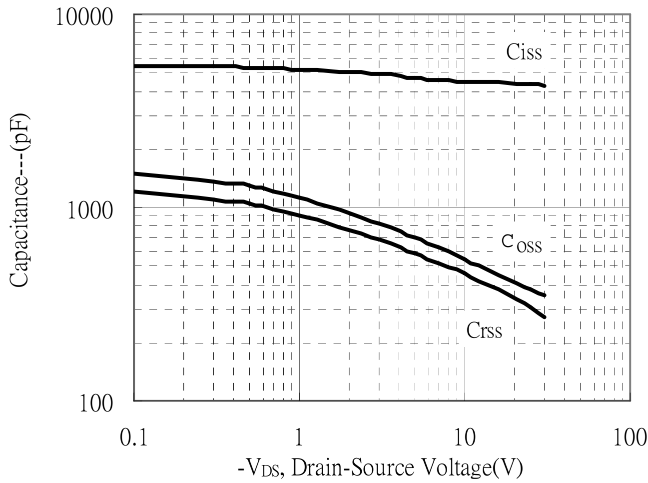


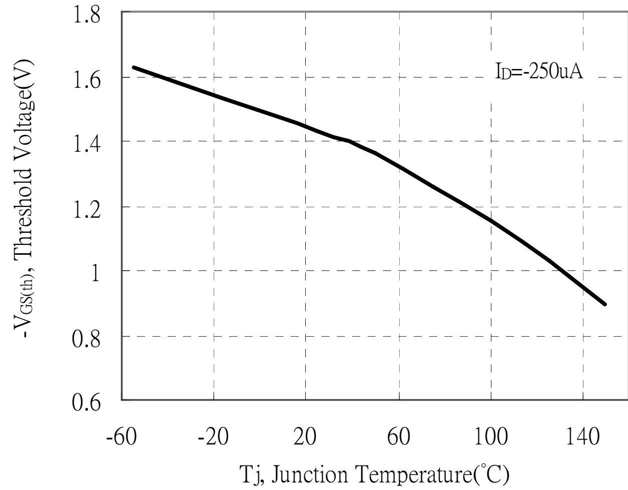


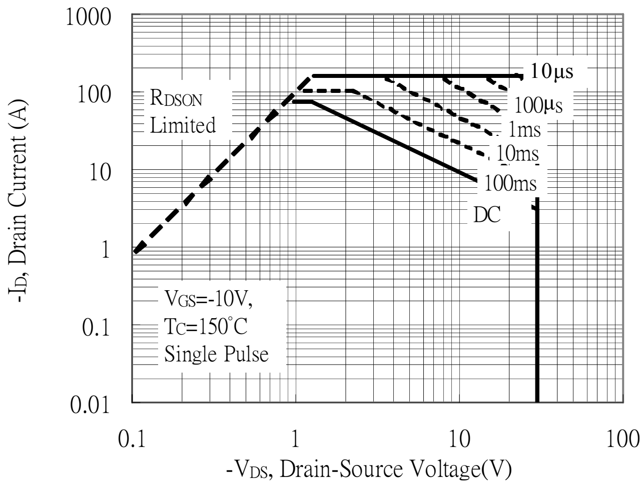


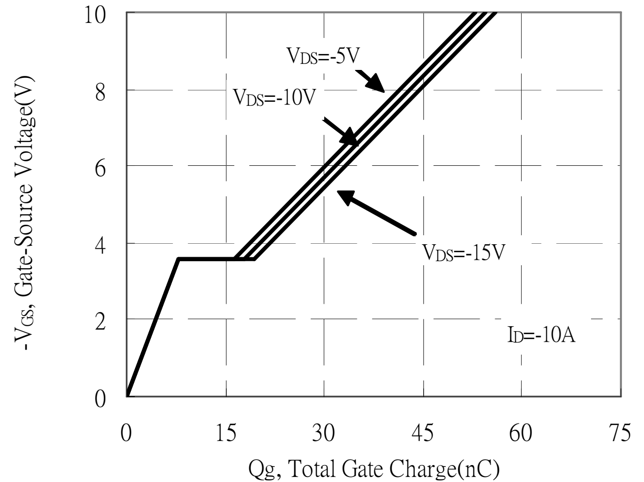


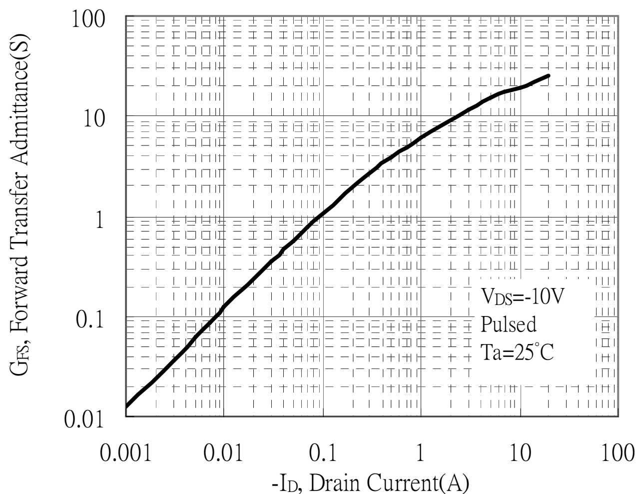
Typical Characteristics(Cont.)

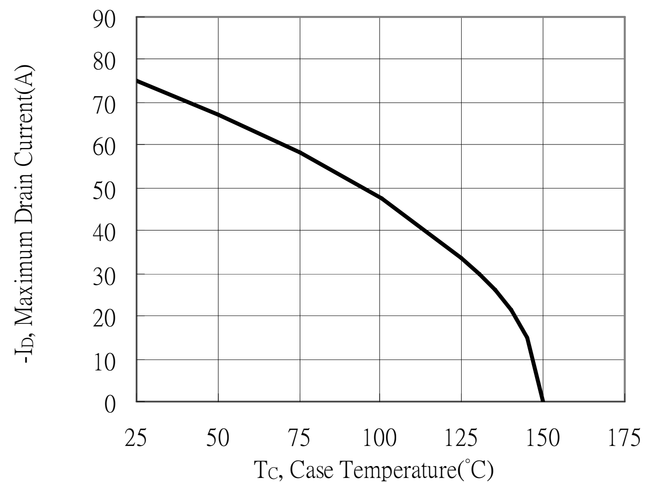




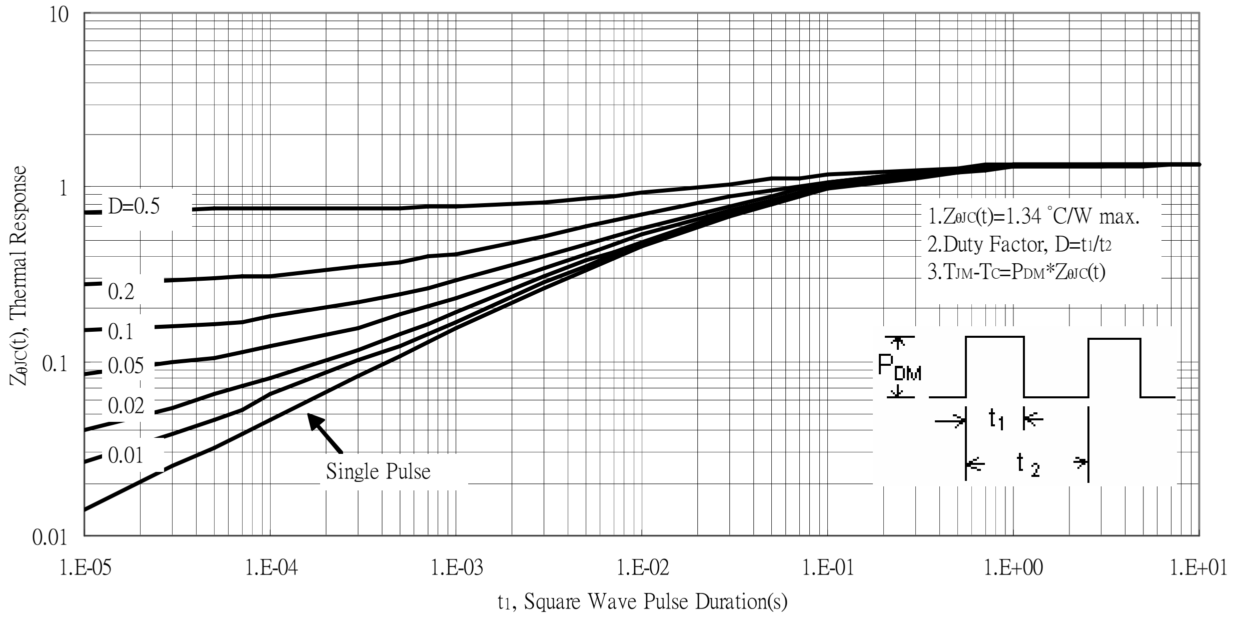




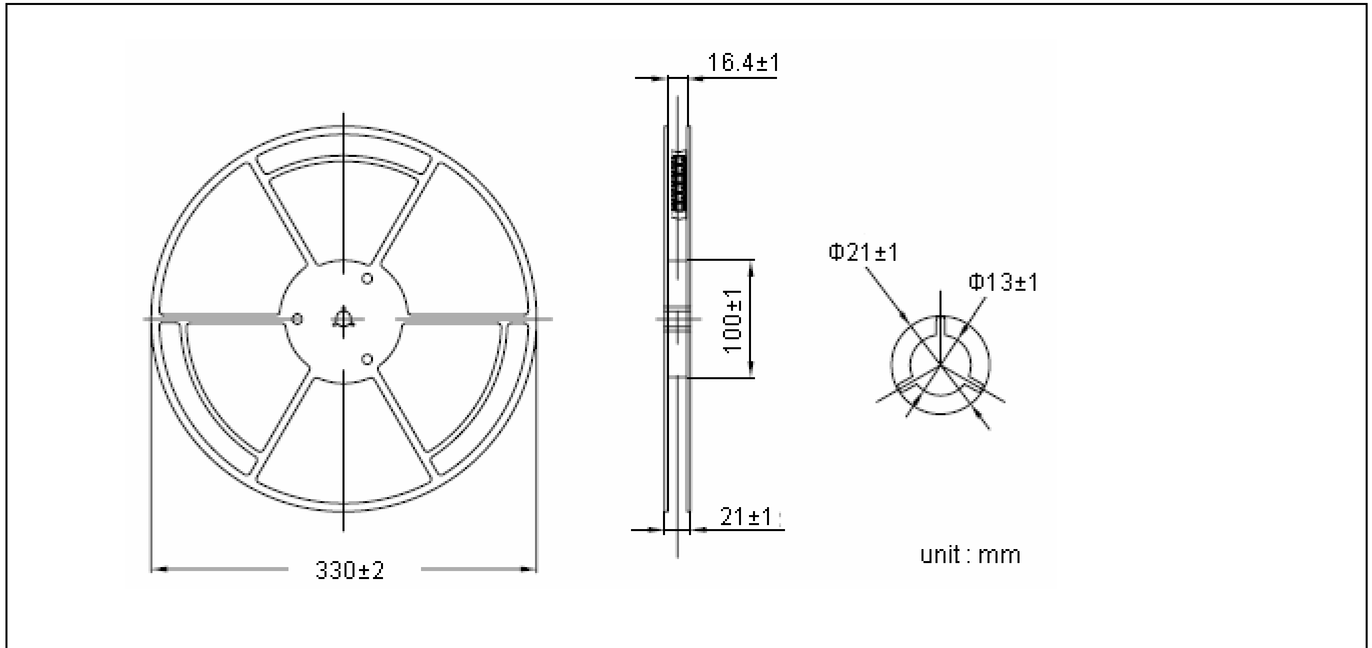




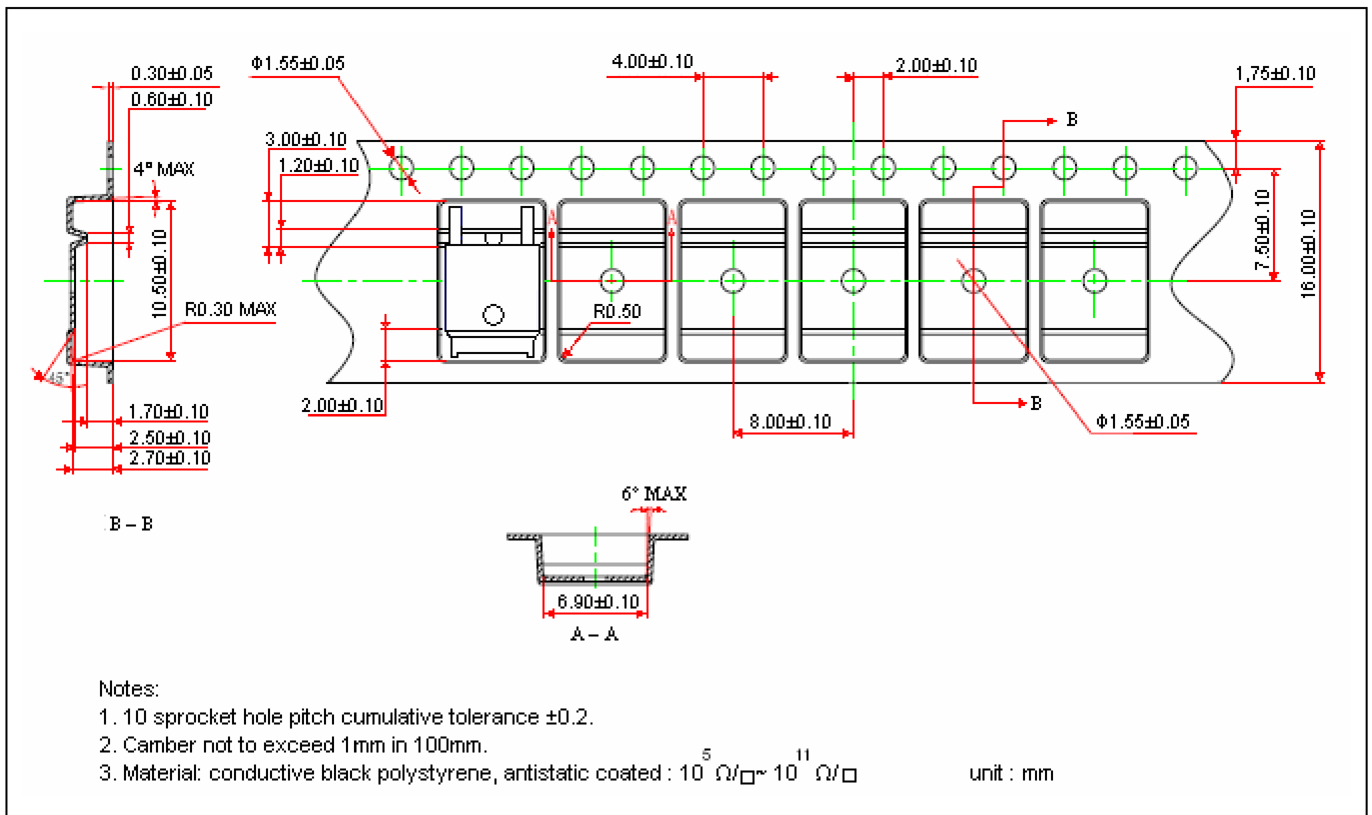
Typical Characteristics(Cont.)



Reel Dimension



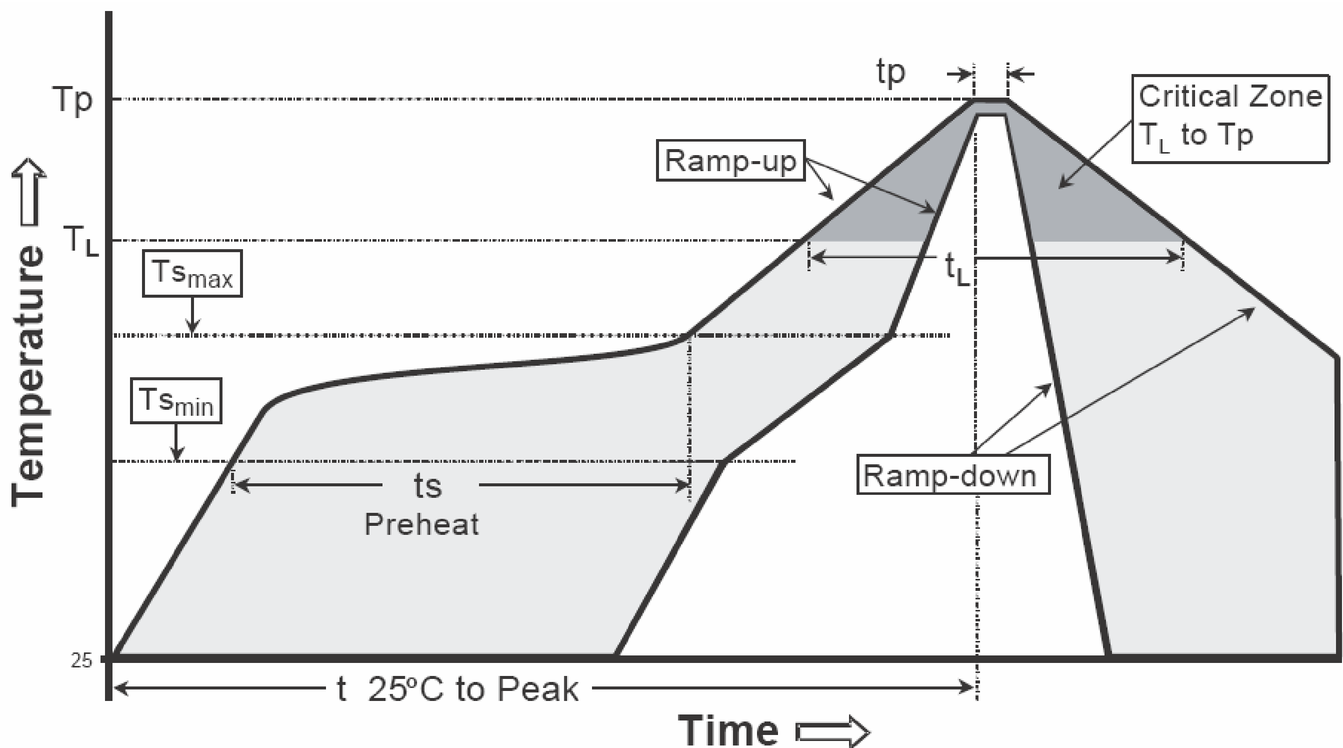
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

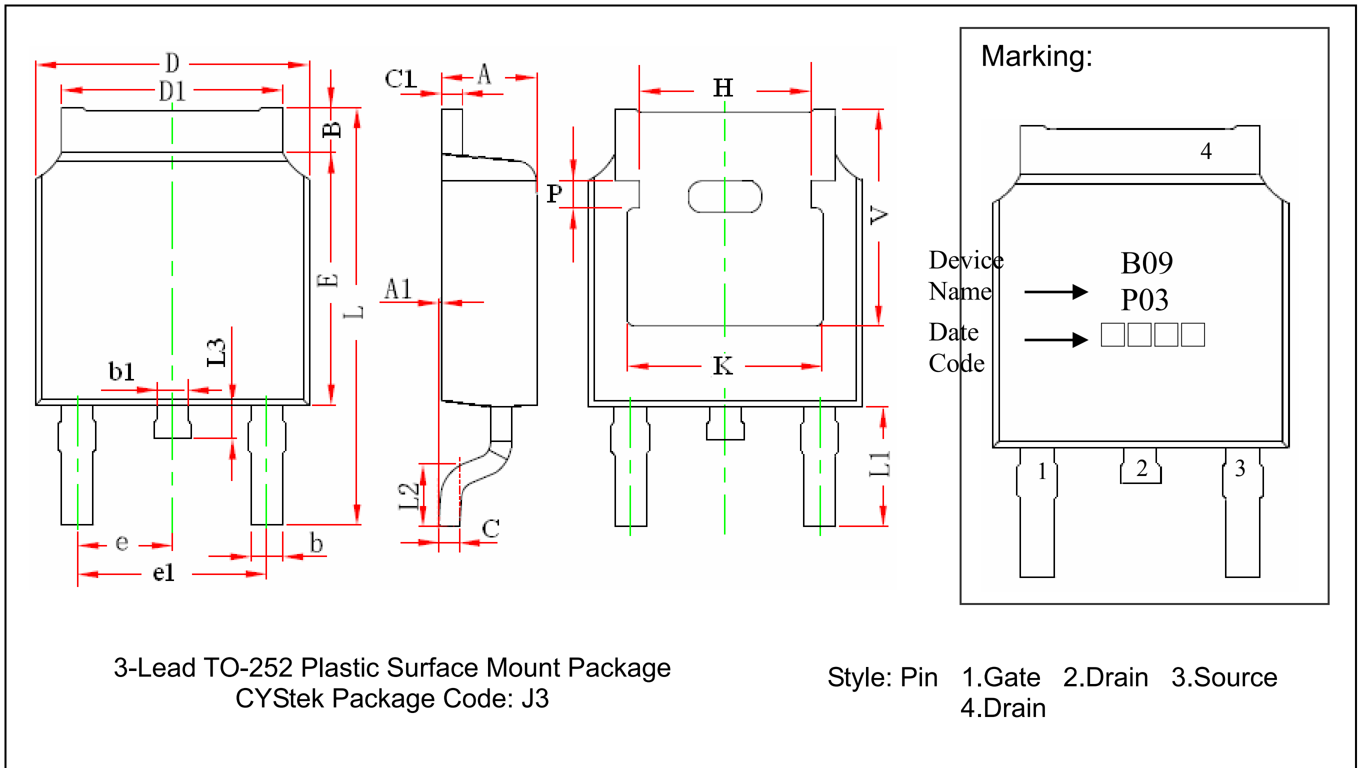
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time(ts_{min} to ts_{max})	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-252 Dimension



3-Lead TO-252 Plastic Surface Mount Package
CYStek Package Code: J3

Style: Pin 1.Gate 2.Drain 3.Source 4.Drain

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.087	0.094	2.200	2.400	e	0.086	0.094	2.186	2.386
A1	0.000	0.005	0.000	0.127	e1	0.172	0.188	4.372	4.772
B	0.039	0.048	0.990	1.210	H	0.163	REF	4.140	REF
b	0.026	0.034	0.660	0.860	K	0.190	REF	4.830	REF
b1	0.026	0.034	0.660	0.860	L	0.386	0.409	9.800	10.400
C	0.018	0.023	0.460	0.580	L1	0.114	REF	2.900	REF
C1	0.018	0.023	0.460	0.580	L2	0.055	0.067	1.400	1.700
D	0.256	0.264	6.500	6.700	L3	0.024	0.039	0.600	1.000
D1	0.201	0.215	5.100	5.460	P	0.026	REF	0.650	REF
E	0.236	0.244	6.000	6.200	V	0.211	REF	5.350	REF

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead : Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.

- CYStek reserves the right to make changes to its products without notice.
- CYStek ***semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.***
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.