Audio 1-Chip SOC

BM94801KUT

General Description

The BM94801KUT is a 1-Chip SOC for multimedia audio systems, which supports the Bluetooth A2DP, USB memory, SD memory card, and CD.
This IC has a built-in ARM946ES processor, SDRAM, and various peripherals. It is designed to download programs from external Serial Flash ROM and execute system control, file system management, Audio CODEC, and a wide range of media control.

Features

This IC includes the following blocks:

Processor
- ARM946ES Microprocessor Core

Memory
- SDRAM
- Initial Program ROM
- Program SRAM
- Data SRAM
- SDRAM Controller

System
- Multilayer AHB
- DMA BUS
- Interrupt Controller
- DMA Controller

Serial, Media I/F
- GPIO
- Pin Controller
- USB2.0 Dual Role (Host/Device) Controller
- SD I/F
- Quad SPI I/F
- SPI I/F (Master/Slave)
- I2C I/F (Master/Slave)
- UART I/F
- I2S Input I/F
- I2S Output I/F
- CD Servo Controllers
- CD-ROM Decoder
- General Purpose A/D Converter

Timer
- Timer
- Watchdog Timer
- Real Time Clock

Other
- Clock Generator
- Reset Generator
- PLL

Package

TQFP128UM
16.00mm × 16.00mm × 1.20mm
0.4 mm pitch

Application

Component Stereo

Application Block

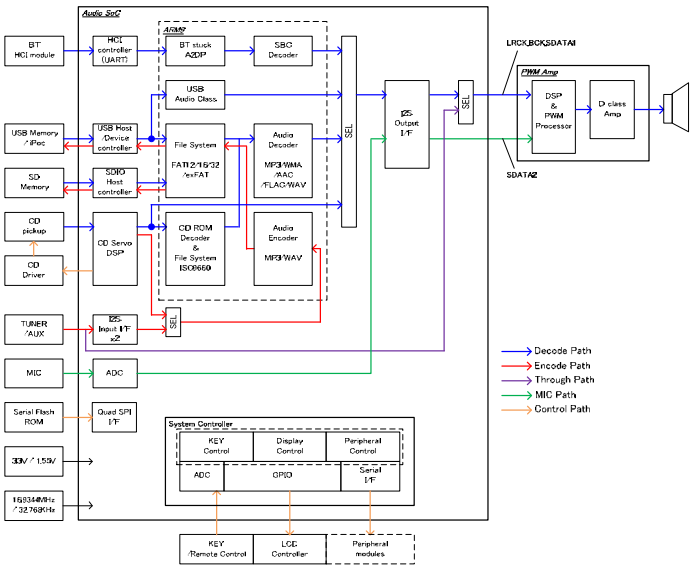


Figure 1.

ARM946ES Microprocessor Core
◇ 32 Bit RISC Processor
◇ Operating Frequency: 96 MHz (118 DMIPS)
◇ 8 kByte Cache
4 kByte Data Cache
4 kByte Instruction Cache

SDRAM
◇ 16 MBits
◇ SDRAM with built-in MSM56V16160K from LAPIS Semiconductor
◇ 2 Bank x 524,288 Word x 16 Bit

Initial Program ROM
◇ ITCM ROM Size: 2 kByte (512 Word x 32 Bit)
◇ Boot Program
◇ No Wait Access

REMAP
◇ Remapping can be implemented by writing to internal registers.

SHADOW SRAM
◇ RAM Size: 512 Byte (128 Word x 32 Bit)
◇ No Wait Access

Program SRAM
◇ ITCM RAM Size: 64 kByte (16,384 Word x 32 Bit)
◇ No Wait Access

Data SRAM
◇ DTCM RAM Size: 64 kByte (16,384 Word x 32 Bit)
◇ No Wait Access

SDRAM Controller
◇ Supports SDRAM
◇ Supports 11 Bit row address, 8-bit column address, and 1-bit bank address to SDRAM

AMBA
◇ Multilayer AHB
◇ 32 Bit Data Bus
◇ Arbitrates ARM and DMA access with an arbiter
◇ Allows parallel access according to different master/slave combinations

Interrupt Controller
◇ 32 IRQ Interrupt Lines
◇ 1 FIQ Interrupt Line
◇ Allows programmable setting of interrupt priority levels
◇ Allows setting of 16 vector addresses

DMA Controller
◇ Up to 2 DMA Channels
◇ Channel FIFO Depth Up to 16 Bytes
◇ Allows programmable setting of transfer data width in the range of 1 byte to 4 bytes
◇ Allows programmable setting of channel priority levels
◇ Maximum Block Length Up to 4,095 Words
◇ Includes 12 handshake interfaces available for assignment to channels with software
◇ Supports multiblock transfers
◇ Connects the master board to system bus

GPIO
◇ GPIO0 (32 pins), GPIO1 (32 pins)
◇ Supports a maximum of 64 I/O pins
◇ Supports the interrupt function
◇ Supports external level-sensitive interrupt

Pin Controller

◇ Controls connection settings between pins and blocks

Block		Number of GPIO Pins
Dedicated GPIO Pins		20
Combined GPIO Pins		44
	One Line of 2-Ch I2S Output	5
	Two Lines of 2-Ch I2S Input	6
	SDIO I/F	8
	SPI Master	4
	SPI Slave	4
	Quad SPI I/F	6
	2-Ch UART	6
	2-Ch I2C Master/Slave	4
	RCR	1

USB 2.0 Dual Role (Host/Device) Controller

◇ USB 2.0 Compatible
◇ Bit Rate: High Speed (480 Mbps) / Full Speed (12 Mbps)
◇ Configurable for up to five transmit endpoint FIFOs and four receive endpoint FIFOs (including endpoint 0)
◇ Each endpoint FIFO supports bulk transfer, interrupt transfer, and isochronous transfer.
◇ 2048-Byte RAM for Endpoint FIFO

SD I/F

◇ Supports SDXC, SDHC, and SD cards
◇ Provide access to SD card in SD Bus mode
◇ Allows control from the AMBA-AHB bus
◇ Includes 512 byte data transmit/receive FIFOs

Quad SPI I/F

◇ Supports quad serial flash ROM
◇ Supports serial flash ROM address up to 24 bits
◇ Allows the setting of control registers from the AMBA-AHB bus
◇ Allows direct access from the memory map of the AMBA-AHB bus to serial flash ROM
◇ Includes 32 byte data transmit/receive FIFOs

SSI Master

◇ FIFO Depth Up to 16 Words and FIFO Data Width Up to 16 Bits
◇ Selectable Data Size from 4 Bits to 16 Bits
◇ Serial protocol supports SPI from Motorola
◇ Includes DMA handshake interface

SSI Slave

◇ FIFO Depth Up to 16 Words and FIFO Data Width Up to 16 Bits
◇ Selectable Data Size from 4 Bits to 16 Bits
◇ Serial protocol supports SPI from Motorola
◇ Includes DMA handshake interface

I2C I/F (Master/Slave)

◇ 2 Ch I2C Serial Interface
◇ Supports two speed modes
  - Standard Mode (100 Kb/s)
  - Fast Mode (400 Kb/s)
◇ Supports I2C Master and Slave operation
◇ Allows 7 and 10 bit address generation
◇ Has built-in 32 stage transmit and receive FIFOs
◇ Includes DMA handshake interface

UART I/F
- ◇ IS16550-Based
- ◇ Allows various baud rate settings with software (up to 6 Mbps)
- ◇ No Support for IrDA
- ◇ FIFO DepthUp to 32 Words and FIFO Data Width Up to 8 Bits
- ◇ Incorporates a function to invert output
- ◇ Includes DMA handshake interface

I2S Input I/F
- ◇ Two Lines of 2-Ch Digital Audio Input
- ◇ I2S, EIAJ Format
- ◇ 16-Bit Data
- ◇ Selectable Bit Clock from 32 fs, 48 fs, and 64 fs
- ◇ Selectable Input Sample Rate from 32 kHz, 44.1 kHz, and 48 kHz
- ◇ One Line of Internal Input from the CD Servo Controller
- ◇ Maximum Input Rate Up to 4×
- ◇ Supports detection of CD-DA link
- ◇ Supports detection of CD-ROM sync
- ◇ Supports CD-ROM data descrambling
- ◇ Acquires Sub-Q data
- ◇ Acquires CD-Text data
- ◇ Built-in DMA

I2S Output I/F
- ◇ 2.1-Ch Digital Audio Output x 1
- ◇ 2 Channels from Decoder, 1 Channel from ADC
- ◇ I2S, EIAJ Format
- ◇ Selectable Output Sample Rate from 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz,176.4 kHz, and 192 kHz
- ◇ Selectable Data Width from 16, 24, and 32 bits
- ◇ 64 fs Bit Clock
- ◇ Supports pitch control (×0.5 to ×2.0 in 25 steps)

CD Servo Controller
- ◇ Supports rotation speed of CD up to 4×
- ◇ Built-in Preservo-Amplifier with Power Save Mode, Which Supports Playback of CD-RW
- ◇ Allows independent offset adjustment of AC, BD, E, and F amplifiers
- ◇ Built-in Auto-Tracking and Focus Adjustment Function
- ◇ Built in PLL and CLV with a Wide Lock Range
- ◇ Built-in Asymmetry Correction Function

CD-ROM Decoder
- ◇ Supports Mode1, Mode2 form1, and Mode2 form2
- ◇ Supports ECC and EDC
- ◇ Built-in DMA

General Purpose A/D Converter
- ◇ 10-Bit SAR ADC, 8 Ch ADC
- ◇ Maximum Frequency for A/D Conversion Up to 736 kHz (for 1 Ch Converter)

Timer
- ◇ Supports five independent programmable timer functions
- ◇ Each timer supports time width up to 32 bits
- ◇ Each timer supports independent interrupt signal

Watchdog Timer
- ◇ Composed of a counter having a set cycle to monitor the occurrence of timeout event
- ◇ Counter Width Up to 32 Bits
- ◇ The counter counts down from the set value and sets timeout occurrence when it reaches zero

Real Time Clock
- ◇ 32 Bit Programmable Timer
- ◇ Supports interrupt signals
- ◇ External 32.768 kHz Crystal Oscillator
  (External 32.768 kHz X'tal)

Remote Controller Receiver (RCR)
◇ Converts infrared remote control signal to code
◇ Compatible with the signal format of the Association for Electric Home Appliances

Clock Generator
◇ Supplies clocks to individual internal blocks
◇ Allows on/off control of clocks to individual blocks
◇ Generates master audio clocks
◇ Supports Power-Down Mode

Reset Generator
◇ Generates a pulse to be supplied to individual blocks

PLL
◇ Generates 192 MHz clock used to generate system clocks
◇ Generates 135.4752 MHz and 147.456 MHz clocks used to generate audio clocks

Power Supply Voltage
◇ I/O Power Supply Voltage: 3.3V (3.0 to 3.5V)
◇ Analog Power Supply Voltage: 3.3V (3.0 to 3.5V)
(used for SDRAM, CD servo, and USB)
◇ Digital Core Power Supply Voltage: 1.55V (1.5 to 1.6V)
(used for digital core and ADC)

Pin Description

Pin Assignment

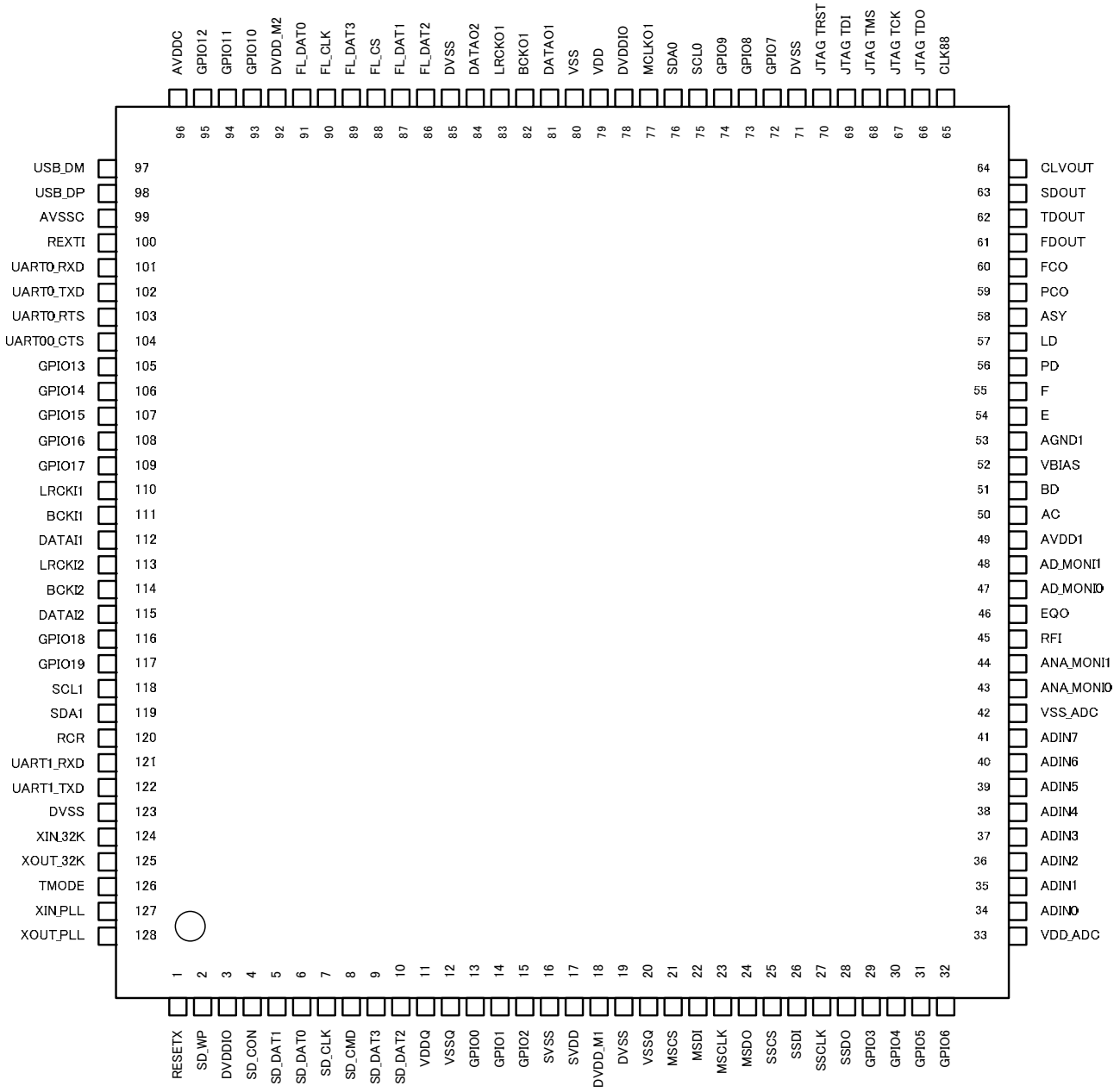


Figure 2. Pin Assignment Diagram

Pin Description

No.	Block	Pin Name	I/O	Function
1	RESET	RESETX	I	H: Release RESET, L: RESET
2	SDIO	SD_WP	I	SD Card I/F WP Detect
3	POWER	DVDDIO	-	VDD (3V)
4	SDIO	SD_CON	I	SD Card I/F Connection Detect
5	SDIO	SD_DAT1	I/O	SD Card I/F Data I/O (1)
6	SDIO	SD_DAT0	I/O	SD Card I/F Data I/O (0)
7	SDIO	SD_CLK	O	SD Card I/F Clock Output
8	SDIO	SD_CMD	O	SD Card I/F Command Output
9	SDIO	SD_DAT3	I/O	SD Card I/F Data I/O (3)
10	SDIO	SD_DAT2	I/O	SD Card I/F Data I/O (2)
11	POWER	VDDQ	-	SDRAM Power Supply (VDD1)
12	POWER	VSSQ	-	SDRAM Ground
13	GPIO	GPIO0	I/O	GPIO I/O (0)
14	GPIO	GPIO1	I/O	GPIO I/O (1)
15	GPIO	GPIO2	I/O	GPIO I/O (2)
16	POWER	SVSS	-	SDRAM Ground
17	POWER	SVDD	-	SDRAM Power Supply (VDD1)
18	POWER	DVDD	-	VDD (1.5V)
19	POWER	DVSS	-	Ground
20	POWER	VSSQ	-	SDRAM Ground
21	Master SIO	MSCS	O	SIO Master Chip Select Output
22	Master SIO	MSDI	I	SIO Master Data Input
23	Master SIO	MSCLK	O	SIO Master Clock Output
24	Master SIO	MSDO	O	SIO Master Data Output
25	Slave SIO	SSCS	I	SIO Slave Chip Select Input
26	Slave SIO	SSDI	I	SIO Slave Data Input
27	Slave SIO	SSCLK	I	SIO Slave Clock Input
28	Slave SIO	SSDO	O	SIO Slave Data Output
29	GPIO	GPIO3	I/O	GPIO I/O (3)
30	GPIO	GPIO4	I/O	GPIO I/O (4)
31	GPIO	GPIO5	I/O	GPIO I/O (5)
32	GPIO	GPIO6	I/O	GPIO I/O (6)
33	POWER	VDD_ADC	-	ADC Power Supply (1.5V)
34	ADC	ADIN0	I	ADC Analog Input (0)
35	ADC	ADIN1	I	ADC Analog Input (1)
36	ADC	ADIN2	I	ADC Analog Input (2)
37	ADC	ADIN3	I	ADC Analog Input (3)
38	ADC	ADIN4	I	ADC Analog Input (4)
39	ADC	ADIN5	I	ADC Analog Input (5)
40	ADC	ADIN6	I	ADC Analog Input (6)
41	ADC	ADIN7	I	ADC Analog Input (7)
42	POWER	VSS_ADC	-	ADC Ground
43	CDDSP	ANA_MONI0	O	Input & Analog Monitor Output
44	CDDSP	ANA_MONI1	O	Input & Analog Monitor Output
45	CDDSP	RFI	I	RF Output Capacitance Coupling Re-Input
46	CDDSP	EQO	O	Output after RF Equalizer
47	CDDSP	AD_MONI0	O	Input & Monitor Signal Output
48	CDDSP	AD_MONI1	O	Input & Monitor Signal Output
49	POWER	AVDD1	-	RF Analog Power Supply
50	CDDSP	AC	I	A + C Voltage Input
51	CDDSP	BD	I	B + D Voltage Input
52	CDDSP	VBIAS	O	Bias Level
53	POWER	AGND1	-	RF Analog Ground
54	CDDSP	E	I	E Voltage Input
55	CDDSP	F	I	F Voltage Input
56	CDDSP	PD	I	APC Photo Detector Input
57	CDDSP	LD	O	APC Laser Drive Output
58	CDDSP	ASY	I	Asymmetric Correction
59	CDDSP	PCO	O	PLL PCO Output
60	CDDSP	FCO	O	PLL FCO-DAC Output
61	CDDSP	FDOUT	O	Focus Drive Output
62	CDDSP	TDOUT	O	Tracking Drive Output
63	CDDSP	SDOUT	O	Sled Drive Output
64	CDDSP	CLVOUT	O	CLV Drive Output
65	CDDSP	CLK88	O	Clock Output for Driver IC

Pin Description - continued

No	Block	Pin Name	I/O	Function
66	JTAG	JTAG TDO	O	JTAG TDO
67	JTAG	JTAG TCK	I	JTAG TCK
68	JTAG	JTAG TMS	I	JTAG TMS
69	JTAG	JTAG TDI	I	JTAG TDI
70	JTAG	JTAG TRST	I	JTAG TRST
71	POWER	DVSS	-	Ground
72	GPIO	GPIO7	I/O	GPIO I/O (7)
73	GPIO	GPIO8	I/O	GPIO I/O (8)
74	GPIO	GPIO9	I/O	GPIO I/O (9)
75	I2C	SCL0	I/O	I^2C clock I/O (0)
76	I2C	SDA0	I/O	I^2C data I/O (0)
77	I2S OUT	MCLKO1	O	Digital Audio Master Clock Output (1)
78	POWER	DVDDIO	-	VDD (3V)
79	POWER	SVDD	-	SDRAM Power Supply (VDD1)
80	POWER	SVSS	-	SDRAM Ground
81	I2S OUT	DATAO1	O	Digital Audio Data Output (1)
82	I2S OUT	BCKO1	O	Digital Audio Bit Clock Output (1)
83	I2S OUT	LRCKO1	O	Digital Audio Channel Clock Output (1)
84	I2S OUT	DATAO2	O	Digital Audio Data Output (2)
85	POWER	DVSS	-	Ground
86	FLASH	FL_DAT2	I/O	Serial Flash ROM I/F Data I/O (2)
87	FLASH	FL_DAT1	I/O	Serial Flash ROM I/F Data I/O (1)
88	FLASH	FL_CS	O	Serial Flash ROM I/F Command Output
89	FLASH	FL_DAT3	I/O	Serial Flash ROM I/F Data I/O (3)
90	FLASH	FL_CLK	O	Serial fFash ROM I/F Clock Output
91	FLASH	FL_DAT0	I/O	Serial Flash ROM I/F Data I/O (0)
92	POWER	DVDD	-	VDD (1.5V)
93	GPIO	GPIO10	I/O	GPIO I/O (10)
94	GPIO	GPIO11	I/O	GPIO I/O (11)
95	GPIO	GPIO12	I/O	GPIO I/O (12)
96	POWER	AVDDC	-	USB Power Supply (VDD1)
97	USB	USB_DM1	I/O	USB D- I/O
98	USB	USB_DP1	I/O	USB D+ I/O
99	POWER	AVSSC	-	USB Ground
100	USB	REXTI	I	Pin is connected to USB reference voltage and AVSSC pin via a 12.3-kΩ USB bias resistor. Connect a resistor of 12.3-kΩ±1% to GND. Only using USB Full Speed, the resistor of 12.3-kΩ±5% is approvable on the USB media playability check.
101	UART	UART0_RXD	I	UART0 Receive Data
102	UART	UART0_TXD	O	UART0 Transmit Data
103	UART	UART0_RTS	O	UART0 Transfer Request
104	UART	UART0_CTS	I	UART0 Clear Request
105	GPIO	GPIO13	I/O	GPIO I/O (13)
106	GPIO	GPIO14	I/O	GPIO I/O (14)
107	GPIO	GPIO15	I/O	GPIO I/O (15)
108	GPIO	GPIO16	I/O	GPIO I/O (16)
109	GPIO	GPIO17	I/O	GPIO I/O (17)
110	I2S IN	LRCKI1	I	Digital Audio Channel Clock Input (1)
111	I2S IN	BCKI1	I	Digital Audio Bit Clock Input (1)
112	I2S IN	DATAI1	I	Digital Adio Data Input (1)
113	I2S IN	LRCKI2	I	Digital Audio Channel Clock Input (2)
114	I2S IN	BCKI2	I	Digital Audio Bit Clock Input (2)
115	I2S IN	DATAI2	I	Digital Audio Data Input (2)
116	GPIO	GPIO18	I/O	GPIO I/O (18)
117	GPIO	GPIO19	I/O	GPIO I/O (19)
118	I2C	SCL1	I/O	I^2C Clock I/O (1)
119	I2C	SDA1	I/O	I^2C Data I/O (1)
120	RCR	RCR	I	Remote Controller Signal Input
121	UART	UART1_RXD	I	UART1 Receive Data
122	UART	UART1_TXD	O	UART1 Transmit Data
123	POWER	DVSS	-	Ground
124	CLOCK	XIN_32K	I	X'tal (32.768 KHz) Connection Input
125	CLOCK	XOUT_32K	O	X'tal (32.768KHz) Connection Output
126	TEST	TMODE	I	Test Mode Terminal: This pin is connected to GND.
127	CLOCK	XIN_PLL	I	X'tal (16.9344MHz) Connection Input
128	CLOCK	XOUT_PLL	O	X'tal (16.9344MHz) Connection Output

Electrical Characteristics

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Remark
Input Voltage (Analog, I/O)	V_{DD1MAX}	−0.3 to +4.5	V	DVDDIO, VDDQ, SVDD, AVDD1, AVDDC
Input Voltage (Core)	V_{DD2MAX}	−0.3 to +2.1	V	DVDD, VDD_ADC
Input Voltage	V_{IN}	−0.3 to V_{DD1}+0.3	V	
Storage Temperature Range	Tstg	−55 to +125	°C	
Operating Temperature Range	Topr	−40 to +75	°C	Using USB High Speed
Operating Temperature Range	Topr	−40 to +85	°C	Using USB Full Speed
Power Dissipation (Note 1)	Pd1	1.96	W	

(Note 1) Derating is done in 19.6 mW/°C for operation above Ta≧25 °C Mount on 2-layer 114.3mm x 76.2mm x 1.6mmt board (bottom side copper layer 74.2mm x 74.2mm)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Rating	Unit	Remark
Input Voltage (Analog, I/O)	V_{DD1}	3.0 to 3.5	V	DVDDIO, VDDQ, SVDD, AVDD1, AVDDC
Input Voltage (Core)	V_{DD2}	1.55 to 1.65	V	DVDD, VDD_ADC (Using USB High Speed)
Input Voltage (Core)	V_{DD2}	1.5 to 1.65	V	DVDD, VDD_ADC (Using USB Full Speed)

Electrical Characteristics

(Unless otherwise noted, Ta=25°C, V_{DD1}=3.3V, V_{DD2}=1.55V, V_{SSQ}=SV_{SS}=DV_{SS}=V_{SS_ADC}=AGND1=AV_{SSC}=0V, XIN_PLL=16.9344 MHz, XIN_32K=32.768 kHz, REXTI PIN's Eeternal Resistance=12.3kΩ±1% (Note 8))

Parameter	Symbol	Rating			Unit	Conditions / Suitable Pin
		Min	Typ	Max		
<Overall>						
Operating Current Consumption (VDD1)	I_{DDHS1}	−	110	180	mA	Using USB High Speed
Operating Current Consumption (VDD1)	I_{DDFS1}	−	60	130	mA	Using USB Full Speed
Operating Current Consumption (VDD2)	I_{DD2}	−	100	200	mA	
<Logic Interface>						
Input "H" Voltage	V_{IH}	V_{DD1} * 0.7	−	V_{DD1}	V	(Note 1)
Input "L" Voltage	V_{IL}	DV_{SS}	−	V_{DD1}*0.3	V	(Note 1)
Output "H" Voltage 1	V_{OH1}	V_{DD1} - 0.4	−	V_{DD1}	V	I_{OH} = −1.6mA (Note 2)
Output "L" Voltage 1	V_{OL1}	0	−	0.4	V	I_{OL} = 1.6mA (Note 2)
Output "L" Voltage 2	V_{OL2}	0	−	0.4	V	I_{OL} = 3.6mA (Note 3)
Output "H" Voltage 3	V_{OH3}	V_{DD1} - 0.4	−	V_{DD1}	V	I_{OH} = −0.6mA (Note 4)
Output "L" Voltage 3	V_{OL3}	0	−	0.4	V	I_{OL} = 0.6mA (Note 4)
Output "H" Voltage 4	V_{OH4}	V_{DD1} - 1.0	−	V_{DD1}	V	I_{OH} = −0.6mA (Note 5)
Output "L" Voltage 4	V_{OL4}	0	−	1.0	V	I_{OL} = 0.6mA (Note 5)
<USB Interface>						
Idle Pull-Up Resistance	R_{PU_ID}	0.9	-	1.575	kΩ	(Note 7)
RX Pull-Up Resistance	R_{PU_RX}	1.425	-	3.09	kΩ	(Note 7)
Pull-Down Resistance	R_{PD}	14.25	-	24.8	kΩ	(Note 6)
HS Idle Voltage	V_{HSOI}	-10	5	25	mV	(Note 6)
HS High Voltage	V_{HSOH}	360	-	440	mV	(Note 6)
HS Low Voltage	V_{HSOL}	-10	5	25	mV	(Note 6)
HS RX Differential Input Sensitivity	V_{HSSQ}	100	-	-	mV	(Note 6)
HS RX Differential Input Range	V_{HSCM}	-50	-	600	mV	(Note 6)
HS Disconnect Judgment Voltage	V_{HSDSC}	525	-	625	mV	(Note 6)
Chirp J Voltage	V_{CHIRPJ}	700	-	1100	mV	Measured at 45Ω Output Termination (Note 6)
Chirp K Voltage	V_{CHIRPK}	-900	-	-500	mV	(Note 6)
FS High Output Impedance	Z_{FDRH}	-	45	-	Ω	(Note 6)
FS Low Output Impedance	Z_{FDRL}	-	45	-	Ω	(Note 6)

Electrical Characteristics – continued

Parameter	Symbol	Rating			Unit	Conditions Suitable Pin
		Min.	Typ.	Max.		
FS High Voltage	V_{FOH}	2.8	-	3.6	V	Measured when pin is pulled down to AV_{SSC} using 15 kΩ resistor (Note 6)
FS Low Voltage	V_{FOL}	0	-	0.3	V	Measured when pin is pulled up to AV_{DDC} using 1.5 kΩ resistor (Note 6)
FS RX Differential Input Range	V_{FLCM}	0.8	-	2.5	V	(Note 6)
FS RX Differential Input Sensitivity	V_{FLSNS}	-	-	200	mV	(Note 6)
Input “H” Voltage	V_{HUSB}	2	-	AV_{DDC}	V	(Note 6)
Input “L” Voltage	V_{ILUSB}	AV_{SSC}	-	0.8	V	(Note 6)
<ADC>						
A/D Conversion Frequency	f_{ADCONV}	-	-	736	kHz	$F_{ADCONV} \leq$ 16.9344MHz/23
Analog Input Voltage Range	V_{AIN}	±0.55	±0.62	±0.69	V	V_{DD_ADC} = Within 1.55V ±1%
Analog Input Voltage Range	V_{AIN}	±0.57	±0.64	±0.71	V	V_{DD_ADC} = Within 1.6V ± 1%
Differential Non-Linearity	DNL	-	-	±5	LSB	
Integral Non-Linearity	INL	-	-	±5	LSB	

(Note 1) 1,2,4 to10,13 to15,21to 32,67 to 70,72 to 77,81 to 84,86 to 91,93 to 95,101 to122,124,127 pins
(Note 2) 13 to15,21 to 32,65 to 66,72 to 74,77,81 to 84,86 to 91,93 to 95,101 to 117,120 to122 pins
(Note 3) 75,76,118,119 pins
(Note 4) 4-10, pin
(Note 5) 125,128 pins
(Note 6) 97,98 pins
(Note 7) 98 pin
(Note 8) Only using USB Full Speed, the resistor of 12.3-kΩ±5% is approvable on the USB media playability check.

Electrical Characteristics – continued

(Unless otherwise noted, Ta=25°C, V_{DD1}=3.3V, V_{DD2}=1.55V, V_{SSQ}=SV_{SS}=DV_{SS}=V_{SS_ADC}=AGND1=AV_{SSC}=0V, XIN_PLL=16.9344 MHz, XIN_32K=32.768 kHz, R_L=10kΩ, VC=Reference)

Parameter	Symbol	Rating			Unit	Conditions Suitable Pin
		Min	Typ	Max		
<PLL (VCO) Block>						
Maximum Oscillation Frequency	f_{VCOH}	4.6	6.5	-	MHz	1/4 of FLAG1 and VCO Output
Minimum Oscillation Frequency	f_{VCOL}	-	1.1	1.7	MHz	1/4 of FLAG1 and VCO Output
<FC DAC>						
Offset Voltage	V_{FCOF}	-50	-	+50	mV	FCO
Maximum Output Voltage	V_{FCH}	0.2	0.5	-	V	FCO
Minimum Output Voltage	V_{FCL}	-	−0.5	−0.2	V	FCO
<PCO>						
Output “L” Voltage	V_{PCH}	-	−1.0	−0.6	V	PCO
Output “H” Voltage	V_{PCL}	0.6	1.0	-	V	PCO
<EFM Comparator>						
Threshold Voltage	V_{EFM}	−200	-	+200	mV	RFI, ANA_MONI0, FLAG2
<Servo ADC>						
Offset Voltage	V_{ADOF}	−140	-	+140	mV	ANA_MONI0, ANA_MONI1
Maximum Conversion Voltage	V_{ADH}	1.0	1.2	+1.4	V	ANA_MONI0, ANA_MONI1
Minimum Conversion Voltage	V_{ADL}	−1.4	−1.2	−1.0	V	ANA_MONI0, ANA_MONI1
<Servo DAC>						
Offset Voltage	V_{DAOF}	-80	-	+80	mV	FDOUT, TDOUT, SDOUT, CLVOUT
Maximum Output Voltage	V_{DAH}	0.8	1.2	-	V	FDOUT, TDOUT, SDOUT, CLVOUT
Minimum Output Voltage	V_{DAL}	-	-1.2	-0.8	V	FDOUT, TDOUT, SDOUT, CLVOUT
<Bias Amplifier>						
Maximum Output Current	I_{BO}	-	±1.5	-	mA	VBIAS, BIAS Fluctuation: 200mV or less
<RF Amplifier>						
Offset Voltage	V_{RFOF}	-	0	-	mV	AC ,BD, EQO
Maximum Output Voltage	V_{RFH}	1.0	1.2	-	V	AC, BD, EQO
Minimum Output Voltage	V_{RFL}	-	−1.3	−1.1	V	AC, BD, EQO
<FE Amplifier>						
Offset Voltage	V_{FEOF}	-	0	-	mV	AC, BD, ANA_MONI0, ANA_MONI1
Maximum Output Voltage	V_{FEH}	1.0	1.4	-	V	AC, BD, ANA_MONI0 ,ANA_MONI1
Minimum Output Voltage	V_{FEL}	-	−1.4	−1.0	V	AC, BD, ANA_MONI0, ANA_MONI1
<TE Amplifier>						
Offset Voltage	V_{TEOF}	-	70	-	mV	E, F, ANA_MONI0, ANA_MONI1
Maximum Output Voltage	V_{TEH}	1.0	1.4	-	V	E, F, ANA_MONI0, ANA_MONI1
Minimum Output Voltage	V_{TEL}	-	−1.4	−1.0	V	E, F, ANA_MONI0, ANA_MONI1
<Asymmetry Amplifier>						
Offset Voltage	V_{ASYOF}	-	0	-	mV	ASY = VC, RFI, ANA_MONI0 (ASY_TEST)
Maximum Output Voltage	V_{ASYH}	1.1	1.4	-	V	ASY, RFI, ANA_MONI0 (ASY_TEST)
Minimum Output Voltage	V_{ASYL}	-	−1.4	−1.1	V	ASY, RFI, ANA_MONI0 (ASY_TEST)
<APC Block>						
Output Voltage 1	V_{APC1}	2.4	2.8	-	V	PD=”H”, LD, ANA_MONI0 (APCREF)
Output Voltage 2	V_{APC2}	-	0.1	0.5	V	PD=”L”, LD, ANA_MONI0 (APCREF)
Maximum Reference Voltage	V_{APCH}	-	220	-	mV	PD, LD, ANA_MONI0 (APCREF)
Minimum Reference Voltage	V_{APCL}	-	145	-	mV	PD, LD, ANA_MONI0 (APCREF)

Application Information

Clock and Reset

Clock

Clock Name	I/O	Function	Remarks
XIN_32K	I	X'tal (32.768KHz) Connection Input Terminal	
XOUT_32K	O	X'tal (32.768 KHz) Connection Terminal	
XIN_PLL	I	X'tal (16.9344 MHz) Connection Input Terminal	
XOUT_PLL	O	X'tal (16.9344 MHz) Connection Terminal	

Reset

Signal Name	I/O	Function	Remarks
RESETX	I	System Reset Input Terminal	

Release reset signal (RESETX = H) 300 us after oscillation of 32.768KHz and 16.9344MHz clock inputs have become stable. (See Figure 3)

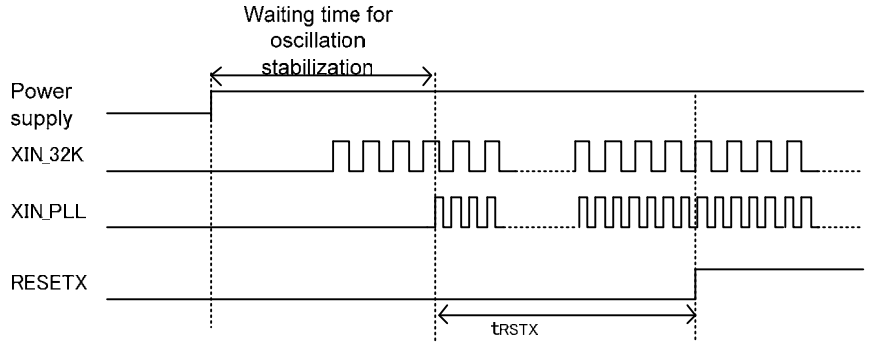


Figure 3.Reset Timing

Item	Symbol	Rating			Unit	Remarks
		Min	Typ	Max		
Reset L Interval	t_{RSTX}	300	-	-	μs	

1. AMBA

1.1. Features

- Consists of multilayer AHB bus matrix
- Includes three AHB buses, which use ARM9, DMAC, and the DMAC of individual peripherals as bus masters
- Includes APB-to-AHB bridge with the bus master arbitration function
- 32-Bit Data Bus
- Arbitrates bus masters with individual peripherals
- Allows parallel access according to different master/slave combinations

1.2. Description

1.2.1. Block Diagram

The following section shows the block diagram of a system bus.

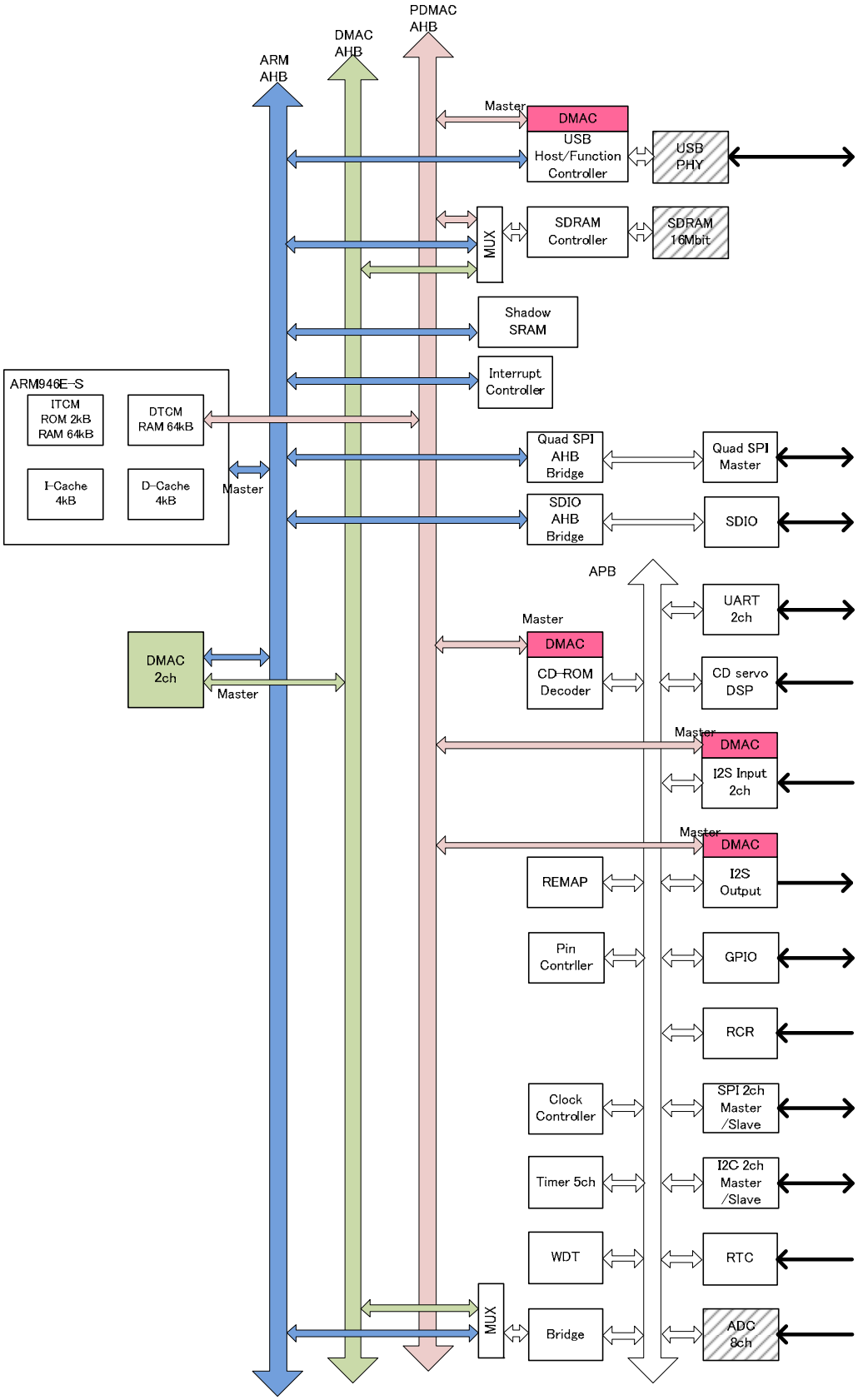


Figure 4.

1.2.2. Memory Map

The following section shows the hardware memory map.

START-ADR	END-ADR	Master			Name	Size (Bytes)
		ARM	DMAC (Note)	PDMAC		
$00000000	$000007FF	○	×	×	Instruction_ROM	2k
$00008000	$00017FFF	○	×	×	Instruction_RAM	64k
$10000000	$1000FFFF	○	×	○	WORK_RAM	64k
AHB						
$20000000	$20FFFFFF	○	×	×	Serial Flash ROM Direct	16M
$70000000	$700001FF	○	×	×	SHADOW RAM	512
$80000000	$801FFFFF	○	○	○	SDRAM Direct	2M
APB						
$D0000000	$D00FFFFF	○	×	×	WDT	
$D0100000	$D01FFFFF	○	×	×	Timer	
$D0200000	$D02FFFFF	○	×	×	Clock/Power Controller	
$D0300000	$D03FFFFF	○	×	×	PIN Controller	
$D0400000	$D04FFFFF	○	×	×	RTC	
$D0500000	$D05FFFFF	○	○	×	UART0	
$D0600000	$D06FFFFF	○	○	×	UART1	
$D0700000	$D07FFFFF	○	○	×	SSI Master	
$D0800000	$D08FFFFF	○	○	×	SSI Slave	
$D0900000	$D09FFFFF	○	○	×	I2C0	
$D0A00000	$D0A0FFFF	○	○	×	I2C1	
$D0B00000	$D0BFFFFF	○	×	×	I2S OUT	
$D0C00000	$D0CFFFFF	○	×	×	CD-DSP	
$D0D00000	$D0DFFFFF	○	×	×	ADC	
$D0E00000	$D0EFFFFF	○	×	×	REMAP	
$D0F00000	$D0FFFFFF	○	×	×	RCR	
$D1000000	$D10FFFFF	○	×	×	GPIO0	
$D1100000	$D11FFFFF	○	×	×	GPIO1	
$D1200000	$D12FFFFF	○	×	×	RESETGEN	
$D1300000	$D13FFFFF	○	×	×	I2SIN/CD-ROM	
AHB						
$E0000000	$E00FFFFF	○	×	×	DMAC	
$E0200000	$E02FFFFF	○	×	×	(Reserved)	
$F0000000	$F00FFFFF	○	×	×	SDRAM Controller Setting	
$F0100000	$F01FFFFF	○	×	×	Quad SPI Controller Setting	
$F0200000	$F02FFFFF	○	×	×	SDIO Controller	
$F8000000	$F80FFFFF	○	×	×	Mentor USB Controller	
$F8100000	$F81FEFFF	○	×	×	USB Connect Detector	
$FFF00000	$FFFFFFFF	○	×	×	Interrupt Controller (ICTL)	

(Note) DMAC Access Size is 32 bits.

1.2.3. ARM AHB

ARM AHB is a single-master AHB, which uses ARM9 as bus master.

1.2.4. DMAC AHB

DMAC AHB is a single-master AHB, which uses DMAC as bus master.

1.2.5. PDMAC AHB

PDMAC AHB is a multi-master AHB, which uses PDMAC and the DMAC of individual peripherals as bus masters.
To access individual bus masters, the arbiter selects the bus master of PDMAC AHB to allow access to the SDRAM or ARM9 DTCM space.

The following table lists priority levels for the arbiter.

Priority Level	Block
1 (High)	I2S Output
2	USB
3	SDIO
4	I2S Input
5	CD-ROM
6 (Low)	(Reserved)

1.2.6. APB

An AHB-to-APB bridge circuit converts from AHB to APB format.
APB allows access from ARM9 and DMAC to APB peripherals.

MUX

If individual AHBs have simultaneous access to the same peripheral, MUX selects a single AHB with a higher priority level and connects the AHB bus to a peripheral bus.
All AHBs, except the selected AHB, enter wait state.

The following table lists the levels of priority for AHB selection.

Priority Level	AHB
1 (High)	PDMAC AHB
2	DMAC AHB
3 (Low)	ARM9 AHB

1.3. I/O Signals

Pin Name	I/O	Function	Destination
clk_i	In	System Clock	CLKCTR
ramclk_i	In	RAM Clock	CLKCTR
nreset_i	In	System Reset	RSTGEN
hbusreq_marm_i	In	AHB HBUSREQ Master	ARM9
htrans_marm_i	In	AHB HTRANS Master	ARM9
hsize_marm_i	In	AHB HSIZE Master	ARM9
hburst_marm_i	In	AHB HBURST Master	ARM9
hwdata_marm_i	In	AHB HWRITE Master	ARM9
haddr_marm_i	In	AHB HADDR Master	ARM9
hwrite_marm_i	In	AHB HWDATA Master	ARM9
hgrant_marm_o	Out	AHB GRANT Master	ARM9
hready_marm_o	Out	AHB HREADY Master	ARM9
hrdata_marm_o	Out	AHB HRDATA Master	ARM9
hresp_marm_o	Out	AHB HRESPM Master	ARM9
hbusreq_mdmac_i	In	DMAC AHB HBUSREQ Master	DMAC
htrans_mdmac_i	In	DMAC AHB HTRANS Master	DMAC
hsize_mdmac_i	In	DMAC AHB HSIZE Master	DMAC
hburst_mdmac_i	In	DMAC AHB HBURST Master	DMAC
hwdata_mdmac_i	In	DMAC AHB HWRITE Master	DMAC
haddr_mdmac_i	In	DMAC AHB HADDR Master	DMAC
hwrite_mdmac_i	In	DMAC AHB HWDATA Master	DMAC
hgrant_mdmac_o	Out	DMAC AHB GRANT Master	DMAC
hready_mdmac_o	Out	DMAC AHB HREADY Master	DMAC
hrdata_mdmac_o	Out	DMAC AHB HRDATA Master	DMAC
hresp_mdmac_o	Out	DMAC AHB HRESPM Master	DMAC
hbusreq_mX_i	In	Peri DMAC AHB HBUSREQ Master	PDMAC
htrans_ mX _i	In	Peri DMAC AHB HTRANS Master	PDMAC
hsize_ mX _i	In	Peri DMAC AHB HSIZE Master	PDMAC
hburst_ mX _i	In	Peri DMAC AHB HBURST Master	PDMAC
hwdata_ mX _i	In	Peri DMAC AHB HWRITE Master	PDMAC
haddr_ mX _i	In	Peri DMAC AHB HADDR Master	PDMAC
hwrite_ mX _i	In	Peri DMAC AHB HWDATA Master	PDMAC
hgrant_ mX _o	Out	Peri DMAC AHB GRANT Master	PDMAC
hready_ mX _o	Out	Peri DMAC AHB HREADY Master	PDMAC
hrdata_ mX _o	Out	Peri DMAC AHB HRDATA Master	PDMAC
hresp_ mX _o	Out	Peri DMAC AHB HRESPM Master	PDMAC
hsel_marm_ setc_o	Out	AHB HSEL Slave	AHB
htrans_setc_o	Out	AHB HTRANS Slave	AHB
hwrite_setc_o	Out	AHB HWRITE DATA Slave	AHB
hsize_setc_o	Out	AHB HSIZE Slave	AHB
haddr_setc_o	Out	AHB HADDR Slave	AHB
hwdata_setc_o	Out	AHB HWDATA Slave	AHB
hready_marm_o	Out	AHB HREADYI Slave	AHB
hready_XXX_i	In	AHB HREADY Out Slave	AHB
hrdata_XXX_i	In	AHB HRDATA Slave	AHB

I/O Signals – continued

Pin Name	I/O	Function	Destination
hresp_XXX_i	In	AHB RESPONSE Slave	AHB
hsel_pdmac_dtcm_o	Out	AHB HSEL Slave	DTCM
htrans_pdmac_o	Out	AHB HTRANS Slave	DTCM
hwrite_pdmac_o	Out	AHB HWRITE DATA Slave	DTCM
hsize_pdmac_o	Out	AHB HSIZE Slave	DTCM
haddr_pdmac_o	Out	AHB HADDR Slave	DTCM
hwdata_pdmac_o	Out	AHB HWDATA Slave	DTCM
hburst_pdmac_o	Out	AHB HREADYI Slave	DTCM
hready_sdtcm_i	In	AHB HREADY Out Slave	DTCM
hrdata_sdtcm_i	In	AHB HRDATA Slave	DTCM
hresp_sdtcm_i	In	AHB RESPONCE Slave	DTCM
psel_x	Out	APB Sel	APB
paddr_sapb_o	Out	APB Addr	APB
penable_sapb_o	Out	APB Enable	APB
pwrite_sapb_o	Out	APB Write Enable	APB
pwdata_sapb_o	Out	APB Write Data	APB
prdata_d0X_i	In	APB Read Data	APB

2. REMAP

2.1. Features

- Controls remapping (from boot memory mapping to normal memory mapping) after completion of initialization sequence
- Generates remap control signals by writing data to internal register
- Connects remap control signals to AHB address decoder
- Supports APB slave interface
- Little-Endian System

2.2. Description

2.2.1. Outline Block Diagram

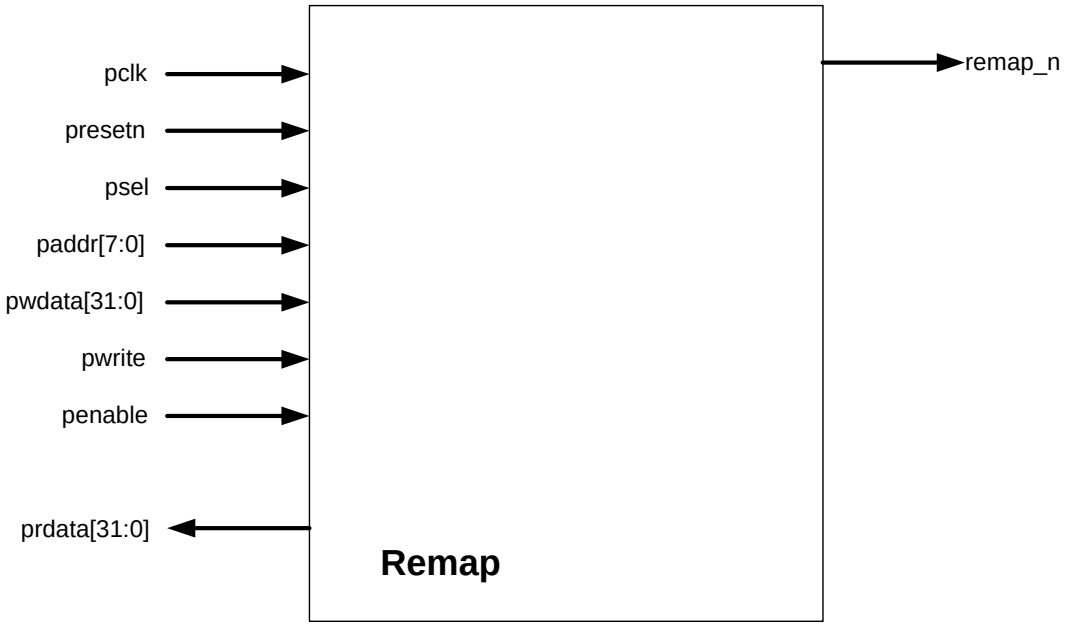


Figure 5. Remap Block

2.2.2. Description

For power-on reset, address 0x0000 is assigned to a program ROM for initialization. This is called boot memory mapping. Setting the remap control register outputs a remap signal to the AHB address recorder after completion of initialization and, subsequently, reassigns the address 0x0000 to a shadow RAM. This is called normal memory mapping.

2.3. I/O Signals

Pin Name	I/O	Function	Destination
pclk	IN	APB Clock	Clock Gen
present	IN	APB Reset	Reset Gen
psel	IN	APB Peripheral Select Signal	APB
paddr [7:0]	IN	APB Address	APB
pwdata [31:0]	IN	APB Write Data	APB
pwrite	IN	APB Write Signal	APB
penable	IN	APB Enable Signal	APB
prdata [31:0]	OUT	APB Read Data	APB
remap_n	OUT	Remap Signal	AHB

2.4. Register

2.4.1. Memory Map

Name	Address Offset	Width	Reset
RemapMode	0x00	1 bit	0x0

2.4.2. Register Detail

RemapMode

Remap Setting Register

Bits	Name	Direction	Reset	Description
0	RemapMode Mode	R/W	0x0	Setting this register to “1” makes remapping execution possible. 0: Boot memory mapping 1: Normal memory mapping

3. SDRAM Controller

3.1. Feature

- ✧ SDRAM is supported.
- ✧ Supports 11 bit row address, 8 bit column address, and 1 bit bank address to SDRAM
- ✧ SDRAM Timing is programmable.
- ✧ The SDRAM Auto-Refresh function and Refresh timing can be arbitrarily set.
- ✧ Supports Power-Down Mode of SDRAM

3.2. Description

3.2.1. FIFO

The memory controller has four "FIFO addresses" and eight "FIFO data" on the AHB interface side. AHB address for MIU (Memory Interface Unit) is stored in FIFO address for decoding.

Data written in memory and control information generated during burst transfer are stored in FIFO data. The depth of FIFO is determined depending on the delay value of SDRAM, which contains the refresh, pre-charge, read latency and write latency etc.

3.2.2. READ_PIPE/WRITE_PIPE

READ_PIPE consists of flip-flops for memory controller, which are used to safely decode read data from SDRAM.

WRITE_PIPE uses a flip-flop to meet the setup time for writing data to SDRAM.

FFs are inserted in all output signals to SDRAM.

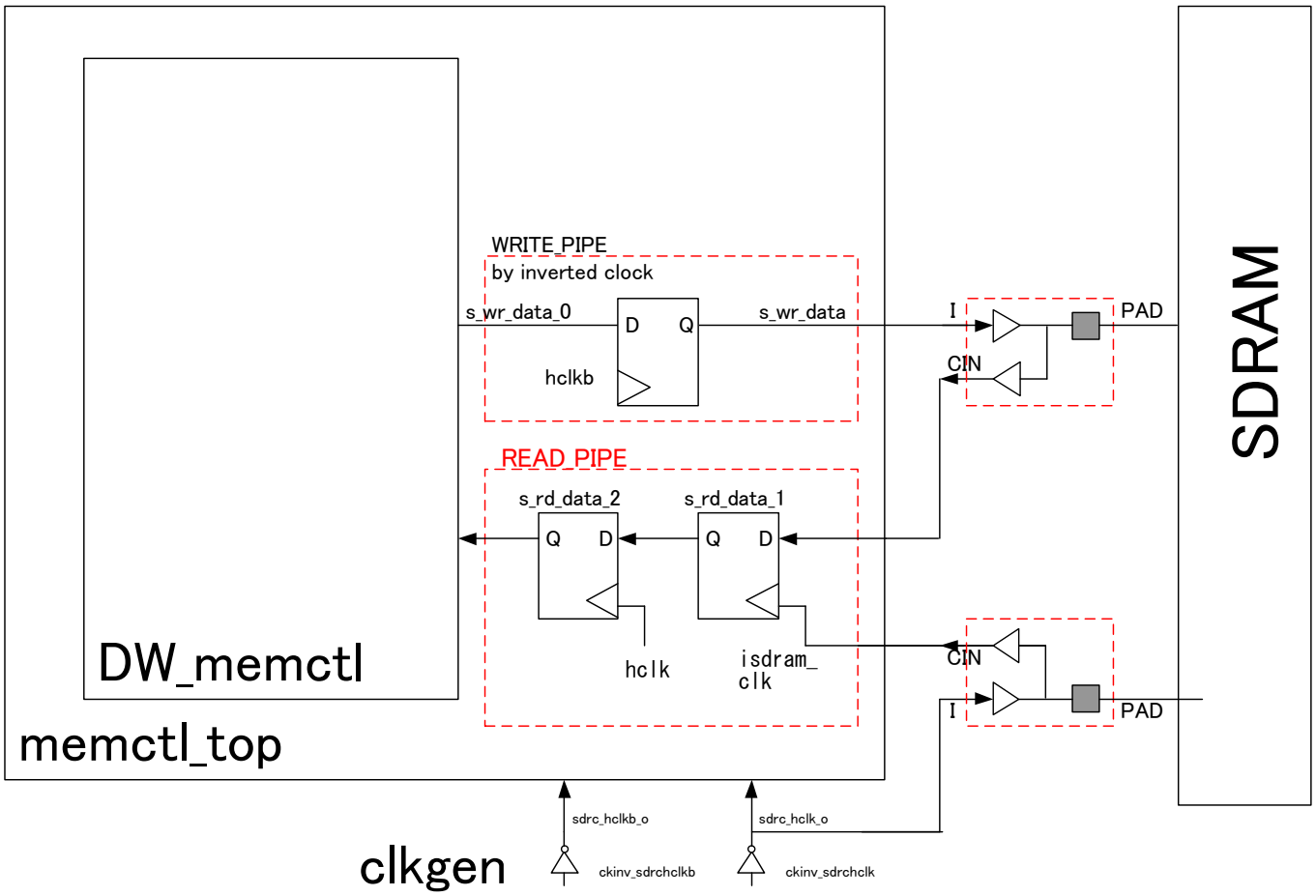


Figure 6. READ_PIPE/WRITE_PIPE

3.2.3. SDRAM

Connection of SDRAM Interface and SDRAM

The pin characteristic in the SDRAM interface is shown in the table below.

SDRAM Interface Pin Characteristic

Pin Name	Function	Direction	Active State
SDCLK	SDRAM Clock Signal	O	Clock
SDCKE	SDRAM Clock Enable Signal	O	High
CS3 - CS0	External RAM Chip Select	O	Low
RAS	SDRAM Row Address Enable	O	Low
CAS	SDRAM Column Address Enable	O	Low
SDWR	SDRAM Write Signal	O	Low
BA1 - BA0	SDRAM Bank Address	O	Address
M_PRE_BIT	SDRAM Pre-Charge Bit (Connected to 10-Bit Address)	O	Address
ADDR22 - ADDR0	SDRAM Addresses	O	Address
DATA31 - DATA0	SDRAM Data Bus	I/O	Data
DQM3 - DQM0	SDRAM Data Mask	O	High

SDRAM Controller's SDRAM Initialization Sequence

Because of the default memory allocation in SDRAM, HW does the SDRAM initialization sequence automatically after power-on reset. However, SDRAM access should be done after register SCTLR[0] becomes 0.

The flow of the initialization sequence is shown in the figure below.

(1) After Power On, SDCLK is enabled and NOP state is maintained during t_init.
(2) Pre-charging of all banks is done.
(3) Auto-Refresh operation is done *num_int_ref* times.
(4) Afterwards, the SDRAM mode register is set.

Moreover, after the initialization sequence ends, writing “1” to register SCTLR[0] can execute the initialization sequence operation again.

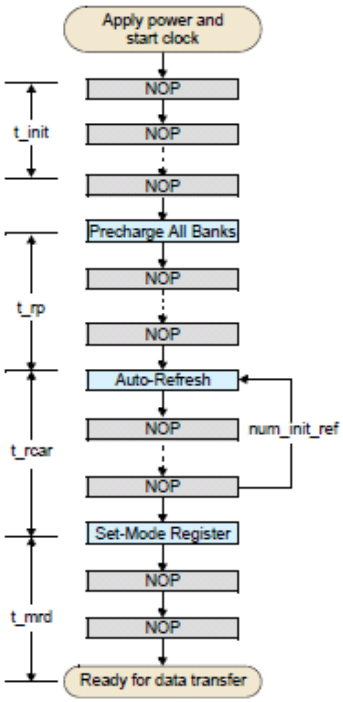


Figure 7. SDRAM Initialization Sequence

About SDRAM Controller's SDRAM Mode Register

The mode register is updated during initialization. Afterwards, mode register update is done by writing '1' to the 9-bit SDRAM Control Register.

The SDRAM controller can change the CAS latency with SDRAM Timing Register as shown in the figure below. However, it is necessary to update the mode register when the value of controller's CAS latency is changed. Data cannot be read correctly. Only burst length of 4 and sequential burst type are supported. However, data transfer is achieved by repeating four bursts and burst stops.

A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Reserved	0	0	0	CAS latency			BT	Burst Length		
							0	0	1	0

A6	A5	A4	CAS latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Figure 8. Definition of Mode Register

SDRAM Controller's SDRAM Command

The SDRAM commands are shown in the table below.

SDRAM Command Truth Table

Function	Symbol	CKE	DQM	CS	RAS	CAS	WE
Detect	NOP	X	X	H	X	X	X
No Operation	NOP	X	X	L	H	H	H
READ	READ	X	X	L	H	L	H
WRITE	WRITE	X	X	L	H	L	L
Bank Activate	ACT	X	X	L	L	H	H
Pre-Charge	PRE	X	X	L	L	H	L
Auto-Refresh	REF	X	X	L	L	L	H
Mode Register Set	MRS	X	X	L	L	L	L
Self Refresh Entry	REF	L	X	L	L	L	H
Self Refresh Exit	-	H	X	H	X	X	X
Power Down Entry	-	L	X	X	X	X	X
Power Down Exit	-	H	X	H	X	X	X
Data Write / Output Enable	-	H	L	X	X	X	X
Data Write / Output Disable	-	H	H	X	X	X	X

・Read/Write
Read and Write operations are executed through this command.

・Burst Terminate
Inputting the burst stop command during read or write cycle ends burst read or write operation.

・Pre-Charge
Pre-Charge state is executed until operation to a present row address is ended and operation to another row address begins. The device automatically returns to idle state when Pre-Charge command has finished.

・Auto Refresh
Auto-Refresh command can only be executed when all the banks of the device are in idle state. A specific row address in all the banks is selected when Auto-Refresh command is inputted and refresh operation is executed. The device automatically returns to idle state when refresh operation has finished executing.

・Mode Register Set
The value of the mode register is updated through address (A0-A10) when Mode Register Set command is inputted. Mode Register Set command can only be executed when all banks are in idle or suspend state.

・Self Refresh
Self-Refresh command, like the Auto-Refresh command, can only be executed when all banks of the device are idle. During operation, the device refresh automatically. Refresh operation need not be executed from outside. After Self-Refresh operation, the device automatically returns to idle state.

・Power Down Mode
Device enters Power Down mode when SDCKE becomes LOW at idle state. All inputs, except SDCLK and SDCKE, are turned off. During this mode, device's power consumption is decreased. To return to previous state (idle or active state), SDCKE should be made HIGH.

The SDRAM Controller's Read/Write Access

Data transmission to SDRAM is done by 4 consecutive burst operations. The Read/Write timing of SDRAM is shown in the figure below. As shown in Figure 10, 4 burst operations are also needed to execute single write. In this case, Dqm is set to HIGH (4'hF) to mask the data to be written. Moreover, in Figure 11, for writing 8 burst data, 4 burst operations are repeated.

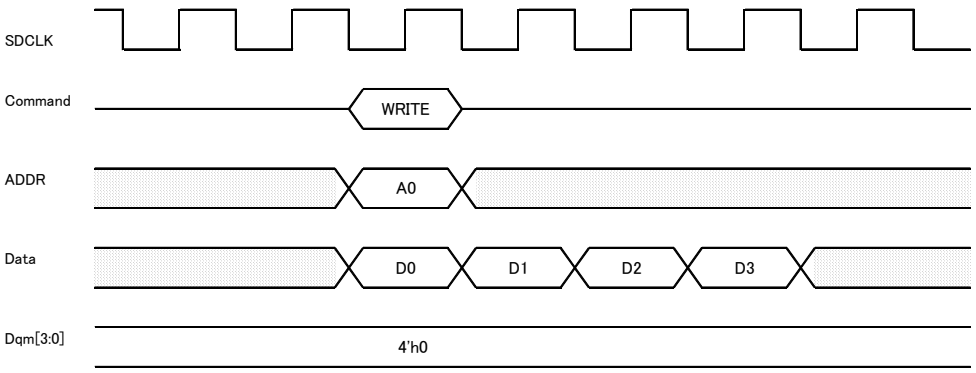


Figure 9. Write Transfer of Four Bursts

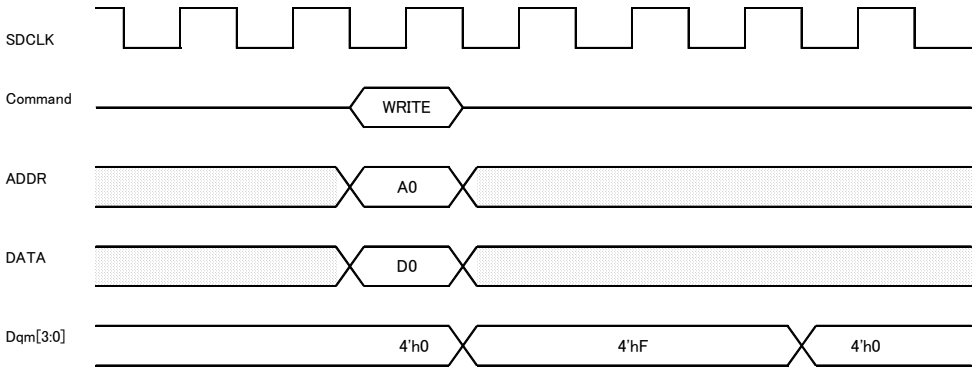


Figure 10. Single Data Write Transfer

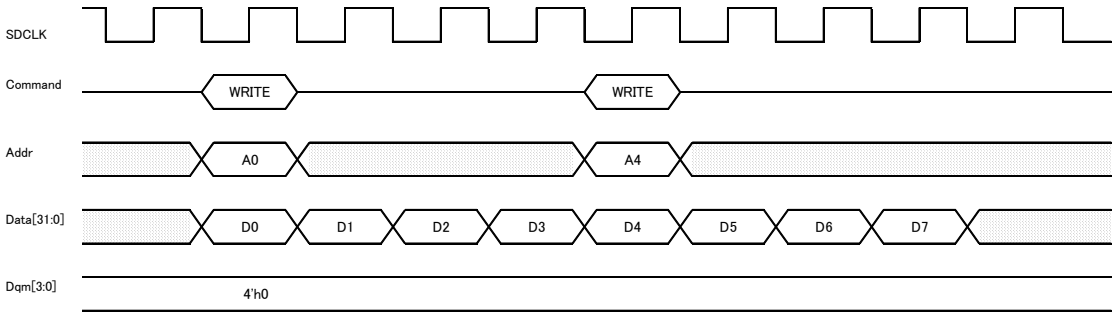


Figure 11. Data Write Transfer of Eight Bursts

Figure 12 is the case where 4 burst read operations are performed by CAS latency =2.
Figure 13is the case where 4 burst read operations are performed by CAS latency =3.
Figure 14 is the case where 8 burst read operations are performed by CAS latency =2.

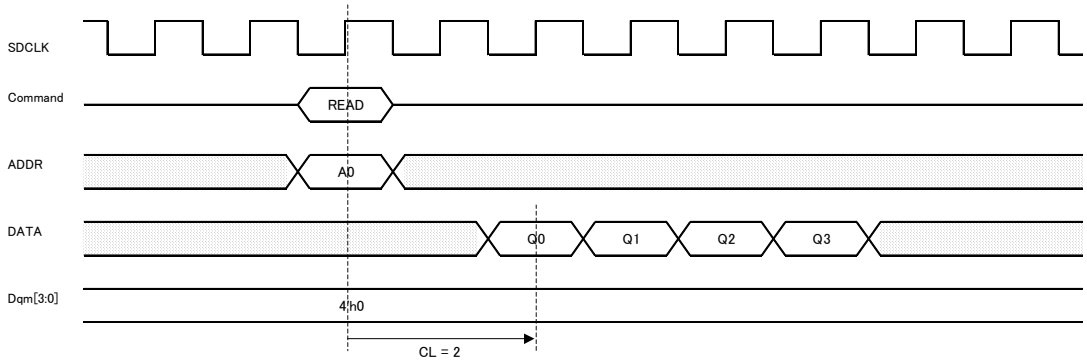


Figure 12. Data Read of Four Bursts (CAS Latency = 2)

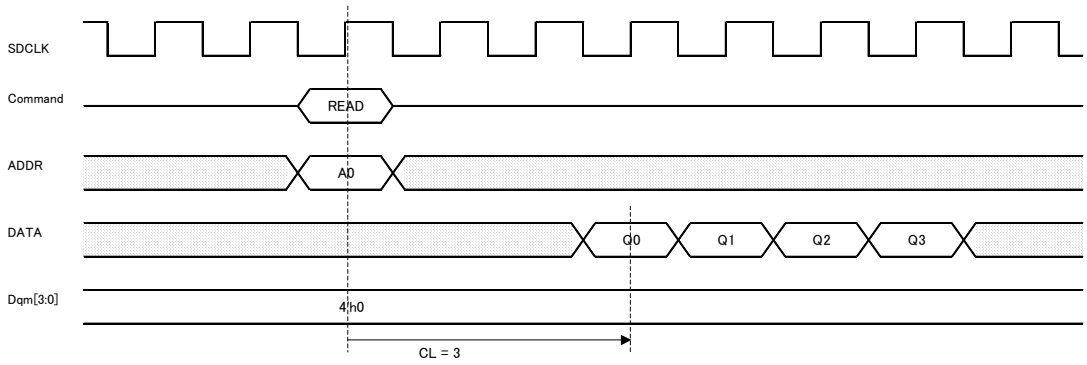


Figure 13. Data Read of Four Bursts (CAS Latency = 3)

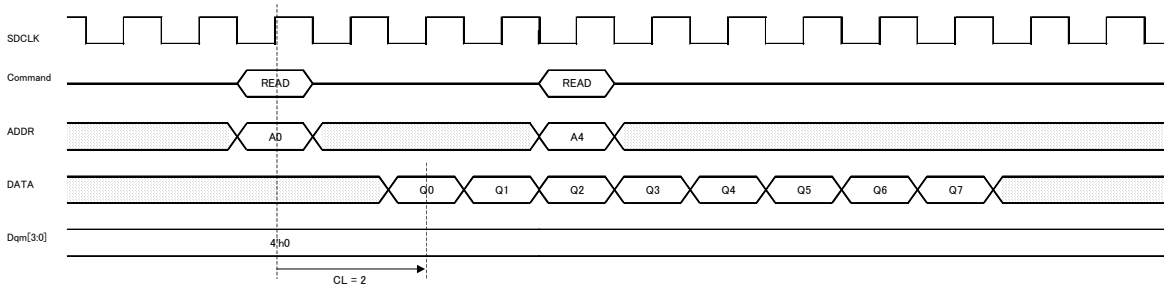


Figure 14. Data Read of Eight Bursts (CAS Latency = 2)

SDRAM Low Power Consumption Mode

The SDRAM controller supports Power Down Mode, Self-Refresh mode, as well as Low Power Consumption Mode.
By writing '1' to SDRAM control register SCTLR[2], the device goes to Power Down Mode.
By writing '1' to SDRAM control register SCTLR[1], the device goes to Self-Refresh Mode.
Device will exit any of these modes by clearing the SDRAM control register (SCTLR = 0).

Power Down Mode

When device is in Power Down Mode, SDRAM clock is disabled, which results to lower power consumption. If SDRAM control register SCTLR[2] = '1', clock enable (CKE) is set to LOW. At this point, Power Down mode will start. Refer to the figure below.
To return to normal operation, clear register SCTLR[2], and CKE is set to HIGH.
Moreover, when in Power Down mode, during refresh cycle, Power Down Mode is cancelled while device performs Refresh operation. When refresh operation has finished executing, device returns to Power Down mode again.
At least one SDCLK cycle should be supplied to SDRAM before setting CKE to HIGH.

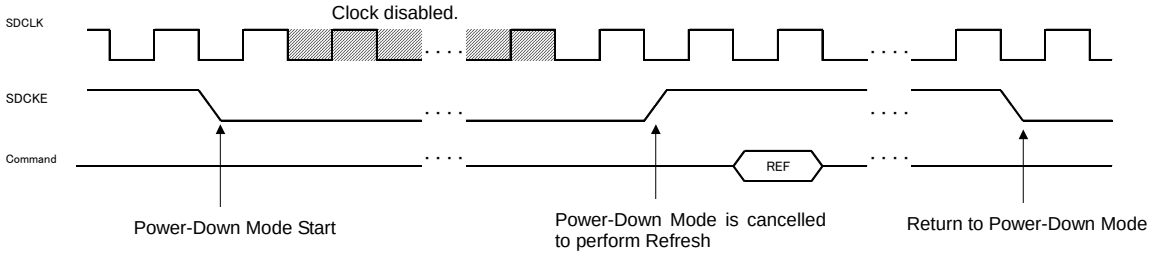


Figure 15. Power Down Mode

Self-Refresh Mode

Like in Power Down Mode, when device is in Self-Refresh mode, clock is disabled and power consumption becomes lower. Refresh operation is automatically executed using the refresh counter inside SDRAM.
This mode takes effect when SDRAM is not accessed for a long time.
Figure 16 shows the timing diagram during Self-Refresh mode.
When SDRAM control register SCTLR[1] is set to '1', clock enable (CKE) is set to LOW. Self-Refresh command is inputted and device enters Self-Refresh mode, as shown in the figure.
To return to normal operation, clear register SCTLR[1], and CKE is set to HIGH.
At least one SDCLK cycle should be supplied to SDRAM before setting CKE to HIGH.

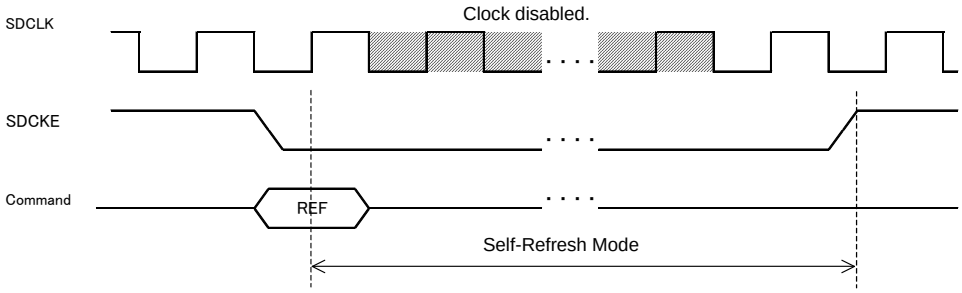
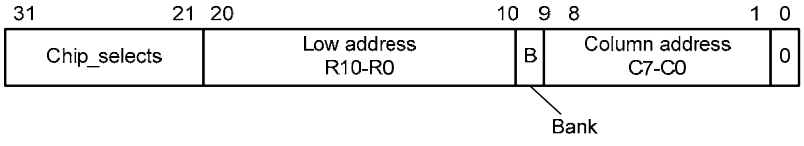


Figure 16. Self-Refresh Mode

About the Address Translation

The figure shows the correspondence of the AHB address and the SDRAM address.



SDRAM Controller's Default

An initial value of memory controller's SDRAM is set as follows:

- Width of Row address: 11 bits
- Width of Column address: 8 bits
- Number of banks: 2
- CAS Latency: 2

Please refer to the configuration list for other settings.

3.2.4. External Memory Interface

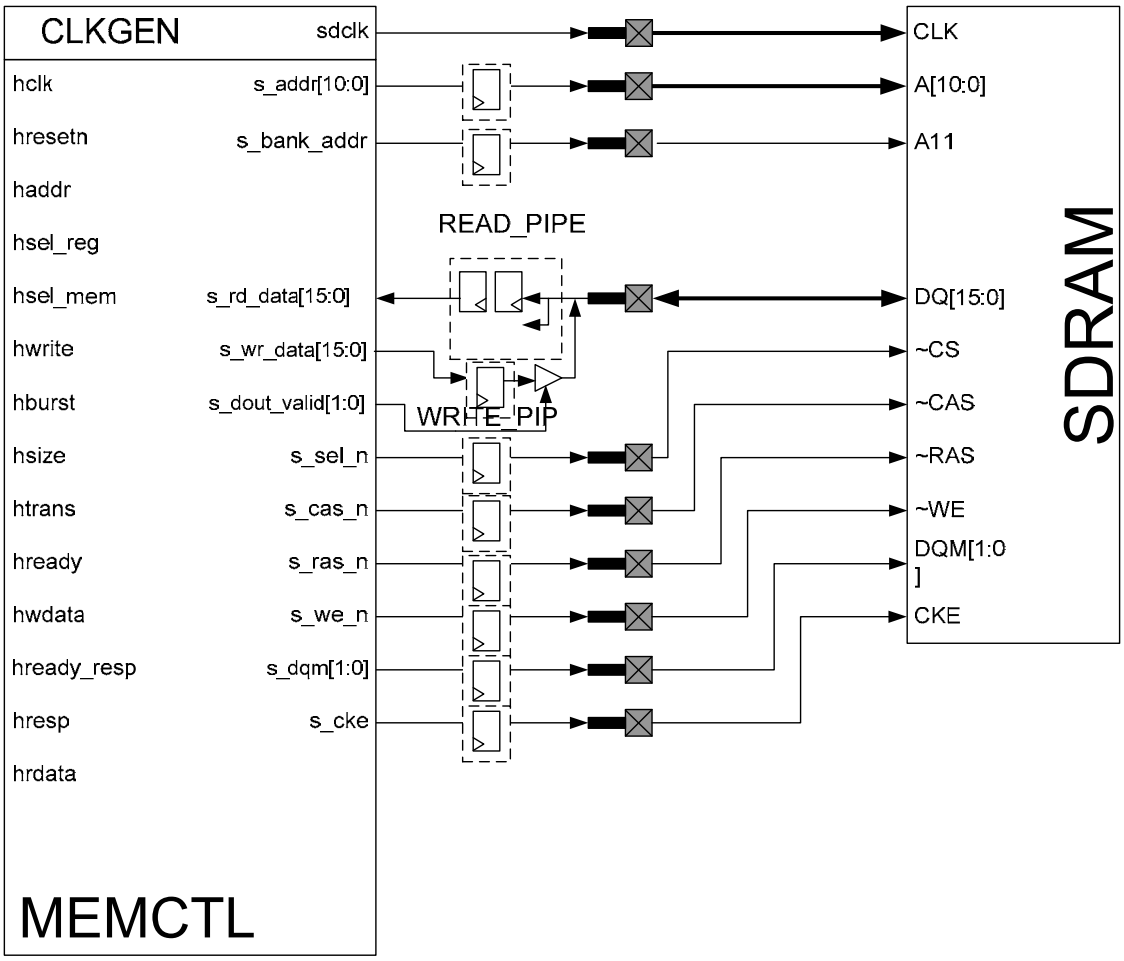


Figure 17. External Memory Interface

3.3. I/O Signal

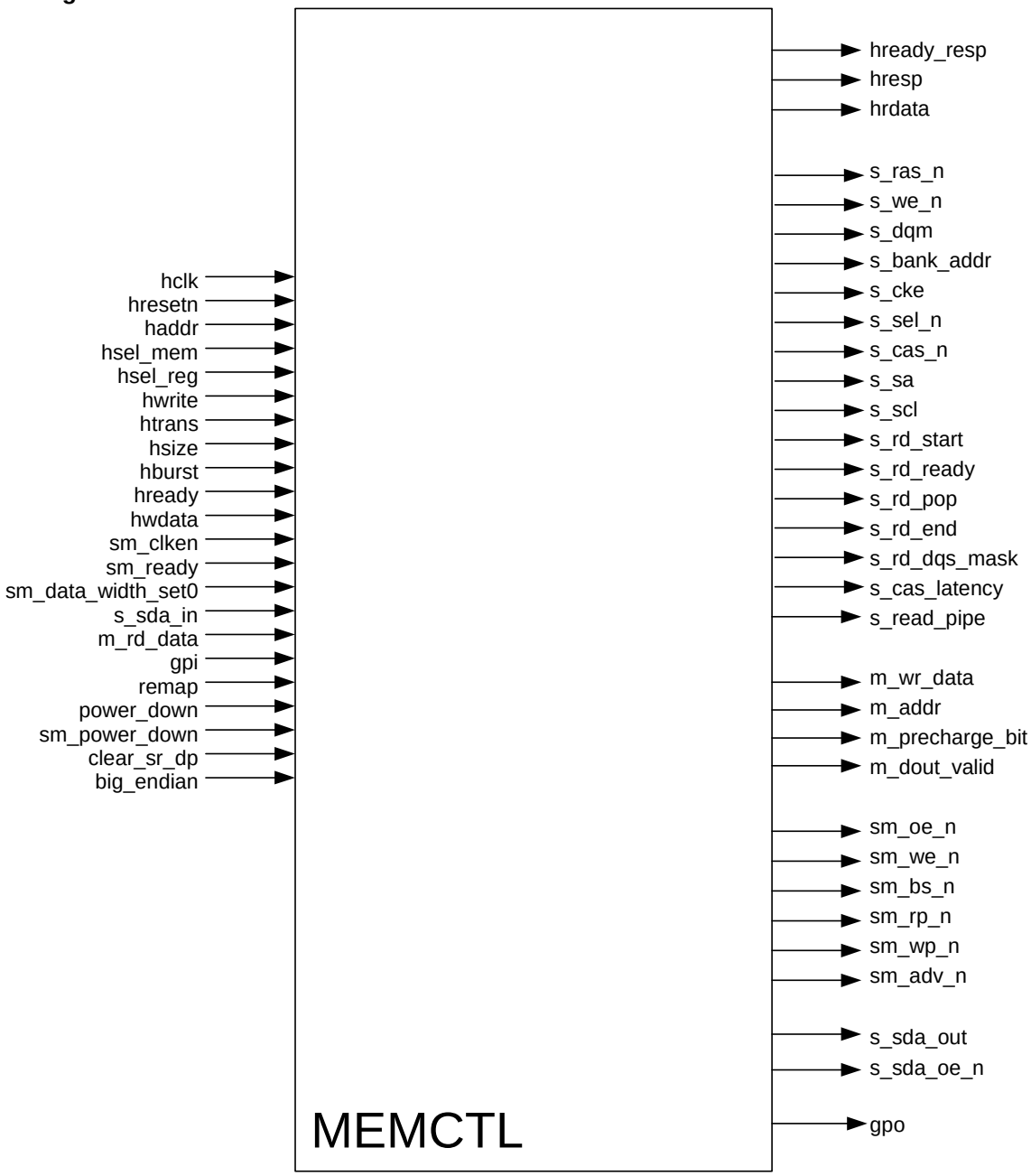


Figure 18. Memory Controller

Pin Name	Dir.	Description	Connection
AHB Interface			
hclk	In	AHB Bus Interface Clock	CLOCK GEN
hresetn	In	AHB Bus Reset (Active Low)	Reset GEN
hsel_mem	In	AHB Select Signal (Memory)	AHB
hsel_reg	In	AHB Select Signal (Register)	AHB
hwrite	In	0: Read 1: Write	AHB
htrans[1:0]	In	AHB Bus Transfer Type	AHB
hsize[2:0]	In	AHB Bus Transfer Size	AHB
hburst[2:0]	In	AHB Bus Burst Type	AHB
hready_resp	Out	AHB Bus Data Ready Response	AHB
hready	In	AHB Bus Data Ready Input	AHB
hresp[1:0]	Out	AHB Bus Transfer Response	AHB
haddr[31:0]	In	AHB Address Bus	AHB
hwdata[31:0]	In	AHB Write Data Bus	AHB
hrdata[31:0]	Out	AHB Read Data Bus	AHB
Miscellaneous Signals			
big_endian	In	Endian setting 0: Little-Endian 1: Big-Endian	Fixed to Low
remap	In	Remap Signal 0: Normal Mode 1: Remap Operation	Fixed to Low
gpo[7:0]	Out	General Purpose Output	Open
gpi[7:0]	In	General Purpose Input: It is possible to read this signal from the SREFR register by connecting it to the FLASH status pin.	Fixed to Low
power_down	In	Power Saving Signal Received from the External Power Management Module (SDRAM exclusive use): This signal is connected to the Power Down bit of SCTLR register. 0：Normal Mode 1：Power Down Mode	Fixed to Low
clear_sr_dp	In	Self-Refresh Signal Received from the external Power Management Module (SDRAM exclusive use)	Fixed to Low
sm_power_down	In	Power Saving Signal Received from the External Power Management Module (FLASH exclusive use):This signal is connected to the Power Down bit of SMCTLR register.	Fixed to Low

Pin Name	Dir.	Description	Connection
scan_mode	In	Scan mode: This signal is used to bypass an internally generated asynchronous reset with hresetn in scan mode. This signal ensures that all flip-flops in the component are controllable and observable during scan testing, during which, the signal must be asserted. At all other times, it must be de-asserted. Dependencies: Must be asserted during scan testing	TESTDEC scanmode
debug_****	Out	For debugging	Open
SDRAM Serial Presence Detect EEPROM Interface Signals			
s_scl	Out	SPD Clock	Open
s_sa[2:0]	Out	SPD Address	Open
s_sda_oe_n	Out	SPD Output Enable (Active Low)	Open
s_sda_out	Out	SPD Data Output	Open
s_sda_in	In	SPD Data Input	Fixed to Low
SDRAM Interface Signals			
s_ras_n	Out	Row Address Select	I/O
s_cas_n	Out	Column Address Select	I/O
s_cke	Out	Clock Enable	I/O
s_rd_data[15:0]	In	SDRAM Read Data from External SDRAM	I/O
s_wr_data[15:0]	Out	SDRAM Write Data to External SDRAM Refer to DW_memctl_miu_ddrwr.v file for more details	I/O
s_addr[10:0]	Out	SDRAM Address Bus to External SDRAM (Also see the m_precharge_bit pin details.)	I/O
s_bank_addr	Out	Bank Address	I/O
s_dout_valid[1:0]	Out	s_dout_valid[1]: SDRAM Valid Signal for Write Data to SDRAM s_dout_valid[0]: decides direction of data flow (Low – Input High – Output)	I/O
s_sel_n	Out	Chip Select	I/O
s_dqm[1:0]	Out	Write Mode: Input Mask Read Mode: Output Enable	I/O
s_we_n	Out	Write Enable	I/O
s_rd_ready	In	Read Data Ready	Fixed to Low
s_rd_start	Out	Read Command Start Signal	Open
s_rd_pop	Out	Read Data POP	Open
s_rd_end	Out	Last Burst Data	Open
s_cas_latency[2:0]	Out	Unnecessary (Open)	Open
s_rd_dqs_mask	Out	DQS Mask Signal for SDRAM and Read	Open
s_read_pipe	Out	Unnecessary (Open)	Open

3.4. Register

3.4.1. Memory Map

Name	Description	Address Offset	R/W	Width	Reset
SCONR	SDRAM Configuration Register	0x000	R/W	32bits	0x00140F40
STMG0R	SDRAM Timing Register 0	0x004	R/W	32bits	0x01999251
STMG1R	SDRAM Timing Register 1	0x008	R/W	32bits	0x00017080
SCTLR	SDRAM Control Register	0x00c	R/W	32bits	0x00001048
SREFR	SDRAM Refresh Register	0x010	R/W	32bits	0x000002EC
SMSKR0	MASK Register 0	0x054	R/W	32bits	0x00000206

3.4.2. Register Detail

SCONR (SDRAM Config Register)
Offset: 0x00
Width: 32 bits

Bits	Direction	Reset	Description
31:21	N/A	0x0	Reserved
20	R/W	0x1	Enable Signal of Data PIN for I2CData I/O Direction Switch for SPD (Not Possible for Use) 0: Read 1: Write
19	R/W	0x0	SPD Access Bit (Not Possible for Use)
18	R/W	0x1	SPD Clock (Not Possible for Use)
17:15	R/W	0x0	SPD Address Bits (Not Possible for Use)
14:13	R/W	0x0	SDRAM Data Bus Width Setting 2'b00: 16 bits 2'b01: 32 bits 2'b10: 64 bits (Not Possible for Use) 2'b11: 128 bits (Not Possible for Use) Please use this bit with a Reset value.
12:9	R/W	0x7	SDRAM Column Address Bit Width Setting 4'hF: Reserved 4'hE: 15 bits 4'hD: 14 bits 4'hC: 13 bits 4'hB: 12 bits 4'hA: 11 bits 4'h9: 10 bits 4'h8: 9 bits 4'h7: 8 bits 4'h6 to 4'h0: Reserved Please use this bit with a Reset value.
8:5	R/W	0xA	SRAM Row Address Bit Width Setting 4'hF: 16 bits 4'hE: 15 bits 4'hD: 14 bits 4'hC: 13 bits 4'hB: 12 bits 4'hA: 11 bits 4'h9 to 4'h0: Reserved Please use this bit with a Reset value.
4:3	R/W	0x0	SDRAM Bank Address Width Setting 2'b11: 4 bits 2'b10: 3 bits 2'b01: 2 bits 2'b00: 1 bit Please use this bit with a Reset value.
2:0	R/W	0x0	Reserved

STMG0R (SDRAM Timing Register 0)
Offset: 0x04
Width: 32 bits

Bits	Direction	Reset	Description
25:22	R/W	T_RC-1 4'h6	Random Read and Write Setting at t_rc Cycle Intervals 4'hF: 16 Clocks 4'hE: 15 Clocks 4'hD: 14 Clocks 4'hC: 13 Clocks 4'hB: 12 Clocks 4'hA: 11 Clocks 4'h9: 10 Clocks 4'h8: 9 Clocks 4'h7: 8 Clocks 4'h6: 7 Clocks 4'h5: 6 Clocks 4'h4: 5 Clocks 4'h3: 4 Clocks 4'h2: 3 Clocks 4'h1: 2 Clocks 4'h0: 1Clock Please use this bit with a Reset value.
31:27 21:18	R/W	T_XSR-1 0x6	Interval Setting to Shift from Self-Refresh Mode to Active or Self-Refresh Mode 0 to 511: 1 to 512 clocks Please use this bit with a Reset value.
17:14	R/W	T_RCAR-1 0x6	Auto-Refresh Interval Setting (t_rcar) 4'hF: 16 Clocks 4'hE : 15 Clocks 4'hD : 14 Clocks 4'hC: 13 Clocks 4'hB : 12 Clocks 4'hA : 11 Clocks 4'h9: 10 Clocks 4'h8 : 9 Clocks 4'h7 : 8 Clocks 4'h6: 7 Clocks 4'h5 : 6 Clocks 4'h4 : 5 Clocks 4'h3: 4 Clocks 4'h2 : 3 Clocks 4'h1 : 2 Clocks 4'h0: 1 Clock Please use this bit with a Reset value.
13:12	R/W	T_WR-1 0x1	Interval Setting from Last Data Write to Pre-Charge Mode 2'h3: 4 Clocks 2'h2: 3 Clocks 2'h1: 2 Clocks 2'h0: 1 Clock Please use this bit with a Reset value.
11:9	R/W	T_RP-1 0x1	Interval Setting for Pre-Charge Mode 3'h7: 8 Clocks 3'h6: 7 Clocks 3'h5: 6 Clocks 3'h4: 5 Clocks 3'h3: 4 Clocks 3'h2: 3 Clocks 3'h1: 2 Clocks 3'h0: 1 Clock Please use this bit with a Reset value.
8:6	R/W	T_RCD -1 0x0	Shortest Value (Duration) of Read/Write Command After Active Is Issued 3'h7: 8 Clocks 3'h6: 7 Clocks 3'h5: 6 Clocks 3'h4: 5 Clocks 3'h3: 4 Clocks 3'h2: 3 Clocks 3'h1: 2 Clocks 3'h0: 1 Clock Please use this bit with a Reset value.
5:2	R/W	T_RAS_MIN-1 0x4	Shortest Value (Duration) of Pre-Charge Command After Active Is Issued 3'h7: 8 Clocks 3'h6: 7 Clocks 3'h5: 6 Clocks 3'h4: 5 Clocks 3'h3: 4 Clocks 3'h2: 3 Clocks 3'h1: 2 Clocks 3'h0: 1 Clock Please use this bit with a Reset value.
26 1:0	R/W	CAS_LATENCY-1 0x1	First Data Interval (CAS Latency) 3'h3: 4 Clocks 3'h2: 3 Clocks 3'h1: 2 Clocks 3'h0: 1 Clock Please use this bit with a Reset value.

STMG1R (SDRAM Timing Register 1)
Offset: 0x08
Width: 32 bits

Bits	Direction	Reset	Description
31:22	N/A	0x0	Reserved
21:20	N/A	0x0	Unnecessary
19:16	R/W	NUM_INIT_REF-1 0x1	Auto-Refresh Frequency Upon Initialization 4'hF: 16 times 4'hE: 15 times 4'hD: 14 times 4'hC: 13 times 4'hB: 12 times 4'hA: 11 times 4'h9: 10 times 4'h8: 9 times 4'h7: 8 times 4'h6: 7 times 4'h5: 6 times 4'h4: 5 times 4'h3: 4 times 4'h2: 3 times 4'h1: 2 times 4'h0: 1 time Please use this bit with a Reset value.
15:0	R/W	T_INIT 28800	Interval Setting of Command After Power Supply Is Turned On [Clock] Please use this bit with a Reset value.

SCTLR (SDRAM Control Register)
Offset: 0x0C
Width: 32 bits

Bits	Direction	Reset	Description
31:19	N/A	0x0	Reserved
18	N/A	0x0	Reserved
17	R/W	0x0	Read Data Ready Mode Setting (Not Possible for Use) 0 : NOT Ready 1: Read Data Ready signal s_rd_ready becomes HIGH. SDRAM read data is outputted after Read is done.
16:12	R/W	OPEN_BANKS- 1 0x1	Number of Active SDRAM Banks Maximum Value: 15 Minimum Value: 0 Please use this bit with a Reset value.
11	R	0x0	SDRAM Self-Refresh Mode 0: Normal Mode 1: Self-Refresh Mode
10	R/W	0x0	Reserved
9	R/W	0x0	Mode Register Update Bit This bit is automatically cleared when updating mode register. 0: Normal Mode 1: Update Mode
8:6	R	READ_PIPE 0x1	Number of Read Pipes During Read Data Passing
5	R/W	0x0	Number of Refresh Operation Done by Memory Controller After SDRAM Has Finished Executing Self-Refresh Mode 0: Only 1 row is refreshed after SDRAM finishes Self-Refresh operation. 1: All rows are refreshed after SDRAM finishes Self-Refresh operation. Please use this bit with a Reset value.
4	R/W	0x0	Number of Refresh Operation Done by Memory Controller Before SDRAM Enters Self-Refresh Mode 0: Only 1 Row is refreshed before SDRAM enters Self-Refresh mode. 1: All rows are refreshed before SDRAM enters Self-Refresh mode.
3	R/W	0x1	Pre-Charge Method Setting on the Specified Row 0: Immediate Pre-Charge: After the write/read operation, the selected row undergoes Pre-Charge operation. 1: Delay Pre-Charge: After the write/read operation, selected row is kept open. Please use this bit with a Reset value.
2	R/W	0x0	SDRAM Power Down Mode Setting 0: Normal Mode 1: Power Down Mode
1	R/W	0x0	SDRAM Self-Refresh Mode Setting 0: Normal Mode 1: Self-Refresh Mode When Self-Refresh operation has finished executing, the memory controller clears this bit.
0	R/W	0x1	SDRAM initialization Sequence Setting 0: Normal Mode 1: Initialization Mode When Initialization Sequence has finished executing, memory controller clears this bit.

SREFR (SDRAM Refresh Interval Register)
Offset: 0x10
Width: 32 bits

Bits	Direction	Reset	Description
31:24	R/W	―	Connected directly to external gpi terminal (Not possible for use)
23:16	R/W	0x0	Connected directly to external gpo terminal (Not possible for use)
15:0	R/W	T_REF 0x2EC	SDRAM Refresh Interval Setting 748 clocks in case of 96MHz: 7.8us Please use this bit with a Reset value.

SCSLR0_LOW (Chip Select Register 0 Low)
Offset: 0x14
Width: 32 bits

Bits	Direction	Reset	Description
31:16	R/W	0x8000	Base Address Chip Select Please use this bit with a Reset value.
15:0	R/W	0x0	Reserved

*When N_CS = 1 is specified by the configuration, this register is deleted.

SMSKR0 (Address Mask Register 0)
Offset: 0x54
Width: 32 bits

Bits	Direction	Reset	Description
31:11	R/W	0x0	Reserved
10:8	R/W	0x0	Timing Parameter Setting This signal becomes Don 't Care for SDRAM. 0: Timing Register 0 1: Timing Register 1 2: Timing Register 2 Please use this bit with a Reset value.
7:5	R/W	0x0	Memory Type Select 2'b00: SDRAM 2'b01: SRAM 2'b10: FLASH 2'b11: ROM Please use this bit with a Reset value.
4:0	R/W	0x6	Memory Size Select 0: Memory is not connected. 1: 64 Kb 2: 128 kB 3: 256 kB 4: 512 kB 5: 1 MB 6: 2 MB 7: 4 MB 8: 8 MB 9: 16 MB 10: 32 MB 11: 64 MB 12: 128 MB 13: 256 MB 14: 512 MB 15: 1 GB 16: 2 GB 17: 4 GB Please use this bit with a Reset value.

4. Interrupt Controller

4.1. Features

- It functions as AMBA-AHB slave device.
- AHB Bus Width: 32 bits
- It corresponds to Little-Endian system.
- The interrupt input from each block is detected, and the interrupt output to CPU is controlled.
- The interrupt input and output are both active low.
- It corresponds to 32-input IRQ and one-input FIQ (interrupt usually) (high-speed interrupt).

4.2. Description

4.2.1. IRQ

- ◇ 16-Stage Priority Controller
- ◇ The interrupt vector is programmable in each stage of priority.
- ◇ Generation of Software Interrupt
- ◇ It is possible to individually enable control for each interrupt.
- ◇ The mask can individually control interrupt.
- ◇ Various status registers are installed.

4.2.2. FIQ

- ◇ The software interrupt can be generated.
- ◇ Various status registers are installed.

4.2.3. IRQ Interrupt Output

- ◇ The IRQ interrupt output circuit is shown below.

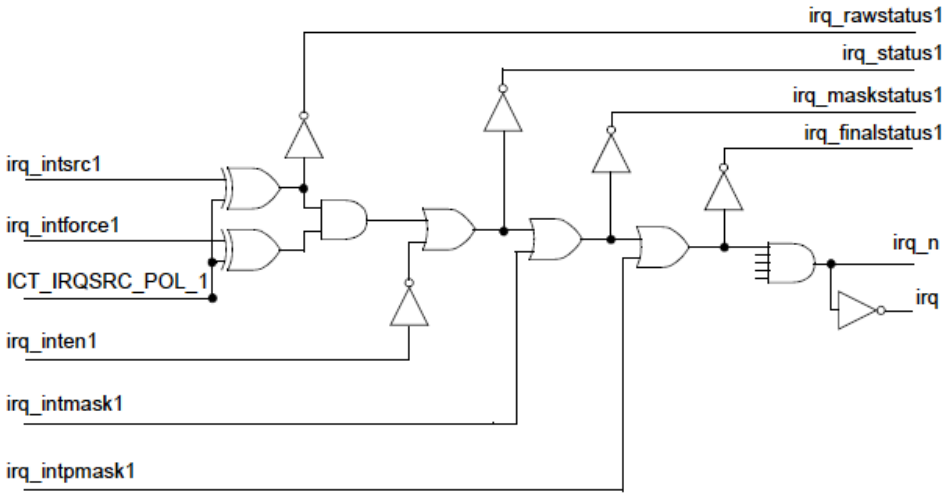


Figure 19. IRQ Interrupt Generation Circuit

4.2.4. IRQ Interrupt Polarity

- ◇ The IRQ interrupt input polarities are all active low.
- ◇ The IRQ interrupt output polarities are all active low.
- ◇ The polarity of the IRQ interrupt output is active low.
- ◇ Each interrupt status is active high.

4.2.5. IRQ Software Interrupt

- ◇ Interrupt can be forced generated from software.
- ◇ Interrupt can be activated by setting L to the corresponding bit of the irq_intforce_i register.
- ◇ At initial state, all interrupts are at inactive state.

4.2.6. Enable IRQ and IRQ Mask

- ◇ It is possible to enable each interrupt input.
- ◇ The interrupt input can be enabled by setting H to the corresponding bit of the irq_inten_i register.
- ◇ At initial state, all interrupts are disabled.
- ◇ The mask can be set at each interrupt input.
- ◇ The mask can do the interrupt input by setting H to the corresponding bit of the irq_intmask_i register.
- ◇ At initial state, all masks are invalid.

4.2.7. IRQ Interrupt Priority Level

◇ Interrupt Input/Priority

Correspondence of IRQ and priority

IRQ Number	Priority	Priority Level Value
0	High	15
1	↑	14
2	:	13
:	:	:
14	↓	1
15 to 31	Low	0

◇ The priority level value can be read.
◇ The priority level is set by the value of 0-15.
◇ Priority Level 15 becomes the highest priority, and the priority falls as the priority level value becomes smaller. Priority Level 0 becomes the lowest level of priority.
◇ System priority level value (0-15) can be set by the irq_plevel register.
◇ An interrupt with a lower priority level than system priority level is disregarded.
◇ The initial value of the system priority level is 0.

4.2.8. IRQ Interrupt Status

◇ The following Interrupt Status can be read and are all active high.
- IRQ raw status (irq_rawstatus)
  Can be read from irq_rawstatus register.
- IRQ status(irq_status)
  Can be read from irq_status register.
- IRQMask status (irq_maskstatus)
  Can be read from irq_maskstatus register.
- IRQFinal status (irq_finalstatus)
  Can be read from irq_finalstatus register.

◇ Please refer to the IRQ interrupt output generation circuit for content of various interrupt status.

4.2.9. IRQ Interrupt Vector

◇ The interrupt vector of each IRQ interrupt priority can be set.
◇ An initial value of each interrupt vector is "0".
◇ Each interrupt vector sets the irq_vector_N (where 0 <= N <= 15) register.

4.2.10. FIQ Interrupt Output

◇ The generation circuit of the FIQ interrupt output is shown below.

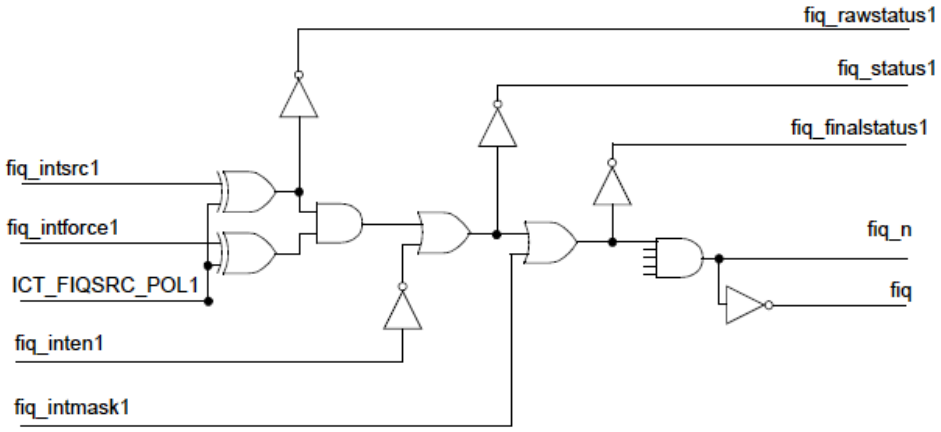


Figure 20. FIQ Interrupt Generation Circuit

4.2.11. FIQ Interrupt Polarity

◇ The polarity of the FIQ interrupt input is active low.
◇ The polarity of the FIQ interrupt output is active low.
◇ If L is written in the fiq_inforce register, the software interrupt becomes active.
◇ Each interrupt status is active high.

4.2.12. FIQ Software Interrupt

◇ Interrupt can be forced generated from software.
◇ Interrupt can be activated by setting L to the corresponding bit of the fiq_intforce register.
◇ At initial state, all software interrupts are at inactive state.

4.2.13. Enable FIQ and FIQ Mask

◇ It is possible to enable each interrupt input.
◇ The interrupt input can be enabled by setting H to the corresponding bit of the fiq_inten register.
◇ At initial state, all interrupts are disabled.
◇ The mask can be set to the interrupt input.
◇ The mask of the interrupt input can be done by setting H to the corresponding bit of the fiq_intmask register.
◇ At initial state, the mask is invalid.

4.2.14. FIQ Interrupt Status

◇ The following interrupt status can be read and all are active high.
- FIQ raw status (fiq_rawstatus)
  Status can be read from fiq_rawstatus register.
- FIQ status (fiq_status)
  Status can be read from fiq_status register.
- FIQ final status (irq_finalstatus)
  Status can be read from fiq_finalstatus register.

◇ Please refer to the FIQ interrupt output generation circuit for content of various interrupt status.

4.3. I/O Signal

Terminal Name	I/O	Description	Connection
hclk	In	AHB Bus Clock	CLOCKGEN
hresetn	In	AHB Bus Reset (Active Low)	RESET GEN
hsel	In	AHB Slave Selection	AHB
hwrite	In	AHB Write	AHB
htrans [1:0]	In	AHB Transfer Type	AHB
hsize [2:0]	In	AHB Transfer Size	AHB
hready	In	AHB Ready Signal	AHB
haddr [31:0]	In	AHB Address	AHB
hwdata [31:0]	In	AHB Write Data	AHB
hresp [1:0]	Out	AHB Slave Response	AHB
hready_resp	Out	AHB Tranfer Completion	AHB
hrdata [31:0]	Out	AHB Read Data	AHB
irq_intsrc [22:0]	In	IRQ Interrupt Source	The following are detailed.
fiq_intsrc	In	FIQ Interrupt Source	Watchdog Timer
irq_n	Out	IRQ Interrupt (Active Low)	ARM
fiq_n	Out	FIQ Interrupt (Active Low)	ARM

List of IRQ Interrupt Connection Destination

Terminal Name	Connection	Terminal Name	Connection
irq_intsrc[0]	TIMER0	irq_intsrc[1]	TIMER1
irq_intsrc[2]	TIMER2	irq_intsrc[3]	TIMER3
irq_intsrc[4]	TIMER4	irq_intsrc[5]	RTC
irq_intsrc[6]	UART0	irq_intsrc[7]	UART1
irq_intsrc[8]	SSI_M	irq_intsrc[9]	SSI_S
irq_intsrc[10]	I2C0	irq_intsrc[11]	I2C1
irq_intsrc[12]	GPIO0	irq_intsrc[13]	GPIO1
irq_intsrc[14]	I2SOUT	irq_intsrc[15]	RCR
irq_intsrc[16]	DMAC	irq_intsrc[17]	QuadSPI
irq_intsrc[18]	I2SIN/CD-ROM	irq_intsrc[19]	SDIO
irq_intsrc[20]	USB	irq_intsrc[21]	USB_DMAC
irq_intsrc[22]	USB CONN		

4.4. Register Map

4.4.1. Memory Map

Name	Offset	R/W	Width	Description
irq_inten_l	0x00	R/W	32	IRQ Source Enable Register Initial Value：0x0000_0000
irq_intmask_l	0x08	R/W	32	IRQ Source Mask Register Initial Value：0x0000_0000
irq_intforce_l	0x10	R/W	32	IRQ Forced Enable Register Initial Value：0xFFFF_FFFF
irq_rawstatus_l	0x18	R	32	IRQ Raw Status Register Initial Value：－
irq_status_l	0x20	R	32	IRQ Status Register Initial Value：－
irq_maskstatus_l	0x28	R	32	IRQ Mask Status Register Initial Value：0x0000_0000
irq_finalstatus_l	0x30	R	32	IRQ Final Status Register Initial Value：0x0000_0000
irq_vector	0x38	R	32	IRQ Vector Register Initial Value：0x0000_0000
irq_vector_0	0x40	R/W	32	Vector Register 0 of IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_1	0x48	R/W	32	Vector Register 1 of IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_2	0x50	R/W	32	Vector Register 2 of IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_3	0x58	R/W	32	Vector Register 3 of IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_4	0x60	R/W	32	Vector Register 4 of IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_5	0x68	R/W	32	Vector Register 5 of IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_6	0x70	R/W	32	Vector Register 6 of IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_7	0x78	R/W	32	Vector Register 7 of IRQ Priority Interrupt Initial Value：0x0000_0000

Memory Map – continued

Name	Offset	R/W	Width	Description
irq_vector_8	0x80	R/W	32	Vector Register 8 of IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_9	0x88	R/W	32	Vector Register 9 of IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_10	0x90	R/W	32	Vector Register 10 of IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_11	0x98	R/W	32	Vector Register 11 of IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_12	0xA0	R/W	32	Vector Register 12 IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_13	0xA8	R/W	32	Vector Register 13 of IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_14	0xB0	R/W	32	Vector Register 14 of IRQ Priority Interrupt Initial Value：0x0000_0000
irq_vector_15	0xB8	R/W	32	Vector Register 15 of IRQ Priority Interrupt Initial Value：0x0000_0000
fiq_inten	0xC0	R/W	1	FIQ Source Enable Register Initial Value：0x0
fiq_intmask	0xC4	R/W	1	FIQ Source Mask Register Initial Value：0x0
fiq_intforce	0xC8	R/W	1	FIQ Compulsory Enable Register Initial Value：0x1
fiq_rawstatus	0xCC	R	1	FIQ Raw Status Register Initial Value：0x0
fiq_status	0xD0	R	1	FIQ Status Register Initial Value：0x0
fiq_finalstatus	0xD4	R	1	FIQ Final Status Register Initial Value：0x0
irq_plevel	0xD8	R/W	32	IRQ System Priority Level Register Initial Value：0x0
irq_pN	0xE8+ 4*N	R/W	4	IRQ Source N Priority Level Setting Register Initial Value：0xF-0xN (N > 15 is "0")

4.4.2. Register Detail

irq_inten_i
IRQ Source Enable Register
Offset：0x00

Bits	Name	R/W	Reset	Description
31:0	Interrupt Enable Enable	R/W	0x0	Interrupt Enable Bit 0: Interrupt Disabled 1: Interrupt Enabled

irq_intmask_i
IRQ Source Mask Register
Offset：0x08

Bits	Name	R/W	Reset	Description
31:0	Interrupt Mask	R/W	0x0	Interrupt Mask Bit 0: Masking is not done. 1: Masking is done.

irq_intforce_i
IRQ Forced Enable Register
Offset：0x10

Bits	Name	R/W	Reset	Description
31:0	Forced InterruptF	R/W	0xFFFF_FFFF	Forced Interrupt Bit Each bit corresponds to each forced interrupt input. If the interrupt input is set to active high, the bit that it corresponds to in this register becomes active high. 0: Active Low 1: Active High

irq_rawstatus_i
IRQ Raw Status Register
Offset：0x18

Bits	Name	R/W	Reset	Description
31:0	Interrupt SourceInt	R	–	Actual Interrupt Source 0: No Interrupt 1: There is interrupt.

irq_status_i
IRQ Status Register
Offset：0x20

Bits	Name	R/W	Reset	Description
31:0	Interrupt Status	R	–	Interrupt Status Forced Interrupt and After Enable Interrupt 0: No Interrupt 1: There is interrupt.

irq_maskstatus_i
IRQ Mask Status Register
Offset：0x28

Bits	Name	R/W	Reset	Description
31:0	Interrupt Mask Status	R	0x0	Interrupt Status After Mask 0: No Interrupt 1: There is interrupt.

irq_finalstatus_i
IRQ Final Status Register
Offset：0x30

Bits	Name	R/W	Reset	Description
31:0	Final Forced Interrupt	R	0x0	Interrupt Status After Filter of Priority Level If the priority interrupt is not set, this register is the same as irq_maskstatus_i. 0 : No Interrupt 1: There is interrupt.

irq_vector
IRQ Vector Register
Offset：0x38

Bits	Name	R/W	Reset	Description
31:0	Vector LocationLocation	R	0x0	When interrupt happens, the vector with the highest priority is shown.

irq_vector_m
IRQ Priority M Interrupt Vector Register
Offset：0x40＋8×m(m=0 to 15)

Bits	Name	R/W	Reset	Description
31:0	Interrupt vector_m	R/W	0x0	Interrupt Vector of Priority Level M

fiq_inten
FIQ Source Enable Register
Offset：0xC0

Bits	Name	R/W	Reset	Description
0	Fast Interrupt EnableD	R/W	0x0	The FIQ Interrupt Enable 0： Interrupt Disabled 1： Interrupt Enabled

fiq_intmask
FIQ Source Mask Register
Offset：0xC4

Bits	Name	R/W	Reset	Description
0	Fast Interrupt MaskFast	R/W	0x0	FIQ Interrupt Mask Bit 0：Masking is not done. 1：Masking is done.

fiq_intforce
FIQ Forced Enable Register
Offset：0xC8

Bits	Name	R/W	Reset	Description
0	Forced Fast InterruptFF	R/W	0x1	FIQ Forced Interrupt Bit This bit corresponds to the fiq_intsrc input. If the interrupt input is set to active high, the bit that it corresponds to in this register becomes active high. 0: Active Low 1: Active High

fiq_rawstatus
FIQ Raw Status Register
Offset：0xCC

Bits	Name	R/W	Reset	Description
0	Fast Interrupt Raw Status	R	0x0	FIQ Interrupt Raw Status 0: No interrupt 1: There is interrupt

fiq_status
FIQ Status Register
Offset：0xD0

Bits	Name	R/W	Reset	Description
31:0	Interrupt Statuss	R	0x0	FIQ Forced Interrupt Status After Interrupt Enable 0: No interrupt 1: There is interrupt.

fiq_finalstatus
FIQ Final Status Register
Offset：0xD4

Bits	Name	R/W	Reset	Description
31:0	Final Forced InterruptFinaL	R	0x0	FIQ Interrupt Status After Mask 0: No interrupt 1: There is interrupt.

irq_plevel
IRQ System Priority Level Register
Offset：0xD8

Bits	Name	R/W	Reset	Description
3:0	Interrupt System Priority Level	R/W	0x0	Interrupt Controller System Priority Level to IRQ Interrupt Source IRQ interrupt that is lower than this system priority level is disregarded.

irq_pN
IRQ Source N Priority Level Setting Register
Offset：0xE8+4*N

Bits	Name	R/W	Reset	Description
3:0	Interrupt Source N Priority Level	R/W	0xF-0xN (N>15 is "0")	Priority Level Value to IRQ iInterrupt Source N Priority is 15 (highest) – 0 (lowest)

5. DMAC (Direct Memory Access Controller)

5.1. Feature

5.1.1. Summary

- It has master/slave interface in accordance with AMBA 2.0.
- Direct Memory Access Controller for Two Channels
- The width of the AHB bus is 32 bits.
- Transfer from memory to memory, memory to peripheral, and peripheral to memory and peripheral to peripherals are supported.
- It is possible to connect with the peripheral of APB through the APB bridge.
- Little-Endian Correspondence
- The master port is connected with the system bus.

5.1.2. Address Generation

- The addresses of the transfer source and transfer destination are programmable.
- Address increment, decrement, and a fixed transfer are supported.
- Three kinds of multi block transfer types are supported.
- Block Chaining by Linked List
- Automatic Reload of Channel Register
- Continuous Address Transfer
- The multi block transfer type can be set independently at each transfer source and transfer destination.

5.1.3. Channel Buffer Ring

- FIFO is 16-word long.
- The depth of FIFO can be changed by the register. (max FIFO size)
- Channel FIFO is composed of D-F/F.

5.1.4. Channel Control

- The transfer type of each channel (memory to memory and peripheral to memory, etc.) can be set.
- Each channel can be programmed to be valid/invalid.
- The addresses of transfer source and transfer destination are programmable.
- Channle priority is programmable.
- The burst transaction length is programmable in each channel.
- Transfer can be interrupted along the way.
- The channel can be disabled without data loss.
- The bus can lock while transfer operation is taking place.
- The channel can lock while transfer operation is taking place.
- The channel is locked at the same time while locking the bus.

5.1.5. Flow Control

- DMAC does the flow control (beginning and end of transfer).

5.1.6. Handshaking

- It has 12 handshaking interfaces.
- The burst and single transactions are supported.
- The polarity of signals can be selected.

5.1.7. Interrupt

- The correspondence of the interrupt output is one is to one CPU.
- Each channel interrupt can be enabled or disabled.
- The timing of interrupt generation is programmable in each channel (when block transfer is completed, when DMA forwarding is completed, and when error occurs).
- Masking can be individually set to each interrupt.

5.2. Description

5.2.1. Transfer Hierarchy

The hierarchy of the memory transfer is shown below.

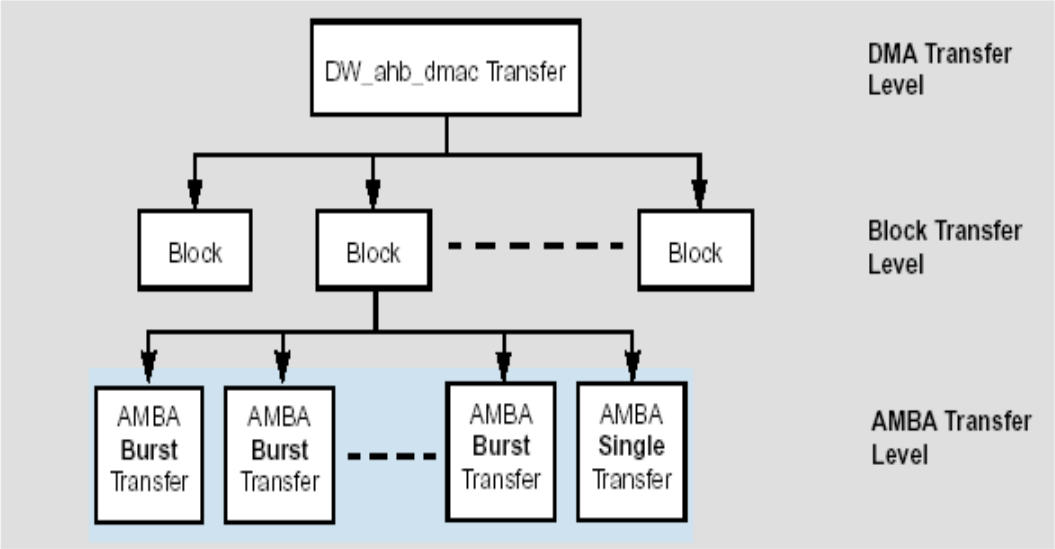


Figure 21. Memory DMA Forwarding Hierarchy Chart

- One DMA transfer level is divided into a single, two, or more block transfers.
- One block transfer is divided into AMBA burst and AMBA single transfer level.
- The block transfer becomes a basic unit of transfer on the programming.
- The transfer method can be set at every block.
- Block length is at maximum when transfering data.

The hierarchy of the peripheral transfer is shown below.

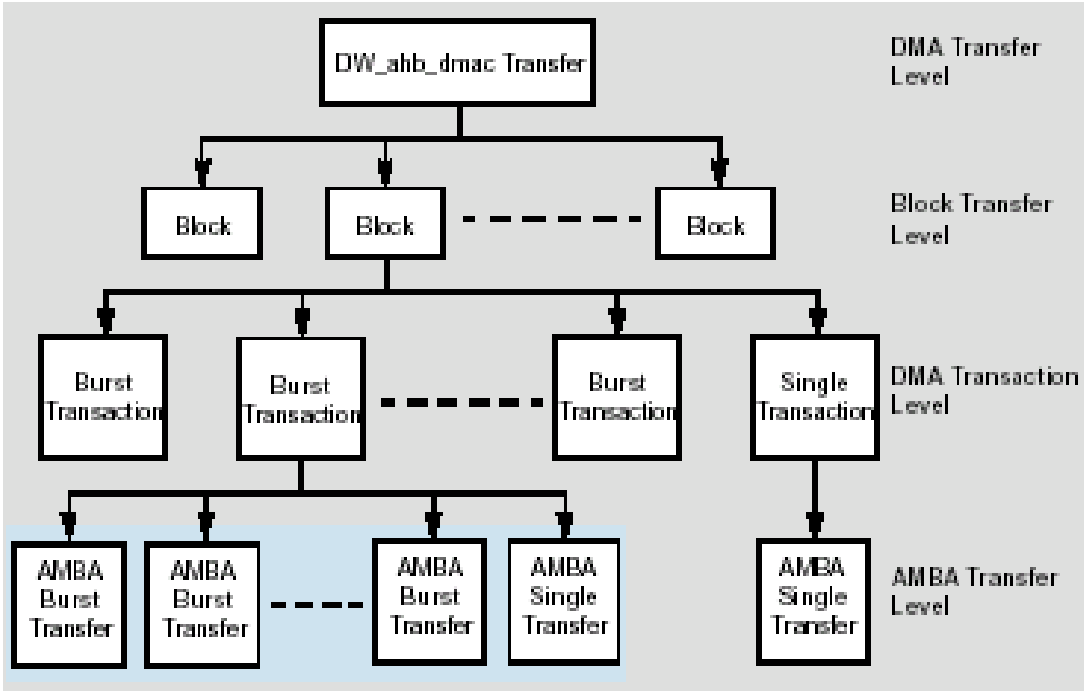


Figure 22. Peripheral DMA Transfer Hierarchy Chart

-

- One DMA transfer level is divided into single, two, or more block transfers.
- One block transfer is divided into burst transaction and single transaction.
- One transaction is divided into AMBA burst and AMBA single transfer.
- The block transfer becomes a basic unit of transfer on the programming.
- The transfer method can be set at every block.
- Block length is at maximum when transferring data.

- Multi block Transfer
  There are three methods of block transfer. Method used, as well as the transfer source and destination can be freely selected. These can be selected freely at each transfer source and transfer destination.

1. Block Chaining by Linked List

The transfer method of the construction of linked list (LLI) in the memory
The linked list is a set of registers necessary for transfer setting. The first address of the linked list, the transfer control register, and the next block (linked list pointer) are included in the linked list at the transfer source and transfer destination.

Linked List Enable is executed when the block transfer ends. If the linked list pointer is set to values other than "0x0" by "1", the transfer of the next block is executed. The linked list is read from the address where DMAC is set to the address where linked list pointer is automatically set before the block transfer begins. When set to this mode, the address register at the transfer source register and transfer destination, the forwarding control register, and the linked list pointer register are rewritten, and the block transfer is initiated.

When the link of the final block is listed, the linked list pointer ends the DMA transfer by setting linked list enable of the control register "0" again.

The allocation of the address of the linked list and the image chart of the block chaining are shown in next page.
Software constructs the linked list only in the necessary memory space, and sets the linked list block link enable. Afterwards, the head of the linked list is loaded when the channel is enabled, and the multi block transfer starts.

The image chart of the linked list is shown below.

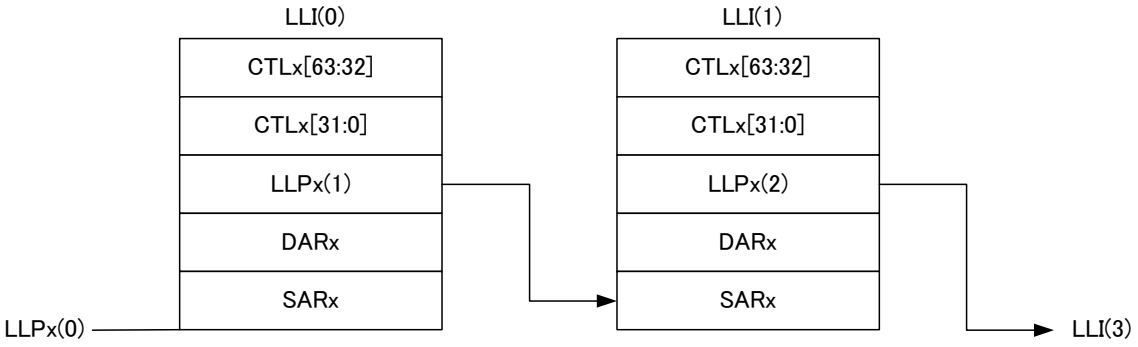


Figure 23. Block Chaining by Linked List

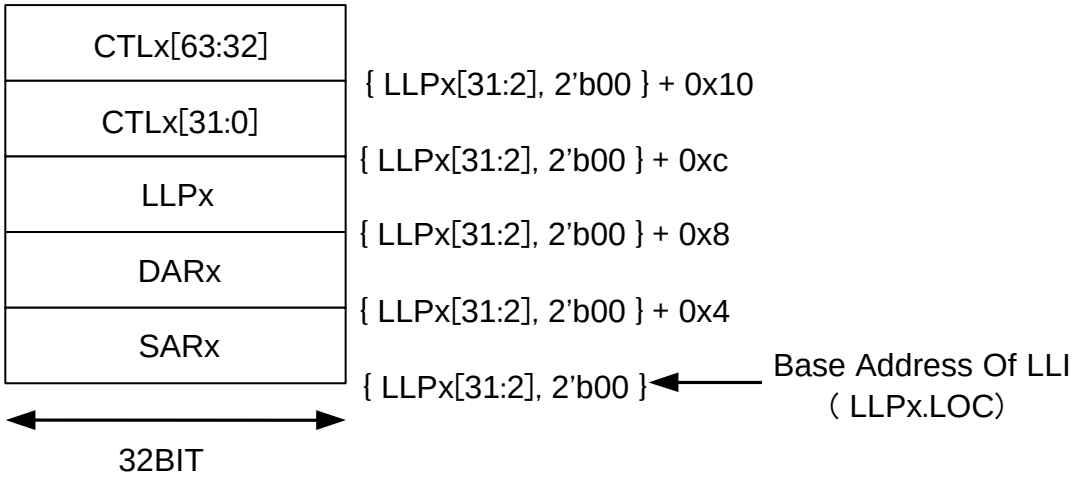


Figure 24. Linked List Address Allocation

2. Address Automatic Reload

When set to this mode, the address at the beginning of block transfer is automatically reloaded when block transfer ends.
Software clears enable signal and set the register address automatic reload before beginning to transfer the final block. Afterwards, DMA transfer is finished. As for this mode alone, transfer of the next block is not executed until the block transfer ends and interrupt is cleared with software (When block transfer ends, interrupt is effective). When final block transfer end interrupt signal is set, automatic reload enable bit is cleared.

3. Transfer to Continuous Address

Transfer to Consecutive Addresses
Both these modes cannot be selected in the multi block transfer at the transfer source and transfer destination. Use either block chaining or automatic reload.
When transfer operation is exeuted on both the transfer souce and transfer destination to consecutive addresses, enlarge the block length and execute a single block transfer. When transferring to a continuous address where the maximum block length is exceeded, either set the continuous address by block chaining or execute a single block transfer two or more times.

The image chart of three kinds of multi block transfers is shown below.

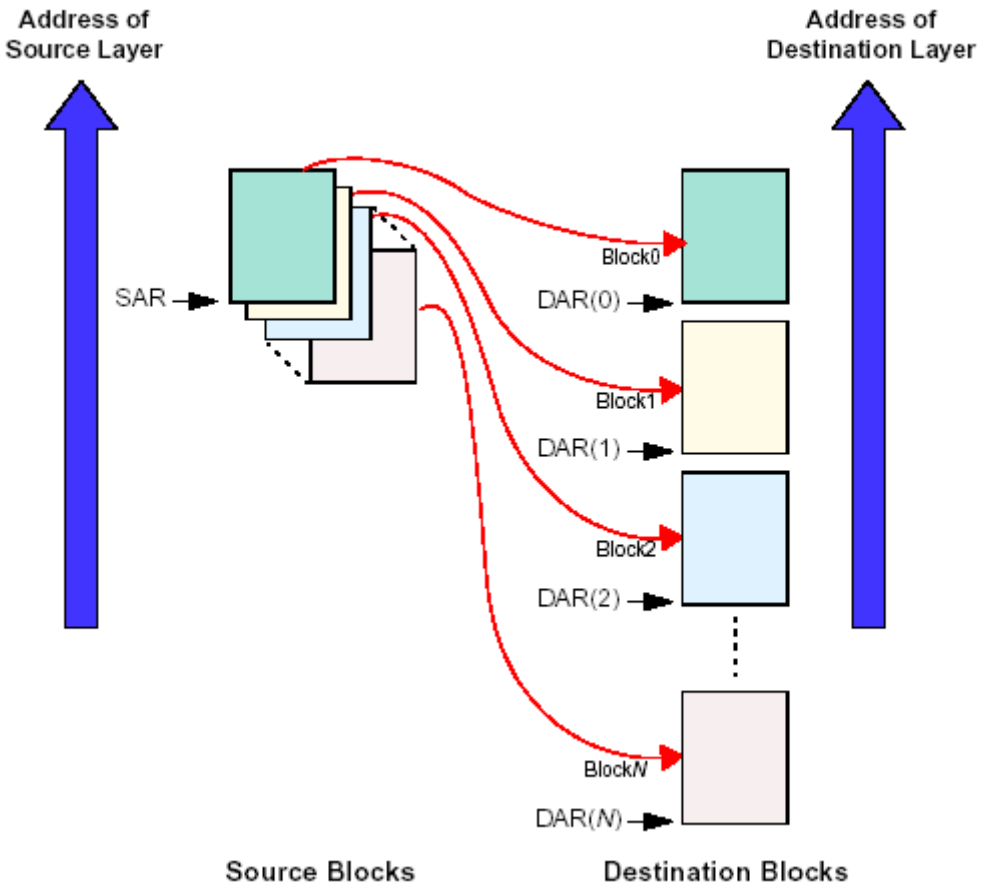


Figure 25. For the linked list block link at the forwarding former automatic operation reload and forwarding destination

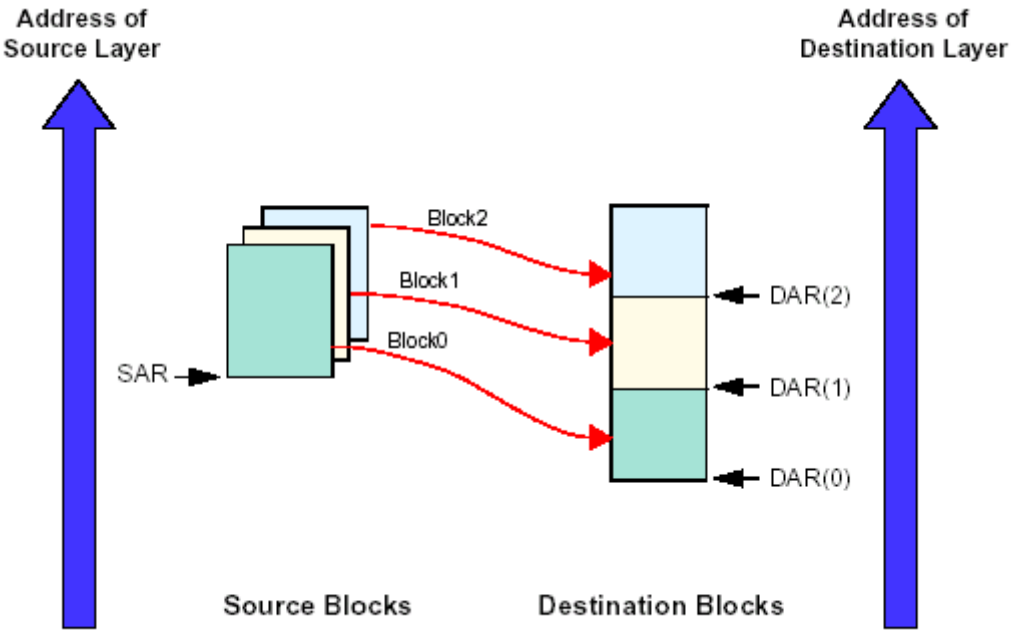


Figure 26. For a continuous address at the forwarding former automatic operation reload and forwarding destination

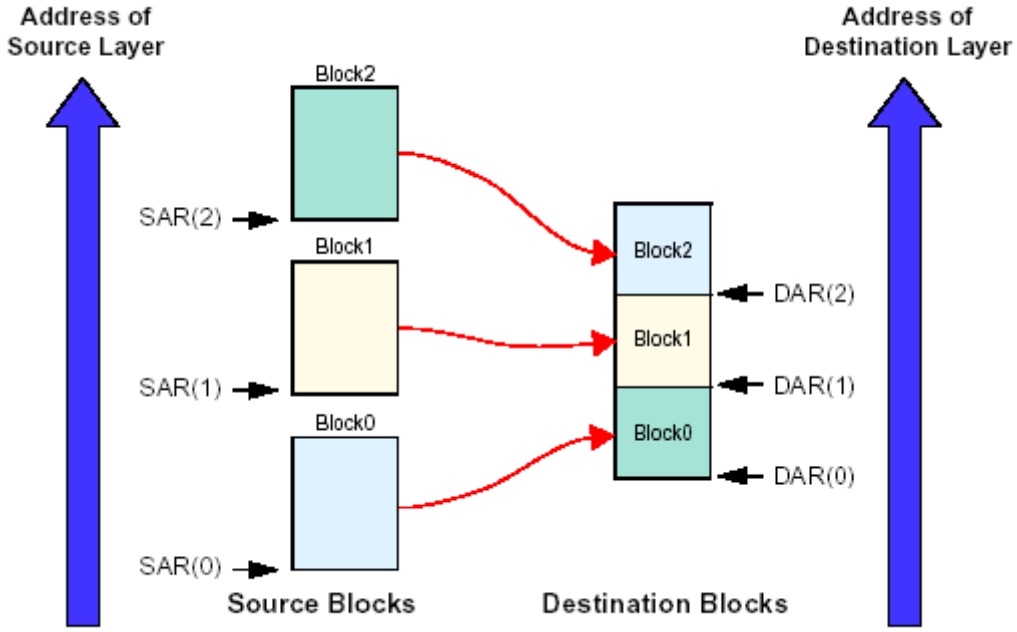


Figure 27. For a continuous address at the forwarding former linked list block link and forwarding destination

5.2.2. Handshaking Interface

The allocation of the handshake interface is as shown in the following table.
The interface of I2C and MMC can be switched with MODE_SEL.

Handshake Interface No	Peripheral
0	UART0 (Transmission)
1	UART0 (Reception)
2	UART1 (Transmission)
3	UART1 (Reception)
4	SSI_M (Transmission)
5	SSI_M (Reception)
6	SSI_S (Transmission)
7	SSI_S (Reception)
8	I2C0 (Transmission)
9	I2C0 (Reception)
10	I2C1 (Transmission)
11	I2C1 (Reception)

5.2.3. Transfer Using Handshaking

Transfer using handshaking signal
Device has 12 handshaking interfaces, and transfer in each channel are programmable.
At this time, the channel, dma_req from the peripheral and dma_single are enabled.
The device waits. The burst transaction of the length set by dma_req is forwarded, and a single transaction is forwarded by dma_single. dma_ack is returned from DMAC at the end of each transfer transaction.
dma_finish is returned from DMAC at the end of the block transfer.
DMAC becomes a flow controller, and flow is controlled (beginning and end of transfer).

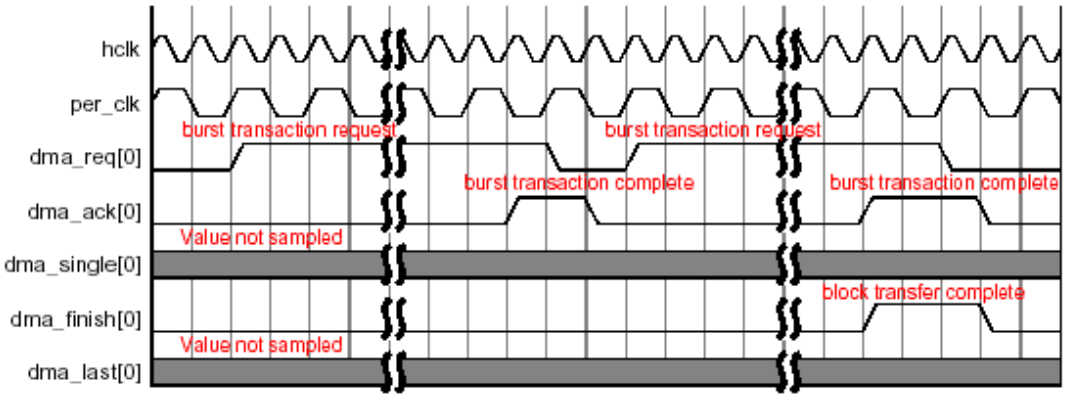


Figure 28. Burst Transfer Transaction (When DMAC is a flow controller.)

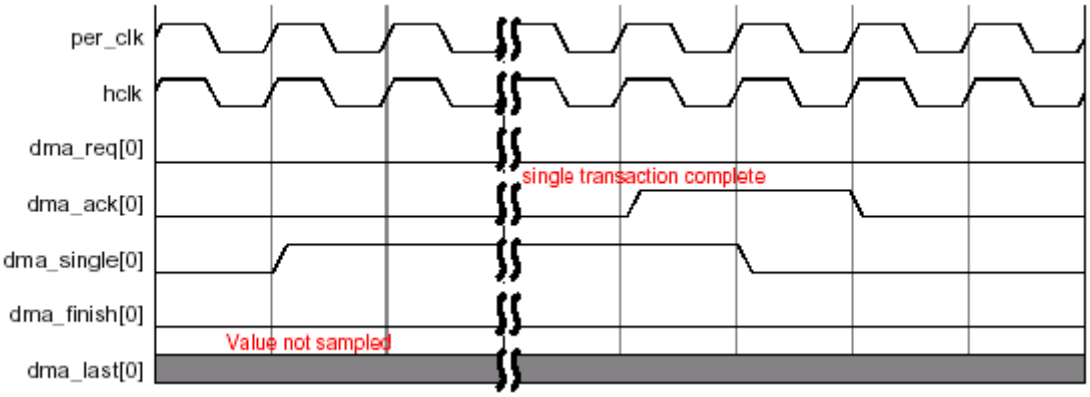


Figure 29. Single Transfer Transaction (DMAC is a flow controller.)

5.3. I/O Signal

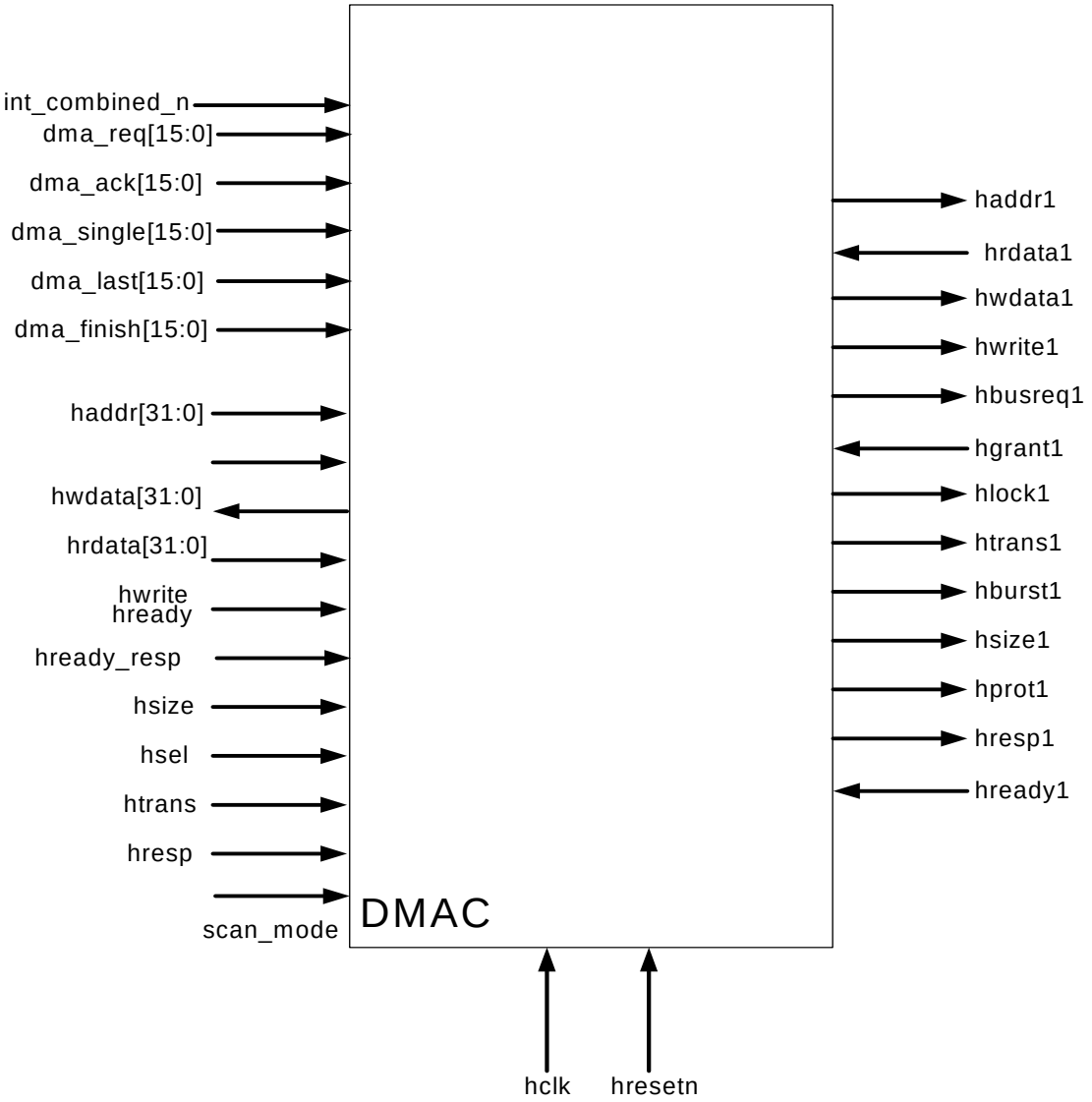


Figure 30. DMAC Module

Terminal List of DMAC Module

Terminal Name	I/O	Description	Connection
hclk	IN	AHB Clock	Clock Gen
hresetn	IN	AHB Reset	Reset Gen
haddr[31:0]	IN	AHB Address	AHB
Hwdata[31:0]	IN	AHB Write Data	AHB
hready	IN	AHB Enable Signal	AHB
hready_resp	OUT	AHB Enable Signal	AHB
hresp	OUT	AHB Response Signal	AHB
hrdata[31:0]	OUT	AHB Read Data	AHB
hsel	IN	AHB Peripheral Selection Signal	AHB
hwrite	IN	AHB Write Signal	AHB
hsize	IN	AHB Transfer Size	AHB
htrans	IN	AHB Transfer Control	AHB
haddrN	OUT	AHB Address	AHB
burstN	OUT	AHB Burst	AHB
hbusreqN	OUT	AHB Bus Request	AHB
hgrantN	IN	AHB Grant	AHB
hlockN	OUT	AHB Bus Lock	AHB
hprotN	OUT	AHB Protection Mode	AHB
hrdataN[31:0]	IN	AHB Read Data	AHB
hreadyN	IN	AHB Enable Signal	AHB
hrespN	IN	AHB Response Signal	AHB
hsizeN	OUT	AHB Transfer Size	AHB
htransN	OUT	AHB Transfer Control	AHB
hwdataN[31:0]	OUT	AHB Write Data	AHB
hwriteN	OUT	AHB Write Signal	AHB
int_combined_n	OUT	DMAC Interrupt (Active Low)	ICTL
dma_ack[15:0]	OUT	DMA Acknowledge	Each block
dma_req[15:0]	IN	DMA Request	Each block
dma_finish[15:0]	OUT	DMA Completion Signal	OPEN
dma_single[15:0]	IN	DMA Single Request	Each block
dma_last[15:0]	IN	DMA Last	L fixation
scan_mode	IN	Scanning Mode Input	TESTDEC

5.4. Register

5.4.1. Memory Map

Name	Description	Address Offset	Width	Reset
SAR0	Channel 0 Source Address Register	0x000	64	0x0
DAR0	Channel 0 Destination Address Register	0x008	64	0x0
LLP0	Channel 0 LLP Address Register	0x010	64	0x0
CTL0	Channel 0 Control Register	0x018	64	0x0000000200004824
CFG0	Channel 0 Configuration Register	0x040	64	0x0000000400000c00
SAR1	Channel 1 Source Address Register	0x58	64	0x0
DAR1	Channel 1 Destination Address Register	0x60	64	0x0
LLP1	Channel 1 LLP Address Register	0x68	64	0x0
CTL1	Channel 1 Control Register	0x70	64	0x0000000200004824
CFG1	Channel 1 Configuration Register	0x98	64	0x0000000400000c20

Memory Map – continued

Name	Description	Address Offset	Width	Reset
RawTrf	Raw Status for IntTrf Interrupt	0x2c0	64	0x0
RawBlock	Raw Status for IntBlock Interrupt	0x2c8	64	0x0
RawSrcTran	Raw Status for IntSrcTran Interrupt	0x2d0	64	0x0
RawDstTran	Raw Status for IntDstTran Interrupt	0x2d8	64	0x0
RawErr	Raw Status for IntErr Interrupt	0x2e0	64	0x0
StatusTrf	Status for IntTrf Interrupt	0x2e8	64	0x0
StatusBlock	Status for IntBlock Interrupt	0x2f0	64	0x0
StatusSrcTran	Status for IntSrcTran Interrupt	0x2f8	64	0x0
StatusDstTran	Status for IntDstTran Interrupt	0x300	64	0x0
StatusErr	Status for IntErr Interrupt	0x308	64	0x0
MaskTrf	Mask for IntTrf Interrupt	0x310	64	0x0
MaskBlock	Mask for IntBlock Interrupt	0x318	64	0x0
MaskSrcTran	Mask for IntSrcTran Interrupt	0x320	64	0x0
MaskDstTran	Mask for IntDstTran Interrupt	0x328	64	0x0
MaskErr	Mask for IntErr Interrupt	0x330	64	0x0

Memory Map – continued

Name	Description	Address Offset	Width	Reset
ClearTrf	Clear Status for IntTrf Interrupt	0x338	64	0x0
ClearBlock	Clear Status for IntBlock Interrupt	0x340	64	0x0
ClearSrcTran	Clear Status for IntSrcTran Interrupt	0x348	64	0x0
ClearDstTran	Clear Status for IntDstTran Interrupt	0x350	64	0x0
ClearErr	Clear Status for IntErr Interrupt	0x358	64	0x0
StatusInt	Status for Each Interrupt Type	0x360	64	0x0
ReqSrcReg	Source Software Transaction Request Register	0x368	64	0x0
ReqDstReg	Destination Software Transaction Request Register	0x370	64	0x0
SglReqSrcReg	Source Single Transaction Request Register	0x378	64	0x0
SglReqDstReg	Destination Single Transaction Request Register	0x380	64	0x0
LstSrcReg	Source Last Transaction Request Register	0x388	64	0x0
LstDstReg	Destination Last Transaction Request Register	0x390	64	0x0
DmaCfgReg	DMA Configuration Register	0x398	64	0x0
ChEnReg	DMA Channel Enable Register	0x3a0	64	0x0
DmaIdReg	DMA ID Register	0x3a8	64	0x1
DmaTestReg	DMA Test Register	0x3b0	64	0x0

5.4.2. Register Detail

DmaCfgReg
DMA Controller Valid/Invalid Set Register
Offset: 0x398
Width: 64 bits

Bits	Direction	Reset	Description
63:1	N/A	0x0	Reserved
0	R/W	0	If "1" is written, DMAC is enabled. When "0" is written when there is an effective channel, the data is not guaranteed to be transferred.

ChEnReg
Channel Enable Register
Offset: 0x3a0
Width: 64 bits

Bits	Direction	Reset	Description
63:10	N/A	0x0	Reserved
9:8	W	0x0	CH_EN_WE [1:0] Channel Write Enable Bit
7:2	N/A	0x0	Reserved
1:0	R/W	0x0	CH_EN [1:0] Channel Enable Bits N-bit corresponds to channel N. It is possible to write to channel N only if the same bit at CH_EN_WE is set to “1”. When an effective channel is disabled, data transfer is not guaranteed to be successful.

SARx
Transfer Former Address Setting Register (x = 0 to 1)
Offset: SAR0 – 0x000 SAR1 – 0x058
Width: 64 bits

Bits	Direction	Reset	Description
63:32	N/A	0x0	Reserved
31:0	R/W	0x0	Each block transfer is set. Moreover, it is always updated according to the address control (Incri, Decri, and fixation) while transferring it. CPU cannot write on a channel when it is in use.

DARx
Transfer Destination Address Setting Register (x = 0 to 1)
Offset: DAR0 – 0x008 DAR1 – 0x060
Width: 64 bits

Bits	Direction	Reset	Description
63:32	N/A	0x0	Reserved
31:0	R/W	0x0	Each block transfer is set. Moreover, it is always updated according to the address control (Incri, Decri, and fixation) while transferring it. CPU cannot write on a channel when it is in use.

LLPx
Linked List Pointer Setting Register (x = 0 to 1)
Offset: LLP0 – 0x010 LLP1 – 0x068
Width: 64 bits

Bits	Direction	Reset	Description
63:32	N/A	0x0	Reserved
31:2	R/W	0x0	LOC The first address of the following linked list. When the multi block transfer with the linked list block is executed, DMAC automatically acquires the linked list from the address that has been set before the block transfer begun. Moreover, the linked list address is 32 bits in length, and storing is not done for two subordinate position bits. When linked list is used： “0x0” NOT included When the linked list is NOT used： “0x0” included CPU cannot write on a channel when it is in use. Setting this register makes ChEnReg effective. When setting this register, invalidate ChEnReg in the selected channel.
1:0	N/A	0x0	Reserved

CTLx
Channel Control Register (x = 0 to 1)
Offset: CTL0 – 0x018 CTL1 – 0x070
Width: 64 bits

<table>
<tr><th>Bits</th><th>Direction</th><th>Reset</th><th>Description</th></tr>
<tr><td>63:44</td><td>N/A</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>43:32</td><td>R/W</td><td>0x2</td><td>BLOCK_TS
Block Register Size Setting
Software cannot write ona channel when it is in use. The number of block data transfer is specified by SRC_TR_WIDTH x BLOCK_TS.</td></tr>
<tr><td>31:29</td><td>N/A</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>28</td><td>R/W</td><td>0x0</td><td>LLP_SRC_EN
Linked List Pointer Enable for Setting Transfer Source
If this bit is set to "1" and LLPx.LOC is not "0x0", the multi block transfer, which uses the linked list is executed.</td></tr>
<tr><td>27</td><td>R/W</td><td>0x0</td><td>LLP_DST_EN
Linked List Enable for Setting Transfer Destination
If this bit is set to "1" and LLPx.LOC is not "0x0", the multi block transfer, which uses the linked list is executed.</td></tr>
<tr><td>26:23</td><td>R/W</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>22:20</td><td>R/W</td><td>0x0</td><td>TT_FC
Transfer Type and Flow Controller's Set Registers
<table><tr><th>TT_FC</th><th>Transfer type</th><th>Flow Controller</th></tr><tr><td>000</td><td>Memory to Memory</td><td>DMAC</td></tr><tr><td>001</td><td>Memory to Peripheral</td><td>DMAC</td></tr><tr><td>010</td><td>Peripheral to Memory</td><td>DMAC</td></tr><tr><td>011</td><td>Peripheral to Peripheral</td><td>DMAC</td></tr></table></td></tr>
<tr><td>19:17</td><td>N/A</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>16:14</td><td>R/W</td><td>0x1</td><td>Burst Transaction Length of Transfer Source Setting
SRC_MSIZE
<table><tr><th>CTLx.SRC_MSIZE / CTLx.DEST_MSIZE</th><th>Number of data items to be transferred (of width CTLx.SRC_TR_WIDTH or CTLx.DST_TR_WIDTH)</th></tr><tr><td>000</td><td>1</td></tr><tr><td>001</td><td>4</td></tr><tr><td>010</td><td>8</td></tr><tr><td>011</td><td>16</td></tr><tr><td>100</td><td>32</td></tr><tr><td>101</td><td>64</td></tr><tr><td>110</td><td>128</td></tr><tr><td>111</td><td>256</td></tr></table></td></tr>
<tr><td>13:11</td><td>R/W</td><td>0x1</td><td>Burst Transaction Length of Transfer Destination Setting
DEST_MSIZE</td></tr>
</table>

CTLx – continued

Bits	Direction	Reset	Description
10:9	R/W	0x0	SINC Transfer Source Address Control Address Change Setting while Transfer Transaction 2'b00 = Increment 2'b01 = Decrement 2'b1x = Fixed
8:7	R/W	0x0	DINC Transfer Destination Address Control Address Change Setting while Transfer Transaction 2'b00 = Increment 2'b01 = Decrement 2'b1x = Fixed
6:4	R	0x2	SRC_TR_WIDTH Data Width at Transfer Source The mapping is done by "Hsize" of AHB. 3'b010: 32 bits
3:1	R	0x2	DST_TR_WIDTH Data Width at Transfer Destination The mapping is done by "Hsize" of AHB. 3'b010: 32 bits
0	R/W	0x1	INT_EN Interrupt Enable Bit If this bit is set to "1", interrupt is enabled.

CFGx
Channel Configuration Register (x = 0 to 1)
Offset: CFG0 – 0x040 CFG1 – 0x098
Width: 64 bits

Bits	Direction	Reset	Description
63:47	N/A	0x0	Reserved
46:43	R/W	0x0	DEST_PER Connected to Handshaking Interface Please allocate only one transfer transaction in one handshaking interface.
42:39	R/W	0x0	SRC_PER Connected to Handshaking Interface Please allocate only one transfer transaction in one handshaking interface.
38:37	N/A	0x0	Reserved
36:34	R/W	0x1	PROTCTL Driven AMBA HPROT Signal 1'b1: HPROT[0] PROTCTL[1]: HPROT[1] PROTCTL[2]: HPROT[2] PROTCTL[3]: HPROT[3]
33	R/W	0x0	FIFO_MODE Sets whether to execute transfer transaction after a certain value of data or until FIFO becomes empty 0: Device executes single AMBA transfer transaction even once. 1: Device waits until half of FIFO becomes empty before transferring data. Setting this bit to "1" raises the bus efficiency by doing burst transfer as much as possible.
32	R/W	0x0	FCMODE When the transfer destination is a flow controller, this bit dictates when to do get data from the transfer source. 0: Data is previously fetched without waiting for the request at the transfer destination. 1: After the request at the transfer destination is set, data is acquired from the transfer source. Because this bit is a flow controller, DMAC is not related.
31	R/W	0x0	RELOAD_DST Reload Enable of Transfer Destination Address When this bit is set to "1", device automatically reloads value on address register (DARx) when block transfer begins at the transfer destination.
30	R/W	0x0	RELOAD_SRC Reload Enable of Transfer Source Address When this bit is set to "1", device automatically reloads value on address register (SARx) when block transfer ends at the transfer source.
29:20	N/A	0x0	Reserved
19	R/W	0x0	SRC_HS_POL Polarity Selection of Transfer Source Handshaking Signal 0: Active High 1: Active Low
18	R/W	0x0	DST_HS_POL Polarity Selection of Transfer Destination Handshaking Signal 0: Active High 1: Active Low
17	R/W	0x0	LOCK_B While signal is set to "1", Hlock is asserted and the bus is locked for the period with LOCK_B_L.
16	R/W	0x0	LOCK_CH While signal is set to "1", channel arbitration in DMAC master interface is disabled for the period with LOCK_CH_L.

CFGx – continued

Bits	Direction	Reset	Description
15:14	R/W	0x0	Period of Bus Lock by LOCK_B 00: Until DMA Transfer Completion 01: Until Block Transfer Completion 1x: Until Transaction Completion
13:12	R/W	0x0	Period of Channel Lock by LOCK_CH 00: Until DMA Transfer Completion 01: Until Block Ttransfer Completion 1x: Until Transaction Completion
11	R/W	0x1	HS_SEL_SRC Transfer Source Handshaking Setting 0: Hardware Handshaking 1: Software Handshaking When the transfer source is a memory, this bit is disregarded.
10	R/W	0x1	HS_SEL_DST Transfer Destination Handshaking Setting 0: Hardware Handshaking 1: Software Handshaking When the transfer destination is a memory, this bit is disregarded.
9	R	0x0	FIFO_EMPTY 0: FIFO is empty. 1: There is data in FIFO.
8	R/W	0x0	CH_SUSP When this bit is “1”, the data reading from the transfer source is interrupted until the bit is cleared. The data that remains in FIFO is transmitted at the transfer destination. It is equivalent to FIFO_EMPTY after transfer is interrupted. Disabling of the channel becomes possible by setting this bit to “0” without data loss.
7:5	R/W	Channel Number	CH_PRIOR Setting of Channel Used in Arbitration in the Master Interface The value of 0-5 is set for six channels. "0" becomes the lowest priority. As the channel number rises, priority level rises.
4:0	N/A	0x0	Reserved

RawTrf, RawBlock, RawSrcTran, RawDstTran, RawErr
Interrupt Factor Status Register
Offset: RawTrf ----- 0x2c0
RawBlock --- 0x2c8
RawSrcTran – 0x2d0
RawDstTran – 0x2d8
RawErr ----- 0x2e0
Width: 64 bits

Bits	Direction	Reset	Description
63:2	N/A	0x0	Reserved
1:0	R	0x0	If the interrupt factor is active, "1" is read from the corresponding bit. RawTrf: DMA Transfer End Interrupt RawBlock: Block Transfer End Interrupt RawSrcTran: Transfer Source Transaction End Interrupt RawDstTran: Transfer Destination Transaction End interrupt RawErr: When error occurs

StatusTrf, StatusBlock, StatusSrcTran, StatusDstTran, StatusErr
Interrupt Factor Enable Status Register
Offset: StatusTrf ----- 0x2e8
StatusBlock --- 0x2f0
StatusSrcTran – 0x2f8
StatusDstTran – 0x300
StatusErr ----- 0x308
Width: 64 bits

Bits	Direction	Reset	Description
63:2	N/A	0x0	Reserved
1:0	R	0x0	If the interrupt factor is active, and if the interrupt is enabled, "1" is read from the corresponding bit. StatusTrf: DMA Transfer End Interrupt StatusBlock: Block Transfer End Interrupt StatusSrcTran: Transfer Source Transaction End Interrupt StatusDstTran: Transfer Destination Transaction End Interrupt StatusErr: When error occurs

MaskTrf, MaskBlock, MaskSrcTran, MaskDstTran, MaskErr
Interrupt Mask Setting Register
Offset:MaskTrf ----- 0x310
MaskBlock --- 0x318
MaskSrcTran – 0x320
MaskDstTran – 0x328
MaskErr ----- 0x330
Width:64 bits

Bits	Direction	Reset	Description
63:10	N/A	0x0	Reserved
9:8	W	0x0	INT_MASK_WE INT_MASK Write Enable
7:2	N/A	0x0	Reserved
1:0	R/W	0x0	INT_MASK Interrupt Mask Setting Bit N-bit correspondsto channel N. It is only possible to write to these bits if INT_MASK_WE is “1”. 0: Masked 1: Unmasked MaskTrf: DMA Transfer End Interrupt MaskBlock: Block Transfer End Interrupt MaskSrcTran: Transfer Source Transaction End Interrupt MaskDstTran: Transfer Destination Transaction End Interrupt MaskErr: When error occurs

ClearTrf, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr
Interrupt Factor Clear Register
Offset: ClearTrf ----- 0x338
ClearBlock --- 0x340
ClearSrcTran – 0x348
ClearDstTran – 0x350
ClearErr ----- 0x358
Width: 64 bits

Bits	Direction	Reset	Description
63:2	N/A	0x0	Reserved
1:0	W	0x0	When corresponding bit is set to “1”, corresponding interrupt factors are cleared. ClearTrf: DMA Transfer End Interrupt ClearBlock: Block Transfer End Interrupt ClearSrcTran: transfer Source Transaction End Interrupt ClearDstTran: Transfer Destination Transaction End Interrupt ClearErr: When error occurs

StatusInt
Interrupt Output Register
Offset: 0x360
Width: 64 bits

Bits	Direction	Reset	Description
63:5	N/A	0x0	Reserved
4	R	0x0	ORed Bits of StatusErr Register
3	R	0x0	ORed Bits of StatusDstTtan Register
2	R	0x0	ORed Bits of StatusSrcTtan Register
1	R	0x0	ORed Bits of StatusBlock Register
0	R	0x0	ORed Bits of StatusTrf Register

ReqSrcReg
Transfer Source Transaction Request Register
Software drives dma_req in the set handshaking interface.
Offset: 0x368
Width: 64 bits

Bits	Direction	Reset	Description
63:10	N/A	0x0	Reserved
9:8	W	0x0	SRC_REQ_WE SRC_REQ Write Enable
7:2	N/A	0x0	Reserved
1:0	R/W	0x0	SRC_REQ Transfer Source Request Bit N-bit corresponds to channel N. It is only possible to write to these bits when SRC_REQ_WE is set to “1”. When software handshaking of the specified channel is disabled, these bits are disregarded. Bits are NOT writable if corresponding bits of SRC_REQ_WE is “0”.

ReqDstReg
Transfer Destination Transaction Request Register
Software drives dma_req in the set handshaking interface.
Offset: 0x370
Width: 64 bits

Bits	Direction	Reset	Description
63:10	N/A	0x0	Reserved
9:8	W	0x0	DST_REQ_WE DST_REQ Write Enable
7:2	N/A	0x0	Reserved
1:0	R/W	0x0	DST_REQ Transfer Destination Request Bit N-bit corresponds to channel N. It is only possible to write to these bits when DST_REQ_WE is set to “1”. When software handshaking of the specified channel is disabled, these bits are disregarded. Bits are NOT writable if corresponding bits of DST_REQ_WE is “0”.

SglReqSrcReg
Transfer Source Single Transaction Request Register
Software drives dma_single in the set handshaking interface.
Offset: 0x378
Width: 64 bits

Bits	Direction	Reset	Description
63:10	N/A	0x0	Reserved
9:8	W	0x0	SRC_SGLREQ_WE SRC_SGLREQ Write Enable
7:2	N/A	0x0	Reserved
1:0	R/W	0x0	SRC_SGLREQ Transfer Source Single Request Bit N-bit corresponds to channel N. It is only possible to write to these bits when SRC_SGLREQ_WE is set to “1”. When software handshaking of the specified channel is disabled, these bits are disregarded.

SglReqDstReg
Transfer Destination Single Transaction Request Register
Software drives dma_single in the set handshaking interface.
Offset: 0x380
Width: 64 bits

Bits	Direction	Reset	Description
63:10	N/A	0x0	Reserved
9:8	W	0x0	DST_SGLREQ_WE DST_SGLREQ Write Enable
7:2	N/A	0x0	Reserved
1:0	R/W	0x0	DST_SGLREQ Transfer Destination Single Request Bit N-bit corresponds to channel N. It is only possible to write to these bits when DST_SGLREQ_WE is set to “1”. When software handshaking of the specified channel is disabled, these bits are disregarded..

LstSrcReg
Transfer Source Transaction Request Register
Software drives dma_last in the set handshaking interface. When DMAC is a flow controller, this register is not used.
Offset: 0x388
Width: 64 bits

Bits	Direction	Reset	Description
63:0	N/A	0x0	Reserved

LstDStReg
Transfer Destination Transaction Request Register
Software drives dma_last in the set handshaking interface. When DMAC is a flow controller, this register is not used.
Offset: 0x390
Width: 64 bits

Bits	Direction	Reset	Description
63:0	N/A	0x0	Reserved

DmaTestReg
DMAC Test Mode Register
Static test mode/normal mode switch register in the AHB slave interface.
Offset: 0x3b0
Width: 64 bits

Bits	Direction	Reset	Description
63:1	N/A	0x0	Reserved
0	R/W	0x0	TEST_SLV_IF The slave interface enters the static test mode when this bit is set to "1". The value read from the register reaches the value written without fail in the static test mode. As a result, register Read/Write test becomes possible.

6. GPIO0/GPIO1

6.1. Feature

- It functions as AMBA-APB slave device.
- The width of the bus of APB is 32 bits.
- It corresponds to the Little-Endian.
- It has the data register and the I/O polarity control register for all bits of all ports.
- It corresponds to the gpio_debounce function for interrupt.
- It corresponds to the interrupt output.
- The interrupt output is outputted by integrated signals in one bit.
- The polarity of the interrupt output is active low.
- The level type and the edge type can be selected individually for each input to the interrupt. Moreover, the selection of active low and active high is also possible.

The state of each port in the initial state (After it resets it) is as follows.
Input and Software Control Mode

6.2. Description

6.2.1. Data Flow and Data Control

Block Description of the part GPIO is shown as follows.

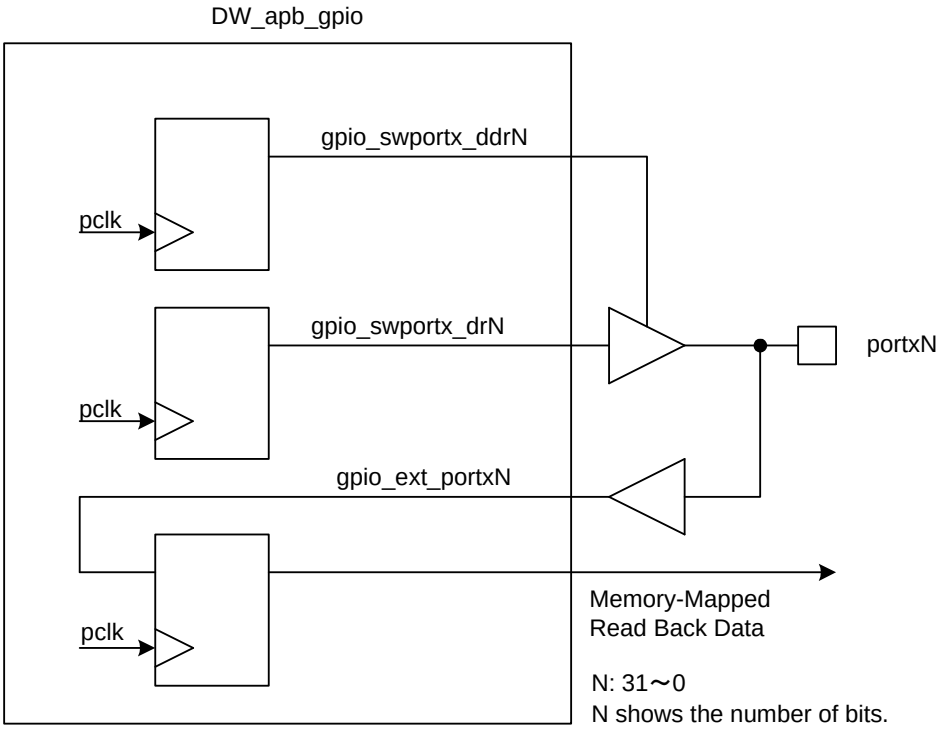


Figure 31. GPIO Block Chart

- The I/O polarity of external I/O pad is controlled.
- It is also possible to read the value of external I/O pad from the register allocated to the memory map.
- The I/O polarity of external I/O can be set according to the gpio_swportx_ddr register.
- The output data to external I/O is set according to the gpio_swportx_dr register.
- Input data from external I/O is from gpio_ext_portx register, which is possible to read.
- It is possible to read from gpio_ext_portx register regardless of control mode.

6.2.2. Interrupt Output

Device can generate the interrupt signal from an external signal.
The generation circuit of the interrupt output is shown below.

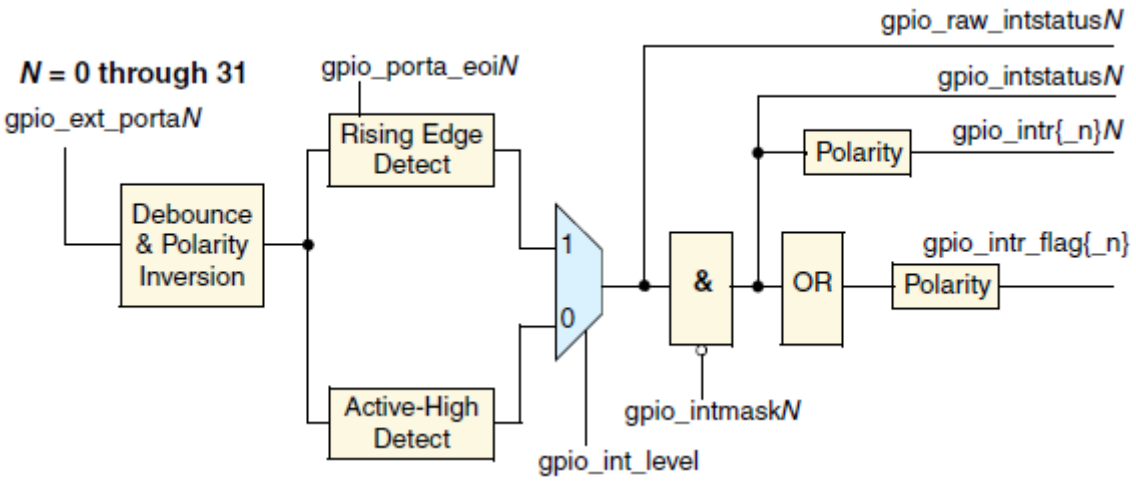


Figure 32

The interrupt is outputted by integrated signals in one bit.
The polarity of the interrupt output is active low.

As for the type of the interrupt input, the selection of the level detection method or the edge detection method is possible according to the gpio_inttype_level register.
Moreover, the selection of active low or active high is possible according to the gpio_int_polarity register.
The mask can control for the interrupt input according to the gpio_intmask register.

The following Interrupt Status can be read.
All status are active high.

- It is possible to read from gpio_rawintstatus register Interrupt status (gpio_rawintstatus) before masking.
- It is possible to read from gpio_intstatus register Interrupt status (gpio_intstatus) after masking.

6.2.3. Debounce Function

A short signal (Gritti) is deleted from an external input signal at one cycle of external debounce clock.
The debounce circuit and the timing chart chart are shown as follows.

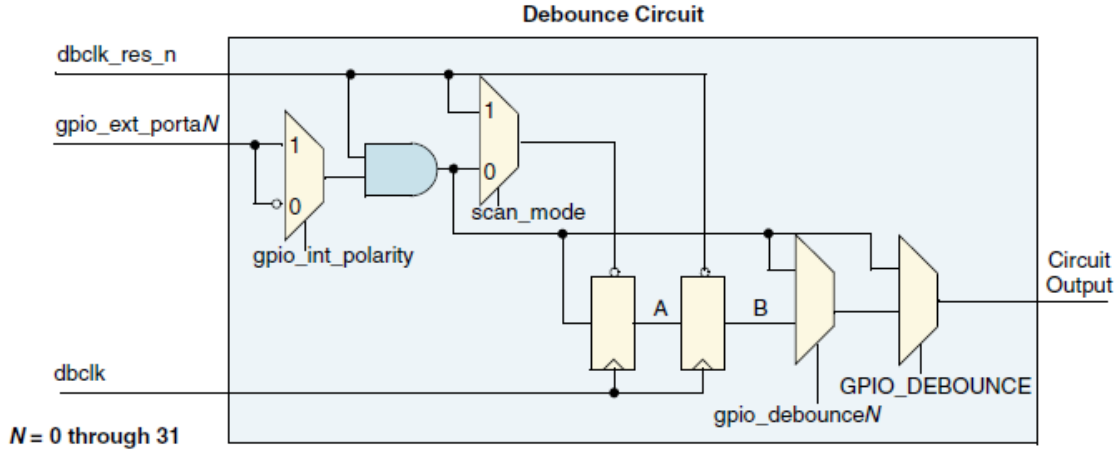


Figure 33.

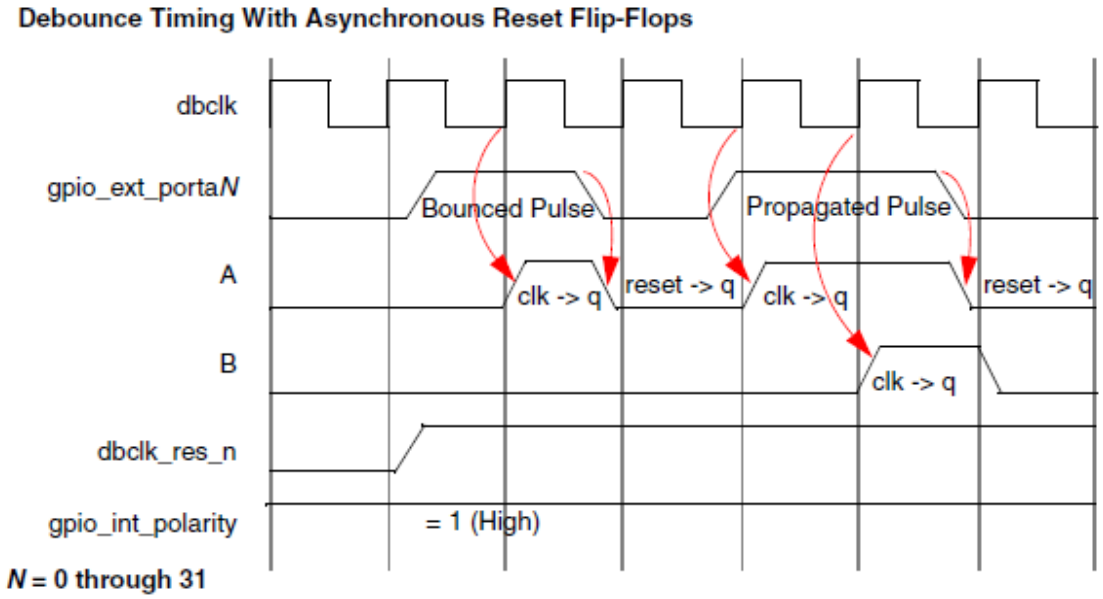


Figure 34.

It is necessary to keep device active by two debounce clock cycles, at minimum, to take the signal value when the interrupt input signal is molded with the Debounce clock.

6.3. I/O Signal

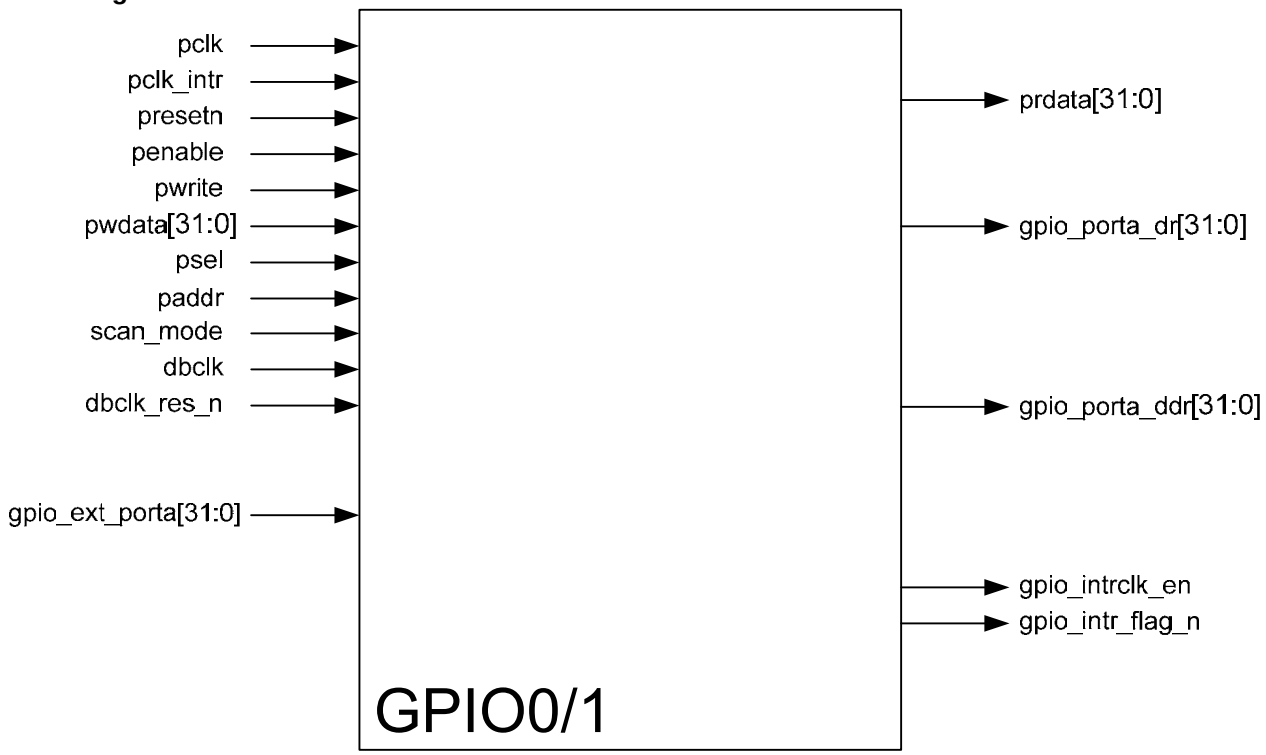


Figure 35.

Terminal List of GPIO Block

Terminal name	I/O	Description	Connection
pclk	In	APB Bus Clock	CLOCKGEN
pclk_intr	In	Interrupt Detection Clock	CLOCKGEN
present	In	APB Bus Reset (Active Low)	RESETGEN
penable	In	APB Enable.	AHB
pwrite	In	APB Write	AHB
pwdata[31:0]	In	APB Write Data	AHB
paddr[31:0]	In	APB Address	AHB
psel	In	APB Slave Selection	AHB
prdata[31:0]	Out	APB Read Data	AHB
gpio_ext_porta[31:0]	In	Data Input	IO_MUX
gpio_porta_dr[31:0]	Out	Data Output	IO_MUX
gpio_porta_ddr[31:0]	Out	Data I/O Control	IO_MUX
gpio_intrclk_en	Out	Enable Signal of Input pclk_intr When Interrupt Enable is Asserted	–
gpio_intr_n	Out	Interrupt Signal (Active Low)	ICTL
scan_mode	In	Scan Mode	TESTDEC
dbclk	In	Debounce Clock	CLOCKGEN
dbclk_res_n	In	Debounce Reset	RESETGEN

6.4. Register

6.4.1. Memory Map

Name	Address Offset	Width	Reset
gpio_swporta_dr	0x00	32	0x0000_0000
gpio_swporta_ddr	0x04	32	0x0000_0000
gpio_inten	0x30	32	0x0000_0000
gpio_intmask	0x34	32	0x0000_0000
gpio_inttype_level	0x38	32	0x0000_0000
gpio_int_polarity	0x3C	32	0x0000_0000
gpio_intstatus	0x40	32	0x0000_0000
gpio_raw_intstatus	0x44	32	0x0000_0000
gpio_debounce	0x48	32	0x0000_0000
gpio_porta_eoi	0x4C	32	0x0000_0000
gpio_ext_porta	0x50	32	0x0000_0000
gpio_ls_sync	0x60	32	0x0000_0000
gpio_id_code	0x64	32	0x0000_0000
- reserved -	0x68	–	–
gpio_ver_id_code	0x6c	32	0x3230_392A

6.4.2. Register Detail

A detailed content of the register is shown below.

gpio_swporta_dr
Output Data Setting
Offset：0x00

Bits	Name	Direction	Reset	Description
31:0	gpio_swporta_dr	R/W	0x0	Output Data When port A is in output mode, this signal is outputted.

gpio_swporta_ddr
I/O Polarity
Offset：0x04

Bits	Name	Direction	Reset	Description
31:0	gpio_swporta_ddr	R/W	0x0	I/O Polarity Setting 1: Output Mode 0: Input Mode

gpio_inten
Interrupt Enable Setting
Offset：0x30

Bits	Name	Direction	Reset	Description
31:0	gpio_inten	R/W	0x0	Interrupt Enable 0: Interrupt is disabled. 1: Interrupt is enabled.

gpio_intmask
Interrupt Mask Setting
Offset：0x34

Bits	Name	Direction	Reset	Description
31:0	gpio_intmask	R/W	0x0	Mask Interrupt Signal 0: Masking Disabled 1: Masking Enabled

gpio_inttype_level
Interrupt Input Type Setting
Offset：0x38

Bits	Name	Direction	Reset	Description
31:0	gpio_inttype_level	R/W	0x0	Interrupt Input Type 0: Level Type 1: Edge Type

gpio_int_polarity
Interrupt Input Polarity
Offset：0x3C

Bits	Name	Direction	Reset	Description
31:0	gpio_int_polarity	R/W	0x0	Interrupt Input Polarity 0: Active Low 1: Active High

gpio_intstatus
Interrupt Status
Offset：0x40

Bits	Name	Direction	Reset	Description
31:0	gpio_intstatus	R	0x0	Interrupt Status (After Masking) 0: No Interrupt 1: There is interrupt.

gpio_rawintstatus
Life Interrupt Status
Offset：0x44

Bits	Name	Direction	Reset	Description
31:0	gpio_intstatus	R	0x0	Interrupt Status (Before Masking) 0: No Interrupt 1: There is interrupt.

gpio_debounce
Debounce Function Control
Offset：0x48

Bits	Name	Direction	Reset	Description
31:0	Debounce enable	R/W	0x0	Debounce Function Control 0: Debounce function is disabled. 1: The debounce function is enabled.

gpio_porta_eoi
Life Interrupt Status
Offset：0x4C

Bits	Name	Direction	Reset	Description
31:0	gpio_porta_eoi	W	0x0	Edge Type Interrupt Clear 0: There is no operation. 1: Interrupt Cleared

gpio_ext_porta
Input Data Register
Offset：0x50

Bits	Name	Direction	Reset	Description
31:0	gpio_ext_porta	R	0x0	It is possible to write to this register when port is in input mode. When in output mode, value of data register of port A can be read and outputted.

gpio_ls_sync
Interrupt Synchronous Level Signal
Offset：0x60

Bits	Name	Direction	Reset	Description
0	gpio_ls_sync	R/W	0x0	Level Type Interrupt Synchronous Setting0 : Device outputs asynchronously. 1 : Device outputs synchronously with pclk.

gpio_id_code
GPIO Individual Code
Offset：0x64

Bits	Name	Direction	Reset	Description
31:0	gpio_id_code	R	0x0	GPIO Individual Code

gpio_ver_id_code
GPIO Version
Offset：0x6C

Bits	Name	Direction	Reset	Description
31:0	gpio_comp_version	R	0x0	GPIO Version

7. Pin Controller

7.1. Features

It controls registers settings, which switch individual pin signals between GPIO block and other blocks. These register settings are set through pin inputs. After resetting, the GPIO block is selected.

7.2. Description

7.2.1. Outline Circuit Diagram

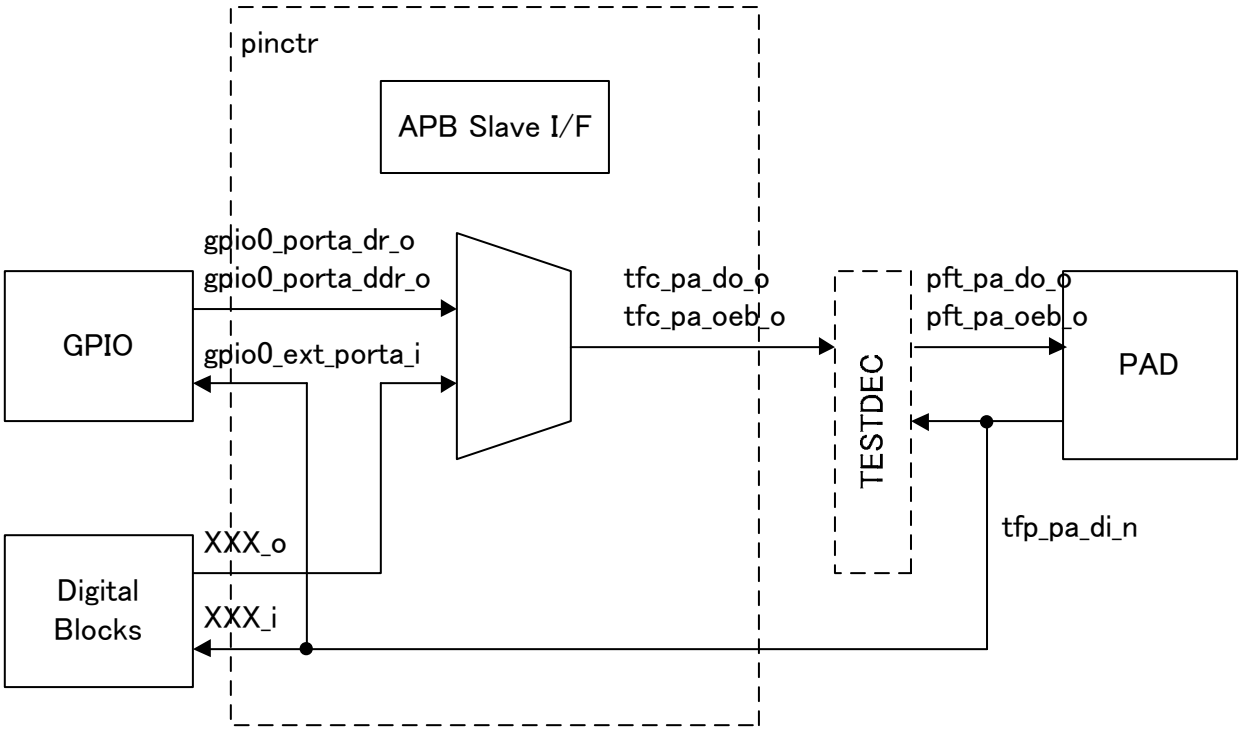


Figure 36

7.3. I/O Signals

Pin Name	I/O	Function	Destination
paddr	In	APB Address	APB
pwdata	In	APB Write Data	APB
pwrite	In	APB Write Enable	APB
penable	In	APB W/R Enable	APB
psel	In	APB Slave Select	APB
pdata	Out	APB Data Out	APB

7.4. Register

7.4.1. Memory Map

Name	AddressOffset	Width	Reset
ctr0_ pa_sel	0x00	32	0x0000_0000
ctr1_ pb_sel	0x04	32	0x0000_0000
ctr2_ pu	0x08	32	0xFFFF_FFFF
ctr3_ pu	0x0C	32	0xFFFF_FFFF
ctr4_i2s_thr	0x10	32	0x0000_0000
ctr5	0x14	32	0x0000_0000
ctr6	0x18	32	0x0000_0000
ctr7	0x1C	32	0x0000_0000
ctr8	0x20	32	0x0000_0000
ctr9	0x24	32	0x0000_0000
ctr10	0x28	32	0x0000_0000
ctr11	0x2C	32	0xFFFF_FFFF

7.4.2. Register Detail

The following section describes details of registers.

ctr0_pa_sel
GPIO0 Setting
Offset: 0x00 , Reset: 0x0

Bits	Name	Direction	Reset	Description
31:0	-	R/W	0x0	0: Connected to GPIO0 1: Connected to Individual Blocks For correspondence between bits and blocks, refer to the table shown below.

ctr1_pb_sel
GPIO1 Setting
Offset: 0x04 , Reset: 0x0

Bits	Name	Direction	Reset	Description
31:0	-	R/W	0x0	0: Connected to GPIO1 1: Connected to Individual Blocks For correspondence between bits and blocks, refer to the table shown below.

	ctr0[x]==1			ctr0[x]==0		ctr1[x]==1			ctr1[x]==0
PIN	Block	PIN NAME	I/O	GPIO	PIN	Block	PIN NAME	I/O	GPIO
2	SDIO	SD_WP	I	GPIO0[0]	84	I2S OUT	DATAO2	O	GPIO1[0]
4	SDIO	SD_CON	I	GPIO0[1]	86	FLASH	FL_DAT2	IO	GPIO1[1]
5	SDIO	SD_DAT1	IO	GPIO0[2]	87	FLASH	FL_DAT1	IO	GPIO1[2]
6	SDIO	SD_DAT0	IO	GPIO0[3]	88	FLASH	FL_CS	O	GPIO1[3]
7	SDIO	SD_CLK	O	GPIO0[4]	89	FLASH	FL_DAT3	IO	GPIO1[4]
8	SDIO	SD_CMD	O	GPIO0[5]	90	FLASH	FL_CLK	O	GPIO1[5]
9	SDIO	SD_DAT3	IO	GPIO0[6]	91	FLASH	FL_DAT0	IO	GPIO1[6]
10	SDIO	SD_DAT2	IO	GPIO0[7]	93	GPIO	GPIO10	IO	GPIO1[7]
13	GPIO	GPIO0	IO	GPIO0[8]	94	GPIO	GPIO11	IO	GPIO1[8]
14	GPIO	GPIO1	IO	GPIO0[9]	95	GPIO	GPIO12	IO	GPIO1[9]
15	GPIO	GPIO2	IO	GPIO0[10]	101	UART	UART1_RXD	I	GPIO1[10]
21	Master SIO	MSCS	I	GPIO0[11]	102	UART	UART1_TXD	O	GPIO1[11]
22	Master SIO	MSDI	I	GPIO0[12]	103	UART	UART1_RTS	O	GPIO1[12]
23	Master SIO	MSCLK	I	GPIO0[13]	104	UART	UART1_CTS	I	GPIO1[13]
24	Master SIO	MSDO	O	GPIO0[14]	105	GPIO	GPIO13	IO	GPIO1[14]
25	Slave SIO	SSCS	I	GPIO0[15]	106	GPIO	GPIO14	IO	GPIO1[15]
26	Slave SIO	SSDI	I	GPIO0[16]	107	GPIO	GPIO15	IO	GPIO1[16]
27	Slave SIO	SSCLK	I	GPIO0[17]	108	GPIO	GPIO16	IO	GPIO1[17]
28	Slave SIO	SSDO	O	GPIO0[18]	109	GPIO	GPIO17	IO	GPIO1[18]
29	GPIO	GPIO3	IO	GPIO0[19]	110	I2S IN	LRCKI1	I	GPIO1[19]
30	GPIO	GPIO4	IO	GPIO0[20]	111	I2S IN	BCKI1	I	GPIO1[20]
31	GPIO	GPIO5	IO	GPIO0[21]	112	I2S IN	DATAI1	I	GPIO1[21]
32	GPIO	GPIO6	IO	GPIO0[22]	113	I2S IN	LRCKI2	I	GPIO1[22]
72	GPIO	GPIO7	IO	GPIO0[23]	114	I2S IN	BCKI2	I	GPIO1[23]
73	GPIO	GPIO8	IO	GPIO0[24]	115	I2S IN	DATAI2	I	GPIO1[24]
74	GPIO	GPIO9	IO	GPIO0[25]	116	GPIO	GPIO18	IO	GPIO1[25]
75	I2C	SCL1	O	GPIO0[26]	117	GPIO	GPIO19	IO	GPIO1[26]
76	I2C	SDA1	IO	GPIO0[27]	118	I2C	SCL2	I	GPIO1[27]
77	I2S OUT	MCLKO1	O	GPIO0[28]	119	I2C	SDA2	IO	GPIO1[28]
81	I2S OUT	DATAO1	O	GPIO0[29]	120	RCR	RCR	IO	GPIO1[29]
82	I2S OUT	BCKO1	O	GPIO0[30]	121	UART	UART2_RXD	IO	GPIO1[30]
83	I2S OUT	LRCKO1	O	GPIO0[31]	122	UART	UART2_TXD	IO	GPIO1[31]

ctr2_pu
GPIO0 Pull Up Resistor Enable
Offset: 0x08 , Reset: 0xFFFF_FFFF

Bits	Name	Direction	Reset	Description
31:0	-	R/W	0xFFFF_FFFF	0: Off 1: On

ctr3_pu
GPIO1 Pull Up Resistor Enable
Offset: 0x0C , Reset: 0xFFFF_FFFF

Bits	Name	Direction	Reset	Description
31:0	-	R/W	0xFFFF_FFFF	0: Off 1: On

Note: I2C / FLASH pin has no built-in pull up resistor.

ctr4_i2s_thr
I2S Through Setting
Offset: 0x10 , Reset: 0x0

Bits	Name	Direction	Reset	Description
31:0	-	R/W	0x0	0: Output from I2SOUT 1: Output LRCK, BCK, and DATA signals from I2SIN CH1 to I2SOUT 2: Output LRCK, BCK, and DATA signals from I2SIN CH2 to I2SOUT

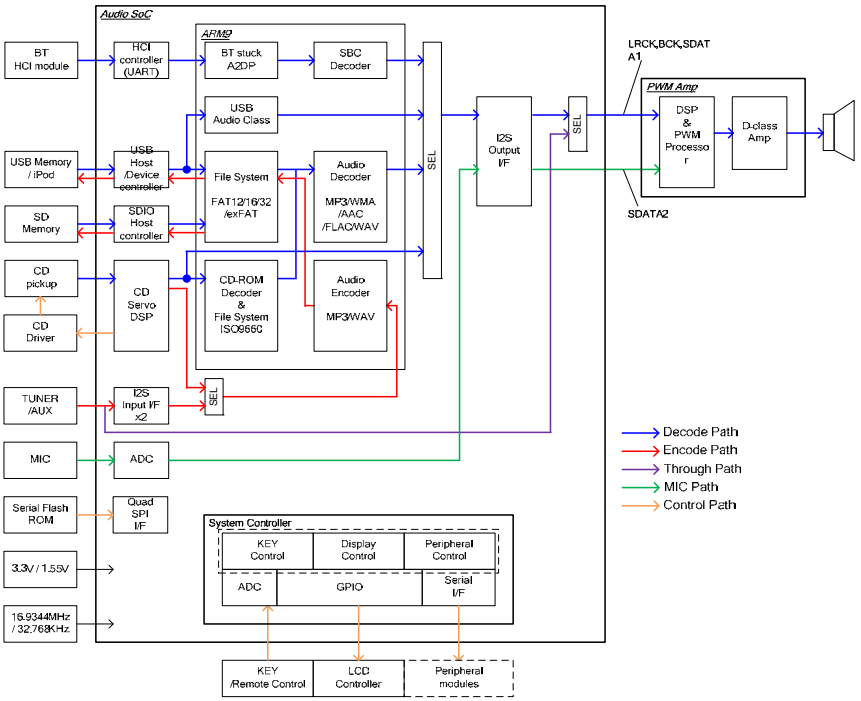


Figure 37.

8. USB 2.0 Dual Role (Host/Device) Controller

- It has built-in USB 2.0 High/Full Speed Host function.
- It has built-in USB 2.0 High/Full Speed Device function.
- It functions as AMBA-AHB slave.
- The end point is composed of 5 options as follows:
  End point0: 64 Bytes for control tranfer
  End point1: 512 Bytes for Tx transfer / 512 Bytes for Rx transfer
  End point2: 8 Bytes for Tx transfer / 64 Bytes for Rx transfer
  End point3: 8 Bytes for Tx transfer / 512 Bytes for Rx transfer
  End point4: 8 Bytes for Tx transfer
- It has built-in UTMI+Level2 interface.

8.1. Outline

8.1.1. Block Chart

The figure below shows the block chart of the USB host controller block.

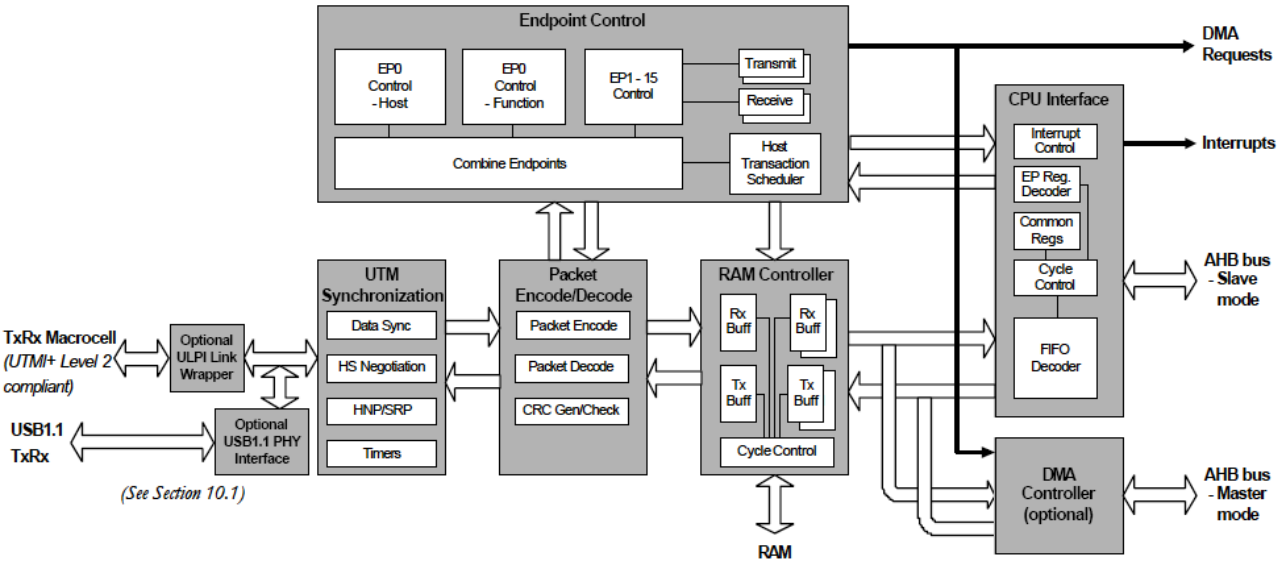


Figure 38. USB Host Controller Block

8.1.2. UTM SYNCRONIZATION

The UTM SYNCRONIZATION block synchronizes the 60MHz clock macro cell and the controller system clock block.

8.1.3. PACKET ENCODING/DECODING

The PACKET ENCODING/DECODING block does the encoding of transmitted header of the data packet to be added and the decoding of the received data packet. The CRC addition to the transmission packet and the CRC check of the reception packet are also done in this block.

8.1.4. ENDPOINT CONTROLLERS

End point 0 is for state control, while end point 1-4 is for transfer control.

8.1.5. CPU INTERFACE

It accesses CPU, control register, status register, and each end point FIFO. Moreover, this block is also responsible for the sending and receiving interrupt.

8.1.6. RAM CONTROLLER

It controls the RAM, which buffers data packets between CPU and USB. The FIFO pointer is acquired from ENDPOINT CONTROLLER. It is then converted to the RAM address pointer, and RAM access control is executed.

8.1.7. MUSBHDRC Configuration

The device has a built-in MUSBHDRC Controller Ver.2.1 made by the USB Mentor company in accordance with UTMI+Level2.
Please refer to MUSBHDRC Product Specification, Programmer 's Guide, and User Guide for details.
The table below shows the composition of the end point.

EndPoint	Description
EP0	Tx /Rx
EP1	Tx /Rx
EP2	Tx /Rx
EP3	Tx /Rx
EP4	Tx

The following table shows the CONFIGURATION setting.
MUSBHDRC CONFIG

Constant	Description	Configuration
C_NUM_EPT	Number of Tx EP (EP0 is included.)	5
C_NUM_ERR	Number of Rx EP (EP0 is included.)	4
C_EP1_DEF	EP1 is set.	Enabled
C_EP1_TX_DEF	EP1 is set to Tx EP.	Enabled
C_EP1_RX_DEF	EP1 is set to Rx EP.	Enabled
C_EP1_TOR_DEF	EP1 is shared and Tx and Rx share FIFO.	Disabled
C_EP1_TAR_DEF	EP1 is shared, but neither FIFO, Tx nor Rx is shared.	Enabled
C_EP2_xxxx	EP2	It is the same as EP1.
C_EP3_xxxx	EP3	It is the same as EP1.
C_EP4_DEF	EP4 is set.	Enabled
C_EP4_TX_DEF	EP4 is set to Tx EP.	Enabled
C_EP1T_BITS	Number of bit of byte addresses used as TxFIFO of EP1	9bit
C_EP1R_BITS	Number of bit of byte addresses used as RxFIFO of EP1	9bit
C_EP2T_BITS	Number of bit of byte addresses used as TxFIFO of EP2	3bit
C_EP2R_BITS	Number of bit of byte addresses used as RxFIFO of EP2	6bit
C_EP3T_BITS	Number of bit of byte addresses used as TxFIFO of EP3	3bit
C_EP3R_BITS	Number of bit of byte addresses used as RxFIFO of EP3	9bit
C_EP4T_BITS	Number of bit of byte addresses used as TxFIFO of EP4	3bit
C_EPxxxT_BITS	EP5-15	2 (Unused)
C_EPxxxR_BITS	EP5-15	2 (Unused)
C_HB_TX	Wideband Tx ISO	Disabled
C_HB_RX	Wideband Rx ISO	Enabled
C_VEND_REG	UTMI Vendor Control Register	Enabled
1C_VCTL_BITS	Width of UTMI of V Control Register	4
C_VSTAT_BITS	Width of UTMI of V Status Register	8
C_DMA	DMA Controller	Enabled
C_DYNFIFO_DEF	Dynamic FIFO Sizing	Disabled
C_NUM_EPS	Entire Number of EP (EP0 is included.)	5
C_EPMAX_BITS	Number of bit of maximum byte addresses of EP FIFO	8 (GUI Generation)
C_RAM_BITS	Number of bit of word addresses of RAM	9

8.1.8. USB Connect Detector

Apart from MUSBHDRC, a connection detection circuit is added to the device for the connection under Standby operation and disconnection detection.

Connect Detection

If either conn [4] or conn [6] bit is set, connection detection is enabled. USB_DP or USB_DM is monitored, and interrupt is generated at the time of connection detection. Interrupt output is ORed to MUSBHDRC interrupt.
Interrupt flag, conn [0], is set to “1” during the generation of interrupt. Interrupt flag is cleared by writing zero.
The timing diagram during a connection detection is shown in Figure 39.

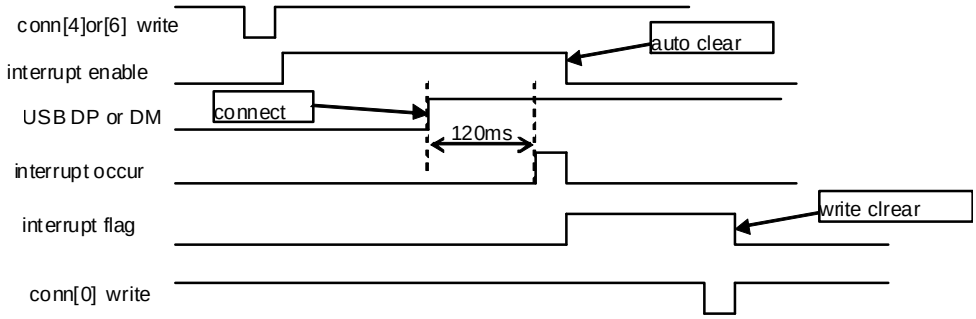


Figure 39. Connection Detection

Disconnect Detection

If either conn [5] or conn [7] bit is set, disconnection detection is enabled. USB_DP or USB_DM is monitored, and interrupt is generated at the time of disconnection detection. Interrupt output is ORed to MUSBHDRC interrupt.
Interrupt flag, conn [1], is set to “1”during the generation of interrupt. interrupt flag is cleared by writing zero.
The timing diagram during a disconnection detection is shown in Figure 40.

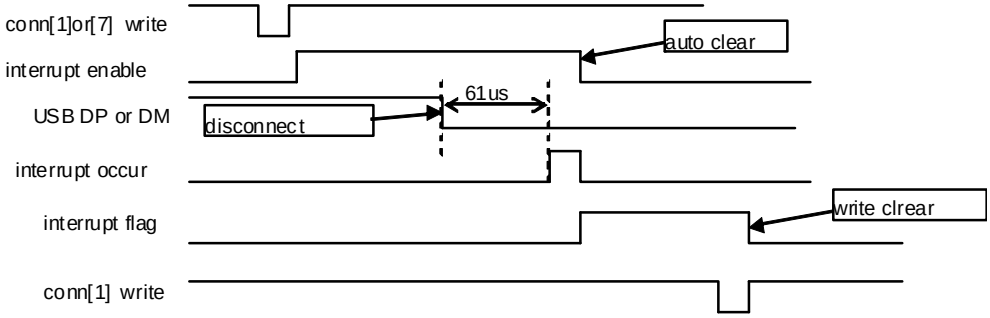


Figure 40. Disconnection Detection

.

Linestate0_latch (DP: conn [8]) and Linestate0_latch (DM: conn [9]) hold Linestate0 (DP: conn [2]) and the value of Linestate1 (DM:conn [3]) during the generation of interrupt.
The device holds it until an interrupt occurs again.

8.1.9. USB-Reset

To shift to SUSPEND mode, control signal PHY of a register from the resetgen block.

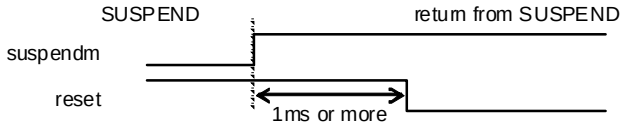


Figure 41.

Reset MUSBHDRC after device has returned from SUSPEND mode. The procedures of return from SUSPEND mode are as follows:

MUSBHDRC generates normal disconnection interrupt.
MUSBHDRC interrupt is disabled. Connection interrupt should be generated.Suspend.
USB interrupt occurs.
Check interrupt factor.
Set control signal suspendm to high.
Reset MUSBHDRC.
Wait for 1ms or more.
Control PHYRESET.
Setup MUSBHDRC again.
MUSBHDRC generates normal connection interrupt.

8.2. I/O Signals

Name	I/O	Explanation	Connection
clk_i	In	System Clock	CLKCTR
xclk_i	In	Transceiver Macro Clock	CLKCTR
usbd_clk_i	In	USB Connection Clock (32.768 kHz)	CLKCTR
usbdbus_clk_i	In	USB Connection Bus Clock (96 MHz / 32.768 kHz)	CLKCTR
ramclk_i	In	RAM Clock	CLKCTR
mrst_i	In	System Reset for musbc (Active Low)	RSTGEN
usbd_rstn_i	In	System Reset usbc_conn, usbc_cpuif, usbtest (Active Low)	RSTGEN
usbphy_rstn_i	In	PHY Input Reset	RSTGEN
phyrst_o	Out	PHY Output Reset	PHY
usb_suspendm_i	In	PHY Input Suspend	RSTGEN
suspendm_o	Out	PHY Output Suspend	PHY
linestate_i	In	Linestate	PHY
opmode_o	Out	Mode of Operation	PHY
rxdata_i	In	USB Data Bus Input	PHY
txdata_o	Out	USB Data Bus Output	PHY
txvalid_o	Out	Transmit Valid	PHY
txvalidh_o	Out	Transmit Valid High	PHY
txready_i	In	Transmit Data Ready	PHY
rxvalid_i	In	Receive Data Valid	PHY
rxvalidh_i	In	Receive Data Valid High	PHY
rxactive_i	In	Receive Active	PHY
rxerror_i	In	Receive Error	PHY
xcvrsel_o	Out	Tranceiver Select	PHY
termsel_o	Out	Termination Select	PHY
drvvbus_o	Out	Vbus Power Enable	PHY
chrgvbus_o	Out	Charge Vbus	PHY
dischrgvbus_o	Out	Discharge Vbus	PHY
hostdiscon_i	In	Device Disconnection Detect	PHY

I/O Signals – continued

Name	I/O	Explanation	Connection
dppulldown_o	Out	PullDown Resistor Enable (DP)	PHY
dmpulldowm_o	Out	Pull Down Resistor Enable (DM)	PHY
hostmode_i	In	Host Select	PHY
mode_o	Out	EHCI/OHCI Mode Switch (0: OHCI 1: EHCI)	PHY
oeb_o	Out	Output Enable	PHY
speed_o	Out	Speed Selection During OHCI Mode	PHY
vpo_o	Out	Single Ended Data Driver Input OHCI	PHY
vmo_o	Out	Single Ended Data Driver Input OHCI	PHY
vstatus_i	In	PHY Status Data	PHY
vcontrol_o	Out	PHY Control Data	PHY
vcontrollloadm_o	Out	New Control Information Read	PHY
ltest_mode_i	In	Loopback Test Enable	TESTDEC
ltest_start_i	In	Loopback Test Start	TESTDEC
ltest_end_o	Out	Loopback Test End	TESTDEC
ltest_ok_o	Out	Loopback Test Result OK	TESTDEC
hs_mode_i	In	HS-Mode Select	TESTDEC
ltest_inc_i	In	TEST_PACKT Data Select	TESTDEC
phyiddq_i	In	USB PHy IDDq Idle Mode	TESTDEC
dcotest_i	In	USB DC Output Test Mode	TESTDEC
dcotxv_i	In	USB DC Output Test Mode Txvalid	TESTDEC
dcotxd_i	In	USB DC Output Test Mode Txdata	TESTDEC
bistdone_o	Out	Memory BIST Done	TESTDEC
bistfail_i	In	Memory BIST Fail	TESTDEC
bisttest_i	In	Memory BIST Test	TESTDEC
bistclk_i	In	Memory BIST Clock	TESTDEC
bistrst_i	In	Memory BIST Reset	TESTDEC
scanmode_i	In	Scan Mode	TESTDEC
bpctr_i	In	Bypass Controller	TESTDEC
mc_nint_o	Out	CPU Interrupt	ICTL
usb_nrst_o	Out	USB Function Reset	RSTGEN
sof_pulse_o	Out	Frame Sync Pulse	PHY
powerdown_o	Out	Clock Stop to Save Power	PHY
bistret_o	Out	Memory BIST Retention	TESTDEC
bistres_i	In	Memory BIST Resume	TESTDEC
pkt_start_i	In	Test Packet Start	TESTDEC
dma_nint_o	Out	DMA Interrupt	ICTL
ahb_hsel	In	AHB HSEL	AHB
ahb_htrans	In	AHB HTRANS	AHB
ahb_hwrite	In	AHB HWRITE DATA	AHB
ahb_hsize	In	AHB HSIZE	AHB
ahb_haddr	In	AHB HADDR	AHB
ahb_hwdata	In	AHB HWDATA	AHB
ahb_hreadyi	In	AHB HREADYI	AHB
ahb_hgrant	In	AHB HGRANT	AHB
ahb_hreadymi	In	AHB HREADY Master	AHB
ahb_hrdatam	In	AHB HRDATA Master	AHB
ahb_hrespm	In	AHB HRESPM Master	AHB
ahb_hreadyo	Out	AHB HREADY Out	AHB
ahb_hrdata	Out	AHB HRDATA	AHB
ahb_hbusreq	Out	AHB HBUSREQ	AHB
ahb_htransm	Out	AHB HTRANS Master	AHB
ahb_hsizem	Out	AHB HSIZE Master	AHB
ahb_hburstm	Out	AHB HBURST Master	AHB
ahb_hwritem	Out	AHB HWRITE Master	AHB
ahb_haddrm	Out	AHB HADDR Master	AHB
ahb_hwdatam	Out	AHB HWDATA Master	AHB

8.3. Register (F8000000 Mentor USB Controller)

8.3.1. Memory Map

Please refer to MUSBHDRC Product Specification, Programmer 's Guide, and User Guide for details.

Common USB Registers

Name	Description	Address Offset	Width
FAddr	Function Address Register	00	8
Power	Power Management Register	01	8
IntrTx	Interrupt Register for Endpoint 0 Plus Tx Endpoints 1 to 15	02,03	16
IntrRx	Interrupt Register for Rx Endpoints 1 to 15	04,05	16
IntrTxE	Interrupt Enable Register for IntrTx	06,07	16
IntrRxE	Interrupt Enable Register for IntrRx	08,09	16
IntrUSB	Interrupt Register for Common USB Interrupts	0A	8
IntrUSBE	Interrupt Enable Register for IntrUSB	0B	8
Frame	Frame Number	0C,0D	16
Index	Index Register for Selecting the Endpoint Status and Control Registers	0E	8
Testmode	USB 2.0 Test ModesEnable	0F	8

Indexed Registers – Peripheral Mode
(Control Status registers for endpoint selected by the Index register when DevCtl.D2 = 0)

Name	Description	Address Offset	Width
TxMaxP	Maximum Packet Size for Peripheral Tx Endpoint (Index register set to select Endpoints 1 – 15 Only)	10,11	8
CSR0	Control Status Register for Endpoint 0 (Index register ret to relect Endpoint 0)	12,13	16
TxCSR	Control Status register for Peripheral Tx Endpoint (Index register set to select Endpoints 1 – 15)		
RxMaxP	Maximum Packet Size for Peripheral Rx Endpoint (Index register set to select Endpoints 1 – 15 only)	14,15	16
RxCSR	Control Status Register for Peripheral Rx Endpoint (Index register set to select Endpoints 1 – 15 only)	16,17	16
Count0	Number of Received Bytes in Endpoint 0 FIFO (Index register set to select Endpoint 0)	18,19	16
RxCount	Number of Bytes in Peripheral Rx Endpoint FIFO (Index register set to select Endpoints 1 – 15)		
–	Reserved.	1A–1B	16
–	Reserved.	1C–1E	16
ConfigData	Returns details of core configuration (Index register is set to Endpoint 0)	1F	8
FIFOSize	Returns configured size of the selected Rx FIFO and Tx FIFOs (Endpoints 1 – 15 only)		

Indexed Registers – Host Mode
(Control Status registers for endpoint selected by the Index register when DevCtl.D2 = 1)

Name	Description	Address Offset	Width
TxMaxP	Maximum Packet Size for Host Tx Endpoint (Index register set to select Endpoints 1 – 15 only)	10,11	8
CSR0	Control Status Register for Endpoint 0 (Index register set to select Endpoint 0)	12,13	16
TxCSR	Control Status Register for Host Tx Endpoint (Index register set to select Endpoints 1 – 15)		
RxMaxP	Maximum Packet Size for Host Rx Endpoint (Index register set to select Endpoints 1 – 15 only)	14,15	16
RxCSR	Control Status register for Host Rx Endpoint (Index register set to select Endpoints 1 – 15 only)	16,17	16
Count0	Number of Received Bytes in Endpoint 0 FIFO (Index register set to select Endpoint 0)	18,19	16
RxCount	Number of Bytes in Host Rx Endpoint FIFO (Index register set to select Endpoints 1 – 15)		
TxType	Sets the transaction protocol and peripheral endpoint number for the host Tx endpoint (Index register set to select Endpoints 1 – 15 only)	1A	8
NAKLimit0	Sets the NAK response timeout on Endpoint 0 (Index register set to select Endpoint 0)	1B	8
TxInterval	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Tx endpoint (Index register set to select Endpoints 1 – 15 only)		
RxType	Sets the transaction protocol and peripheral endpoint number for the host Rx endpoint (Index register set to select Endpoints 1 – 15 only)	1C	8
RxInterval	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Rx endpoint (Index register set to select Endpoints 1 – 15 only)	1D	8
–	Reserved.	1E	8
ConfigData	Returns details of core configuration (Index register set to select Endpoint 0.)	1F	8
FIFOSize	Returns the configured size of the selected Rx FIFO and Tx FIFOs (Endpoints 0 – 15 only)		

FIFOs

Name	Description	Address Offset	Width
EP0 FIFO	FIFOs for Endpoints 0	0x20-23	32
EP1 FIFO	FIFOs for Endpoints 1	0x24-27	32
EP2 FIFO	FIFOs for Endpoints 2	0x28-2B	32
EP3 FIFO	FIFOs for Endpoints 3	0x2C-30	32
EP4 FIFO	FIFOs for Endpoints 4	0x30-33	32

Additional Control & Configuration Registers (60h – 7Fh)

Name	Description	Address Offset	Width
DevCtl	Device Control Register	0x60	8
-	Reserved	0x61	8
VControl/ VStatus	UTMI+PHY Vendor Register	0x6A	16

DMA REGISTERS

Name	Description	Address Offset	Width
INTR	Indicates pending DMA interrupts	0x200	1
CNTL(1)	DMA Channel 1 Control: D0: DMA Enable D1: Direction: 0 = DMA Write (Rx endpoint), 1 = DMA Read (Tx endpoint) D2: DMA Mode D3: Interrupt Enable D7–4: Endpoint Number D8: Bus Error D10–9: Burst Mode 00 = Burst Mode 0 : Bursts of Unspecified Length 01 = Burst Mode 1 : INCR4 or Unspecified Length 10 = Burst Mode 2 : INCR8, INCR4 or Unspecified Length 11 = Burst Mode 3 : INCR16, INCR8, INCR4 or Unspecified Length	0x204	16
ADDR(1)	DMA Channel 1 AHB Memory Address (32 bits)	0x208	32
COUNT(1)	DMA Channel 1 Byte Count (32 bits)	0x20C	32

8.3.2. Resister Detail

Common USB Registers

FADDR

FADDR is an 8-bit register, where the 7-bit address of peripheral transaction is written. In Host mode (DevCtl.D2=1), this register stores the value of the peripheral device address sent through SET_ADDRESS command.
In Peripheral mode (DevCtl.D2=0), this register stores the address received through SET_ADDRESS command, which will then be used for decoding the function address in the subsequent token packets.
Offset: 0x00
Width: 8 bits

Bits	Name	Direction	Reset	Description
7	Unused	R	0x0	Unused, Always Returns 0
6:0	Func Addr	R/W	0x0	Function Address

POWER

POWER is an 8-bit register, which is used to control Suspend and Resume signals. Offset: 0x01
Width: 8 bits

Bits	Name	Direction	Reset	Description
7	ISO Update	R/W	0x0	When CPU set this bit to “1”, the MUSBHDRC will wait for an SOF token from the time TxPktRdy is set before sending the packet. If an IN token is received before an SOF token, then a zero length data packet will be sent. Note: This is only valid in Peripheral Mode. Also, this bit only affects endpoints performing isochronous transfers.
6	-	N/A	0x0	Unused, Always Returns 0
5	HS Enab	R/W	0x1	When CPU set this bit to “1”, the MUSBHDRC will make device operate in high-speed mode when reset. Otherwise, the device will only operate in full-speed mode.
4	HS Mode	R	0x0	When set to “1”, this read-only bit indicates that device operates in high-speed mode successfully during USB reset.
3	Reset	R	0x0	This bit is set when Reset signaling is present on the bus. Note: This bit is Read/Write from the CPU in Host Mode but Read-Only in Peripheral Mode.
2	-	R/W	0x0	Reserved
1	Suspend Mode	R	0x0	In Host mode, CPU sets this bit to “1” to enter Suspend mode. In Peripheral mode, this bit is set to “1” upon entry to Suspend mode. It is cleared when the CPU reads the interrupt register.
0	-	R/W	0x0	Reserved

INTRTX
INTRTX is a 16-bit register that shows which interrupt of TXEndpoints 1-15 is currently active. Moreover, it shows whether the interrupt of Endpoint 0 is currently active. When this register is read, all active interrupts are cleared.
Offset: 0x02
Width: 16 bits

Bits	Name	Direction	Reset	Description
15:5	-	N/A	0x0	Unused, Always returns 0
4	EP4 Tx	R	0x0	Tx Endpoint 4 Interrupt
3	EP3 Tx	R	0x0	Tx Endpoint 3 Interrupt
2	EP2 Tx	R	0x0	Tx Endpoint 2 Interrupt
1	EP1 Tx	R	0x0	Tx Endpoint 1 Interrupt
0	EP0 Tx	R	0x0	Endpoint 0 Interrupt

INTRRX
INTRRX is a 16-bit read-only register, which shows currently active interrupts of RXEndpoints 1-15. When this register is read, all active interrupts are cleared.
Offset: 0x04
Width: 16 bits

Bits	Name	Direction	Reset	Description
15:5	-	N/A	0x0	Unused, Always returns 0
4	EP4 Rx	R	0x0	Rx Endpoint 4 Interrupt
3	EP3 Rx	R	0x0	Rx Endpoint 3 Interrupt
2	EP2 Rx	R	0x0	Rx Endpoint 2 Interrupt
1	EP1 Rx	R	0x0	Rx Endpoint 1 Interrupt
0	-	N/A	0x0	Unused, Always returns 0

INTRTXE
INTRTXE is a 16-bit interrupt enable register for Endpoint 0 and TxEndpoints 1-4.
Offset: 0x06
Width: 16 bits

Bits	Name	Direction	Reset	Description
15:5	-	N/A	0x7FF	Unused, Always returns 1
4	EP4 TxE	R/W	0x1	Tx Endpoint 4 Interrupt Enable
3	EP3 TxE	R/W	0x1	Tx Endpoint 3 Interrupt Enable
2	EP2 TxE	R/W	0x1	Tx Endpoint 2 Interrupt Enable
1	EP1 TxE	R/W	0x1	Tx Endpoint 1 Interrupt Enable
0	EP0	R/W	0x1	Endpoint 0 Interrupt Enable

INTRRXE
INTRRXE is a 16-bit interrupt enable register for RxEndpoints1-4.
Offset: 0x08
Width: 16 bits

Bits	Name	Direction	Reset	Description
15:3	-	N/A	0x7FF	Unused, Always returns 1
4	EP4 RxE	R/W	0x1	Rx Endpoint 4 Interrupt Enable
3	EP3 RxE	R/W	0x1	Rx Endpoint 3 Interrupt Enable
2	EP2 RxE	R/W	0x1	Rx Endpoint 2 Interrupt Enable
1	EP1 RxE	R/W	0x1	Rx Endpoint 1 Interrupt Enable
0	-	N/A	0x0	Unused, Always returns 0

INTRUSB

INTRUSB is an 8-bit read-only register, which shows currently active USB interrupts. When this register is read, all active interrupts are cleared.
Offset: 0x0a
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:6	-	N/A	0x0	Unused, Always returns 0
5	Discon	R	0x0	In Host Mode, bit is set to “1” when a device disconnection is detected. In Peripheral Mode, bit is set to “1” when a session ends.
4	Conn	R	0x0	This bit is only valid in Host mode. It is set to “1” when a device connection is detected.
3	SOF	R	0x0	This bit is set to “1” at the beginning of each frame.
2	Babble/Reset	R	0x0	In Host Mode, bit is set to “1” when babble is detected. *Note:* Only active after first SOF has been sent. In Peripheral Mode, bit is set to “1” when reset signal is detected on the bus.
1	-	R	0x0	Reserved
0	Suspend	R	0x0	This bit is only valid in Peripheral mode. It is set to “1” when Suspend signal is detected on the bus.

INTRUSBE

INTRUSBE is an 8-bit interrupt enable register for INTRUSB. Offset: 0x0b
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:6	-	N/A	0x0	Unused, Always returns 0
5	Discon	R/W	0x0	1’b0: Disable Discon Interrupt 1’b1: Enable Discon Interrupt
4	Conn	R/W	0x0	1’b0: Disable Conn Interrupt 1’b1: Enable Conn Interrupt
3	SOF	R/W	0x0	1’b1: Enable SOF Interrupt 1’b0 : Disable SOF Interrupt
2	Reset	R/W	0x1	1’b1: Enable Reset Interrupt 1’b0 : Disable Reset Interrupt
1	Resume	R/W	0x1	1’b1: Enable Resume Interrupt 1’b0 : Disable Resume Interrupt
0	Suspend	R/W	0x0	1’b1: Enable Suspend Interrupt 1’b0 : Disable Suspend Interrupt

FRAME

FRAME is a 16-bit read-only register, which holds the last received frame number.
Offset: 0x0c
Width: 16 bits

Bits	Name	Direction	Reset	Description
15:11	-	N/A	0x0	-
10:0	Frame Number	R	0x0	Frame Number

Index

Index is an 8-bit register, which determines the endpoint that can be accsessed by address 0x10-0x1f Registers.
Offset: 0x0c
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:4	-	N/A	0x0	-
3:0	Selected Endpoint	R	0x0	Selected Endpoint

Testmode

Testmode is an 8-bit register, which sets the MUSBHDRC test modes in high-speed operation. Offset: 0x0f
Width: 8 bits

<table>
<tr><th>Bits</th><th>Name</th><th>Direction</th><th>Reset</th><th>Description</th></tr>
<tr><td>7</td><td>Force_Host</td><td>R/W</td><td>0x0</td><td>The CPU sets this bit to instruct the core to enter Host Mode when the session bit is set.
The operating speed is determined by the Force_HS and Force_FS bits as follows:
<table>
<tr><th>Force_HS</th><th>Force_FS</th><th>Operating Speed</th></tr>
<tr><td>0</td><td>0</td><td>Low Speed</td></tr>
<tr><td>0</td><td>1</td><td>Full Speed</td></tr>
<tr><td>1</td><td>0</td><td>High Speed</td></tr>
</table></td></tr>
<tr><td>6</td><td>FIFO_Access</td><td>R/W</td><td>0x0</td><td>The CPU sets this bit to transfer the packet in the Endpoint 0 Tx FIFO to the Endpoint 0 Rx FIFO. It is cleared automatically.</td></tr>
<tr><td>5</td><td>Force_FS</td><td>R/W</td><td>0x0</td><td>The CPU sets this bit either in conjunction with bit 7 above or to force the MUSBHDRC into Full-speed mode when it receives a USB reset.</td></tr>
<tr><td>4</td><td>Force_HS</td><td>R/W</td><td>0x0</td><td>The CPU sets this bit either in conjunction with bit 7 above or to force the MUSBHDRC into High-speed mode when it receives a USB reset.</td></tr>
<tr><td>3</td><td>Test_Packet</td><td>R/W</td><td>0x0</td><td>(High-speed mode) The CPU sets this bit to enter the Test_Packet test mode. In this mode, the MUSBHDRC repetitively transmits on the bus a 53-byte test packet.
The test packet has a fixed format and must be loaded into the Endpoint 0 FIFO before the test mode is entered.</td></tr>
<tr><td>2</td><td>Test_K</td><td>R/W</td><td>0x0</td><td>(High-speed mode) The CPU sets this bit to enter the Test_K test mode. In this mode, the MUSBHDRC transmits a continuous K on the bus.</td></tr>
<tr><td>1</td><td>Test_J</td><td>R/W</td><td>0x0</td><td>(High-speed mode) The CPU sets this bit to enter the Test_J test mode. In this mode, the MUSBHDRC transmits a continuous J on the bus.</td></tr>
<tr><td>0</td><td>Test_SE0_NAK</td><td>R/W</td><td>0x0</td><td>(High-speed mode) The CPU sets this bit to enter the Test_SE0_NAK test mode. In this mode, the MUSBHDRC remains in High-speed mode but responds to any valid IN token with a NAK.</td></tr>
</table>

DEVCTL
Offset: 0x60
Width: 8 bits

<table>
<tr><th>Bits</th><th>Name</th><th>Direction</th><th>Reset</th><th>Description</th></tr>
<tr><td>7</td><td>B-Device</td><td>R</td><td></td><td>This read-only bit indicates whether the MUSBHDRC is operating as the ‘A’ device or the ‘B’ device.
0:‘A’ device
1:‘B’ device
This bit is only valid while a session is in progress.
Note: If the core is in Force_Host mode (i.e. a session has been started with Testmode.D7 = 1), this bit will indicate the state of the HOSTDISCON input signal from the PHY.</td></tr>
<tr><td>6</td><td>FSDev</td><td>R</td><td></td><td>This read-only bit is set when a connection of a full-speed or high-speed device to the port has been detected. (High-speed devices are distinguished from full-speed by checking for high-speed chirps when the device is reset.) Only valid in Host mode.</td></tr>
<tr><td>5</td><td>LSDev</td><td>R</td><td></td><td>This read-only bit is set when a connection of low-speed device to the port has been detected. Only valid in Host mode.</td></tr>
<tr><td>4:3</td><td>VBus[1:0]</td><td>R</td><td></td><td>The read-only bit encodes the following VBus level:
<table><tr><th>D4</th><th>D3</th><th>Meaning</th></tr><tr><td>0</td><td></td><td>Below Session End</td></tr><tr><td>0</td><td>1</td><td>Above Session End, below AValid</td></tr><tr><td>1</td><td>0</td><td>Above AValid, below VBusValid</td></tr><tr><td>1</td><td>1</td><td>Above VBusValid</td></tr></table>Value 0x11 is read.</td></tr>
<tr><td>2</td><td>Host Mode</td><td>R</td><td></td><td>This Read-only bit is set when the MUSBHDRC is acting as a Host.</td></tr>
<tr><td>1</td><td>-</td><td>R/W</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>0</td><td>Session</td><td>R/W</td><td></td><td>When operating as an ‘A’ device, this bit is set or cleared by the CPU to start or end a session.
When operating as a ‘B’ device, this bit is set/cleared by the MUSBHDRC when a session starts/ends.
Note: Clearing this bit is forbidden when the core is not suspended.</td></tr>
</table>

Indexed Registers

CSR0 in Peripheral mode

Offset: 0x12 (with the Index register set to 0)

Width: 16 bits

Bits	Name	Direction	Reset	Description
15:9	-	R	0x0	Unused, Returns 0 when read.
8	FlushFIFO	R/W	0x0	The CPU sets this bit to “1” to flush the next packet to be transmitted/read from the Endpoint 0 FIFO. The FIFO pointer is reset and the TxPktRdy/RxPktRdy bit (below) is cleared. Note: FlushFIFO should only be used when TxPktRdy/RxPktRdy is set. At other times, it may cause data to be corrupted.
7	ServicedSetupEnd	R/W	0x0	The CPU sets this bit to “1” to clear the SetupEnd bit. It is cleared automatically.
6	ServicedRxPktRdy	R/W	0x0	The CPU sets this bit to “1” to clear the RxPktRdy bit. It is cleared automatically.
5	SendStall	R/W	0x0	The CPU sets this bit to “1” to terminate the current transaction. The STALL handshake will be transmitted and then this bit will be cleared automatically. Note: The FIFO should be flushed before SendStall is set.
4	SetupEnd	R	0x0	This bit is set to “1” when a control transaction ends before the DataEnd bit has been set. An interrupt will be generated and the FIFO flushed at this time. The bit is cleared when CPU sets ServicedSetupEnd bit to “1”..
3	DataEnd	R/W	0x0	The CPU sets this bit: 1. when setting TxPktRdy for the last data packet 2. when clearing RxPktRdy after unloading the last data packet 3. when setting TxPktRdy for a zero length data packet It is cleared automatically.
2	SentStall	R/W	0x0	This bit is set when a STALL handshake is transmitted. The CPU should clear this bit.
1	TxPktRdy	R/W	0x0	The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when the data packet has been transmitted. An interrupt is generated (if enabled) when the bit is cleared.
0	RxPktRdy	R	0x0	This bit is set when a data packet has been received. An interrupt is generated when this bit is set. The CPU clears this bit by setting the ServicedRxPktRdy bit.

CSR0 in Host mode
Offset: 0x12 (with the Index register set to 0)
Width: 16 bits

Bits	Name	Direction	Reset	Description
15:12	-	R	0x0	Unused. Return 0 when read.
11	Dis Ping			The CPU sets this bit to “1” to instruct the core not to issue PING tokens in data and status phases of a high-speed control transfer (for devices that do not respond to PING).
10:9	-	R	0x0	Unused, Returns 0 when read.
8	FlushFIFO	R/W	0x0	The CPU sets this bit to “1” to flush the next packet to be transmitted/read from the Endpoint 0 FIFO. The FIFO pointer is reset and the TxPktRdy/RxPktRdy bit (below) is cleared. Note: FlushFIFO should only be used when TxPktRdy/RxPktRdy is set. At other times, it may cause data to be corrupted.
7	NAK Timeout	R/W	0x0	This bit is set to “1” when Endpoint 0 is halted following the receipt of NAK responses for longer than the time set by the NAKLimit0 register. The CPU should clear this bit to allow the endpoint to continue.
6	StatusPkt	R/W	0x0	The CPU sets this bit to “1” at the same time as the TxPktRdy or ReqPkt bit is set, to perform a status stage transaction.
5	ReqPkt	R/W	0x0	The CPU sets this bit to “1” to request an IN transaction. It is cleared when RxPktRdy is set.
4	Error	R	0x0	This bit will be set to “1” when three attempts have been made to perform a transaction with no response from the peripheral. The CPU should clear this bit. An interrupt is generated when this bit is set.
3	SetupPkt	R/W	0x0	The CPU sets this bit to “1”, at the same time as the TxPktRdy bit is set, to send a SETUP token instead of an OUT token for the transaction.
2	RxStall	R/W	0x0	This bit is set to “1” when a STALL handshake is received. The CPU should clear this bit.
1	TxPktRdy	R/W	0x0	The CPU sets this bit to “1” after loading a data packet into the FIFO. It is cleared automatically when the data packet has been transmitted. An interrupt is generated (if enabled) when the bit is cleared.
0	RxPktRdy	R	0x0	This bit is set to “1” when a data packet has been received. An interrupt is generated (if enabled) when this bit is set. The CPU should clear this bit when the packet has been read from the FIFO.

Count0
Count0 is a 7-bit read-only register, which indicates the number of received data bytes in the Endpoint 0 FIFO.
The value returned changes as the contents of the FIFO change and is only valid while RxPktRdy (CSR0.D0) is set.
Offset: 0x18 (with the Index register set to 0)
Width: 8 bits

Bits	Name	Direction	Reset	Description
8	-	N/A	0x0	-
7:0	Endpoint 0 Rx Count	R	0x0	Endpoint 0 Rx Count

ConfigData
ConfigData is an 8-bit read-Only register that returns information about the selected core configuration.
Reset value is configuration dependent.
Offset: 0x18 (with the Index register set to 0)
Width: 8 bits

Bits	Name	Direction	Reset	Description
7	MPRxE	R	-	When set to '1', automatic concatenation of bulk packets is selected (see Section 9)
6	MPTxE	R	-	When set to '1', automatic splitting of bulk packets is selected (see Section 9)
5	BigEndian	R	-	When set to '1' indicates Big Endian ordering is selected.
4	HBRxE	R	-	When set to '1' indicates High-bandwidth Rx ISO Endpoint Support selected.
3	HBTxE	R	-	When set to '1' indicates High-bandwidth Tx ISO Endpoint Support selected.
2	DynFIFO Sizing	R	-	When set to '1' indicates Dynamic FIFO Sizing option selected.
1	SoftConE	R	-	When set to '1' indicates Soft Connect/Disconnect option selected.
0	UTMI DataWidth	R	-	Indicates selected UTMI+ data width: 0: 8 bits 1: 16 bits

NAKLIMIT0 (Host Mode only)
NAKLimit0 is a 5-bit register that sets the number of frames/microframes (High-Speed transfers) after which Endpoint 0 should timeout on receiving a stream of NAK responses.
(Equivalent settings for other endpoints can be made through their TxInterval and RxInterval registers)
The number of frames/microframes selected is $2^{(m-1)}$ (where m is the value set in the register, valid values 2 – 16).
If the host receives NAK responses from the target for more frames than the number represented by the limit set in this register, the endpoint will be halted. Note: A value of 0 or 1 disables the NAK timeout function.
Offset: 0x1B (with the Index register set to 0)
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:5	-	N/A	0x0	-
4:0	Endpoint 0 NAK Limit (m)	R	0x0	Endpoint 0 NAK Limit (m)

TxMaxP
The TxMaxP register defines the maximum amount of data that can be transferred through the selected Tx endpoint in a single operation. There is a TxMaxP register for each Tx endpoint (except Endpoint 0).
Offset: 0x10
Width: 16 bits

Bits	Name	Direction	Reset	Description
15:11	-	N/A	0x0	-
10:0	Maximum Payload/transaction	R/W	0x0	Maximum Payload/Transaction

TXCSR in Peripheral Mode
Offset: 0x12
Width: 16 bits

Bits	Name	Direction	Reset	Description
15	AutoSet	R/W	0x0	If the CPU sets this bit, TxPktRdy will be automatically set when data of the maximum packet size (value in TxMaxP) is loaded into the Tx FIFO. If a packet of less than the maximum packet size is loaded, then TxPktRdy will have to be set manually. Note: This bit should not be set for either high-bandwidth isochronous endpoints or high-bandwidth interrupt endpoints.
14	ISO	R/W	0x0	The CPU sets this bit to enable the Tx endpoint for isochronous transfers, and clears it to enable the Tx endpoint for Bulk or Interrupt transfers. Note: This bit is only valid in Peripheral mode. In Host mode, it always returns zero.
13	Mode	R/W	0x0	The CPU sets this bit to enable the endpoint direction as Tx, and clears it to enable the endpoint direction as Rx. Note: This bit is only valid when the same endpoint FIFO is used for both Tx and Rx transactions.
12	DMAReqEnab	R/W	0x0	The CPU sets this bit to enable the DMA request for the Tx endpoint.
11	FrcDataTog	R/W	0x0	The CPU sets this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received. This can be used by Interrupt Tx endpoints that are used to communicate rate feedback for Isochronous endpoints.
10	DMAReqMode	R/W	0x0	The CPU sets this bit to select DMA Mode 1 and clears this bit to select DMA Mode 0. Note: This bit must not be cleared either before or in the same cycle as the above DMAReqEnab bit is clear
9:8	–	R	0x0	Unused, Always return 0
7	IncompTX	R/W	0x0	When the endpoint is being used for high-bandwidth isochronous / interrupt transfers, this bit is set to indicate where a large packet has been split into 2 or 3 packets for transmission but insufficient IN tokens have been received to send all the parts. Note: In anything other than a high-bandwidth transfer, this bit will always return 0.
6	ClrDataTog	R/W	0x0	The CPU sets this bit to “1” reset the endpoint data toggle to 0.
5	SentStall	R/W	0x0	This bit is set when a STALL handshake is transmitted. The FIFO is flushed and the TxPktRdy bit is cleared (see below). The CPU should clear this bit.
4	SendStall	R/W	0x0	The CPU sets this bit to “1” to issue a STALL handshake to an IN token. The CPU clears this bit to terminate the stall condition. Note (i) The FIFO should be flushed before SendStall is set. (ii) This bit is invalid when the endpoint is being used for isochronous transfers.
3	FlushFIFO	R/W	0x0	The CPU sets this bit to “1” to flush the latest packet from the endpoint Tx FIFO. The FIFO pointer is reset, the TxPktRdy bit (below) is cleared and an interrupt is generated. This may be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. Note: FlushFIFO should only be used when TxPktRdy is set. At other times, it may cause data to be corrupted. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.
2	UnderRun	R/W	0x0	The USB sets this bit to “1” if an IN token is received when the TxPktRdy bit not set. The CPU should clear this bit.

TXCSR in Peripheral Mode – continued

Bits	Name	Direction	Reset	Description
1	FIFONotEmpty	R/W	0x0	The USB sets this bit to “1” when there is at least 1 packet in the Tx FIFO.
	TxPktRdy	R/W	0x0	The CPU sets this bit to “1” after loading a data packet into the FIFO. It is cleared automatically when the data packet has been transmitted. An interrupt is generated (if enabled) when the bit is cleared. TxPktRdy is also automatically cleared prior to loading a second packet into a double-buffered FIFO.
0	RxPktRdy	R	0x0	This bit is set to “1” when a data packet has been received. An interrupt is generated when this bit is set. The CPU clears this bit by setting the ServicedRxPktRdy bit.

TXCSR in Host Mode
Offset: 0x12
Width: 16 bits

Bits	Name	Direction	Reset	Description
15	AutoSet	R/W	0x0	When CPU sets this bit, TxPktRdy will be automatically set when data of the maximum packet size (value in TxMaxP) is loaded into the Tx FIFO. If a packet of less than the maximum packet size is loaded, then TxPktRdy will have to be set manually. Note: This bit should not be set for either high-bandwidth isochronous endpoints or high-bandwidth Interrupt endpoints.
14	-	R/W	0x0	Unused, Always Returns 0
13	Mode	R/W	0x0	CPU sets this bit to “1” to enable the endpoint direction as Tx, and clears it to enable the endpoint direction as Rx. Note: This bit only has any effect where the same endpoint FIFO is used for both Tx and Rx transactions.
12	DMAReqEnab	R/W	0x0	CPU sets this bit to “1” to enable the DMA request for the Tx endpoint.
11	FrcDataTog	R/W	0x0	CPU sets this bit to “1” to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received. This can be used by Interrupt Tx endpoints that are used to communicate rate feedback for isochronous endpoints.
10	DMAReqMode	R/W	0x0	The CPU sets this bit to “1” to select DMA Mode 1 and clears this bit to select DMA Mode 0. Note: This bit must not be cleared either before or in the same cycle as the above DMAReqEnab bit is clear
9:8	–	R	0x0	Unused, Always Returns 0
7	NAK Timeout IncompTX	R/W	0x0	Bulk endpoints only: This bit is set to “1” when the Tx endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the TxInterval register. The CPU should clear this bit to allow the endpoint to continue. High-bandwidth Interrupt endpoints only: This bit will be set if no response is received from the device to which the packet is being sent.
6	ClrDataTog	R/W	0x0	CPU sets this bit to “1” to reset the endpoint data toggle to 0.
5	SentStall	R/W	0x0	This bit is set to “1” when a STALL handshake is received. When this bit is ”1”, any DMA request that is in progress is stopped, the FIFO is completely flushed and the TxPktRdy bit is cleared (see below). The CPU should clear this bit.

TXCSR in Host Mode – continued

Bits	Name	Direction	Reset	Description
4	–	R	0x0	Unused, Returns 0 when read
3	FlushFIFO	R/W	0x0	The CPU sets this bit “1” to flush the latest packet from the endpoint Tx FIFO. The FIFO pointer is reset, the TxPktRdy bit (below) is cleared and an interrupt is generated. This bit may be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. Note: FlushFIFO should only be used when TxPktRdy is set. At other times, it may cause data to be corrupted. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.
2	Error	R/W	0x0	The USB sets this bit to “1” when 3 attempts have been made to send a packet and no handshake packet has been received. When this bit is ”1”, an interrupt is generated, TxPktRdy is cleared and the FIFO completely flushed. The CPU should clear this bit. Valid only when the endpoint is operating in Bulk or Interrupt mode.
1	FIFONotEmpty	R/W	0x0	The USB sets this bit to “1” when there is at least 1 packet in the Tx FIFO.
0	TxPktRdy	R/W	0x0	CPU sets this bit to “1” after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared prior to loading a second packet into a double-buffered FIFO.

RxMaxP

The RxMaxP register defines the maximum amount of data that can be transferred through the selected Rx endpoint in a single operation. There is a RxMaxP register for each Rx endpoint (except Endpoint 0).
Offset: 0x14
Width: 16 bits

Bits	Name	Direction	Reset	Description
15:11	-	N/A	0x0	-
10:0	Maximum Payload/transaction	R/W	0x0	Maximum Payload/Transaction

RXCSR in Peripheral Mode
Offset: 0x16
Width: 16 bits

<table>
<tr><th>Bits</th><th>Name</th><th>Direction</th><th>Reset</th><th>Description</th></tr>
<tr><td>15</td><td>AutoClear</td><td>R/W</td><td>0x0</td><td>When CPU sets this bit to “1”, the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the Rx FIFO. When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually. When using the DMA to unload the Rx FIFO, data is read from the Rx FIFO in 4 byte chunks regardless of the RxMaxP. Therefore, the RxPktRdy bit will be cleared as follows:
<table>
<tr><th>Remainder (RxMaxP/4)</th><th>Actual Bytes Read</th><th>Packet Sizes that will clear RxPktRdy.</th></tr>
<tr><td>0 (i.e. RXMaxP = 64 bytes)</td><td>RXMAXP</td><td>RXMAXP, RXMAXP-1, RXMAXP-2, RXMAXP-3</td></tr>
<tr><td>3 (i.e. RXMaxP = 63 bytes)</td><td>RXMAXP+1</td><td>RXMAXP, RXMAXP-1, RXMAXP-2</td></tr>
<tr><td>2 (i.e. RXMaxP = 62 bytes)</td><td>RXMAXP+2</td><td>RXMAXP, RXMAXP-1</td></tr>
<tr><td>1 (i.e. RXMaxP = 61 bytes)</td><td>RXMAXP+3</td><td>RXMAXP</td></tr>
</table>
Note: This bit should not be set for high-bandwidth isochronous endpoints.</td></tr>
<tr><td>14</td><td>ISO</td><td>R/W</td><td>0x0</td><td>CPU sets this bit to “1” to enable the Rx endpoint for isochronous transfers, and clears it to enable the Rx endpoint for bulk or interrupt transfers.</td></tr>
<tr><td>13</td><td>DMAReqEnab</td><td>R/W</td><td>0x0</td><td>CPU sets this bit “1” to enable the DMA request for the Rx endpoint.</td></tr>
<tr><td>12</td><td>DisNyet/ PID Error</td><td>R/W</td><td>0x0</td><td>Bulk/Interrupt Transactions: The CPU sets this bit to “1” to disable the sending of NYET handshakes. When set, all successfully received Rx packets are ACK'd including at the point at which the FIFO becomes full. Note: This bit is only valid in High-speed mode, in which it should be set for all Interrupt endpoints.
ISO Transactions: The core sets this bit to “1” to indicate a PID error in the received packet.</td></tr>
<tr><td>11</td><td>DMAReqMode</td><td>R/W</td><td>0x0</td><td>The CPU sets this bit to “1” to select DMA Mode 1 and clears this bit to select DMA Mode 0.
Note: This bit should not be cleared in the same cycle as RxPktRdy is cleared.</td></tr>
<tr><td>10:9</td><td>–</td><td>R</td><td>0x0</td><td>Unused, Always Returns 0.</td></tr>
<tr><td>8</td><td>IncompRx</td><td>R/W</td><td>0x0</td><td>This bit is set in a high-bandwidth isochronous/interrupt transfer if the packet in the Rx FIFO is incomplete because parts of the data were not received. It is cleared when RxPktRdy is cleared. Note: In anything other than a high-bandwidth transfer, this bit will always return 0.</td></tr>
<tr><td>7</td><td>ClrDataTog</td><td>R/W</td><td>0x0</td><td>The CPU sets this bit to “1” to reset the endpoint data toggle to 0.</td></tr>
<tr><td>6</td><td>SentStall</td><td>R/W</td><td>0x0</td><td>This bit is set to “1” when a STALL handshake is transmitted. The CPU should clear this bit.</td></tr>
</table>

RXCSR in Peripheral Mode – continued

Bits	Name	Direction	Reset	Description
5	SendStall	R/W	0x0	The CPU sets this bit to “1” to issue a STALL handshake. The CPU clears this bit to terminate the stall condition. Note: (a) The FIFO should be flushed before SendStall is set. (b) This bit has no effect when the endpoint is being used for isochronous transfers.
4	FlushFIFO	R/W	0x0	The CPU sets this bit to “1” to flush the next packet to be read from the endpoint Rx FIFO. The FIFO pointer is reset and the RxPktRdy bit (below) is cleared. Note: FlushFIFO should only be used when RxPktRdy is set. At other times, it may cause data to be corrupted. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.
3	DataError	R	0x0	This bit is set to “1” if RxPktRdy is set when the data packet has a CRC or bit-stuff error. It is cleared when RxPktRdy is cleared. Note: This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.
2	OverRun	R/W	0x0	This bit is set to “1” if an OUT packet cannot be loaded into the Rx FIFO. The CPU should clear this bit. Note: This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.
1	FIFOFull	R	0x0	This bit is set to “1” when no more packets can be loaded into the Rx FIFO.
0	RxPktRdy	R/W	0x0	This bit is set to “1” when a data packet has been received. The CPU should clear this bit when the packet has been unloaded from the Rx FIFO. An interrupt is generated when the bit is set.

RXCSR in Host Mode
Offset: 0x16
Width: 16 bits

<table>
<tr><th>Bits</th><th>Name</th><th>Direction</th><th>Reset</th><th>Description</th></tr>
<tr><td>15</td><td>AutoClear</td><td>R/W</td><td>0x0</td><td>When the CPU sets this bit to “1”, the RxPktRdy bit will be automatically cleared when a packet of RxMaxP bytes has been unloaded from the Rx FIFO. When packets of less than the maximum packet size are unloaded, RxPktRdy will have to be cleared manually. When using the DMA to unload the Rx FIFO, data is read from the Rx FIFO in 4 byte chunks regardless of the RxMaxP. Therefore, the RxPktRdy bit will be cleared as follows:
<table>
<tr><th>Remainder (RxMaxP/4)</th><th>Actual Bytes Read</th><th>Packet Sizes that will clear RxPktRdy.</th></tr>
<tr><td>0 (i.e. RXMaxP = 64 bytes)</td><td>RXMAXP</td><td>RXMAXP, RXMAXP-1, RXMAXP-2, RXMAXP-3</td></tr>
<tr><td>3 (i.e. RXMaxP = 63 bytes)</td><td>RXMAXP+1</td><td>RXMAXP, RXMAXP-1, RXMAXP-2</td></tr>
<tr><td>2 (i.e. RXMaxP = 62 bytes)</td><td>RXMAXP+2</td><td>RXMAXP, RXMAXP-1</td></tr>
<tr><td>1 (i.e. RXMaxP = 61 bytes)</td><td>RXMAXP+3</td><td>RXMAXP</td></tr>
</table>
Note: This bit should not be set for high-bandwidth isochronous endpoints.</td></tr>
<tr><td>14</td><td>AutoReq</td><td>R/W</td><td>0x0</td><td>When CPU sets this bit to “1”, the ReqPkt bit will be automatically set when the RxPktRdy bit is cleared. Note: This bit is automatically cleared when a short packet is received.</td></tr>
<tr><td>13</td><td>DMAReqEnab</td><td>R/W</td><td>0x0</td><td>CPU sets this bit to “1” to enable the DMA request for the Rx endpoint.</td></tr>
<tr><td>12</td><td>DisNyet/ PID Error</td><td>R</td><td>0x0</td><td>ISO Transactions Only: The core sets this bit ”1” to indicate a PID error in the received packet.
Bulk/Interrupt Transactions: This bit is disregarded.</td></tr>
<tr><td>11</td><td>DMAReqMode</td><td>R/W</td><td>0x0</td><td>The CPU sets this bit to select DMA Mode 1 and clears this bit to select DMA Mode 0.
Note: This bit should not be cleared in the same cycle as RxPktRdy is cleared.</td></tr>
<tr><td>10:9</td><td>–</td><td>R</td><td>0x0</td><td>Unused, Always Returns 0</td></tr>
<tr><td>8</td><td>IncompRx</td><td>R/W</td><td>0x0</td><td>This bit will be set in a high-bandwidth isochronous/interrupt transfer if the packet received is incomplete. It will be cleared when RxPktRdy is cleared.
Note: In anything other than a high-bandwidth transfer, this bit will always return 0.</td></tr>
<tr><td>7</td><td>ClrDataTog</td><td>R/W</td><td>0x0</td><td>CPU sets this bit to “1” to reset the endpoint data toggle to 0.</td></tr>
<tr><td>6</td><td>RxStall</td><td>R/W</td><td>0x0</td><td>When a STALL handshake is received, this bit is set to “1” and an interrupt is generated. The CPU should clear this bit.</td></tr>
</table>

RXCSR in Host Mode – continued

Bits	Name	Direction	Reset	Description
5	ReqPkt	R/W	0x0	CPU sets this bit to “1” to request an IN transaction. It is cleared when RxPktRdy is set.
4	FlushFIFO	R/W	0x0	The CPU sets this bit to “1” to flush the next packet to be read from the endpoint Rx FIFO. The FIFO pointer is reset and the RxPktRdy bit (below) is cleared. Note: FlushFIFO should only be used when RxPktRdy is set. At other times, it may cause data to be corrupted. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.
3	DataError/ NAK Timeout	R/W	0x0	When operating in ISO mode, this bit is set to “1” when RxPktRdy is set if the data packet has a CRC or bit-stuff error and cleared when RxPktRdy is cleared. In Bulk mode, this bit will be set to “1” when the Rx endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK Limit by the RxInterval register. The CPU should clear this bit to allow the endpoint to continue.
2	Error	R/W	0x0	The USB sets this bit to “1” when 3 attempts have been made to receive a packet and no data packet has been received. The CPU should clear this bit. An interrupt is generated when the bit is set. Note: This bit is only valid when the Tx endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.
1	FIFOFull	R	0x0	This bit is set to “1” when no more packets can be loaded into the Rx FIFO.
0	RxPktRdy	R/W	0x0	This bit is set to “1” when a data packet has been received. The CPU should clear this bit when the packet has been unloaded from the Rx FIFO. An interrupt is generated when the bit is set.

RxCount

RxCount is a 16-bit read-only register, which holds the number of received data bytes in the packet currently in line to be read from the Rx FIFO. If the packet was transmitted as multiple bulk packets, the number given will be for the combined packet.

Note: The value returned changes as the FIFO is unloaded and is only valid while RxPktRdy (RxCSR.D0) is set.

Offset: 0x18

Width: 16 bits

Bits	Name	Direction	Reset	Description
15:13	-	N/A	0x0	-
12:0	Endpoint Rx Count	R	0x0	Endpoint Rx Count

TxType(Host Mode Only)

Offset: 0x1A

Width: 6 bits

Bits	Name	Direction	Reset	Description
5:4	Protocol	R/W	2'h0	The CPU sets these bits to select the required protocol for the Tx endpoint: 00: Illegal 01: Isochronous 10: Bulk 11: Interrupt
3:0	Target Endpoint Number	R/W	4'h0	The CPU should set this value to the endpoint number contained in the Tx endpoint descriptor returned to the MUSBHDRC during device enumeration.

TxInterval (Host Mode Only)
TxInterval is an 8-bit register that, for interrupt and isochronous transfers, defines the polling interval for the currently-selected Tx endpoint. For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a TxInterval register for each configured Tx endpoint (except Endpoint 0).
Offset: 0x1B
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:0	Tx Polling Interval/NAK Limit (m)	R/W	8'h0	Tx Polling Interval/NAK Limit (m)

RxType (Host Mode Only)
Offset: 0x1A
Width: 6 bits

Bits	Name	Direction	Reset	Description
5:4	Protocol	R/W	2'h0	The CPU sets thest bits to select the required protocol for the Rx endpoint: 00: Illegal 01: Isochronous 10: Bulk 11: Interrupt
3-0	Target Endpoint Number	R/W	4'h0	The CPU should set this value to the endpoint number contained in the Rx endpoint descriptor returned to the MUSBHDRC during device enumeration.

RxInterval (Host Mode Only)
RxInterval is an 8-bit register that, for interrupt and isochronous transfers, defines the polling interval for the currently selected Rx endpoint. For Bulk endpoints, this register sets the number of frames/microframes after which the endpoint should timeout on receiving a stream of NAK responses. There is a RxInterval register for each configured Rx endpoint (except Endpoint 0).
Offset: 0x1B
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:0	Rx Polling Interval/NAK Limit (m)	R/W	8'h0	Rx Polling Interval/NAK Limit (m)

FIFOSize
FIFOSize is an 8-bit register, which returns sizes of the FIFOs associated with the selected additional Tx/Rx endpoints.
Values of 3 – 13 correspond to a FIFO size of 2n bytes (8 – 8192 bytes).
If an endpoint has not been configured, a value of 0 will be displayed.
When the Tx and Rx endpoints share the same FIFO, the Rx FIFO size will be encoded as 0xF.
Offset: 0x1F
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:4	Rx FIFO Size	R		Rx FIFO Size
3:0	Tx FIFO Size	R		Tx FIFO Size

FIFOx
This address range provides 16 addresses for CPU access to the FIFOs for each endpoint. Writing to these addresses loads data into the Tx FIFO for the corresponding endpoint. Reading from these addresses unloads data from the Rx FIFO for the corresponding endpoint.
Offset:FIFO0:0x20 FIFO1:0x24 FIFO2:0x28 FIFO3:0x2C FIFO4:0x30
Width: 32 bits

Bits	Name	Direction	Reset	Description
31:0	FIFOx	R/W		FIFOx

Additional Control & Configuration Registers (60h – 7Fh)

VControl (Write Only)

UTMI+ PHY Vendor Register
Offset: 0x68
Width: 16 bits

Bits	Name	Direction	Reset	Description
15:4	-	-	-	Reserved
3:0	VControl	W		VControl

VStatus (Read Only)

UTMI+ PHY Vendor Register
Offset: 0x68
Width: 16 bits

Bits	Name	Direction	Reset	Description
15:8	-	-	-	Reserved
7:0	VStatus	R		VStatus

DMA REGISTERS

Address	Register	Direction	Reset	Description
200h	INTR	R/W		D0: Indicates pending DMA Interrupts for Channel 1
204h	CNTL (1)	R/W		DMA Channel 1 Control: D0: Enable DMA D1: Direction 0 = DMA Write (Rx endpoint) 1 = DMA Read (Tx endpoint) D2: DMA Mode D3: Interrupt Enable D7–4: Endpoint number D8: Bus Error D10–9: Burst Mode 00 = Burst Mode 0 : Bursts of Unspecified Length 01 = Burst Mode 1 : INCR4 or Unspecified Length 10 = Burst Mode 2 : INCR8, INCR4 or Unspecified Length 11 = Burst Mode 3 : INCR16, INCR8, INCR4 or Unspecified Length
208	ADDR (1)	R/W		DMA Channel 1 AHB Memory Address (32 Bits)
20C	COUNT (1)	R/W		DMA Channel 1 Byte Count (32 Bits)

8.4. Register (F8100000 USB Connect Detector)

8.4.1. Memory Map

Name	Offset	R/W	Bit	Description
CONNECT	0xCC	R/W	10	USB Connection Detection Register Hold DP DM Line State At Reset：0x0
POWER	0xD0	W	4	PHY Suspend Control Register At Reset：0x0
UTMISEL	0x1400	W	6	UTMI Connection Setting Register At Reset：0x0
USBTEST	0x1404	W	1	USB Test Packet Setting Register Reset：0x1

8.4.2. Register Detail

USB connection Detection Register
Offset : 0xCC , Reset : 0x0

Bit	Name	R/W	Reset	Description
9	Linestate1_latch (DM)	R	x	Hold Linestate1 (DM) Value at the Time of Connection and Disconnection Detection
8	Linestate0_latch (DP)	R	x	Hold Linestate1 (DP) Value at the Time of Connection and Disconnection Detection
7	Discon_en _DM	R/W	0x0	Disconnection Detection Flag DM Enable (Clear at Detection)
6	Conn_en _DM	R/W	0x0	Connection Detection Flag DM Enable (Clear at Detection)
5	Discon_en _DP	R/W	0x0	Disconnection Detection Flag DP Enable (Clear at Detection)
4	Conn_en _DP	R/W	0x0	Connection Detection Flag DP Enable (Clear at Detection)
3	Linestate1 (DM)	R	x	Linestate[1] (DM) Monitor
2	Linestate0 (DP)	R	x	Linestate[0] (DP) Monitor
1	Discon_flg	R/W	0x0	Disconnection Detection Flag
0	Conn_flg	R/W	0x0	Connection Detection Flag

PHY Suspend Control Register
Offset : 0xD0 , reset : 0x0

Bit	Name	R/W	Reset	Description
15	REGSW	R/W	0x0	0: rstgen controls suspendm to PHY 1: MUSBHDRC controls suspendm to PHY
14:0	—	R/W	0x0	—

UTMI Connection Setting Register
Offset : 0x1400 , Reset : 0x0

Bit	Name	R/W	Reset	Description
8	—	R/W	0x0	Select MUSBHDRC's IDDIG input 0：A-Type (Normal) 1：B-Type
7	—	R/W	0x0	Select DMPULLDOWN to PHY 0：Fix 1 (Enable) 1：MUSBHDRC controls DMPULLDOWN
6	—	R/W	0x0	Select DPPULLDOWN to PHY 0：Fix 1 (Enable) 1：MUSBHDRC controls DMPULLDOWN
5	OPMODESEL	R/W	0x0	0: Normal Connection 1: Fix Opmode[1:0] = 2'b01 Please use this bit with a Reset value.
4	RXVALIDSEL	R/W	0x0	0：Normal Connection 1: Only 1 Pulse Rise Edge Please use this bit with a Reset value.
3	XCVRSEL	R/W	0x0	0：Normal Connection 1：xcvrsel[0] = 1 Please use this bit with a Reset value.
2	HOSTDISCON	R/W	0x0	0：Normal Connection 1：hostdiscon = 0 Please use this bit with a Reset value.
1	RXERROR	R/W	0x0	0：Normal Connection 1：rxerror = 0 Please use this bit with a Reset value.
0	DELAY	R/W	0x0	0：Normal Connection 1：rxactive,rxvalid,rxerror：1 cycle delay Regading rxvalid, DELAY(bit0) select delay ON/OFF to the signal selected by RXVALIDSEL (bit4) Please use this bit with a Reset value.

USB Test Packet Setting Register
Offset : 0x1404 , Reset : 0x0

Bit	Name	R/W	Reset	Description
0	USBTEST	R/W	0x0	0：Normal Connection 1：Issue Test Packet

9. SD I/F

Refer to another document [BM94081 KUT SD I/F block datasheet] for the function of SD I/F block.

10. Quad SPI I/F

10.1. Features

- Supports Quad serial flash ROM
- Supports serial flash ROM addresses up to 24 bits
- Allows the control of control registers from the AMBA-AHB bus
- Allows direct access from the memory map of the AMBA-AHB bus to serial flash ROM
- Includes 32-byte data transmit/receive FIFOs

10.2. Description

10.2.1. Block Diagram

The following section shows a quad serial flash controller block.

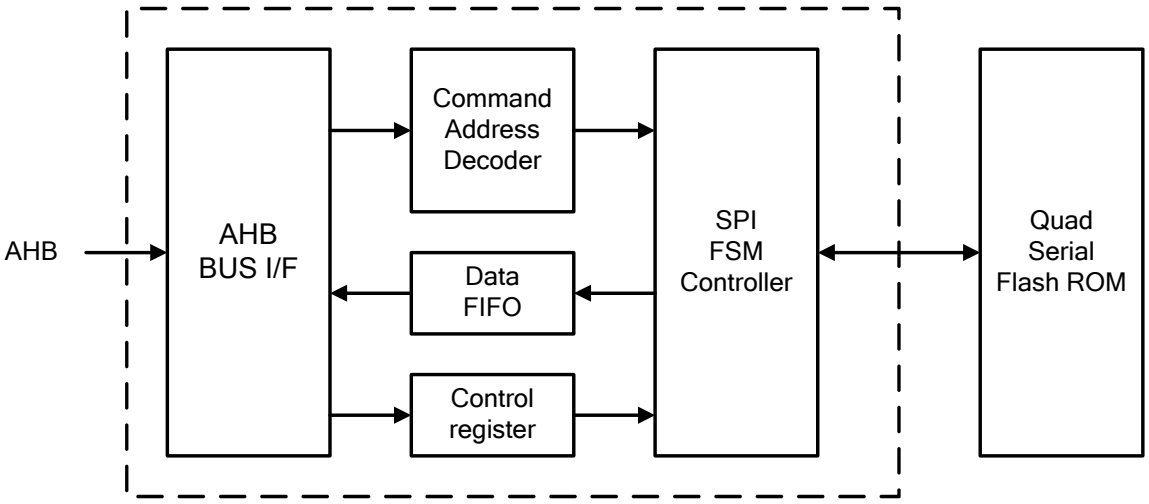


Figure 42. Quad Serial Flash Controller Block

10.2.2. Connection

The following section shows an example of connection with the quad serial flash ROM.

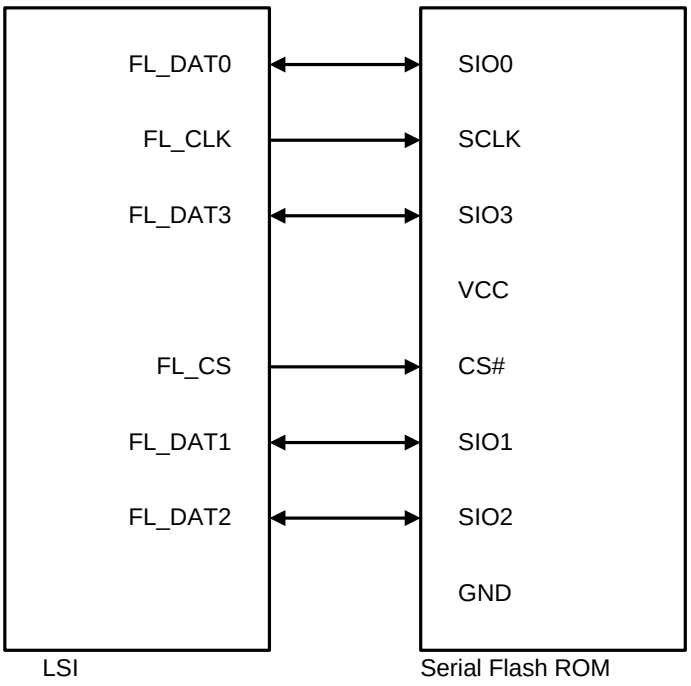


Figure 43. Connection Example

10.2.3. Command & Address Decoder

In case of any access to the serial flash ROM on the AHB memory map, the command & address decoder translates AHB address to serial flash ROM address and to a command. The command uses a value set with the Command ID register.
At this time, SPI communication is automatically initiated.
During data read to the serial flash ROM is in progress, the AHB bus master is placed into a wait state waiting to be disabled.

Access from AHB supports single read/transfer of one word of 32 bits and burst read/transfer of eight words of 32 bits.

10.2.4. Control Register

The control register allows access from the AHB bus to registers that are used to control the start/stop of SPI communication, command setting, address setting, and communication setting.
The register supports the width of AHB bus address and data up to 32 bits.

10.2.5. Data FIFO

Eight 32-bit data receive FIFOs are built in.
Eight 32-bit data transmit FIFOs are built-in.

10.2.6. SPI Format

The SPI format supports SPI Format MODE0.
This allows clock frequency setting from the format control register.
The length of data frame is configurable in steps of 8 bits.

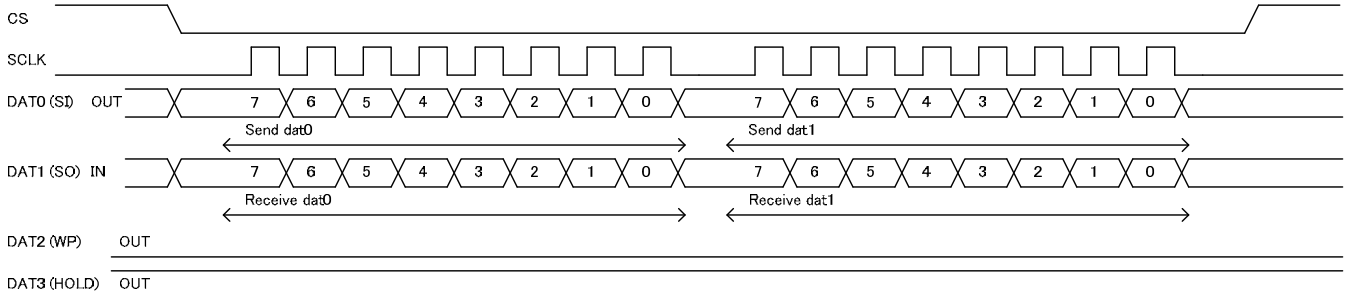


Figure 44. SPI MODE0 (Rising clock edge: Data latch, Falling clock edge: Data shift)

10.2.7. Transfer Modes

Single-SPI Mode

Single-SPI mode allows simultaneous data transmit and receive.
This mode is designed to exit upon completion of data transfer for the number of bytes set with the Transmit data amount setting and the Receive data amount setting parameters.
Transmitted and received data are written and read by the SndFifo and RcvFifo registers in the base address 0xF010_0000 area.
The following diagram shows waveforms.

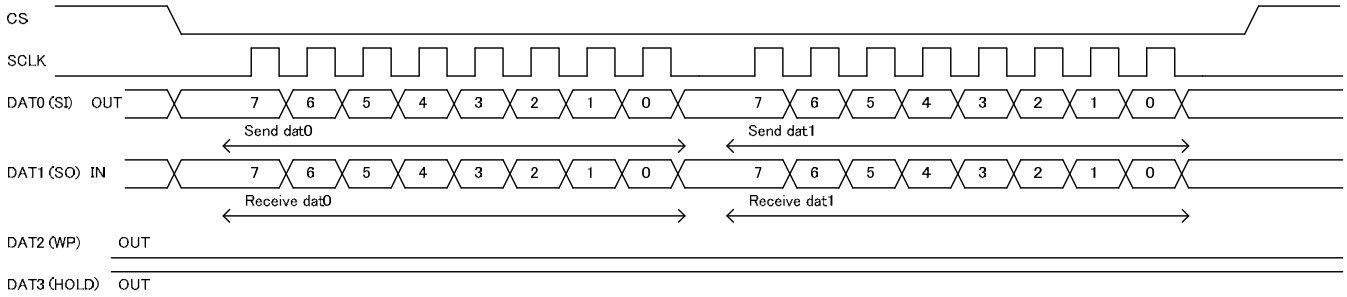


Figure 45.

Serial Flash Mode2

Serial Flash mode2 allows operation from data transmit through data receive.
Four data lines are used to execute serial communications. DAT3 serves as the MSB to execute 1-byte communication in two cycles.
Upon completion of data transfer for the number of bytes set with the Transmit data amount setting parameter, the data lines serve as input lines.
Upon completion of data transfer for the number of bytes set with the Receive data amount setting parameter, this mode exits.
In the command block, one data line (DAT0) is used to execute communications in eight cycles.
Serial Flash mode2 supports Quad Input / Output FAST_READ (EBh) operation.
Received data are read by direct access to the base address 0x2000_0000 area.
The following diagram shows waveforms.

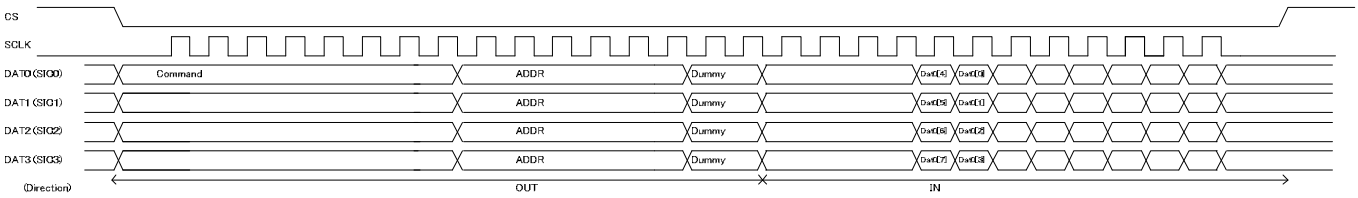


Figure 46.

10.2.8. Interrupt

Single-SPI mode generates a CPU interrupt upon completion of data transfer for the set number of bytes.
The interrupt signal polarity is low active.

10.3. I/O Signals

Pin Name	I/O	Function	Destination
sys_clk_i	In	AHB BUS Clock	CLKCTR
sfr_clk_i	In	Serial Flash Clock	CLKCTR
rstb_i	In	Reset (Active Low)	RSTGEN
FL_DAT0	In/Out	Serial Flash DATA[0]	PAD
FL_SCLK	Out	Serial Flash Clock	PAD
FLDAT3	In/Out	Serial Flash DATA[3]	PAD
FL_CS	Out	Serial Flash Chip Select	PAD
FL_DAT1	In/Out	Serial Flash DATA[1]	PAD
FL_DAT2	In/Out	Serial Flash DATA[2]	PAD
hsel_ssfr_i	In	AHB HSEL Slave – Serial Flash ROM Direct	AHB
htrans_ ssfr _i	In	AHB HTRANS Slave	AHB
hwrite_ ssfr _i	In	AHB HWRITE DATA Slave	AHB
hsize_ ssfr _i	In	AHB HSIZE Slave	AHB
haddr_ ssfr _i	In	AHB HADDR Slave	AHB
hwdata_ ssfr _i	In	AHB HWDATA Slave	AHB
hready_ ssfr _i	In	AHB HREADYI Slave	AHB
hready_ssfr_o	Out	AHB HREADY Out Slave	AHB
hrdata_ssfr_o	Out	AHB HRDATA Slave	AHB
hresp_ssfr_o	Out	AHB RESPONCE Slave	AHB

10.4. Register

10.4.1. Memory Map

Name	Description	Address Offset	Width	Reset
Control0	Transfer Control	0x00	16	16'h0000
Control1	Format Control	0x04	32	32'h033E2000
Sndbyte	Send Byte Number	0x08	8	8'h10
Rcvbyte	Received Byte Number	0x0C	8	8'h10
Status	Internal Status	0x10	16	16'h08a0
Interrupt1	Interrupt Setting 1	0x14	8	8'h00
Interrupt2	Interrupt Setting 2	0x18	8	8'hFF
Interrupt3	Interrupt Monitor	0x1C	8	8'hFF
SndFifo	Send FIFO Data	0x20	32	32'h00000000
RcvFifo	Receive FIFO Data	0x24	32	32'h00000000
Fifocnt	FIFO Control	0x28	32	32'h00000000
CommandID	Command ID & Dummy ID	0x2C	32	32'h0000EB00

10.4.2. Register Detail

Control0 Transfer Control
Offset: 0x00
Width: 16 bits

Bits	Name	Direction	Reset	Description
15:8		R/W	0x0	-
7:4		R/W	0x0	Transfer Mode Setting 0: - 1: - 2: Single-SPI Transmit/Receive 3: - 4: - 5: - 6: - 7: Serial Flash Mode2
3		R/W	-	-
2		R/W	0x0	AHB Direct Access 0: Disabled AHB Direct Access 1: Enabled AHB Direct Access
1		R/W	0x0	- Set "0" to this bit to write data.
0		R/W	0x0	SPI start Normally, "0" is read. Writing "1" starts SPI transfer.

Control1 Format Control
Offset: 0x04
Width: 32 bits

Bits	Name	Direction	Reset	Description
21:28		R/W	0x0	-
27:24		R/W	0x3	Sets the wait time after CS is activated until SCLK starts up or after the last serial communication is completed before CS is deactivated. [3:0] *SCLK
23:20		R/W	0x3	Sets the wait time during serial transmit (8 bits). [3:0] *SCLK
19:18		R/W	0x3	Sets the FL_DAT3 pin status in CS deactivated mode or in Single-SPI mode. 0, 1: Input 2: Low output 3: High output
17:16		R/W	0x2	Sets the FL_DAT2 pin status in CS deactivated mode or in Single-SPI mode. 0, 1: Input 2: Low output 3: High output
15:14		R/W	0x0	Sets the FL_DAT1 pin status in CS deactivated mode 0, 1: Input 2: Low output 3: High output
13:12		R/W	0x2	Sets the FL_DAT0 pin status in CS deactivated mode 0, 1: Input 2: Low output 3: High output
11		R/W	0x0	-
10		R/W	0x0	Fixes CS output to Low
9		R/W	0x0	Fixes CS output to High
8		R/W	0x0	- Set “0” to this bit to write data.
7		R/W	0x0	- Set “0” to this bit to write data.
6		R/W	0x0	- Set “0” to this bit to write data.
5		R/W	0x0	- Set “0” to this bit to write data.
4		R/W	0x0	0: Activates SCLK output 1: Deactivates SCLK output
3:0		R/W	0x0	SCLK frequency setting Settlement of the transfer mode =2:Single-SPI mode 0x3 : 73.728MHz /8 0x4 : 73.728MHz /16 0x5 : 73.728MHz /32 0x6 : 73.728MHz /64 Settlement of the transfer mode =7: Serial Flash mode2 0x0 : 73.728MHz/1 0x1 : 73.728MHz/2 0x2 : 73.728MHz /4 0x3 : 73.728MHz /8 0x4 : 73.728MHz /16 0x5 : 73.728MHz /32 0x6 : 73.728MHz /64

Sndbyte
Offset: 0x08
Width: 8 bits

Bits	Name	Direction	Reset	Description
5:0		R/W	0x10	Transmitted data amount setting (in terms of bytes) Data for the number of bytes set in this parameter is transmitted. The maximum set value is 32bytes.

Rcvbyte
Offset: 0x0C
Width: 8 bits

Bits	Name	Direction	Reset	Description
5:0		R/W	0x10	Received data amount setting (in terms of bytes) Data for the number of bytes set in this parameter is received. The maximum set value is 32bytes.

Status
Offset: 0x10
Width: 16 bits

Bits	Name	Direction	Reset	Description
11		R	0x1	Interrupt status at the end of transfer
10		R	0x0	-
9		R	0x0	-
8		R	0x0	-
7		R	0x1	Internal receive FIFO empty
6		R	0x0	Internal receive FIFO full
5		R	0x1	Internal transmit FIFO empty
4		R	0x0	Internal transmit FIFO full
3		R	0x0	-
2		R	0x0	-
1		R	0x0	SPI transfer complete flag (This flag is cleared at transfer startup)
0		R	0x0	SPI active flag

Interrupt1
Offset: 0x14
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:1		R/W	0x0	-
0		R/W	0x0	Clear SPI transfer complete interrupt. 1: Clear interrupt (One shot signal is set to High) “0” is read for readout.

Interrupt2
Offset: 0x18
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:1		R/W	0x7F	-
0		R/W	0x1	Masks SPI transfer complete interrupt. 0: Not mask interrupt 1: Mask interrupt

Interrupt3
Offset: 0x1C
Width: 8 bits

Bits	Name	Direction	Reset	Description
7		R	0x1	Quad serial flash controller interrupt status (Status after masking is outputted) 0: Interrupt generated 1: No interrupt generated
6:1		R	0x3F	-
0		R	0x1	SPI transfer complete interrupt status 0: Interrupt generated 1: No interrupt generated

SndFifo
Offset: 0x20
Width: 32 bits

Bits	Name	Direction	Reset	Description
31:0		W	0x0	Write data to transmit data FIFO.

RcvFifo
Offset: 0x24
Width: 32 bits

Bits	Name	Direction	Reset	Description
31:0		R	0x0	Read data from receive data FIFO.

Fifocnt
Offset: 0x28
Width: 24 bits

Bits	Name	Direction	Reset	Description
23:16		R	0x0	Reads the number of data bytes saved in receive data FIFO.
15:8		R	0x0	Reads the number of data bytes saved in transmit data FIFO.
7:2		R/W	0x0	-
1		R/W	0x0	Clears receive data FIFO. 0: Normal FIFO operation 1: Clear the read pointer of receive data FIFO
0		R/W	0x0	Clears transmit data FIFO. 0: Normal FIFO operation 1: Clear the write pointer of transmit data FIFO

CommandID
Offset: 0x2C
Width: 16 bits

Bits	Name	Direction	Reset	Description
15:8		R/W	0xEB	Sets the command ID used for direct access to AHB or read command ID for flash ROM.
7:0		R/W	0x00	Sets the command ID used for direct access to AHB or dummy ID used to read flash ROM. The ID is output by the MSB Fast method.

11. SSI Master

11.1. Feature

- It is connected with the APB interface of the AMBA standard.
- The APB bus width is 32 bits.
- It operates as a master device.
- The mask of all the interrupt signals can be done.
  - Transmit FIFO Overflow Interrupt
  - Transmit FIFO Underflow Interrupt
  - Receive FIFO Overflow Interrupt
  - Receive FIFO Underflow Interrupt
  - Receive FIFO FULL Interrupt
- The depth of the first two FIFO is 16 words at the transfer destination. The FIFO data width is 16 bits.
- When data is transmitted, two slaves or less can be selected.
- A uniting interrupt signal is outputted with active low polarity.
  - The serial protocol corresponds to Motorola, Inc. SPI.
- The bit rate of the serial clock for the data transfer is controlled.
- The programmer can decide the size of sent and received data from 4 bits to 16 bits.
- SSI clk can be chosen from dividing the system clock (1-8 dividing frequency). (Refer to the ClockController block). It has the DMA handshake interface for transmission and reception.

11.2. Description

11.2.1. Serial Protocol

SPI

This is the serial protocol developed in Motorola, Inc. The rising edge of the clock can be selected.
Slave's selection signal is fixed to HIGH when SSI is IDLE or if it is inactive.

11.2.2. Clock Ratio

The frequency of the serial input clock should be less than or equal to the frequency of pclk. When SSI is a master device, the maximum frequency of bit rate clock (sclk_out) is 1/4 of the frequency of ssi_clk.

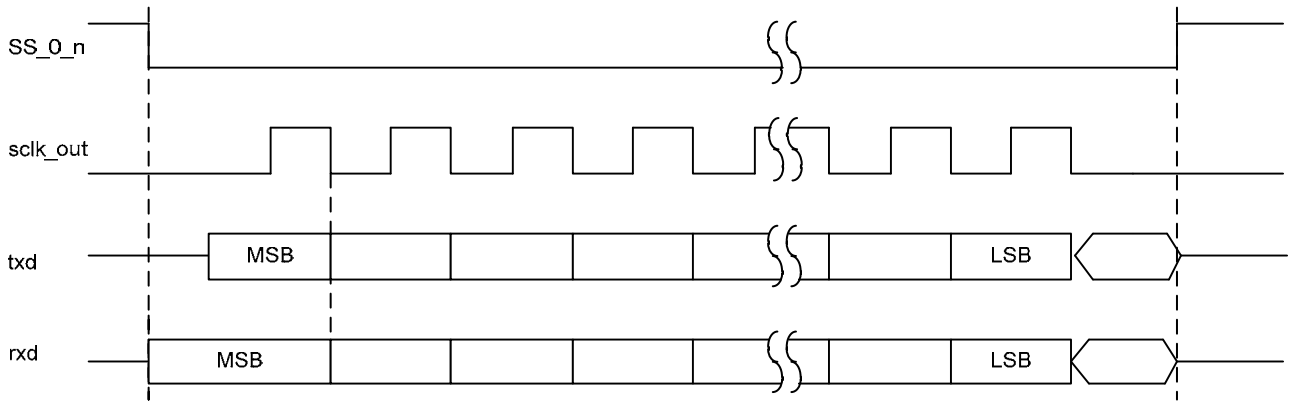


Figure 47. Serial Format

11.3. I/O Signal

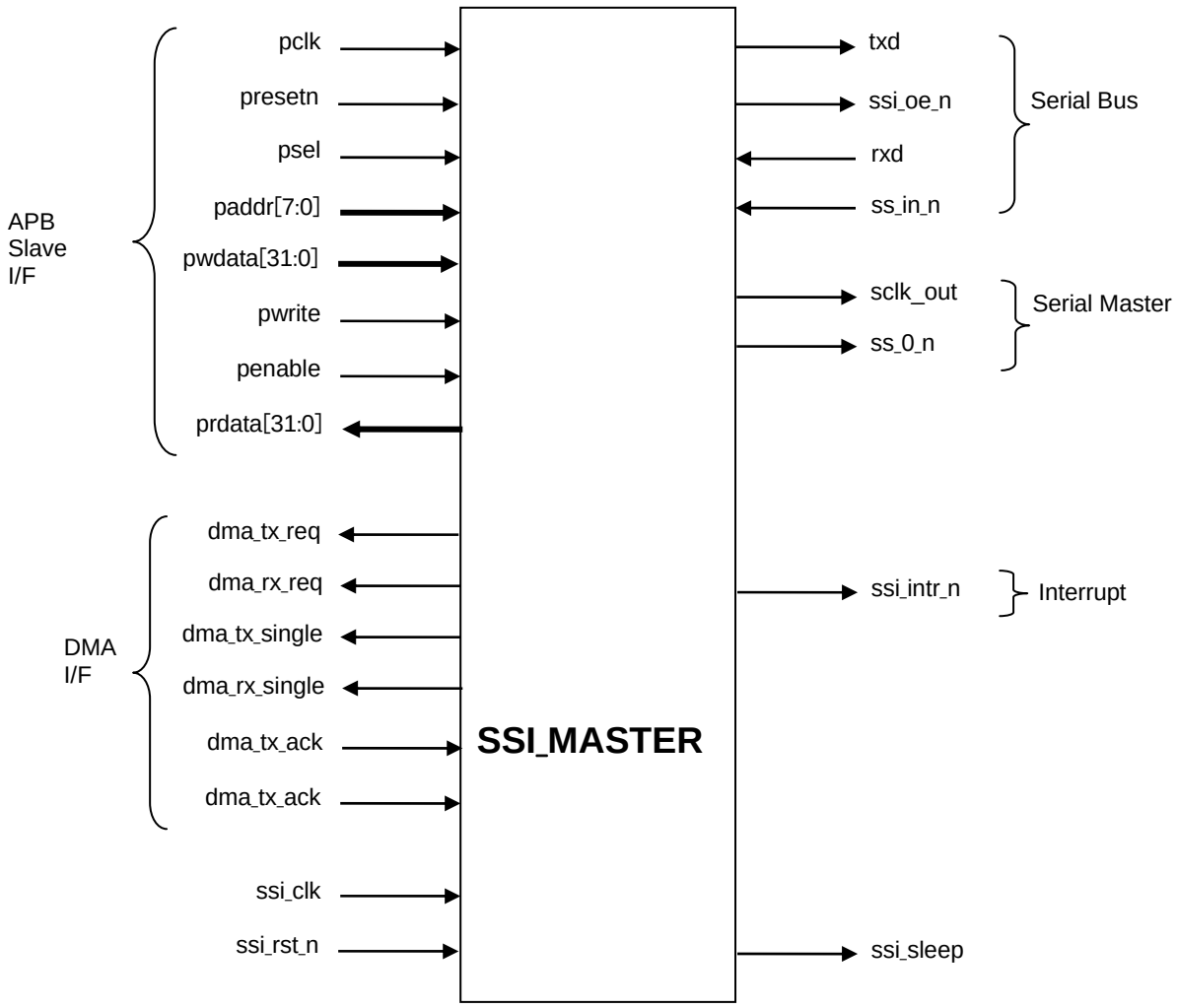


Figure 48. SSI_M Module

Terminal list of SSI_M module

Terminal Name	I/O	Description	Connection
pclk	In	APB Clock	Clock Gen
presetn	In	APB Reset	Reset Gen
psel	In	APB Peripheral Select Signal	APB
paddr[7:0]	In	APB Address	APB
pwdata[31:0]	In	APB Write Data	APB
pwrite	In	APB Write Signal	APB
penable	In	APB Enable Signal	APB
prdata[31:0]	Out	APB Read Data	APB
ssi_clk	In	The Serial Clock	Clock Gen
ssi_rst_n	In	SSI Module Reset Signal	Reset Gen
txd	Out	Transmission Data The data transfer is done using this signal from the master to the slave.	I/O
rxd	In	Reception Data The data transfer is done using this signal from the master to the slave.	I/O
ss_in_n	In	The Slave Select Signal (Active Low) The multi master system is fixed to High because it has no connection.	"1"
ssi_oe_n	Out	Output Enable Signal (Active Low)	I/O
ssi_sleep	Out	SSI Enable Flag This signal becomes active when SSI is enabled. System clock generator/control module can disable the ssi_clk input. This reduces the power consumption of the system. 0:SSI is enabled. 1:SSI is disabled.	OPEN
sclk_out	Out	Serial Bit Rate Clock It is generated from ssi_clk by the SSI module.	I/O
ss_0_n	Out	One Slave Select Signal (Active Low for SPI)	I/O
ssi_intr_n	Out	SSI Module Interrupt Flag of the Individual Interrupt Signal	ICTL
dma_tx_req	Out	FIFO DMA Transmission Request This is effective when DMA controller is needed. 0: There is no request. 1: There is a request.	DMAC
dma_rx_req	Out	FIFO DMA Reception Request This is effective when DMA controller is needed. 0: There is no request. 1: There is a request.	DMAC
dma_tx_single	Out	FIFO Single DMA Transmission Signal 0: FIFO for the transmission is full. 1: FIFO for the transmission is not full.	DMAC
dma_rx_single	Out	FIFO single signal for the DMA reception. 0: FIFO for the reception is full. 1: FIFO for the reception is not full.	DMAC
dma_tx_ack	In	Acknowledge for DMA Transmission	DMAC
dma_rx_ack	In	Acknowledge for DMA Reception	DMAC

11.4. Register

11.4.1. Memory Map

Name	Description	Address Offset	R/W	Width	Reset
CTRLR0	Control Register 0	0x0	R/W	16 bits	0x00000007
CTRLR1	Control Register 1	0x4	R/W	16 bits	0x00000000
SSIENR	SSI Enable Register	0x8	R/W	1 bit	0x00000000
SER	Slave Enable Register	0x10	R/W	1 bit	0x00000000
BAUDR	Baud Rate Select	0x14	R/W	16 bits	0x00000000
TXFTLR	Transmit FIFO Threshold Level	0x18	R/W	5 bits	0x00000000
RXFTLR	Receive FIFO Threshold Level	0x1C	R/W	5 bits	0x00000000
TXFLR	Transmit FIFO Level Register	0x20	R	5 bits	0x00000000
RXFLR	Receive FIFO Level Register	0x24	R	5 bits	0x00000000
SR	Status Register	0x28	R	7 bits	0x00000006
IMR	Interrupt Mask Register	0x2C	R/W	6 bits	0x0000003F
ISR	Interrupt Status Register	0x30	R	6 bits	0x00000000
RISR	Raw Interrupt Status Register	0x34	R	6 bits	0x00000000
TXOICR	Transmit FIFO Overflow Interrupt Clear Register	0x38	R	1 bit	0x00000000
RXOICR	Receive FIFO Overflow Interrupt Clear Register	0x3C	R	1 bit	0x00000000
RXUICR	Receive FIFO Underflow Interrupt Clear Register	0x40	R	1 bit	0x00000000
MSTICR	Multi-Master Interrupt Clear Register	0x44	R	1 bit	0x00000000

Memory Map – continued

Name	Description	Address Offset	R/W	Width	Reset
ICR	Interrupt Clear Register	0x48	R	1 bit	0x00000000
DMACR	DMA Control Register	0x4C	R/W	2 bits	0x00000000
DMATDLR	DMA Transmit Data Level	0x50	R/W	4 bits	0x00000000
DMARDLR	DMA Receive Data Level	0x54	R/W	4 bits	0x00000000
IDR	Identification Register	0x58	R	32 bits	0x00000000
SSI_COMP_VERSION	Core Kit Version ID	0x5C	R	32 bits	0x3332322A
DR (Note 1)	Data Register	0x60-9C	R/W	16 bits	0x00000000

(Note 1) Width is given to the address so that the AHB address may do the increment at the burst access by AHB Master like DMA controller, and the memory map is prepared for 16 cycles in 32 bits or less width increment type burst, and AddressOffset=0x60-0x9C.

11.4.2. Register Detail.

CTRLR0

This register controls the serial data transfer. Writing cannot be done to this register when SSI is enabled. Writing can be done for the SSIENR register by disabling the SSI.

Address Offset : 0x0

Bits	Name	Direction	Reset	Description
15:12	CFS	R/W	0x0	(reserved)
11	SRL	R/W	0x0	Shift Register Loop This is used during test. 0: Normal Mode 1: Test Mode TXD is internally connected with RXD when changing to TEST mode Consequently, Sfit Register Loop can be tested
9:8	TMOD	R/W	0x0	Transfer Mode Setting the transfer mode of the serial communication. It shows whether received data or the transmitted data is effective. Transmission ONLY mode Receiving data from an external device is invalid, and is not stored in FIFO for reception. It is rewritten by the next forwarding stage Reception ONLY mode Transmission data is invalid. After writing in FIFO for transmission, the data of the same word is sent again for the forwarding period. Transmission & Receiving mode Both the transmission and the reception are effective. The data transfer continues until FIFO for transmission empties. The data received from an external device is stored in Receive FIFO, and can be accessed from the host. 00 : Transmission & reception 01 : TransmissionONLY 10 : ReceptionONLY 11 : (reserved)
7:6				Reserved and read as zero
5:4	FRF	R	0x0	Frame Format The protocol is set. 0. Motorola, Inc. SPI * Only Motorola, Inc. SPI is supported in this device.
3:0	DFS	R/W	0x7	Setting of size of data frame The size of the frame in 16 bits or less can be set. 0000: Reserved 0001: Reserved 0010: Reserved 0011: 4bit Serial Data Transfer 0100: 5bit Serial Data Transfer 0101: 6bit Serial Data Transfer 0110: 7bit Serial Data Transfer 0111: 8bit Serial Data Transfer 1000: 9bit Serial Data Transfer 1001: 10bit Serial Data Transfer 1010: 11bit Serial Data Transfer 1011: 12bit Serial Data Transfer 1100: 13bit Serial Data Transfer 1101: 14bit Serial Data Transfer 1110: 15bit Serial Data Transfer 1111: 16bit Serial Data Transfer

CTRLR1
This register becomes effective only when it is used as master device. The end of the serial transfer is controlled at receiving only mode. This register cannot be set when SSI is enabled.
Address Offset : 0x04

Bits	Name	Direction	Reset	Description
15:0	NDF	R/W	0x0	The number of data frames is set. The number of data frames received by SSI is set at TMOD=10 or TMOD=11. It keeps receiving until the number of received data frames becomes the same number as this register +1. However, the maximum is 64KB. Forwarding continues as long as the slave is selected at the slave device.

SSIENR
SSI is disabled or it is set as enable.
Address Offset : 0x08

Bits	Name	Direction	Reset	Description
0	SSI_EN	R/W	0x0	SSI is enabled. All serial transfers interrupt at once. FIFO is cleared. Control register cannot be set when this is enabled.

SER
It is effective when SSI is a master device. It is possible to output it from the master to an individual slave.
Address Offset : 0x10

Bits	Name	Direction	Reset	Description
0	SER	R/W	0x0	Slave Select signal Each bit deals with each slave. 0: Not Selected 1: Selected

BAUDR
This register becomes effective only when it is used as master device. The frequency of the clock that does the data transfer is set.
Address Offset : 0x14

Bits	Name	Direction	Reset	Description
15: 0	SCKDV	R/W	0x0	The ratio of dividing frequency of the clock is set. LSB is set to "0" always (The ratio of dividing frequency is an even number from 4 to 65534). sclk_out output is "0x0", SCLK_OUT = SSI_CLK/SCKDV

TXFTLR
The threshold of the FIFO memory for the transmission is set.
Address Offset : 0x18

Bits	Name	Direction	Reset	Description
4: 0	TFT	R/W	0x0	The FIFO threshold for the transmission. It is necessary to set the value smaller than the depth of FIFO. The value that becomes the trigger of the interrupt output is set.

RXFTLR
The threshold of the FIFO memory for the reception is set.
Address Offset : 0x1C

Bits	Name	Direction	Reset	Description
4: 0	RFT	R/W	0x0	The FIFO threshold for the reception. It is necessary to set the value below the depth of FIFO. The value that becomes the trigger of the interrupt output is set.

TXFLR

This register contains the number of valid data that can be stored in the FIFO memory during transmission.
Address Offset : 0x20

Bits	Name	Direction	Reset	Description
4: 0	TXTFL	R	0x0	Quantity of data there is in FIFO for the transmission.

RXFLR

This register contains the number of valid data that can be stored in the FIFO memory for the reception.
Address Offset : 0x24

Bits	Name	Direction	Reset	Description
4: 0	RXTFL	R	0x0	Quantity of data there is in FIFO for the reception.

SR

This register contains the state, the FIFO status, and the sending and receiving error of the present forwarding.
Address Offset : 0x28

Bits	Name	Direction	Reset	Description
6	DCOL	R	0x0	Data Collision Error Only effective when using as a master device. When another master selects the device as a slave, SSI is set to "1" in the data transfer. It is cleared by reading. 0: No Error 1:There is data collision error.
5	TXE	R	0x0	Transfer Error Once transfer starts, this register is asserted when FIFO for transfer is empty. This bit is only effective when used as a slave device. Data from forwarding the previous state is sent again to the TxD line. 0: No Error 1:Forwarding error.
4	RFF	R	0x0	FIFO for Reception is Full. When FIFO for the reception is filled, this bit is set. 0: NOT FULL 1: FULL
3	RFNE	R	0x0	FIFO for Reception is not full. When Clear is done and at least one or more FIFO for the reception has data or is empty FIFO, this register is modified. 0:Receive FIFO is empty. 1:Receive FIFO is not empty.
2	TFE	R	0x1	FIFO for Transmission is empty. This bit is set when Transmit FIFO is empty. When FIFO has data, this bit is cleared. 0:Transmit FIFO is not empty. 1:Transmit FIFO is empty.
1	TFNF	R	0x1	Transmit FIFO has data. When FIFO is full or has data, it is set. 0:Transmit FIFO is FULL. 1:Transmit FIFO is NOT FULL.
0	BUSY	R	0x0	The BUSY flag. This register is set during serial transfer. When SSI is disabled or IDLE, this register is cleared.

IMR

The mask of all the interrupt signals can be done. The MSTIM bit becomes invalid when using it as a slave.
After reset, the mask is not done as for the interrupt signal.
Address Offset : 0x2C

Bits	Name	Direction	Reset	Description
5	MSTIM	R/W	0x1	The Master Transfer Collision Interrupt Mask 0: Mask 1: NO mask
4	RXFIM	R/W	0x1	Receive FIFO FULL Interrupt Mask 0: Mask 1: NO mask
3	RXOIM	R/W	0x1	Receive FIFO Overflow Interrupt Mask 0: Mask 1: NO mask
2	RXUIM	R/W	0x1	The FIFO Underflow Interrupt Mask for Reception 0: Mask 1: NO mask
1	TXOIM	R/W	0x1	The FIFO Overflow Interrupt Mask for Transmission 0: Mask 1: NO mask
0	TXEIM	R/W	0x1	The FIFO EMPTY Interrupt Mask for Transmission 0: Mask 1: NO mask

ISR

For the mask state, the generated interrupt is seen.
Address Offset : 0x30

Bits	Name	Direction	Reset	Description
5	MSTIS	R	0x0	The Master Transfer Collision Interrupt 0: No interrupt 1: Interrupt
4	RXFIS	R	0x0	Receive FIFO FULL Interrupt 0: No interrupt 1: Interrupt
3	RXOIS	R	0x0	Receive FIFO Overflow Mask 0: No interrupt 1: Interrupt
2	RXUIS	R	0x0	The FIFO Underflow Interrupt for Reception 0: No interrupt 1: Interrupt
1	TXOIS	R	0x0	The FIFO Overflow Interrupt for Transmission 0: No interrupt 1: Interrupt
0	TXEIS	R	0x0	The FIFO EMPTY Interrupt for Transmission 0: No interrupt 1: Interrupt

RISR

The generated interrupt is displayed.
Address Offset : 0x34

Bits	Name	Direction	Reset	Description
5	MSTIR	R	0x0	The Master Transfer Collision Interrupt 0: No interrupt 1: Interrupt
4	RXFIR	R	0x0	Receive FIFO FULL Interrupt 0: No interrupt 1: Interrupt
3	RXOIR	R	0x0	Receive FIFO Overflow Interrupt 0: No interrupt 1: Interrupt
2	RXUIR	R	0x0	The FIFO Underflow Interrupt for Reception 0: No interrupt 1: Interrupt
1	TXOIR	R	0x0	The FIFO Overflow Interrupt for Transmission 0: No interrupt 1: Interrupt
0	TXEIR	R	0x0	The FIFO EMPTY Interrupt for Transmission 0: No interrupt 1: Interrupt

TXOICR
Transmit FIFO overflow interrupt clear register
Address Offset : 0x38

Bits	Name	Direction	Reset	Description
0	TXOICR	R	0x0	Transmit FIFO Overflow Interrupt Clear Register

RXOICR
Receive FIFO overflow interrupt clear register
Address Offset : 0x3C

Bits	Name	Direction	Reset	Description
0	RXOICR	R	0x0	Receive FIFO Overflow Interrupt Clear Register

RXUICR
Receive FIFO underflow interrupt clear register
Address Offset : 0x40

Bits	Name	Direction	Reset	Description
0	RXUICR	R	0x0	Receive FIFO Underflow Interrupt Clear Register

MSTICR
Master collision interrupt clear register
Address Offset : 0x44

Bits	Name	Direction	Reset	Description
0	MSTICR	R	0x0	Master Collision Interrupt Clear Register

ICR
All interrupt clear register
Address Offset : 0x48

Bits	Name	Direction	Reset	Description
0	ICR	R	0x0	All Interrupt Clear Register

DMACR
The DMA control register.
Address Offset : 0x4C

Bits	Name	Direction	Reset	Description
1	TDMAE	R/W	0x0	Transmission DMA is enabled. The DMA channel is turned on and off with this bit. 0 :Transmission DMA is disabled. 1 :Transmission DMA is enabled.
0	RDMAE	R/W	0x0	Reception DMA is enabled. The DMA channel is turned on and off with this bit. 0 :Reception DMA is disabled. 1 :Reception DMA is enabled.

DMATDLR
The DMA transmission data level
Address Offset : 0x50

Bits	Name	Direction	Reset	Description
3:0	DMATDLR	R/W	0x0	The Transmission Data Level Timing in which the DMA request output can be set. When becoming equal, the numbers of data collected in FIFO output the dma_tx_req signal with the set value.

DMARDLR
The DMA receive data level
Address Offset : 0x54

Bits	Name	Direction	Reset	Description
3:0	DMARDLR	R/W	0x0	The Receive Data Level Timing in which the DMA request output can be set. When becoming equal, the data collected in FIFO outputs the dma_rx_req signal with the set value.

IDR
Individual recognition code
Address Offset : 0x58

Bits	Name	Direction	Reset	Description
31: 0	IDCODE	R	-	SSI Module Identification Number

SSI_COMP_VERION
Version of SSI
Address Offset : 0x5C

Bits	Name	Direction	Reset	Description
31: 0	SSI_COMP_ VERSION	R	-	SSI Module Version Management Number

DR
SSI has FIFO with 16-bit width for transmission and reception. The value of Receive FIFO can be read by accessing this register.
When writing is finished, data is written in Transmit FIFO. It reads out data from the FIFO, and it writes it automatically on any address whether read or write.
Address Offset : 0x60-0x9C

Bits	Name	Direction	Reset	Description
15: 0	DR	RW	0x0	The Data Register When writing by right adjust, and reading it, writing is right adjust.

12. SSI Slave

12.1. Feature

- It is connected with the APB interface of the AMBA standard.
- The width of the APB bus is 32 bits.
- It operates as a slave device.
- Interrupt and masking are independently done.
  - Transmit FIFO Overflow Interrupt
  - Transmit FIFO Underflow Interrupt
  - Receive FIFO Overflow Interrupt
  - Receive FIFO Underflow Interrupt
  - Receive FIFO FULL Interrupt
- The depth of both transfer source and destination FIFO is 16 words. The width of FIFO data is 16 bits.
- The uniting interrupt signal is outputted, and the polarity of interrupt is active low.
  - The serial protocol interface corresponds to Motorola, Inc. SPI.
- The programmer can decide the size of the sent and received data from 4 bits to 16 bits.
- ssi_clk can be chosen from dividing the system clock (1-8 dividing frequency). (Refer to the Clock Controller block.)
- It uses handshake for DMA transmission and reception interface.

12.2. Description

12.2.1. Clock Ration

When the device functions as slave, the frequency of ssi_clk is needed to 16 times or more than the sclk_in clock.

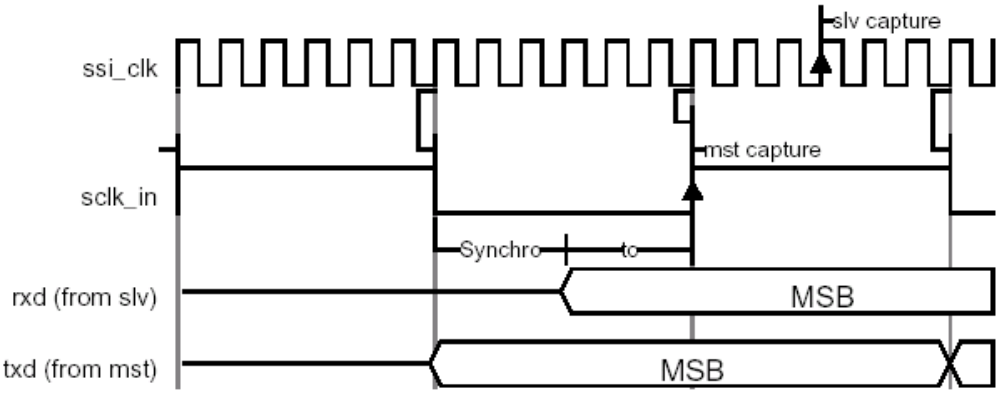


Figure 49. sclk_out ssi_clk

12.3. I/O Signal

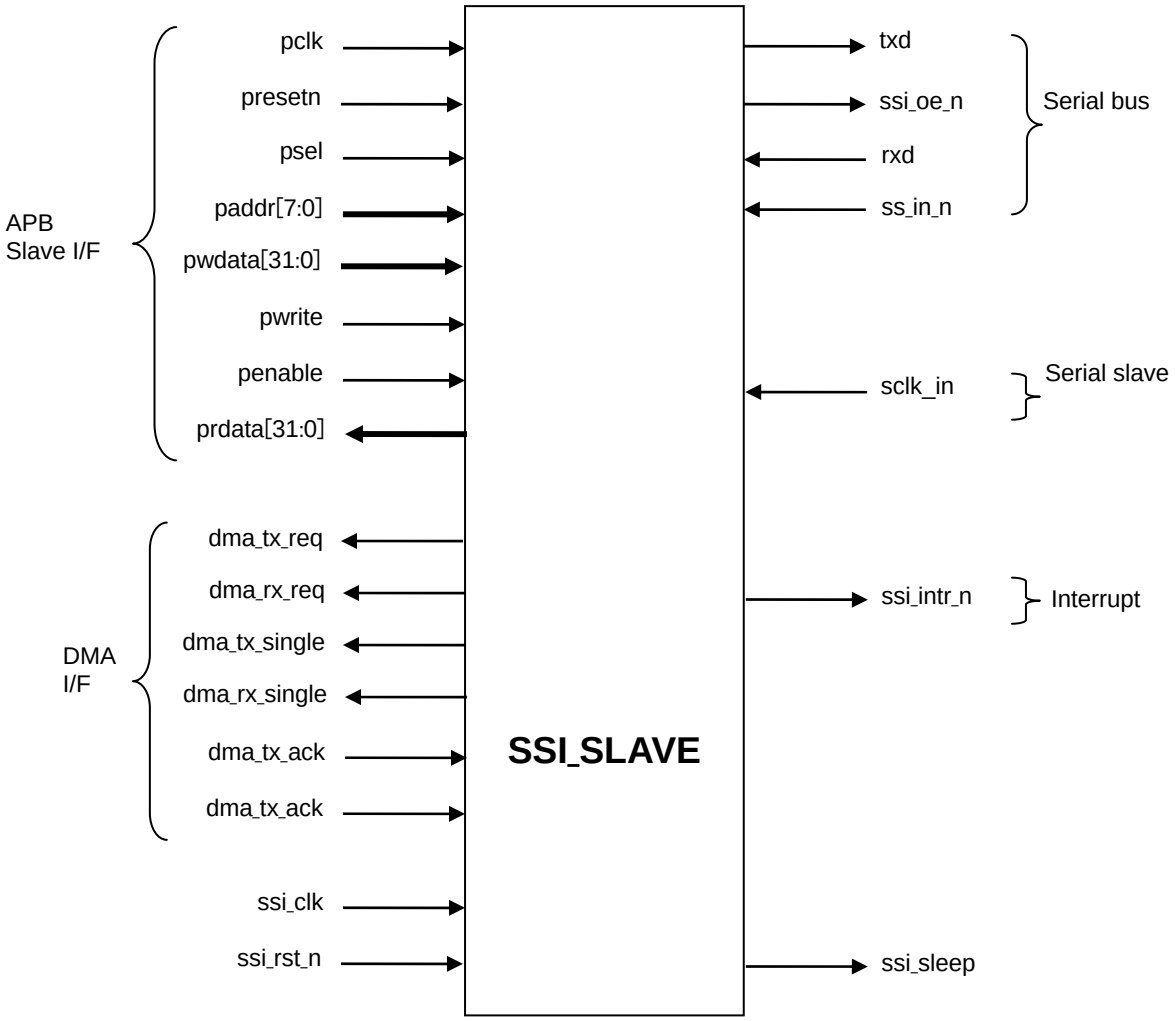


Figure 50.

Terminal List of SSI Slave Module

Terminal Name	I/O	Description	Connection
pclk	In	APB Clock	Clock Gen
presetn	In	APB Reset	Reset Gen
psel	In In	APB Peripheral Selection Signal	APB
paddr[7:0]	In	APB Address	APB
pwdata[31:0]	In	APB Write Data	APB
pwrite	In	APB Write Signal	APB
penable	In	APB Enable Signal	APB
prdata[31:0]	Out	APB Read Data	APB
ssi_clk	In	The Serial Clock	Clock Gen
ssi_rst_n	In	SSI Module Reset Signal	Reset Gen
txd	Out	Transmission Data The data transfer is done using this signal from the master to the slave.	I/O
rxd	In	Received Data. The data transfer is done using this line from the master to the slave.	I/O
ss_in_n	In	Slave Select Signal	I/O
ssi_oe_n	Out	Out Enable Signal (Active Low)	I/O
ssi_sleep	Out	SSI Enable Flag This signal becomes active when ssi is enabled. System clock generator / control module can disable ssi_clkIn. This reduces the power consumption of the system. 0: SSI is enable. 1: SSI is disabled.	OPEN
sclk_in	In	Serial Bit Rate Clock Out is done from the external master device.	I/O
ssi_intr_n	Out	SSI Module Interrupt Flag Result of ORed individual interrupt signals	ICTL
dma_tx_req	Out	FIFO DMA Transmission Request When this bit is set to “1”, DMA executes transmission request. 0: There is no request. 1: There is a request.	DMAC
dma_rx_req	Out	FIFO DMA Reception Request When this bit is set to “1”, DMA executes reception request. 0: There is no request. 1: There is a request.	DMAC
dma_tx_single	Out	FIFO DMA Single Transmission Signal 0: FIFO is NOT full for the transmission. 1: FIFO is full for the transmission.	DMAC
dma_rx_single	Out	FIFO DMA Single Reception Signal 0: FIFO is NOT full for the reception. 1: FIFO is full for the reception.	DMAC
dma_tx_ack	In	Acknowledge for DMA Transmission	DMAC
dma_rx_ack	In	Acknowledge for DMA Reception	DMAC

12.4. Register

12.4.1. Memory Map

Name	Description	Address Offset	R/W	Width	Reset
CTRLR0	Control Register 0	0x0	R/W	16bits	0x00000007
SSIENR	SSI ENABLE Register	0x8	R/W	1bit	0x00000000
MWCR	Micro-wire Control Register	0xC	R/W	3bits	0x00000000
TXFTLR	Transmit FIFO Threshold Level	0x18	R/W	5bits	0x00000000
RXFTLR	Receive FIFO Threshold Level	0x1C	R/W	5bits	0x00000000
TXFLR	Transmit FIFO Level Register	0x20	R	5bits	0x00000000
RXFLR	Receive FIFO Level Register	0x24	R	5bits	0x00000000
SR	Status Register	0x28	R	5bits	0x00000006
IMR	Interrupt Mask Register	0x2C	R/W	5bits	0x0000001F
ISR	Interrupt Status Register	0x30	R	5bits	0x00000000
RISR	Raw Interrupt Status Register	0x34	R	5bits	0x00000000
TXOICR	Transmit FIFO Overflow Interrupt Clear Register	0x38	R	1bit	0x00000000
RXOICR	Receive FIFO Overflow Interrupt Clear Register	0x3C	R	1bit	0x00000000
RXUICR	Receive FIFO Underflow Interrupt Clear Register	0x40	R	1bit	0x00000000
MSTICR	Multi-Master Interrupt Clear Register	0x44	R	1bit	0x00000000
ICR	Interrupt Clear Register	0x48	R	1bit	0x00000000
DMACR	DMA Control Register	0x4C	R/W	2bits	0x00000000
DMATDLR	DMA Transmit Data Level	0x50	R/W	4bits	0x00000000
DMARDLR	DMA Receive Data Level	0x54	R/W	4bits	0x00000000
IDR	Identification Register	0x58	R	32bits	0x00000000
SSI_COMP_VERSION	Core Kit Version ID	0x5C	R	32bits	0x33302322A
DR (Note 1)	Data Register	0x60-9C	R/W	16bits	0x00000000

(Note 1) Width is given to the address so that the AHB address may do the increment at the burst access by AHB Master like DMA controller, and the memory map is prepared for 16 cycles in 32bits or less width increment type burst, and AddressOffset=0x60-0x9C.

12.4.2. Register Detail

CTRLR0

This register controls the serial data transfer. Writing cannot be done to this register when SSI is enabled. Writing can be enabled for the SSIENR register by disabling SSI.Address Offset : 0x00

Bits	Name	Direction	Reset	Description
15:12	CFS	R/W	0x0	(Reserved)
11	SRL	R/W	0x0	Shift Register Loop Test 0: Normal Mode 1: Test Mode TXD is connected with RXD internally when changing to the test mode, and loop can test.
10	SLV_OE	R/W	0x0	Slave Output Enable This bit is only valid when device is operating as slave. ssi_oe_nOut is set from slave's SSI.Ssi_oe_nOut doesn't actively become it for "1". In Ssi_oe_n, it connects with tri-state I/O, and when this bit is "1", it is in high impedance state. It returns successful when the master does the data transfer to all slaves. After reset, it is necessary to disable this bit with software to be enabled, and to make the device work. 0 : Slave TXD is enabled. 1 : Slave TXD is disabled.
9:8	TMOD	R/W	0x0	Transfer Mode These bits dictate the transfer mode of the serial communication. These bits show data reception or data transmission is taking place. Transmission ONLY Mode Data reception from an external device is invalid. Data are not stored in Receive FIFO and are rewritten on the next transfer. Reception ONLY Mode Data transmission is invalid. After writing in the Transmit FIFO, the data of the same word is sent again for the next transfer period. Transmission & Reception Mode Both data transmission and reception are valid. The data transfer continues until Transmit FIFO empties. The data received from an external device is stored in Receive FIFO, and can be accessed from the host. 00 : Transmission & Reception 01 : Transmission ONLY 10 : Reception ONLY 11 : (Reserved)

CTRLR0 – continued

Bits	Name	Direction	Reset	Description
7	SCPOL	R	0x0	Serial Clock Polarity This bit is only valid when device is using SPI protocol. This bit sets the serial clock polarity of level data transfer. 0: Stopping of Level Data Transfer Low 1 : Stopping of Level Data Transfer High
6	SCPH	R	0x0	Serial Clock Phase This bit is only valid when device is using SPI protocol. 0: Data is taken from the first edge of the serial clock. 1: The serial clock begins a one-cycle toggle after SSI slave line is enabled. Data is taken on the following clock cycle.
5:4	FRF	R	0x0	Frame Format These bits set the protocol to be used. 00 : Motorola, Inc. SPI *This device only supports Motorola, Inc. SPI.
3:0	DFS	R/W	0x7	Data Frame Size The size of the frame can be set to 16 bits or less. 0000: Reserved 0001: Reserved 0010: Reserved 0011: 4-Bit Serial Data Transfer 0100: 5-Bit Serial Data Transfer 0101: 6-Bit Serial Data Transfer 0110: 7-Bit Serial Data Transfer 0111: 8-Bit Serial Data Transfer 1000: 9-Bit Serial Data Transfer 1001: 10-Bit Serial Data Transfer 1010: 11-Bit Serial Data Transfer 1011: 12-Bit Serial Data Transfer 1100: 13-Bit Serial Data Transfer 1101: 14-Bit Serial Data Transfer 1110: 15-Bit Serial Data Transfer 1111: 16-Bit Serial Data Transfer

SSIENR

SSI is disabled or enabled.
Address Offset : 0x08

Bits	Name	Direction	Reset	Description
0	SSI_EN	R/W	0x0	SSI Enable Signal All serial transfers interrupt at once. FIFO is cleared. The control register cannot be set when this signal is enabled.

TXFTLR

TXFTLR sets the threshold of the FIFO memory for Transmission.
Address Offset : 0x18

Bits	Name	Direction	Reset	Description
4: 0	TFT	R/W	0x0	FIFO Threshold for Transmission It is necessary to set this value less than the depth of FIFO. This sets the value to trigger the interrupt.

RXFTLR

RXFTLR sets the threshold of the FIFO memory for Reception.
Address Offset : 0x1C

Bits	Name	Direction	Reset	Description
4: 0	RFT	R/W	0x0	FIFO Threshold for Reception It is necessary to set this value less than the depth of FIFO. This sets the value to trigger the interrupt.

TXFLR

TXFLR indicates how much valid data are to be stored in the FIFO memory for Transmission.
Address Offset : 0x20

Bits	Name	Direction	Reset	Description
4: 0	TXTFL	R	0x0	Available Data in FIFO for Transmission

RXFLR

RXFLR indicates how much valid data are to be stored in the FIFO memory for Reception.
Address Offset : 0x24

Bits	Name	Direction	Reset	Description
4: 0	RXTFL	R	0x0	Available Data in FIFO for Reception

SR

Status Register tells the current FIFO status of the ongoing transfer transaction.
Address Offset : 0x28

Bits	Name	Direction	Reset	Description
5	TXE	R	0x0	Transfer Error When transfer starts, this bit is set to “1” when transfer FIFO is empty. This bit is only used when device operates as slave. Data from previous transfer transaction is sent again to the transmission line. 0: No Error 1 :Transfer error occured.
4	RFF	R	0x0	Receive FIFO is full. This bit is set to “1” when FIFO for Reception is full. 0: NOT FULL 1: FULL
3	RFNE	R	0x0	Receive FIFO is NOT empty. This bit is set to “1” when at least one Reception of FIFO is NOT emptied, after clear is executed.0: Receive FIFO is empty. 1: Receptio nFIFO is NOT empty.
2	TFE	R	0x1	Transmit FIFO is empty. This bit is set to “1” when Transmit FIFO is empty. When Transmit FIFO is not empty, this bit is cleared. 0: Transmit FIFO is NOT empty. 1: Transmit FIFO is empty.
1	TFNF	R	0x1	Transmit FIFO is NOT full. This bit is set to “1” when Transmit FIFO is NOT full. 0: Transmit FIFO is FULL. 1: Transmit FIFO is NOT FULL.
0	BUSY	R	0x0	BUSY Flag This bit is set to “1” when there is an ongoing serial transfer. It is cleared at Idle mode, when SSI is disabled.

IMR

Masking of all the interrupt signals can be done. The MSTIM bit becomes invalid when device operates as a slave.
After reset, masking is not done on the interrupt signal.
Address Offset : 0x2C

Bits	Name	Direction	Reset	Description
4	RXFIM	R/W	0x1	Receive FIFO FULL Interrupt Mask 0: Masking Enabled 1: Masking Disabled
3	RXOIM	R/W	0x1	Receive FIFO Overflow Interrupt Mask 0: Masking Enabled 1: Masking Disabled
2	RXUIM	R/W	0x1	Receive FIFO Underflow Interrupt Mask 0: Masking Enabled 1: Masking Disabled
1	TXOIM	R/W	0x1	Transmit FIFO Overflow Interrupt Mask0: Masking Enabled 1: Masking Disabled
0	TXEIM	R/W	0x1	Transmit FIFO EMPTY Interrupt Mask 0: Masking Enabled 1: Masking Disabled

ISR
Generated Interrupts During Masking
Address Offset : 0x30

Bits	Name	Direction	Reset	Description
4	RXFIS	R	0x0	Receive FIFO FULL Interrupt Mask 0: Interrupt Disabled 1: Interrupt Enabled
3	RXOIS	R	0x0	Receive FIFO Overflow Interrupt Mask 0: Interrupt Disabled 1: Interrupt Enabled
2	RXUIS	R	0x0	Receive FIFO Underflow Interrupt Mask 0: Interrupt Disabled 1: Interrupt Enabled
1	TXOIS	R	0x0	Transmit FIFO Overflow Interrupt Mask 0: Interrupt Disabled 1: Interrupt Enabled
0	TXEIS	R	0x0	Transmit FIFO EMPTY Interrupt Mask 0: Interrupt Disabled 1: Interrupt Enabled

RISR
RISR displays the generated interrupts.
Address Offset : 0x34

Bits	Name	Direction	Reset	Description
4	RXFIR	R	0x0	Receive FIFO FULL Interrupt Mask 0: Interrupt Disabled 1: Interrupt Enabled
3	RXOIR	R	0x0	Receive FIFO Overflow Interrupt Mask 0: Interrupt Disabled 1: Interrupt Enabled
2	RXUIR	R	0x0	Receive FIFO Underflow Interrupt Mask 0: Interrupt Disabled 1: Interrupt Enabled
1	TXOIR	R	0x0	Transmit FIFO Overflow Interrupt Mask 0: Interrupt Disabled 1: Interrupt Enabled
0	TXEIR	R	0x0	Transmit FIFO EMPTY Interrupt Mask 0: Interrupt Disabled 1: Interrupt Enabled

TXOICR
Transmit FIFO Overflow Interrupt Clear Register
Address Offset : 0x38

Bits	Name	Direction	Reset	Description
0	TXOICR	R	0x0	Transmit FIFO Overflow Interrupt Clear Register

RXOICR
Receive FIFO Overflow Interrupt Clear Register
Address Offset : 0x3C

Bits	Name	Direction	Reset	Description
0	RXDICR	R	0x0	Receive FIFO Overflow Interrupt Clear Register

RXUICR
Receive FIFO Underflow Interrupt Clear Register
Address Offset : 0x40

Bits	Name	Direction	Reset	Description
0	RXUICR	R	0x0	Receive FIFO Underflow Interrupt Clear Register

MSTICR
Master Collision Interrupt Clear Register
Address Offset : 0x44

Bits	Name	Direction	Reset	Description
0	MSTICR	R	0x0	Master Collision Interrupt Clear Register

ICR
All Interrupt Clear Register
Address Offset : 0x48

Bits	Name	Direction	Reset	Description
0	ICR	R	0x0	All Interrupt Clear Register

DMACR
DMA Control Register
Address Offset : 0x4C

Bits	Name	Direction	Reset	Description
1	TDMAE	R/W	0x0	DMA Transmission Enable This bit enables data transmission in DMA channel. 0: DMA transmission is disabled. 1: DMA transmission is enabled.
0	RDMAE	R/W	0x0	DMA Reception Enable This bit enables data reception in DMA channel. 0: DMA reception is disabled. 1: DMA reception is enabled.

DMATDLR
DMA Transmission Data Level
Address Offset : 0x50

Bits	Name	Direction	Reset	Description
3:0	DMATDLR	R/W	0x0	DMA Transmission Data Level This register sets the timing in which DMA request is executed. When dma_tx_req is set, it dictates the number of collected FIFO data to be outputted.

DMARDLR
DMA Reception Data Level
Address Offset : 0x54

Bits	Name	Direction	Reset	Description
3:0	DMARDLR	R/W	0x0	The Reception data level This register sets the timing in which DMA request is executed. When dma_rx_req is set, it dictates the number of collected FIFO data to be read.

IDR
Individual Recognition Code
Address Offset : 0x58

Bits	Name	Direction	Reset	Description
31: 0	IDCODE	R	-	SSI Module Identification Number

SSI_COMP_VERION
SSI Version
Address Offset : 0x5C

Bits	Name	Direction	Reset	Description
31: 0	SSI_COMP_VERSION	R	-	SSI Module Version Management Number

DR
SSI has a 16-bit FIFO for transmission and reception. The value of the Receive FIFO can be read by accessing this register. When writing is done, data is written in the Transmission either writing or reading is possible in any address.
Address Offset : 0x60-0x9C

Bits	Name	Direction	Reset	Description
15: 0	DR	RW	0x0	Data Register When writing or reading, operation starts from the right.

13. I2C0/I2C1

13.1. Feature

- I2C serial interface.
- Two speed modes are supported.
- Standard mode (100Kb/s)
- Fast mode (400Kb/s)
- The MASTER SLAVE I2C operation is supported.
  - 7-bit slave address in a 10-bit packet format in both modes.
- 32-steps FIFO is built-in for Transmission and for Reception.
- DMA handshake interface.

13.2. Description

13.2.1. I2C Protocol

Start Condition and Stop Condition protocol

The I2C protocol of DW_apb_I2c is shown below Figure 51:

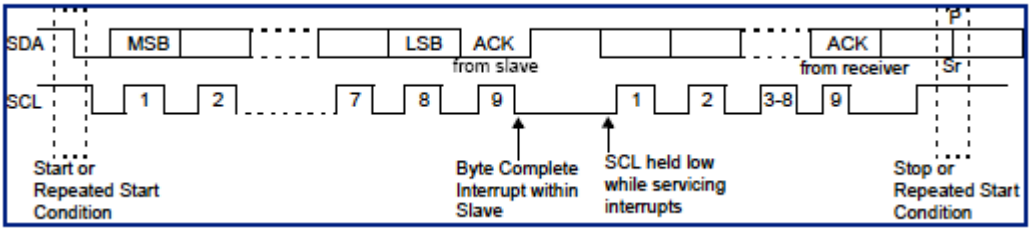


Figure 51. DW_apb_I2c Start and Stop Condition

When the I2C bus is IDLE, SDA and SCL becomes H due to a pull-up resistance set externally. When the communication begins, during SCL is H, SDA transitions from H to L in the master side (start condition). When the communication ends, during SCL is H, SDA transitions from L to H in the master side (stop condition). When SCL is L, the data is transferred inside for every change in SDA.

I2C Protocol – continued

■ **Protocol in Slave Address**

7-bit slave address in a 10-bit packet format in both modes is shown. Moreover, a special 10-bit slave address packet format is shown in the following table.

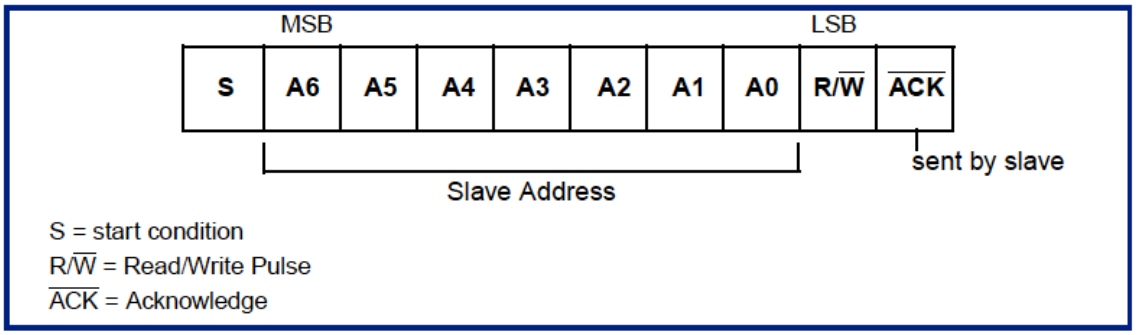


Figure 52. 7-bit Address Format

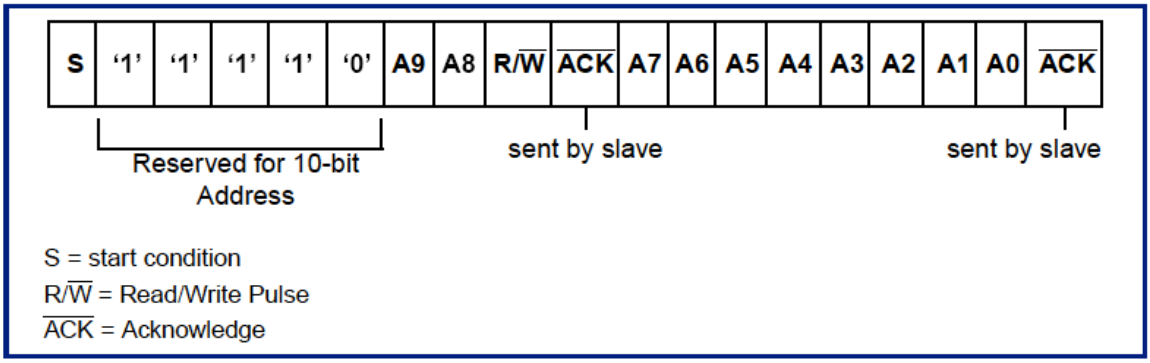


Figure 53. 10-bit Address Format

I^2C Definition of Bits in First Byte

Slave Address	R/W Bit	Description
000_0000	0	General Call Address
000_0000	1	Start Byte: The slave doesn't have the ACK response.
000_0001	x	CBUS Address: The I2C module ignores this access.
000_0010	x	Reserved
000_0011	x	Reserved
000_01xx	x	High-Speed Master Code
111_11xx	x	Reserved
111_10xx	x	10-Bit Slave Addressing (Refer to Figure 52.)

■ **Sending and Receiving Protocol**
Sending and Receiving Protocol is shown.

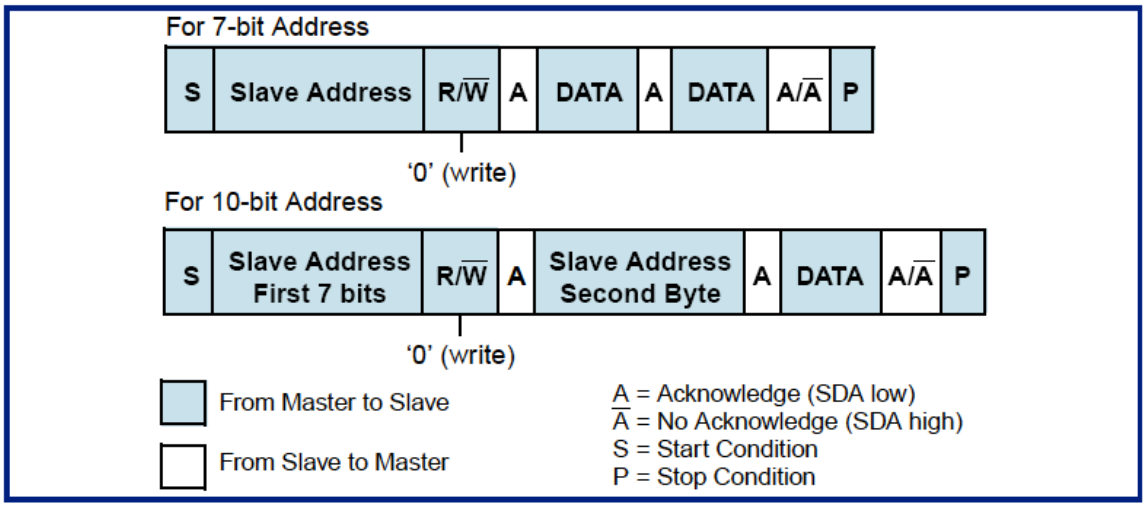


Figure 54. Master-Transmitter Protocol

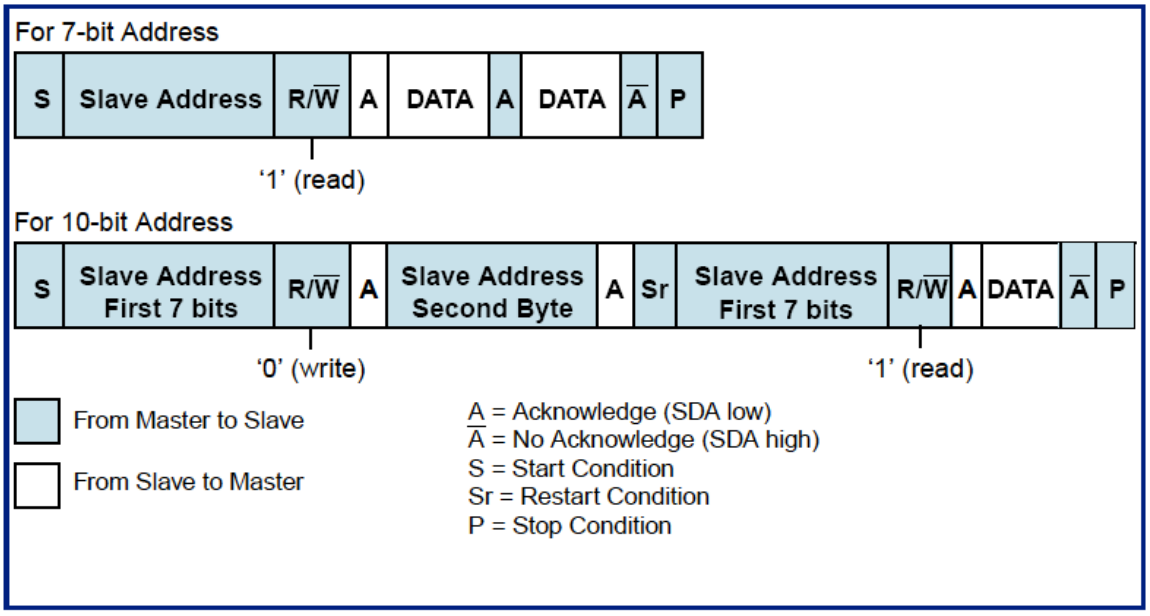


Figure 55. Master-Receiver Protocol

■ **START Byte Forwarding Protocol**
START byte forwarding protocol is shown in Figure 56. START byte forwarding is done according to the following procedures.

Master generates start condition(S).
Master forwards START byte (0000_0001).
Master generates the ACK clock pulse.
There should be no response from the slave. (SDA=H)
Master generates repeated Start condition(Sr).

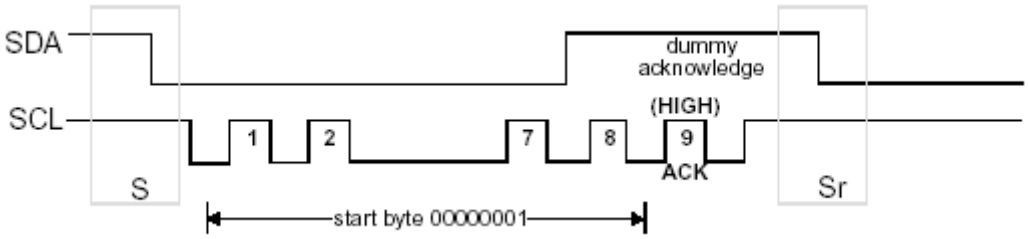


Figure 56. START byte transfer

13.2.2. Arbitration and Clock Generation

■ **Clock synchronization**
The synchronization of the clock is done by controlling SCL from L to H or from H to L using the device with the shortest H period or the device with the longest L period. This is for the case where two or more master is controlling the I2C bus to generate the SCL clock during data transfer.

■ **Arbitration**
Two or more master controlling the I2C bus for data transfer at the same time can happen. Because the transmission level does not correspond to the level of the bus when two or more master sends signal to SDA line during transmission, the data becomes erroneous. As a result, the SDA line should be mediated (arbitration).

13.2.3. Operation mode

Slave mode operation

- Initialization
  The IC_ENABLE register is adjusted to 0.
  The slave address is set to the IC_SAR register.
  A required setting for the IC_CON register is done.
  The IC_ENABLE register is adjusted to one.

- Data Transmission operation procedure(Slave-Transmitter)
  A corresponding address to IC_SAR from the master is forwarded.
  The address and the direction of forwarding are determined by a recognized response.
  The RD_REQ interrupt is generated, and SCL is made L.
  The TX_ABRT interrupt is generated when data has remained in TX_FIFO before reading. The data in the TX_FIFO is then deleted.
  Data is written in the IC_DATA_CMD register. (The CMD bit is 0 always.)
  RD_REQ and TX_ABRT interrupt are cleared.
  SCL is active, and byte data is transmitted.
  Master opens the I2C bus by holding the stop condition or in restart condition.

- Data Reception operation procedure (Slave-Receiver)
  A corresponding address to IC_SAR from master is forwarded.
  The address and the direction of forwarding are determined by a recognized response.
  Data is stored during reception in the reception buffer.
  Status and interrupt bit of the reception buffer are updated.
  The IC_DATA_CMD register is read.
  Master opens the I2C bus by holding the stop condition or in restart condition.

- Bulk transfer
  After the first reading is requested, the data of multiple byte packets can be written in TX_FIFO when it is recognized that the master device requested data reception of multiple byte packets. As a result, RD_REQ interrupts SCL during the requested reading since the second byte becomes unnecessary. When the number of demand bytes from master is less than the number of databytes written in TX_FIFO, the data that remains in TX_FIFO is cleared.

Mastering mode operation

- Initialization
  The IC_ENABLE register is adjusted to 0.
  The slave address is set to the IC_SAR register. (If necessary)
  A setting for the IC_CON register is done.
  The address of the slave device that becomes an object is written in the IC_TAR register, or the START byte and the general call address are set.
  The IC_ENABLE register is adjusted to one.
  This is written in the IC_DATA_CMD register.

- Data sending and receiving operation
  The CMD bit is written when data transmission is done and 0 byte data is written. When data reception is done, one is written in the CMD bit. At this time, the DATA byte is ignored. When data is transmitted, status and the interrupt signal of the Transmission buffer and the Reception buffer are updated.

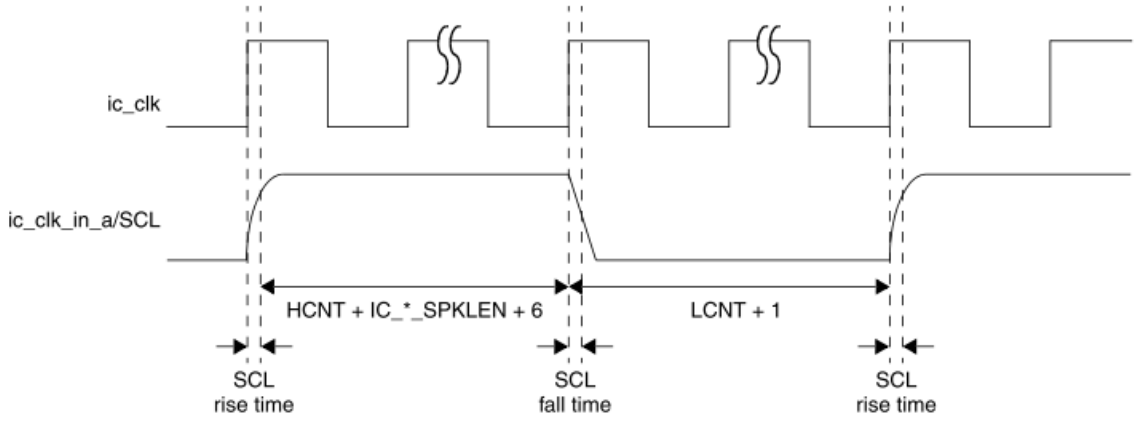
- Clock frequency setting
  Default setting is 109 kHz in standard speed mode and 484kHz in fast speed mode.
  In master mode, it is necessary to set the following registers to an appropriate value.
  IC_SS_SCL_LCNT is used for the maintenance period in idle state of the bus. Secure first the bus line when using it from this state.

Standard Speed Mode Setting Example (99kHz)

Offset	Register	Value	Description
0x14	IC_SS_SCL_HCNT	0x1B7 (439)	≧ 0x180 (384= 96MHz x 4.0us)
0x18	IC_SS_SCL_LCNT	0x203 (515)	≧ 0x1C4 (452= 96MHz x 4.7us)

fast speed mode setting example (396kHz)

Offset	Register	Value	Description
0x1C	IC_FS_SCL_HCNT	0x4B (75)	≧ 0x3A (58= 96MHz x 0.6us)
0x20	IC_FS_SCL_LCNT	0x9F (159)	≧ 0x7D (125= 96MHz x 1.3us)



SCL_High_time = [(HCNT + IC_*_SPKLEN + 6) * ic_clk] + SCL_Fall_time
SCL_Low_time = [(LCNT + 1) * ic_clk] - SCL_Fall_time + SCL_Rise_time

Figure 57. Generated SCL

13.2.4. Spike Control

A separate internal counter is installed in SCL and SDA, the number of clock pulses is counted, and the signal is taken at any value of IC_*_SPKLEN. This is the function to filter the spike of SCL and SDA. It is shown in Figure 58.

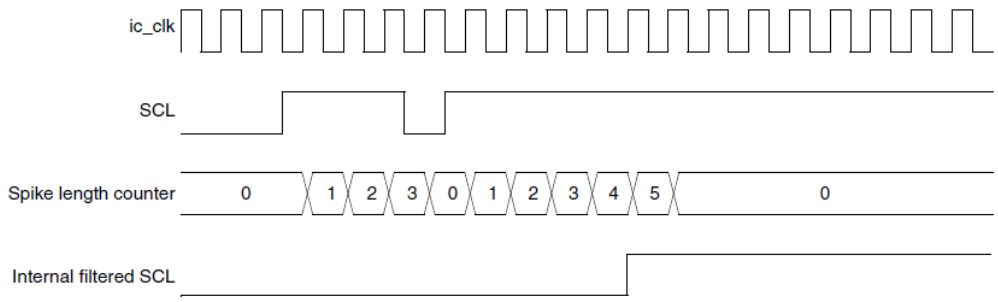
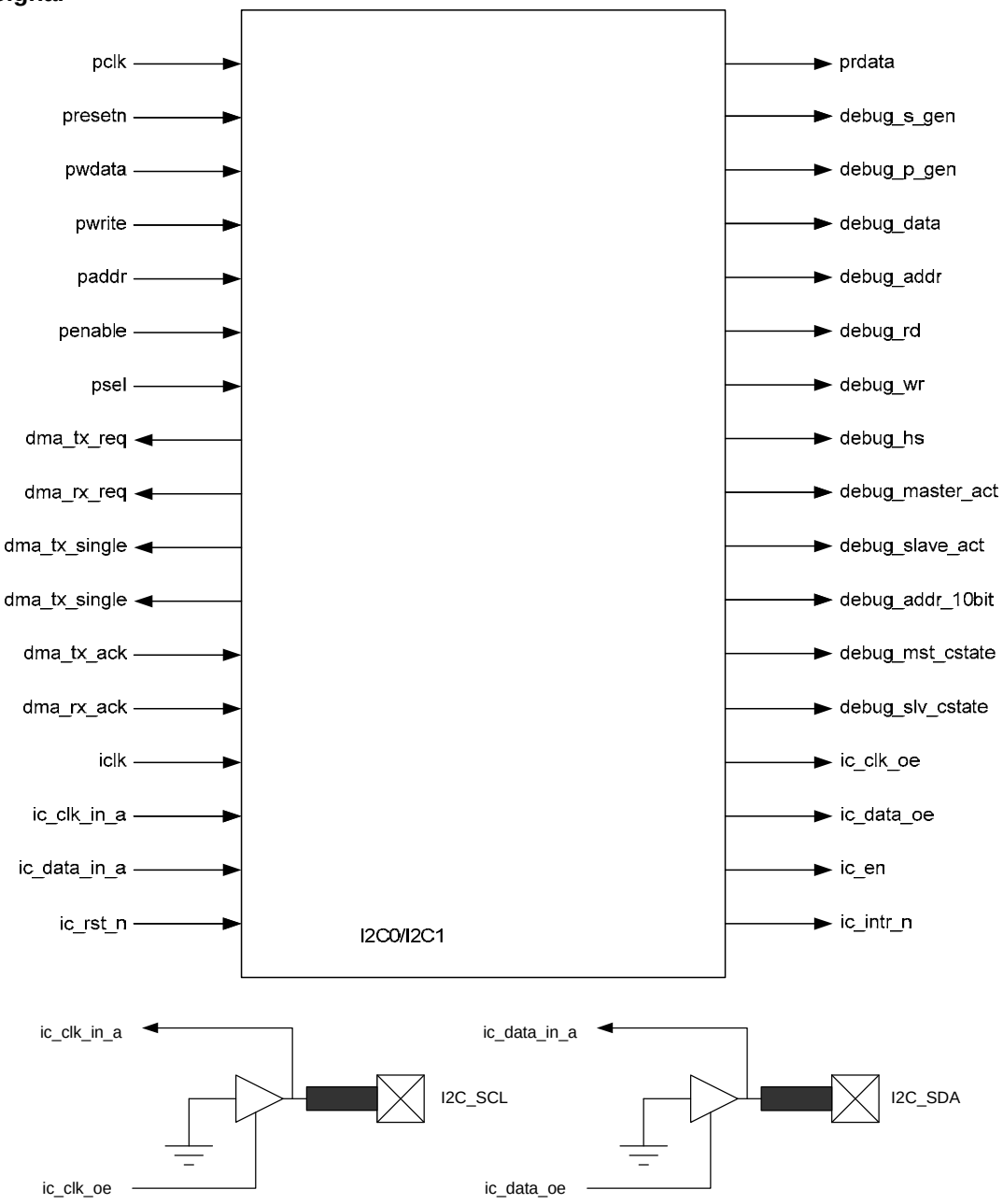


Figure 58. Spike Filter Example

13.3. I/O Signal



Terminal name	I/O	Description	Connection
pclk	In	APB Clock	Clock Gen
presetn	In	APB Reset	Reset Gen
psel	In	APB Peripheral Select Signal	APB
paddr[7:0]	In	APB Address	APB
pwdata[31:0]	In	APB Write Data	APB
pwrite	In	APB Write Signal	APB
penable	In	APB Enable Signal	APB
prdata[31:0]	Out	APB Read Data	APB
ic_clk	In	The Source Clock for I2C	Clock GEN
ic_clk_in_a	In	I2C Forwarding Clock SCL (Asynchronous System)	I/O
ic_data_in_a	In	Data for I2C (Asynchronous System).	I/O
ic_rst_in	In	Reset for I2C	Reset GEN
ic_clk_oe	Out	I2C Forwarding Clock SCL	I/O
ic_data_oe	Out	Data Out for I2C	I/O
ic_en	Out	I2C Interface Enable Signal Output	OPEN
Ic_intr_n	Out	The Interrupt Signal	INTR
debug_*	Out	The Debug Signal	OPEN
dma_tx_req	Out	DMA Request for Transmit FIFO	DMA
dma_rx_req	Out	DMA Request for Receive FIFO	DMA
dma_tx_single	Out	Transmit FIFO Status Signal	DMA
dma_rx_single	Out	Receive FIFO Status Signal	DMA
dma_tx_ack	In	DMA Transmission ACK	DMA
dma_rx_ack	In	DMA Reception ACK	DMA

13.4. Register

13.4.1. Memory Map

The composition of the memory map is shown below.

Mode：master mode(M)／slave mode(S)

Name	Offset	R/W	Width	Mode	Description
IC_CON	0x00	R/W	7	M/S	I2C Control Register Initial value：0x0000_007D (Def：IC_SLAVE_DISABLE, IC_RESTART_EN, IC_10BITADDR_MASTER, IC_10BITADDR_SLAVE, IC_MAX_SPEED_MODE, IC_MASTER_MODE)
IC_TAR	0x04	R/W	12	M	I2C Target Address Register Initial value：0x0000_0855 (Def：IC_10BITADDR_MASTER 0 0 IC_DEFAULT_TAR_SLAVE_ADDR)
IC_SAR	0x08	R/W	10	S	I2C Slave Address Register Initial value：0x0000_0055 (Def：IC_DEFAULT_SLAVE_ADDR)
IC_DATA_CMD	0x10	R/W	8(R) 9(W)	M/S	I2C Sending and Receiving Data Buffer & Command Register Initial value：0x0000_0000
IC_SS_SCL_HCNT	0x14	R/W	16	M	During Standard Speed Mode SCL clock H section setting register Initial value： 0x0000_0190 (Def：IC_SS_SCL_HIGH_COUNT)
IC_SS_SCL_LCNT	0x18	R/W	16	M	During Standard Speed Mode SCL clock L section setting register Initial value： 0x0000_01D6 (Def：IC_SS_SCL_LOW_COUNT)
IC_FS_SCL_HCNT	0x1C	R/W	16	M	During Fast Speed Mode SCL clock H section setting register Initial value： 0x0000_003C (Def：IC_FS_SCL_HIGH_COUNT)
IC_FS_SCL_LCNT	0x20	R/W	16	M	During Fast Speed Mode SCL clock L section setting register Initial value： 0x0000_0082 (Def：IC_FS_SCL_LOW_COUNT)
IC_INTR_STAT	0x2C	R	12	M/S	I2C Interrupt Status Register Initial value：0x0000_0000
IC_INTR_MASK	0x30	R/W	12	M/S	I2C Interrupt Mask Register Initial value：0x0000_08FF
IC_RAW_INTR_STAT	0x34	R	12	M/S	I2C Interrupt Status Register Initial value：0x0000_0000
IC_RX_TL	0x38	R/W	8	M/S	I2C Receive FIFO Status Hold Register Initial value：0x0000_0000 (Def：IC_RX_TL)
IC_TX_TL	0x3C	R/W	8	M/S	I2C Transmit FIFO Status Hold Register Initial value：0x0000_0000 (Def：IC_TX_TL)
IC_CLR_INTR	0x40	R	1	M/S	All Interrupt Clear Register Initial value：0x0000_0000
IC_CLR_RX_UNDER	0x44	R	1	M/S	Reception Under Interrupt Clear Register Initial value：0x0000_0000
IC_CLR_RX_OVER	0x48	R	1	M/S	Reception Over Interrupt Clear Register Initial value：0x0000_0000
IC_CLR_TX_OVER	04C	R	1	M/S	Transmission Over Interrupt Clear Register Initial value：0x0000_0000
IC_CLR_RD_REQ	0x50	R	1	S	Reading Request Interrupt Clear Register Initial value：0x0000_0000

Memory Map – continued

Name	Offset	R/W	Width	Mode	Description
IC_CLR_TX _ABRT	0x5	R	1	M/S	Transmission Abort Interrupt Clear Register Initial value：0x0000_0000
IC_CLR_RX _DONE	0x58	R	1	S	Reception Completion Interrupt Clear Register Initial value：0x0000_0000
IC_CLR _ACTIVITY	0x5C	R	1	M/S	Activity Interrupt Clear Register Initial value：0x0000_0000
IC_CLR STOP_DET	0x60	R	1	M/S	Stop Detection Interrupt Clear Register Initial value：0x0000_0000
IC_CLR START_DET	0x64	R	1	M/S	Start Detection Interrupt Clear Register Initial value：0x0000_0000
IC_CLR GENCALL	0x68	R	1	S	GEN_CALL Interrupt Clear Register Initial value：0x0000_0000
IC_ENABLE	0x6C	R/W	2	M/S	I2C Enable Register Initial value：0x0000_0000
IC_STATUS	0x70	R	7	M/S	I2C Status Register Initial value：0x0000_0006
IC_TXFLR	0x74	R	6	M/S	Transmit FIFO Level Register Initial value：0x0000_0000
IC_RXFLR	0x78	R	6	M/S	Receive FIFO Level Register Initial value：0x0000_0000
IC_SDA_HOLD	0x7C	R/W	16		Length Setting of SDA Hold Time Register Initial value：0x0000_0001
IC_TX_ABRT _SOURCE	0x80	R/W	32	M/S	I2C Transmission Abort Status Register Initial value：0x0000_0000
IC_DMA_CR	0x88	R/W	2	M/S	The Control Register for DMA Handshake Interface for Sending and Receiving Initial value：0x0000_0000
IC_DMA_TDLR	0x8C	R/W	5	M/S	The FIFO Threshold Register for Transmission Initial value：0x0000_0000
IC_DMA_RDLR	0x90	R/W	5	M/S	The FIFO Threshold Register for Reception Initial value：0x0000_0000
IC_SDA_SETUP	0x94	R/W	8		I2C SDA Setup Register Initial value:0x0000_0064
IC_ACK_GENERA L_CALL	0x98	R/W	1		I2C General Call Ack Response Setting Register Initial value:0x0000_0001
IC_ENABLE_STAT US	0x9C	R	3		I2C Enable Status Register Initial value：0x0000_0000
IC_FS_SPKLEN	0xA0	R/W	8		Standard/Fast Mode Spike Control Limit Value Initial value：0x0000_0001

13.4.2. Register Detail.

Detailed content of the register is shown below.

IC_CON (It is possible to set it only at IC_ENABLE=0.)
I2C control register. This register is writable only in I2C disabled state (IC_ENABLE=0).
Address Offset : 0x00

Bits	Name	R/W	Default	Mode	Description
31:7	Reserved	N/A	-	-	-
6	IC_SLAVE_DISABLE	R/W	0	ー	0: The slave function is enabled 1: Slave function disabled
5	IC_RESTART_EN	R/W	1	M	1: Restart transmission is possible
4	IC_10BITADDR_MASTER	R/W	1	M	Address Mode Setting 0: 7 bits 1: 10 bits
3	IC_10BITADDR_SLAVE	R/W	1	S	Address Mode Setting 0: 7 bits 1: 10 bits
2:1	IC_MAX_SPEED_MODE	R/W	0x2	M	Speed Mode Setting 0: No permission (Fast Speed Mode) 1: Standard Speed Mode 2:Fast speed mode 3: Fast Speed Mode (Not Connected to High Speed Mode)
0	IC_MASTER_MODE	R/W	1	ー	0: Master function disabled 1: Master function is enabled

IC_TAR (It is possible to set it only at IC_ENABLE=0.)
Target address setting register. This register is writable only in I2C disabled state (IC_ENABLE=0).
Address Offset : 0x04

Bits	Name	R/W	Default	Description
31:12	Reserved	N/A	-	-
11	SPECIAL	R/W	0	1: I2C special command execution set by GC_OR_START bit
10	GC_OR_START	R/W	0	0: General Call Address 1: Start byte
9:0	IC_TAR	R/W	0x055	Target Address

IC_SAR (It is possible to set it only at IC_ENABLE=0.)
Slave address setting register. This register is writable only in I2C disabled state (IC_ENABLE=0).
Address Offset : 0x08

Bits	Name	R/W	Default	Description
31:10	Reserved	N/A	-	-
9:0	IC_SAR	R/W	0x055	Slave Address

IC_DATA_CMD
The I2C data transfer register
Address Offset : 0x10

Bits	Name	R/W	Default	Description
31:9	Reserved	N/A	-	-
8	CMD	R/W	0	0 during write: transmission setting 1: 0 during read
7:0	DAT	R/W	0x00	I2C bus sending and receiving data

IC_SS_SCL_HCNT (It is possible to set it only at IC_ENABLE=0.)
Setting for high pulse width of SCL during I2C standard speed mode
Address Offset : 0x14

Bits	Name	R/W	Default	Description
31:16	Reserved	N/A	-	-
15:0	IC_SS_SCL_HCNT	R/W	0x0190	Minimum value of SCL clock H section at standard mode: 6

IC_SS_SCL_LCNT (It is possible to set it only at IC_ENABLE=0.)
Setting for low pulse width of SCL during I2C standard speed mode
Address Offset : 0x18

Bits	Name	R/W	Default	Description
31:16	Reserved	N/A	-	-
15:0	IC_SS_SCL_LCNT	R/W	0x01d6	SCL clock L section at standard mode Minimum value：8

IC_FS_SCL_HCNT (It is possible to set it only at IC_ENABLE=0.)
Setting for high pulse width of SCL during I2C fast speed mode
Address Offset : 0x1C

Bits	Name	R/W	Default	Description
31:16	Reserved	N/A	-	-
15:0	IC_FS_SCL_HCNT	R/W	0x003c	SCL clock H section during fast mode Minimum value：6

IC_FS_SCL_LCNT (It is possible to set it only at IC_ENABLE=0.)
Setting for low pulse width of SCL during I2C fast speed mode
Address Offset : 0x20

Bits	Name	R/W	Default	Description
31:16	Reserved	N/A	-	-
15:0	IC_FS_SCL_LCNT	R/W	0x0082	SCL clock L section during fast mode Minimum value：8

IC_INTR_STAT
During interrupt mask state, the generated interrupt is updated in this register.
Address Offset : 0x2C

Bits	Name	R/W	Default	Description
31:12	Reserved	N/A	-	-
11	R_GEN_CALL	R	0	General Call Request Interrupt 0: No reception 1: General call request in reception
10	R_START_DET	R	0	Begin of Transmission Interrupt 0: No start condition 1: Start condition detected
9	R_STOP_DET	R	0	End of Transmission Interrupt When the stop condition is detected by the I2C protocol, it is set. 0: No stop condition 1: Stop condition detected
8	R_ACTIVITY	R	0	Interrupt During Transmission This register is set during I2C transmission. Value remains until it is possible to clear from the idle state. Reset condition: ・I2C error. ・IC_CLR_ACTIVITY register read ・IC_CLR_INTR register read ・System reset 0: No transmission 1: Initial transmission during I2C activity
7	R_RX_DONE	R	0	Reception Complete Interrupt When there is NACK from the I2C master during transmission, this bit is set. 0: Incomplete reception 1: Complete reception
6	R_TX_ABRT	R	0	Transmission Abort Interrupt The Transmission abort occurs when there is NACK after first byte is transmitted (I2C master mode). Refer to IC_TX_ABRT_SOURCE for the set condition. 0: No abort 1: Transmission abort
5	R_RD_REQ	R	0	Reception Request Interrupt This register is set when there is reception request (read) from other I2C masters in I2C slave mode. (The I2C bus maintains its value until it is changed to waiting state) 0: No request 1: Read request
4	R_TX_EMPTY	R	0	Empty Transmission Buffer Interrupt 0: Transmission buffer level > IC_TX_TL 1: Transmission buffer level ≦IC_TX_TL
3	R_TX_OVER	R	0	Transmission Buffer Overflow Interrupt 0: No overflow.

Bits	Name	R/W	Default	Description
				1: Transmission buffer overflow
2	R_RX_FULL	R	0	Reception Buffer Full Interrupt 0: Reception buffer level ≦IC_RX_TX 1: Reception buffer level > IC_RX_TL
1	R_RX_OVER	R	0	Reception Buffer Overflow Interrupt 0: No overflow. 1: Reception buffer overflow
0	R_RX_UNDER	R	0	Reception Buffer Underflow Interrupt Set when the reception buffer level = 0. Read IC_DATA_CMD register

IC_INTR_MASK

The interrupt mask register
Write 0 to mask the interrupt
Address Offset : 0x30

Bits	Name	R/W	Default	Description
31:12	Reserved	N/A	-	-
11	M_GEN_CALL	R/W	1	General Call Demand Interrupt Mask 0: Mask interrupt 1: Mask none
10	M_START_DET	R/W	0	Start Transmission Interrupt Mask 0: Mask interrupt 1: Mask none
9	M_STOP_DET	R/W	0	End Transmission Interrupt Mask 0: Mask interrupt 1: Mask none
8	M_ACTIVITY	R/W	0	Interrupt Mask During Transmission 0: Mask interrupt 1: Mask none
7	M_RX_DONE	R/W	1	Reception Completion Interrupt Mask 0: Mask interrupt 1: Mask none
6	M_TX_ABRT	R/W	1	Transmission Abort Interrupt Mask 0: Mask interrupt 1: Mask none
5	M_RD_REQ	R/W	1	Reception Request Interrupt Mask 0: Mask interrupt 1: Mask none
4	M_TX_EMPTY	R/W	1	Transmission Buffer Empty Interrupt Mask 0: Mask interrupt 1: Mask none
3	M_TX_OVER	R/W	1	Transmission Buffer Overflow Interrupt Mask 0: Mask interrupt 1: Mask none
2	M_RX_FULL	R/W	1	Reception Buffer Full Interrupt Mask 0: Mask interrupt 1: Mask none
1	M_RX_OVER	R/W	1	Reception Buffer Overflow Interrupt Mask 0: Mask interrupt 1: Mask none
0	M_RX_UNDER	R/W	1	Reception Buffer Underflow Interrupt Mask 0: Mask interrupt 1: Mask none

IC_RAW_INTR_STAT
Generated Interrupt
Address Offset : 0x34

Bits	Name	R/W	Default	Mode	Description
31:12	Reserved	N/A	-	-	-
11	GEN_CALL	R	0	S	General Call Demand Interrupt 0: No response 1: General call request response
10	START_DET	R	0	M/S	Beginning of Transmission Interrupt 0: Start condition not detected 1: Start condition detected
9	STOP_DET	R	0	M/S	End of Transmission Interrupt 0: Stop condition not detected 1: Stop condition detected
8	ACTIVITY	R	0	M/S	Interrupt During Transmission This register is set during I2C transmission. Value remains until it is possible to clear from the idle state. Reset condition: ・I2C error. ・IC_CLR_ACTIVITY register read ・IC_CLR_INTR register read ・System reset 0: No transmission 1: Initial transmission during I2C activity
7	RX_DONE	R	0	S	Reception Complete Interrupt When there is NACK from the I2C master during transmission, this bit is set. 0: Incomplete reception 1: Complete reception
6	TX_ABRT	R	0	M/S	Transmission Abort Interrupt The Transmission abort occurs when there is NACK after first byte is transmitted (I2C master mode). Refer to IC_TX_ABRT_SOURCE for the set condition. 0: No abort 1: Transmission abort
5	RD_REQ	R	0	S	Reception Request Interrupt This register is set when there is reception request (read) from other I2C masters in I2C slave mode. (The I2C bus maintains its value until it is changed to waiting state) 0: No request 1: Read request

IC_RAW_INTR_STAT – continued

Bits	Name	R/W	Default	Mode	Description
4	TX_EMPTY	R	0	M/S	Empty Transmission Buffer Interrupt 0: Transmission buffer level > IC_TX_TL 1: Transmission buffer level ≦IC_TX_TL
3	TX_OVER	R	0	M/S	Transmission Buffer Overflow Interrupt 0: No overflow on transmission buffer 1: Transmission buffer overflow
2	RX_FULL	R	0	M/S	Reception Buffer Full Interrupt 0: Reception buffer level ≦IC_RX_TX 1: Reception buffer level > IC_RX_TL
1	RX_OVER	R	0	M/S	Reception Buffer Overflow Interrupt 0: No overflow on reception buffer 1: Reception buffer overflow
0	RX_UNDER	R	0	M/S	Set when there are Reception buffer level =0 IC_DATA_CMD register reading

IC_RX_TL
Memory Threshold Setting for Receive FIFO
Address Offset : 0x38

Bits	Name	R/W	Default	Description
31:8	Reserved	N/A	-	-
7:0	RX_TL	R	0x00	Threshold for RX_FULL Interrupt

IC_TX_TL
Memory Threshold Setting for Transmit FIFO
Address Offset : 0x3C

Bits	Name	R/W	Default	Description
31:8	Reserved	N/A		
7:0	TX_TL	R	0x00	Threshold for TX_EMPTY Interrupt

IC_CLR_INTR
This register clears all interrupts.
Address Offset : 0x40

Bits	Name	R/W	Default	Description
31:1	Reserved	N/A	-	-
0	CLR_INTR	R	0	All the interrupt clears after reading.

IC_CLR_RX_UNDER
Set this register when IC_DATA_CMD is read to empty Receive FIFO and clears interrupt.
Address Offset : 0x44

Bits	Name	R/W	Default	Description
31:1	Reserved	N/A	-	-
0	CLR_RX_UNDER	R	0	The RX_UNDER interrupt clears after reading.

IC_CLR_RX_OVER
This register clears the interrupt generated when data is done from the I2C interface to Full ReceptionFIFO in Reception.
Address Offset : 0x48

Bits	Name	R/W	Default	Description
31:1	Reserved	N/A	-	-
0	CLR_RX_OVER	R	0	The RX_OVER interrupt is cleared after reading.

IC_CLR_TX_OVER
This register clears the interrupt set when IC_DATA_CMD is written in Full TransmissionFIFO.
Address Offset : 0x4C

Bits	Name	R/W	Default	Description
31:1	Reserved	N/A	-	-
0	CLR_TX_OVER	R	0	The TX_OVER interrupt is cleared after reading.

IC_CLR_RD_REQ
This register clears the interrupt when there is reception request from other I2C masters (in slave mode).
Address Offset : 0x50

Bits	Name	R/W	Default	Description
31:1	Reserved	N/A	-	-
0	CLR_RD_REQ	R	0	The RD_REQ interrupt is cleared after reading.

IC_CLR_TX_ABRT
This register clears the interrupt generated when transmission is aborted.
Address Offset : 0x54

Bits	Name	R/W	Default	Description
31:1	Reserved	N/A	-	-
0	CLR_TX_ABRT	R	0	IC_TX_ABRT_SOURCE register clears the interrupt by reading TX_ABRT.

IC_CLR_RX_DONE
This register clears the interrupt when reception response is completed during transmission as I2C slave.
Address Offset : 0x58

Bits	Name	R/W	Default	Description
31:1	Reserved	N/A	-	-
0	CLR_RX_DONE	R	0	The RX_DONE interrupt is cleared.

IC_CLR_ACTIVITY
This register clears the interrupt during the start of I2C interface transmission.
Address Offset : 0x5C

Bits	Name	R/W	Default	Description
31:1	Reserved	N/A	-	-
0	CLR_ACTIVITY	R	0	The ACTIVITY interrupt is cleared.

IC_CLR_STOP_DET
This register clears the interrupt set at the stop condition in the I2C interface.
Address Offset : 0x60

Bits	Name	R/W	Default	Description
31:1	Reserved	N/A	-	-
0	CLR_STOP_DET	R	0	The STOP_DET interrupt is cleared after reading.

IC_CLR_START_DET
This register clears the interrupt set at the start condition in the I2C interface.
Address Offset :1 0x64

Bits	Name	R/W	Default	Description
31:1	Reserved	N/A	-	-
0	CLR_START_DET	R	0	The START_DET interrupt is cleared after reading.

IC_CLR_GEN_CALL
This register clears the interrupt set by the general call.
Address Offset : 0x68

Bits	Name	R/W	Default	Description
31:1	Reserved	N/A	-	-
0	CLR_GEN_CALL	R	0	The GEN_CALL interrupt is cleared after reading.

IC_ENABLE
This register enables I2C interface. Please disable after transfger in the I2C interface ends.
Address Offset : 0x6C

Bits	Name	R/W	Default	Description
31:1	Reserved	N/A		
0	ENABLE	R/W	0	0: I2C is disabled. 1: I2C is enabled.

IC_STATUS
The current state of I2C transmission and the state of FIFO.
Address Offset : 0x70

Bits	Name	R/W	Default	Description
31:5	Reserved	N/A	-	-
4	RFF	R	0	0: Receive FIFO is not full. 1: Receive FIFO is full.
3	RFNE	R	0	0: Receive FIFO is full. 1: Receive FIFO has data.
2	TFE	R	1	0: Transmit FIFO is not empty. 1: Transmit FIFO is full.
1	TFNF	R	1	0: Transmit FIFO is full. 1: Transmit FIFO is not full.
0	ACTIVITY	R	0	0: Idle 1: I2C is in transmission state

IC_TXFLR
The current state of the FIFO memory for transmission.
Address Offset : 0x74

Bits	Name	R/W	Default	Description
31:7	Reserved	N/A	-	-
5:0	TXFLR	R	0x0	Transmission buffer level (0 to 32)

IC_RXFLR
The current state of the FIFO memory for reading.
Address Offset : 0x78

Bits	Name	R/W	Default	Description
31:4	Reserved	N/A	-	-
5:0	RXFLR	R	0x0	Reception buffer level(0 to 32)

IC_SDA_HOLD

Length setting of SDA Hold Time register. The unit is ic_clk.

Address Offset : 0x7C

Bits	Name	R/W	Default	Description
31:16	Reserved	N/A	-	-
15:0	IC_SDA_HOLD	R/W	0x01	SDA Hold Time setting

IC_TX_ABRT_SOURCE

The I2C Transmission abort register

Address Offset : 0x80

Bits	Name	R/W	Default	Mode	Description
31:16	Reserved	N/A	-	-	-
15	ABRT_SLVRD_INTX	R	0	S	If CMD=1 after the Reception request is received from the master, this bit is set. 0: No Abort 1: Abort
14	ABRT_SLV_ARBLOST	R	0	S	When arbitration doesn't permit communication, this bit is set (Bit 12 is set at the same time). 0: No Abort 1: Abort
13	ABRT_SLVFLUSH_TXFIFO	R	0	S	The buffer is cleared when there is data in the transmission buffer when the reception request is received. Then this bit is set.0: No Abort 1: Abort
12	ABRT_LOST	R	0	M/S	When arbitration doesn't permit communication from master devices or when bit 14 is set, this bit is also set. 0: No Abort 1: Abort
11	ABRT_MASTER_DIS	R	0	―	When the function that disables the master is set, this bit is also set 0: No Abort 1: Abort
10	ABRT_10B_RD_NORSTRT	R	0	M	In 10-bit address mode, when the read command is sent and the restart function is in disabled state (IC_RESTART_EN=0), this bit is set. 0: No Abort 1: Abort
9	ABRT_SBYTE_NORSTRT	R	0	M	When the START byte is sent during transmission using the IC_TAR register and the restart function is in disabled state, this bit is set. Transmission using the I2C bus is not done at this time. 0: No Abort 1: Abort
8	ABRT_HS_NORSTRT	R	0	―	0 always
7	ABRT_SBYTE_ACKDET	R	0	M	This bit is set when there ACK response during transmission of START byte (abnormal operation). 0: No Abort 1: Abort
6	ABRT_HS_ACKDET	R	0	―	Fixed to Low

IC_TX_ABRT_SOURCE – continued

Bits	Name	R/W	Default	Mode	Description
5	ABRT_GCALL_READ	R	0	M	When the reading command is sent when the General call is sent, it is set. 0: No Abort 1: Abort
4	ABRT_GCALL_NOACK	R	0	M	It is set when there is no ACK response to the General call. 0: No Abort 1: Abort
3	ABRT_TXDATA_NOACK	R	0	M	It is set when there is no ACK response for data Transmission. 0: No Abort 1: Abort
2	ABRT_10ADDR2_NOACK	R	0	M	It is set when there is no ACK response to Transmission of ten bit address mode in the second the byte in address. 0: No Abort 1: Abort
1	ABRT_10ADDR1_NOACK	R	0	M	It is set when there is no ACK response to Transmission of ten bit address mode in the first the byte in address. 0: No Abort 1: Abort
0	ABRT_7B_ADDR_NOACK	R	0	M	It is set when there is no ACK response to address Transmission of seven bit address mode. 0: No Abort 1: Abort

DMACR

The DMA control register

Address Offset : 0x88

Bits	Name	Direction	Reset	Description
1	TDMAE	R/W	0x0	Transmit DMA is enable. The DMA channel is turned on and off with this bit. 0: Transfer DMA is disable 1: Transfer DMA is enable
0	RDMAE	R/W	0x0	Receive DMA is enable. The DMA channel is turned on and off with this bit. 0: Reception DMA is disable 1: Reception DMA is enable

DMATDLR

The DMA transmission data level

Address Offset : 0x8C

Bits	Name	Direction	Reset	Description
4:0	DMATDLR	R/W	0x0	Transmission Data Level Timing in which the DMA request is done. When equal, TDAME=1, dma_tx_req signal is outputted based on the number of data collected in FIFO as the set value.

IC_DMA_RDLR

The FIFO threshold register for reception

Address Offset : 0x90

Bits	Name	Direction	Reset	Description
31:5	Reserved	N/A	-	-
4:0	DMARDLR	R/W	0x0	Reception Data Level Timing in which the DMA request is done. dma_rx_req signal is outputted when the data (value + 1) collected in FIFO becomes equal and RDAME=1.

IC_SDA_SETUP
(Possible to modify only if IC_ENABLE 0=0)
SDA setup timing register setting (The unit is ic_clk)
Address Offset : 0x94

Bits	Name	Direction	Reset	Description
31:8	Reserved	N/A	-	-
7:0	SDA_SETUP	R/W	0x64	This register sets SDA setup timing. Minimum value is two.

IC_ACK_GENERAL_CALL
The general call response (ACK) setting register
Address Offset : 0x98

Bits	Name	Direction	Reset	Description
31:1	Reserved	N/A	-	-
0	ACK_GEN_CALL	R/W	0x1	When general call is done during reception, the ACK response is generated.

IC_ENABLE_STATUS
When IC_ENABLE 0 is set from 1 to 0, the hardware status of I2C can be read.
Address Offset : 0x9C

Bits	Name	Direction	Reset	Description
31:3	Reserved	N/A	-	-
2	SLV_RX_DATA_LOST	R	0x0	When I2C slave mode reception is disabled, data byte reception status can be read. 0: Data is not reception when disabled. 1: Data is reception when disabled.
1	SLV_DISABLED_WHHILE_BUSY	R	0x0	The address byte and the data byte are set for I2C to be disabled during reception by the I2C slave mode.
0	IC_EN	R	0x0	0: I2C is disabled. 1: I2C is active.

IC_FS_SPKLEN
The spike control limit value setting register of the fast mode or standard mode (The unit is ic_clk)
Address Offset : 0xA0

Bits	Name	Direction	Reset	Description
31:8	Reserved	N/A	-	-
7:0	IC_FS_SPKLEN	R/W	0x1	The width of the filtered glitch: Minimum value is one.

14. UART0/UART1

14.1. Feature

- It is connected with the APB interface of the AMBA standard.
- Its system clock of DW_apb_uart is independent to the APB interface clock.
- The width of the APB bus is 32 bits.
- Its function is based on IS16550.
- The width of transmitted and received data is fixed to 8 bits.
- The width of FIFO data is fixed to 8 bits.
- The depth of Transfer Source FIFO is 32 bits,
- FIFO can be selected, enabled and disabled.
- It has Auto-Flow Control Mode similar to Standard IS16750 (Only in UART0).
- It has the Transmitter Holding Register Empty (THRE) Interrupt Mode.
- The baud rate can be calculated by:

$$\text{baud rate} = \frac{\text{serial clock frequence}}{16 \times \text{divisor}}$$

- It uses 96 MHz serial clock.
- It uses handshake for Transmission and Reception in the DMA interface.

14.2. Description

14.2.1. UART Serial Protocol

The serial data in one transaction of the DW_apb_uart circuit format is shown in Figure 59.

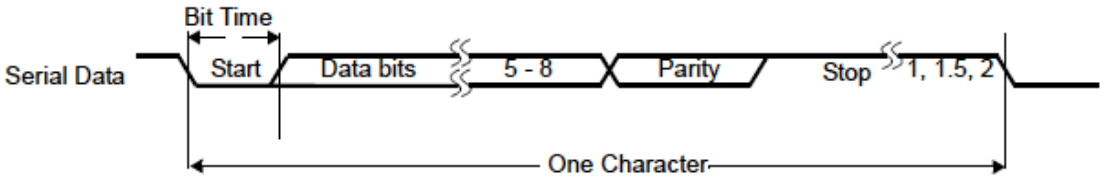


Figure 59. Serial Data Format

After the start bit, the data bit is sent from LSB. The parity bit that does the error check of the received data is added before the stop bit after MSB of data. Moreover, the parity bit is an option. Stop bits are 1, 1.5 or 2 bits, and it continues after the parity bit. The width of the sending and receiving data or parity, etc. can be set by the LCR register. As for all transmission bits, transmission is done accurately at same intervals of time. This is called Bit Period or Bit Time. 1 Bit time is equal to 16 Baud clock. The sample point of serial data reception is shown in Figure 60.

UART Serial Protocol – continued

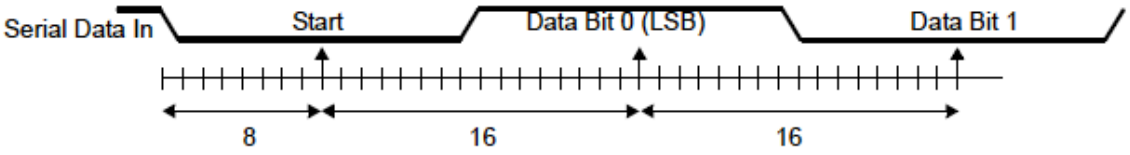


Figure 60. Sample Point of Received Serial Data

The received data is 16 cycles from the midpoint of the start bit after baud clock.
Out can do baud clock by the option. The timing diagram of baud clock is shown in Figure 61. In DW_apb_uart, baud clock is controlled by sclk or pclk and Divisor Latch Register(=divisor). Moreover, the frequency of baud clock can be shown by the following expressions:

$$\text{baud rate} = \frac{\text{serial clock frequence}}{16 \times \text{divisor}}$$

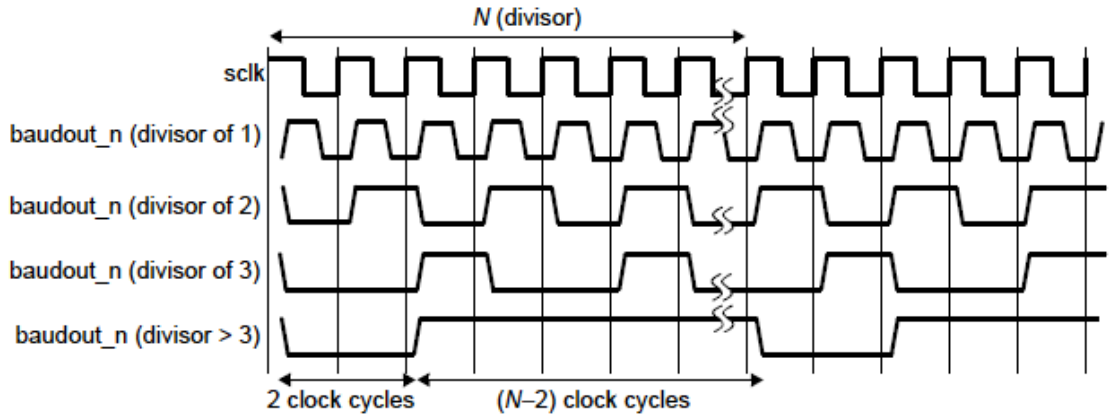


Figure 61. Timing diagram of baud clock

14.2.2. Buffer for Transmission and Reception

DW_apb_uart can have FIFO. The data width is fixed to 8 bits. The FIFO depth is 32. FIFO is composed of D-FF. Moreover, reading and writing for transmission and Receive FIFO are possible. This FIFO function can be enabled or disabled according to the register.

14.2.3. Interrupt

Interrupt can be done to any of the five fixed priority levels attached to DW_apb_uart.. Moreover, interrupt can be enabled or disabled in the IER register. Examples of interrupt occurrence are shown as follows. Please refer to the IIR register for details.

- When Reception error occurs
- When the Reception data can be used
- When FIFO is used, character time-out is generated
- When FIFO for Transmission becomes below the threshold when the THRE interrupt is used
- Modem status

DW_apb_uart has THRE interrupt (Transmitter Holding Register Empty Interrupt). When the Transmission data becomes below a set threshold of TransmissionFIFO, interrupt is generated.

14.2.4. Auto-Flow Control (UART0 Only)

DW_apb_uart has Auto-Flow Control mode compatible with IS16750. Signals rts_n and cts_n are active low. The terminal rts_n should be connected with the terminal cts_n of other UART when using Auto-Flow Control. When the received data exceeds the threshold of FIFO, rts_n goes Low. However, when Auto-Flow Control is used, IrDA 1.0 SIR cannot be supported. The timing diagram of Auto RTS and Auto CTS is shown in Figure 62 and Figure 63.

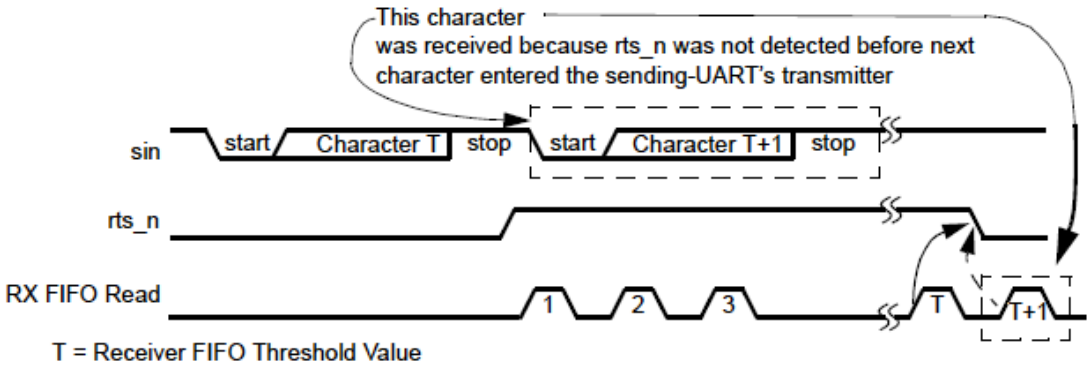


Figure 62. Timing Diagram of Auto RTS

rts_n becomes High when the received data exceeded the threshold of FIFO in Figure 62 rts_n becomes Low when device has finished reading the data that exists in Receive FIFO.

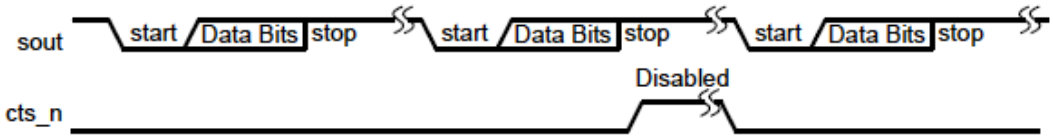


Figure 63. Timing Diagram of Auto CTS

When cts_n becomes High inFigure 63 transmission of data is temporarily interrupted. When cts_n becomes Low, transmission of data is exeucted again.

14.3. I/O Signal

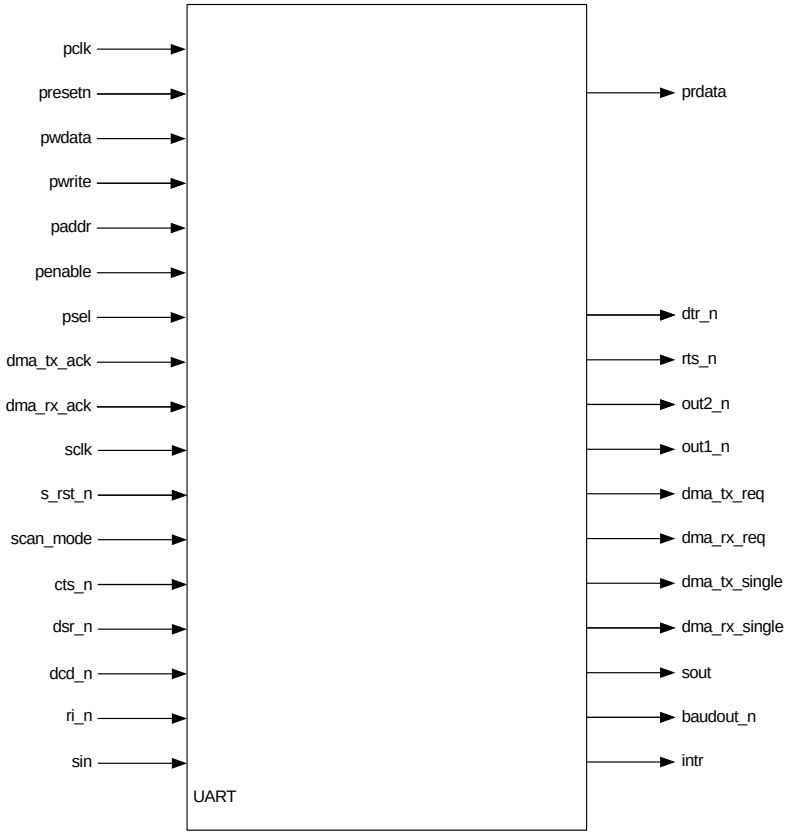


Figure 64. UART Module

Terminal list of DW_apb_uart

Terminal name	I/O	Description	Connection
pclk	In	APB Clock	Clock Gen
presetn	In	APB Reset	Reset Gen
psel	In	APB Peripheral Select Signal	APB
paddr	In	APB Sddress [7:0]	APB
pwdata	In	APB Write Data [31:0]	APB
pwrite	In	APB Write Signal	APB
penable	In	APB Enable Signal	APB
prdata	Out	APB Read Data [31:0]	APB
sclk	In	Serial Clock	Clock Gen
s_rst_n	In	Serial Reset Signal	Reset Gen
scan_mode	In	Scan Mode Select Signal	TESTDEC
cts_n	In	Transmission Clear Signal	I/O
dsr_n	In	Data Set Signal	"HI fixation"
dcd_n	In	Data Carry Detection Signal	"HI fixation"
ri_n	In	Ring Indicator Signal	"HI fixation"
dma_tx_ack	In	DMA Transmission Acknowledge	DMAC
dma_rx_ack	In	DMA Reception Acknowledge	DMAC
dtr_n	Out	Data Terminal Signal	OPEN
rts_n	Out	Transmission Request Signal	I/O
out2_n	Out	Programmable Signal 2	OPEN
out1_n	Out	Programmable Signal 1	OPEN
dma_tx_req	Out	DMA Transmission Request	DMAC
dma_tx_single	Out	DMA Transmission Request	DMAC
dma_rx_req	Out	DMA Reception Request	DMAC
dma_rx_single	Out	DMA Reception Request	DMAC
sin	In	Serial In	I/O
sout	Out	Serial Out	I/O
intr	Out	Interrupt Signal	ICTL
baudout_n	Out	Baud Clock Out Signal	OPEN

14.4. Register

14.4.1. Memory Map

Name	Description	Address Offset	R/W	Width	Reset
RBR	Receive Buffer Register LCR 7 = At 0	0x00	R	8 bit	0x0
THR	Transmit Holding Register LCR 7 = At 0		W	8 bit	0x0
DLL	Divisor Latch (Low) LCR 7 = At one		R/W	8 bit	0x0
DLH	Divisor Latch (High) LCR[7] = at 1	0x04	R/W	8 bit	0x4
IER	Interrupt Enable Register LCR[7] =at 0		R/W	8 bit	0x0
IIR	Interrupt Identification Register	0x08	R	8 bit	0x1
FCR	FIFO Control Register		W	8 bit	0x0
LCR	Line Control Register	0x0C	R/W	8 bit	0x0
MCR	Modem Control Register	0x10	R/W	8 bit	0x0
LSR	Line Status Register	0x14	R	8 bit	0x60
MSR	Modem Status Register	0x18	R	8 bit	0x0
SCR	Scartchpad Register	0x1C	R/W	8 bit	0x0
Reserved	-	0x20 – 0x2C	-	-	-
FAR	FIFO Access Register	0x70	R/W	1 bit	0x0
USR	UART Status Register	0x7C	R	5 bit	0x6
TFL	Transmit FIFO Level	0x80	R	6 bit	0x0
RFL	Receive FIFO Level	0x84	R	6 bit	0x0
HTX	Halt TX	0xA4	R/W	1 bit	0x0
DMASA	DMA Software Acknowledge	0xA8	W	1 bit	0x0
Reserved	-	0xAC – 0xF0	-	-	-
UCV	UART Component Version	0xF8	R	32 bit	0x3331 342A
CTR	Component Type Register	0xFC	R	32 bit	0x4457 0110

14.4.2. Register Detail

RBR (Receive Buffer Register)

Address Offset : 0x0

Bits	Name	Direction	Reset	Description
7:0	Receive Buffer Register	R	0x0	Reception Buffer Register for Serial In LSR 0 = At one, the read data is valid. FCR 0 = It can access the head of FIFO at one (selected FIFO).

THR (Transmit Holding Register)

Address Offset : 0x0

Bits	Name	Direction	Reset	Description
7:0	Transmit Holding Register	W	0x0	Transmission Data Register for Serial Out THRE = Write data none at one (LSR 5). FCR 0 = 1(selected FIFO) and THRE = The size of FIFO that can be written at one.

DLH (Divisor Latch High)

Address Offset : 0x4

Bits	Name	Direction	Reset	Description
7:0	Divisor Latch (High)	R/W	0x0	The higher bits of Divisor Latch Register (DLR) which sets the value of baud rate.This register becomes accessible when DLAB bit (LCR 7) is set to "1", and when USR 0 bit is "0". The baud rate can be calculated using the following expressions: Baud rate = (serial clock freq) / (16 * DLR) It is necessary to send and receive dataq after 8 clock cycles even if DLR was set to the slowest clock conversion in DW_apb_uart.

DLL (Divisor Latch Low)

Address Offset : 0x0

Bits	Name	Direction	Reset	Description
7:0	Divisor Latch (Low)	R/W	0x0	The lower bits of Divisor Latch Register (DLR), to be formed with DLH register. This register becomes accessible when DLAB bit (LCR 7) is set to "1", and when USR 0 bit is "0". The baud rate can be calculated using the following expressions: Baud rate = (serial clock freq) / (16 * DLR) It is necessary to send and receive dataq after 8 clock cycles even if DLR was set to the slowest clock conversion in DW_apb_uart..

IER (Interrupt Enable Register)

Address Offset : 0x4

Bits	Name	Direction	Reset	Description
7	PTIME	R/W	0x0	THRE Interrupt Enable Signal 0 = Disabled 1 = Enabled
6:4	Reserve and read as zero			
3	EDSSI	R/W	0x0	Modem Status Interrupt Enable Signal This interrupt has a high priority level of 4. 0 = Disabled 1 = Enabled
2	ELSI	R/W	0x0	Reception Line Status Interrupt Enable Signal This interrupt has the highest priority level. 0 = Disabled 1 = Enabled
1	ETBEI	R/W	0x0	Tranmission Maintenance Register Empty (THRE) Interrupt Enable Signal This interrupt has a high priority level of 3. 0 = Disabled 1 = Enabled
0	ERBFI	R/W	0x0	Reception Data and Character Timeout Interrupt Enable Signal (FIFO is effective) This interrupt has a high priority level of 2. 0 = Disabled 1 = Enabled

IIR (Interrupt Identify Register)

Address Offset : 0x8

Bits	Name	Direction	Reset	Description
7:6	FIFOs Enabled	R	0x0	FIFO Enable Signal 00 = Disabled 11 = Enabled
5:4	Reserve and read as zero			
3:0	Interrupt ID (Note 1)	R	0x1	Interrupt ID 0000 = Modem Status 0001 = No Pending Interrupt 0010 = THR Empty 0100 = Received Data Available 0110 = Reception Line Status 0111 = Busy Detect 1100 = Character Timeout

(Note 1) Details of Interrupt ID

IIR (Interrupt Identify Register) – continued

ID	Priority	Meaning	Interrupt Generation Factor	Interrupt Reset
0001	–	None	None	–
0110	1 (The height)	Reception line status	Overrun / Parity / Framing Error / Break Generation	Line status register (LSR) was read.
0100	2	Reception data effective	When FIFO is invalid, the Reception data became effective. When FIFO is valid, tt reached at the FIFO trigger level.	When FIFO is invalid FIFO that read Reception buffer register (RBR) became below the FIFO trigger level when it was valid.
1100	2	Character time-out	Interrupt is generated when more than one character data remained in FIFO and device did not accessed it in the fixed amount of time (four character time).	Reception buffer register (RBR) was read.
0010	3	THR is empty.	The THRE mode where THR is empty and fell below the FIFO threshold when it was valid.	Or that read IIR It wrote it in THR (FIFO or THRE was invalid) Or Transmit FIFO became more than the threshold. (THRE is effective.)
0000	4	Modem Status	Clear To Send (CTS) / Data Set Ready (DSR) / Ring Indicator (RI) / Data Carrier Detect (DCD) Generation	Modem status register (MSR) was read.
0111	5	Busy detection	Interrupt is generated when device writes to line control register (LCR) while UART is busy.	UART status register (USR) was read.

FCR (FIFO Control Register)

Address Offset : 0x8

Bits	Name	Direction	Reset	Description
7:6	RCVR Trigger	W	0x0	The threshold of Receive FIFO is selected. 1. Interrupt Generation 2. It is used to de-assert rts_n signal at Auto_Flow_control upon receipt of data. 3. It is used for dma_rx_req_n signal assert of the DMA handshake. 00 = There is one character. 01 = FIFO 1/4 10 = FIFO 1/2 11 = there are two characters in FIFO.
5:4	TX Empty Trigger	W	0x0	The threshold of Transmit FIFO is selected. 1. THRE interrupt generation 2. It is used for assert of the dma_tx_req_n signal of the DMA handshake. 00 = The FIFO is empty. 01 = There are two characters in FIFO 10 = FIFO 1/4 11 = FIFO 1/2
3	-	W	0x0	This bit is only valid when DMA handshake interface is not used.
2	XMIT FIFO Reset	W	0x0	Transmit FIFO Clear Bit Transmission request via DMA handshake is cleared. This bit is cleared automatically.
1	RCVR FIFO Reset	W	0x0	Receive FIFO Clear Bit Reception request via DMA handshake is cleared. This bit is cleared automatically.
0	FIFO Enable	W	0x0	Transmission and Receive FIFO Enable Signal

LCR (Line Control Register)
Address Offset : 0xC

Bits	Name	Direction	Reset	Description
7	DLAB	R/W	0x0	DLL and DLH Write Enable for Baud Rate Setting Writing to this bit is only possible when USR 0 = 0. Please clear this bit after setting the baud rate.
6	Break	R/W	0x0	It enters in the state of the Transmission hit.
5	Stick Parity	Reserve and read as zero		
4	EPS	R/W	0x0	Parity Select Signal (Parity is enabled) Writing to this bit is only possible when USR 0 = 0. 0: Odd Parity 1: Even Parity
3	PEN	R/W	0x0	Parity enable Signal Writing to this bit is only possible when USR 0 = 0. 0 = Parity is disabled. 1 = Parity is enabled.
2	STOP	R/W	0x0	It is used to select the number of stop bits of each character. Writing to this bit is only possible when USR 0 = 0. 0 = 1 Stop Bit 1 = 1.5 Stop Bit at time LCR [1:0] = 0 1 = 2 Stop Bit at other time
1:0	DLS	R/W	0x0	Data Length Select Writing to this bit is only possible when USR 0 = 0. It is used to select the number of data bits in one character. 00=5 bits 01=6 bits 10=7 bits 11=8 bits

MCR (Modem Control Register)
Address Offset : 0x10

Bits	Name	Direction	Reset	Description
6	SIRE	R	0x0	SIR Mode Enable Signal Writing to this bit is not possible because IrDA mode is not supported.
5	AFCE	R/W	0x0	Auto-Flow Control Enable Signal When this bit is set to “1”, the selected FIFO operates in Auto-Flow Control mode. 0 = Auto-Flow Control Mode is disabled 1 = Auto-Flow Control mode is enabled.
4	Loop Back	R/W	0x0	Loop Back Test Mode 0 = Normal Mode 1 = Loop Back Mode In Loop Back Mode, terminal SOUT is fixed to HIGH and Serial Out is connected to an internal SIN line.
3	OUT2	R/W	0x0	It is used to control out2_nOut of the user definition directly. 0 = out2_n de-asserted (= 1) 1 = out2_n asserted (= 0)
2	OUT1	R/W	0x0	It is used to control out1_nOut of the user definition directly. 0 = out1_n de-asserted (= 1) 1 = out1_n asserted (= 0)
1	RTS	R/W	0x0	It is used to control transmission request (rts_n) Out directly. 0 = rts_n de-asserted (= 1) 1 = rts_n asserted (= 0) This bit is asserted when device is in Auto-Flow Control mode and when Receive FIFO is below threshold.
0	DTR	R/W	0x0	Data Terminal Ready It is used to control data terminal preparation completion (dtr_n) Out directly. 0 = dtr_n de-asserted (= 1) 1 = dtr_n asserted (= 0)

LSR (Line Status Register)
Address Offset : 0x14

Bits	Name	Direction	Reset	Description
7	RFE	R	0x0	Receiver FIFO Error Bit This bit asserts when a parity or framing error in Receive FIFO occurs. 0 = no error in RX_FIFO 1 = error in RX_FIFO When the character with the error is at the head of Receive FIFO, and the LSR register is read when there is no error, this bit is cleared.
6	TEMT	R	0x1	Transmitter Empty Bit This bit asserts when Transmission shift register and Transmit FIFO (when valid) are both empty. FIFO sets the Transmission register and the Transmission shift register when it is invalid and sets this bit when both registers are empty.
5	THRE	R	0x1	Transmit Holding Register Empty Bit This bit is asserted when the THRE mode is invalid, and when the Transmission register or Transmit FIFO is empty. This bit is set to “1” when data transfer is executed but there are data available for transmission from the Transmission Register or Transmit FIFO to Transmission shift register. In this case, interrupt is generated. The THRE mode and FIFO show whether Transmit FIFO is full or not when it is effective. At this time, the THRE interrupt is controlled by FCR [5:4].
4	BI	R	0x0	Break Interrupt Bit It is used to show the detection of the break sequence on Serial In data. This bit is cleared once it is read.
3	FE	R	0x0	Framing Error Bit It is used to detect framing error in the Receive FIFO. It happens when an effective STOP bit in the Reception data cannot be detected. This bit is cleared once it is read. 0 = no framing error 1 = framing error
2	PE	R	0x0	Parity Error Bit It is used to detect parity error in the Receive FIFO. This bit is cleared once it is read. 0 = no parity error 1 = parity error
1	OE	R	0x0	Overrun Error Bit It is used to detect if overrun error occurred. Overrun occurs when new data is generated before old data is read. 0 = no overrun error 1 = overrun error
0	DR	R	0x0	Data Ready Bit It is asserted when there is at least one character in RBR or Receive FIFO. 0 = no data ready 1 = data ready

MSR (Modem Status Register)
Address Offset : 0x18

Bits	Name	Direction	Reset	Description
7	DCD	R	0x0	Data Carrier Detect This is used to show current status of modem control line dcn_n. 0 = dcd_n input de-asserted (= 1) 1 = Dcd_n input asserted (= 0) It is the same as MCR [3] at the Loop Back mode.
6	RI	R	0x0	Ring Indicator This is used to show current status of modem control line ri_n. 0 = ri_n input de-asserted (= 1) 1 = ri_n input asserted (= 0) It is the same as MCR [2] at the Loop Back mode.
5	DSR	R	0x0	Data Set Ready This is used to show current status of modem control line dsr_n. 0 = dsr_n input de-asserted (= 1) 1 = Dsr_n input asserted (= 0) It is the same as MCR [0] at the Loop Back mode.
4	CTS	R	0x0	This is used to show current status of modem control line cts_n. 0 = cts_n input de-asserted (= 1) 1 = Cts_n input asserted (= 0) It is the same as MCR [1] at the Loop Back mode.
3	DDCD	R	0x0	Delta Data Carrier Detect This is used so that MSR may show that modem control line dcd_n changed after reading of MSR. 0 = no change on dcd_n since last read of MSR 1 = there is a change on dcd_n since last read of MSR This bit is cleared by reading. Changing of MCR [3] is at the Loop Back mode.
2	TERI	R	0x0	Trailing Edge Ring Indicator This is used so that MSR may show that ri_nln changed after reading of MSR. 0 = no change on ri_n since last read of MSR 1 = there is a change on ri_n since last read of MSR This bit is cleared by reading. Changing of MCR [2] (H -> L) is shown at the Loop Back mode.
1	DDSR	R	0x0	Delta Data Set Ready This is used so that MSR may show that modem control line dsr_n changed after reading of MSR. 0 = no change on dsr_n since last read of MSR 1 = there is a change on dsr_n since last read of MSR This bit is cleared by reading. Changing of MCR [0] is shown at the Loop Back mode.
0	DCTS	R	0x0	Delta Clear to Send This is used so that MSR may show that modem control line cts_n changed after reading of MSR. 0 = no change on cts_n since last read of MSR 1 = there is a change on cts_n since last read of MSR This bit is cleared by reading. Changing of MCR [1] is shown at the Loop Back mode.

SCR (Scratchpad Register)
Address Offset : 0x1C

Bits	Name	Direction	Reset	Description
7:0	Scratchpad Register	R/W	0x0	The programmer uses this register as temporary storage space. It doesn't have any defined purpose in DW_apb_uart.

FAR (FIFO Access Register)
Address Offset : 0x70

Bits	Name	Direction	Reset	Description
0	FIFO Access Register	R/W	0x0	It is used to enable the FIFO access mode for test. When this bit is set to “1”, it is possible to read and write to Transmission and Receive FIFO. 0 = Disabled 1 = Enabled

USR (UART Status Register)
Address Offset : 0x7C

Bits	Name	Direction	Reset	Description
4	RFF	R	0x0	Receive FIFO Full This is used to show that Receive FIFO is full. 0 = Receive FIFO is not full. 1 = Receive FIFO is full.
3	RFNE	R	0x0	Receive FIFO Not Empty This is used to show that there is one or more data in Receive FIFO. 0 = Receive FIFO is empty. 1 = Receive FIFO is not empty.
2	TFE	R	0x1	Transmit FIFO Empty This is used to show that Transmit FIFO is empty. 0 = Transmit FIFO not empty. 1 = Transmit FIFO is empty.
1	TFNF	R	0x1	Transmit FIFO Not Full This is used to show that Transmit FIFO is not full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
0	BUSY	R	0x0	UART Busy It is used to show that the serial transfer is in progress. 0 = DW_apb_uart is idle or inactive 1 = DW_apb_uart is busy

TFL (Transmit FIFO Level)
Address Offset : 0x80

Bits	Name	Direction	Reset	Description
5:0	Transmit FIFO Level	R	0x0	Transmit FIFO Level This shows the number of data in Transmit FIFO.

RFL (Receive FIFO Level)
Address Offset : 0x84

Bits	Name	Direction	Reset	Description
5:0	Recieve FIFO Level	R	0x0	Receive FIFO Level This shows the number of data in Receive FIFO.

HTX (Halt TX)
Address Offset : 0xA4

Bits	Name	Direction	Reset	Description
0	Halt TX	R/W	0x0	This register is used to stop Transmission for test. 0 = Halt TX disabled 1 = Halt TX enabled

DMASA (DMA Software Acknowledge)
Address Offset : 0xA8

Bits	Name	Direction	Reset	Description
0	DMA Software Acknowledge	W	0x0	DMA Software Acknowledge. This bit is asserted when DMA request is done without error. This bit is cleared automatically.

UCV (UART Component Version)
Address Offset : 0xF8

Bits	Name	Direction	Reset	Description
31:0	UART Component Version	R	0x3330312a	ASCII Value of Component Version

CTR (Component Type Register)
Address Offset : 0xFC

Bits	Name	Direction	Reset	Description
31:0	Peripheral ID	R	0x44570110	Peripheral ID

15. I2S Input I/F and CD-ROM Decoder

15.1. Features

- ◇ 2-Ch Digital Audio Input x 2
- ◇ I2S/EIAJ Format
- ◇ 16-Bit Data
- ◇ Selectable Bit Clock from 32 fs, 48 fs, and 64 fs
- ◇ Selectable Input Sample Rate from 32 kHz, 44.1 kHz, and 48 kHz
- ◇ One Line of Internal Input from the CD Servo Controller
- ◇ Up to 4× Maximum Input Rate
- ◇ Supports CD-DA Link Detection
- ◇ Supports CD-ROM Sync Detection
- ◇ Supports CD-ROM Data Descrambling
- ◇ Acquires Sub-Q Data
- ◇ Acquires CD-Text Data
- ◇ Built-in DMA

15.2. Description

15.2.1. Block Diagram

The following figure shows an I2S input controller block diagram.

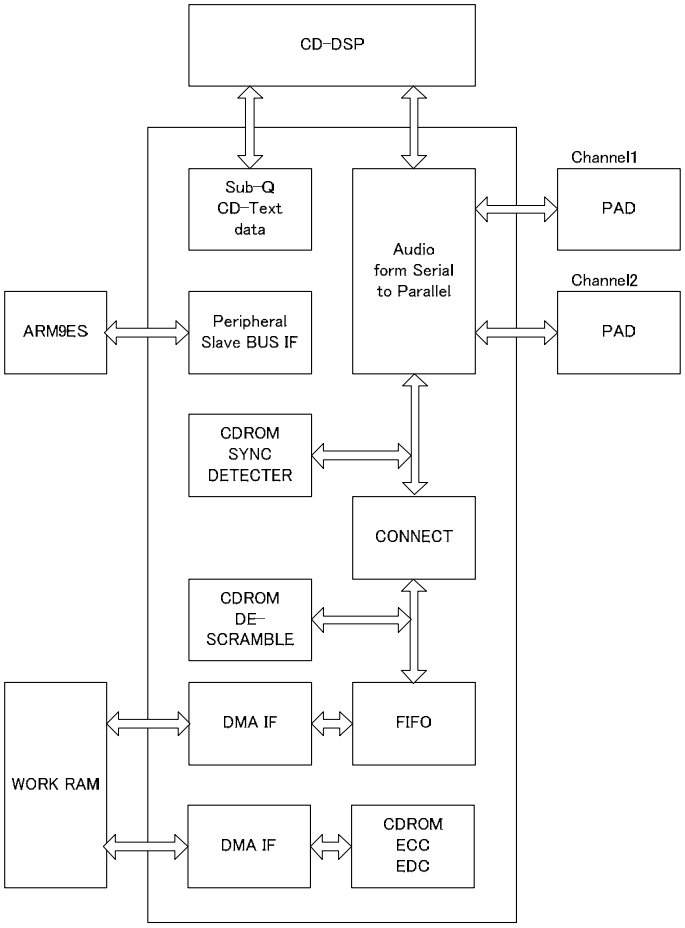


Figure 65. I2S Input Controller Block Diagram

15.2.2. Serial-to-Parallel Conversion Through 3-Wire (3-line) Input Interface

The I2S input interface converts serial data input through a 3-wire interface from CD-DA and CD-ROM to parallel data.
The interface supports 16- and 24-bit input data width. To input 24 bits of data, the bottom 8 bits of data are dropped.
This allows input of signals in a variety of formats by setting clock-edge polarity, etc.
The interface has a total of three input lines - two lines from PAD and one line from the internal CD-DSP. These lines are designed for exclusive use.

15.2.3. INREQI

For input of 1 sample data (LR = 32), the data is considered valid when INREQI is set to H at the end of sample data input.
When INREQI is set to L, the data is considered invalid and is not written to the internal buffer.

15.2.4. BFULLO

BFULLO becomes H when writing to buffer cannot be executed. (When READY bit of selected FIFO is L).
BFULLO becomes L when INREQI is L and sample input data has is written successfully to buffer (When READY bit of selected FIFO is H).

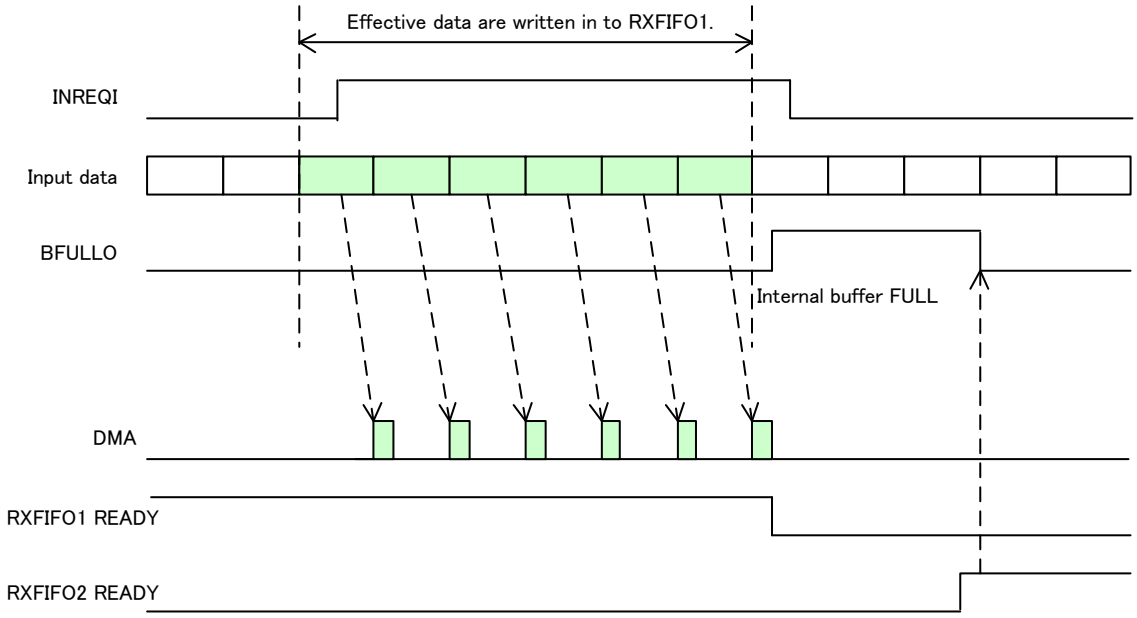


Figure 66

15.2.5. Receive Buffer

The receive buffer uses part of working RAM as receive FIFOs and has 8-byte FIFOs as registers in the circuit.
The receive buffer can configure four FIFO areas with buffer size up to 4,095 bytes.
FIFOs are written in the order of No. 1, 2, 3, 4, 1, 2, … When written data reaches the set FIFO size, a termination interrupt is generated to write data to the subsequent FIFO.
At this time, unless READY of the subsequent FIFO is set to H, the receive buffer is considered FULL so data write is not possible. To avoid this event, set READY of the subsequent or later FIFOs to H before the completion of the previous FIFO.
DMA is automatically conducted from the set FIFO start address until the set number of transfers is completed.
Working RAM addresses are automatically incremented from the start address.

In order to prevent failures to acquire data for interpolation, configure the four FIFO areas as shown below for receiving data from CD-ROM.
Stack sync FIFO in 12 bytes in each area.

Start address	Size
RX FIFO1: addr1	2364Byte
RX FIFO2: addr1 + 2352 Byte	2364Byte
RX FIFO3: addr2 + 2352 Byte	2364Byte
RX FIFO4: addr3 + 2352 Byte	2364Byte

15.2.6. CD-ROM Input

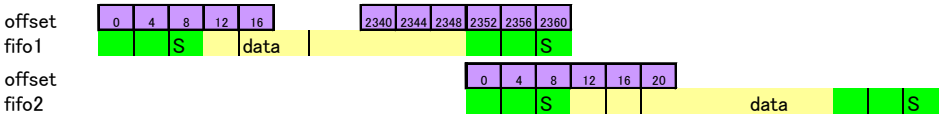
When the CD-ROM input function is enabled, it detects a synchronous pattern (96'h00FF_FFFF_FFFF_FFFF_FFFF_FF00) in the sector for an input signal.
Data are written in the internal buffer from the data after the synchronous pattern is detected (i.e., from the 13th byte).
Synchronous sector detection state includes three states: Open, State0, and State1.
Open state is a state in which no synchronous pattern has been detected. In this state, the internal counter is not working and, as a result, no data are written to the internal RAM. When a synchronous pattern is detected, the detection state is switched to State0. In State0, every time a synchronous sector pattern is inputted, it is detected as the synchronous pattern. When a subsequent synchronous pattern is detected in a sector containing 2,352 bytes in State0, the detection state is switched to State1. If no synchronous pattern is inputted in a sector containing 2,352 or more bytes in State0, the synchronous pattern is considered lost and the detection state is switched to Open state.
In State1, the detection of patterns in a sector within −16 bytes from the position in which normal synchronous pattern was detected is regarded as the detection of synchronous pattern, and detection in any positions other than the said position is ignored. The detection of synchronous pattern in a sector within +12 bytes from the position in which normal synchronous pattern was detected is regarded as the detection of synchronous pattern from back gate. If no synchronous pattern is inputted in a sector within −16 or +12 bytes from the position in which normal synchronous pattern was detected in State1, the synchronous pattern is considered lost to interpolate and write data to the counter or RAM. If no synchronous pattern is detected in a sector containing 2,352 bytes in State1, the detection state is switched to State0.

12 to 2,351 bytes of data in each sector are descrambled by the feedback shift register corresponding to x15+x+1. (0 to 11 bytes in a sector are used for synchronous patterns.)

When a sector status in each stage of DMA FIFO is defined, an interrupt is generated. Sector status are read from the register.

CD-ROM Data Storage Format

FIFO size: 2,352 bytes + 12 bytes = 2,364 bytes/area



Note: An interrupt is generated when data acquisition is completed and sector status is defined in each area.
Note: Overwrite data in the SYNC area by FW.

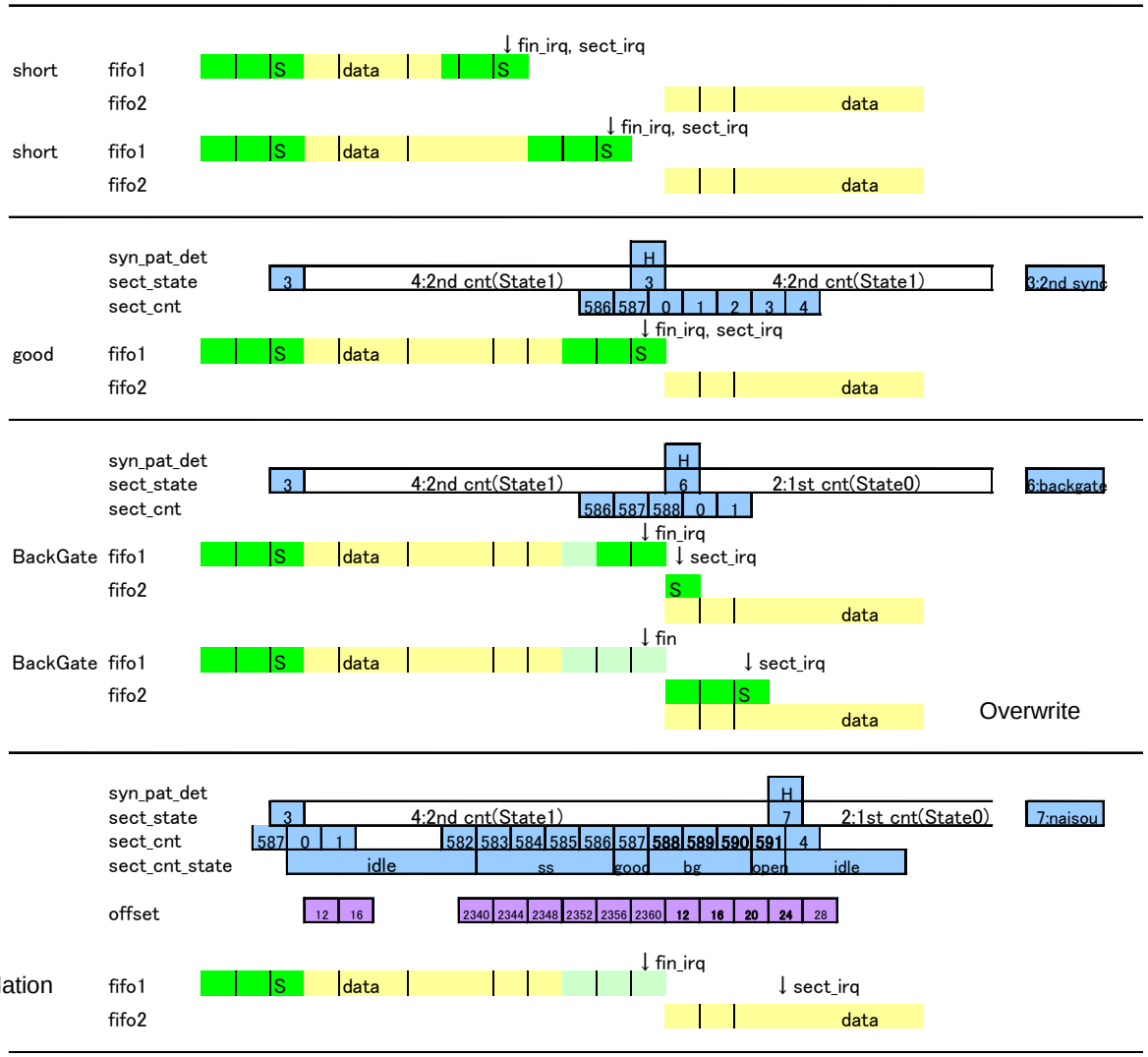


Figure 67.

15.2.7. Error Correction

ECC
After completion of setting the sector start address (i.e., 0th byte in the synchronous area) to the DMA start address setting register for ECC and EDC, ECC is started by having a write access to the ECC start register. ECC makes PQ corrections to the CD-ROM MODE1 format for the set number of correction times regardless of MODE and FORM settings. When ECC is completed, a termination interrupt is generated. The correction results can be read from the status register MONI4.
Determine the presence or absence of uncorrectable data after completion of corrections for the set number of times using pqucf_flag bit 8.
For MODE2 FORM1, fill data with zeros in the Header area, and then execute ECC.

EDC
After completion of start address setting, EDC is executed to any of CD-ROM MODE1, MODE2 FORM1, and MODE2 FORM2 formats according to edcmode register setting by having write access to the EDC start register. When EDC is completed, a termination interrupt is generated. The correction results can be read from the status register.
For MODE1, fill data with zeros in the SYNC area, and then execute EDC.

Required cycle number (calculated with 96 MHz operating frequency)
Input data: WAV data (48 kHz stereo sampling frequency)
Format: MODE1or MODE2 FORM1
2,048 bytes for user data per sector = 512 bytes of sample data = 1024,000 cycles =10.67 ms

wait_busreq register setting: 14 (dec) (Minimum hbusreq cycles: 32 per system clock)
1×PQ correction = 38,373 cycles
3×EDC = 27,128 cycles
1×PQ correction + 3×EDC =65,500 cycles = 1.36 ms =6.4%

Note: Cycles including master with priority level higher than CD-ROM (i.e., USB, I2S OUT, SDIO, and CDIN) are additionally applied to bus arbitration.

CD-ROM format

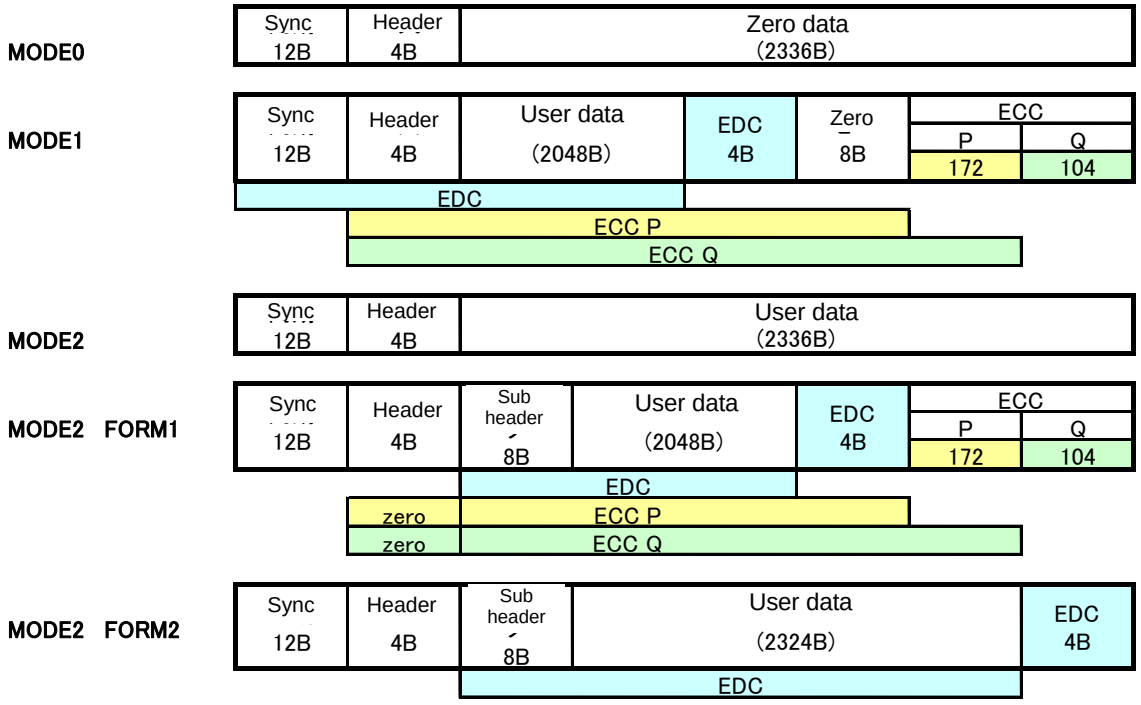


Figure 68

15.2.8. Sub-Q Data and CD-Text Data Acquisition

Retrieve Sub-Q data and CD-Text data from Subcode data of CD-DSP.
Generate 12-byte Sub-Q data [95:0] and 18-byte CD-Text data [143:0]. When these data are completed, an interrupt is generated. Retrieved data can be read from the register.
Careful attention should be paid to the byte order of Sub-Q [95:0] and CD-Text [143:0].
Normally, Sub-Q data are given small numbers to bytes received earlier such as Q1, Q2, …
Giving numbers according to this rule comes from
Sub-Q [95] = Q1, Sub-Q [94] = Q2, ……, and Sub-Q [0] = Q96
The same rule applies to CD-Text [143:0]. CD-Text [143] represents a byte received first.

15.3. I/O Signals

Pin Name	I/O	Function	Destination
sys_clk_i	In	APB BUS Clock	CLKCTR
cdin_clk__i	In	CD-IN Clock	CLKCTR
cdec_clk__i	In	CD-ROM Clock	CLKCTR
rstb_i	In	Reset (Active Low)	RSTGEN
peri_addr_i	In	APB BUS Address	APB
peri_en_i	In	APB BUS Enable	APB
peri_di_i	In	APB BUS Write Data	APB
peri_we_i	In	APB BUS Write Enable	APB
psel_i	In	APB BUS Selector	APB
peri_do_o	Out	APB BUS Read Data	APB
hgrant_i	In	Master X Bus Grant for Audio Data	PDMAC AHB
hrespm_i[1:0]	In	RAM Transport Response for Audio Data	PDMAC AHB
hreadymi_i	In	RAM Transport Finish for Audio Data	PDMAC AHB
hrdatam_i	In	RAM Read Data for Audio Data	PDMAC AHB
hbusreq_o	Out	Master X Bus Request for Audio Data	PDMAC AHB
htrans_o[1:0]	Out	Master X Transport Type for Audio Data	PDMAC AHB
hsize_o[1:0]	Out	Master X Transport Size for Audio Data	PDMAC AHB
hwrite_o	Out	Master X Transport Direction for Audio Data	PDMAC AHB
haddr_o[19:0]	Out	Master X Address for Audio Data	PDMAC AHB
hwdata_o[31:0]	Out	Master X Write Data for Audio Data	PDMAC AHB
hgrant_cdrom_i	In	Master X Bus Grant for CD-ROM ECC	PDMAC AHB
hrespm_cdrom_i[1:0]	In	RAM Transport Response for CD-ROM ECC	PDMAC AHB
hreadym_cdromi_i	In	RAM Transport Finish for CD-ROM ECC	PDMAC AHB
hrdatam_cdrom_i	In	RAM Read Data for CD-ROM ECC	PDMAC AHB
hbusreq_cdrom_o	Out	Master X Bus Request for CD-ROM ECC	PDMAC AHB
htrans_cdrom_o[1:0]	Out	Master X Transport Type for CD-ROM ECC	PDMAC AHB
hsize_cdrom_o[1:0]	Out	Master X Transport Size for CD-ROM ECC	PDMAC AHB
hwrite_cdrom_o	Out	Master X Transport Direction for CD-ROM ECC	PDMAC AHB
haddr_cdrom_o[19:0]	Out	Master X Address for CD-ROM ECC	PDMAC AHB
hwdata_cdrom_o[31:0]	Out	Master X Write Data for CD-ROM ECC	PDMAC AHB
lrck_ch1_i	In	LR Clock Input from Channel 1	PAD
bck_ch1_i	In	Bit Clock Input from Channel 1	PAD
data_ch1_i	In	Data Input from Channel 1	PAD
lrck_ch2_i	In	LR Clock Input from Channel 2	PAD
bck_ch2_i	In	Bit Clock Input from Channel 2	PAD
data_ch2_i	In	Data Input from Channel 2	PAD
lrck_cddsp_i	In	LR Clock Input from CD-DSP	CD-DSP
bck_cddsp_i	In	Bit Clock Input from CD-DSP	CD-DSP
data_cddsp_i	In	Data Input from CD-DSP	CD-DSP
sbsy_i	In	Subcode Block Signal	CD-DSP
sfsy_i	In	Subcode Frame Signal	CD-DSP
sbclk_o	Out	Subcode Shift Clock Signal	CD-DSP
subd_i	In	Subcode Data Signal	CD-DSP
i2sin_irq_o	Out	Interrupt (Active Low)	ICTL

15.4. Register

15.4.1. Memory Map

Name	Description	Address Offset	R/W	Width Bit	Reset
CDIN_SET0	CD-IN Input Format Setting	0x00	R/W	8	0x00
CDIN_SET1	DMA/CD-ROM Setting	0x04	R/W	5	0x00
CDIN_SET3	RX FIFO READY Setting	0x0C	R/W	4	0x0
CDIN_SET4	RX FIFO1 Start Address Setting	0x10	R/W	32	0x0
CDIN_SET5	RX FIFO1 Size Setting	0x14	R/W	12	0x400
CDIN_SET6	RX FIFO2 Start Address Setting	0x18	R/W	32	0x0
CDIN_SET7	RX FIFO2 Size Setting	0x1C	R/W	12	0x400
CDIN_SET8	RX FIFO3 Start Address Setting	0x20	R/W	32	0x0
CDIN_SET9	RX FIFO3 Size Setting	0x24	R/W	12	0x400
CDIN_SET10	RX FIFO4 Start Address Setting	0x28	R/W	32	0x0
CDIN_SET11	RX FIFO4 Size Setting	0x2C	R/W	12	0x400
CDIN_SET12	Connection Setting	0x30	R/W	8	0x80
CDIN_SET13	Connection Data 0 Setting	0x34	R/W	32	0x00
CDIN_SET14	Connection Data 1 Setting	0x38	R/W	32	0x00
CDIN_SET15	Connection Data 2 Setting	0x3C	R/W	32	0x00
CDIN_SET16	ECC/EDC Setting	0x40	R/W	21	0x0E0000
CDIN_SET17	ECC/EDCDMA Start Address Setting	0x44	R/W	32	0x0
ECCSTART	ECC Start	0x48	W	—	0x0
EDCSTART	EDC Start	0x4C	W	—	0x0
Irq_set0	IRQ Mask Setting	0x60	R/W	16	0xFFFF
Irq_set1	IRQ Clear Setting	0x64	R/W	16	0x0000
Irq_set2	IRQ Monitor	0x68	R	16	0xFFFF
MONI1	MONI1	0x80	R	32	0x280
MONI2	MONI2	0x84	R	32	0x0
MONI3	MONI3	0x88	R	32	0x3FF0080
MONI3B	MONI3B Sector Status Monitor	0x8C	R	16	0x0
MONI4	CD-ROM ECC Status Register	0x90	R	28	0x0
MONI5	CD-ROM EDC Status Register	0x94	R	6	0x0
INREQ	INREQ Setting Register	0x98	R/W	1	0x0
SUBQ1	SUBQ Data Acquisition Register 1	0x9C	R	32	0x00000000
SUBQ2	SUBQ data Acquisition Register 2	0xA0	R	32	0x00000000
SUBQ3	SUBQ data Acquisition Register 3	0xA4	R	32	0x00000000
CD-TEXT1	CD-Text Data Acquisition Register 1	0xA8	R	32	0x00000000
CD-TEXT2	CD- Text Data Acquisition Register 2	0xAC	R	32	0x00000000
CD-TEXT3	CD- Text Data Acquisition Register 3	0xB0	R	32	0x00000000
CD-TEXT4	CD- Text Data Acquisition Register 4	0xB4	R	32	0x00000000
CD-TEXT5	CD- Text Data Acquisition Register 5	0xB8	R	16	0x0000
CHANSEL	Input Channel Setting Register	0xBC	R/W	2	0x0

15.4.2. Register Detail

CDIN_SET0
CD-IN Input Format Setting
Offset : 0x00 , Reset : 0x00

Bits	Name	Direction	Reset	Description
7:6		R/W	0x0	-
5		R/W	0x0	I2S Mode Setting 0: EIAJ 1: I2S
4		R/W	0x0	LRCK Polarity Setting 0: L-Ch set to H 1: L-Ch set to L
3		R/W	0x0	Data Width Setting 0: 16 bits 1: 24 bits
2		R/W	0x0	Data Align Setting 0: Right-aligned 1: Left-aligned
1		R/W	0x0	Data LSB Fast Setting 0: MSB Fast 1: LSB Fast
0		R/W	0x0	Data Latch Setting 0: BCK rising edge 1: BCK falling edge

CDIN_SET1
DMA Enable Setting
Offset : 0x04 , Reset : 0x00

Bits	Name	Direction	Reset	Description
4		R/W	0x0	CD IN DMA Enable Setting 0: OFF 1: ON
3		R/W	0x0	-
2		R/W	0x0	CD-ROM Sequence Clear Setting 0: Not clear 1: Clear
1		R/W	0x0	CD-ROM Descramble Setting 0: Descramble ON 1: DescrambleOFF
0		R/W	0x0	CD-ROM Enable Setting 0: OFF 1: ON

CDIN_SET3
RX FIFO READY Setting
Offset: 0x0C , reset : 0x00

Bits	Name	Direction	Reset	Description
3		R/W	0x0	RX FIFO4 READY Write “1” to this register when data write is ready. The register is set to “0” upon completion of writing to the FIFO. When data write not ready, no data are written to it. 0: NOT-READY 1: READY
2		R/W	0x0	RX FIFO3 READY Write “1” to this register when data write is ready. The register is set to “0” upon completion of writing to the FIFO. When data write not ready, no data are written to it. 0: NOT-READY 1: READY
1		R/W	0x0	RX FIFO2 READY Write “1” to this register when data write is ready. The register is set to “0” upon completion of writing to the FIFO. When data write not ready, no data are written to it. 0: NOT-READY 1: READY
0		R/W	0x0	RX FIFO1 READY Write “1” to this register when data write is ready. The register is set to “0” upon completion of writing to the FIFO. When data write not ready, no data are written to it. 0: NOT-READY 1: READY

CDIN_SET4
RX FIFO1 Start Address Setting
Offset : 0x10 , Reset : 0x00

Bits	Name	Direction	Reset	Description
31:0		R/W	0x0	RX FIFO1 Start Address Setting Setting to [1:0] byte is ignored, and [1:0] byte is set to x00.

CDIN_SET5
RX FIFO1 Size Setting
Offset : 0x14 , Reset : 0x400

Bits	Name	Direction	Reset	Description
11:0		R/W	0x400	RX FIFO1 Size Setting This register is used to set FIFO size. When the amount of data written to RAM reaches the set value, a termination interrupt is generated to start writing data to the subsequent FIFO.

CDIN_SET6
RX FIFO2 Start Address Setting
Offset : 0x18 , Reset : 0x00

Bits	Name	Direction	Reset	Description
31:0		R/W	0x0	RX FIFO2 Start Address Setting Setting to [1:0] byte is ignored, and [1:0] byte is set to x00.

CDIN_SET7
RX FIFO2 Size Setting
Offset : 0x1C , Reset : 0x400

Bits	Name	Direction	Reset	Description
11:0		R/W	0x400	RX FIFO2 Size Setting This register is used to set FIFO size. When the amount of data written to RAM reaches the set value, a termination interrupt is generated to start writing data to the subsequent FIFO.

CDIN_SET8
RX FIFO3 Start Address Setting
Offset : 0x20 , Reset : 0x00

Bits	Name	Direction	Reset	Description
31:0		R/W	0x0	RX FIFO3 Start Address Setting Setting to [1:0] byte is ignored, and [1:0] byte is set to x00.

CDIN_SET9
RX FIFO3 Size Setting
Offset : 0x24 , Reset : 0x400

Bits	Name	Direction	Reset	Description
11:0		R/W	0x400	RX FIFO3 Size Setting This register is used to set FIFO size. When the amount of data written to RAM reaches the set value, a termination interrupt is generated to start writing data to the subsequent FIFO.

CDIN_SET10
RX FIFO4 Start Address Setting
Offset : 0x28 , Reset : 0x00

Bits	Name	Direction	Reset	Description
31:0		R/W	0x0	RX FIFO4 Start Address Setting Setting to [1:0] byte is ignored, and [1:0] byte is set to x00.

CDIN_SET11
RX FIFO4 Size Clock Selector Setting
Offset : 0x2C , Reset : 0x400

Bits	Name	Direction	Reset	Description
11:0		R/W	0x400	RX FIFO4 Size Setting This register is used to set FIFO size. When the amount of data written to RAM reaches the set value, a termination interrupt is generated to start writing data to the subsequent FIFO.

CDIN_SET12
Connection Setting
Offset : 0x30 , Reset : 0x80

Bits	Name	Direction	Reset	Description
7		R	0x1	Connection Operation Invalid Status
6		R	0x0	Data Match Connection Start Status
5		R	0x0	Data Match Status
4		R	0x0	Connection Data Under Comparison
3:1		R/W	0x0	Connection Operation Mode Setting 0: 3 Pair Data Connection 1: 2 Pair Data Connection (DATA0 and DATA1) 2: 2 Pair Data Connection (DATA1, DATA2) 4: 1 Pair Data Connection (DATA0) 5: 1 Pair Data Connection (DATA1) 6: 1 Pair Data Connection (DATA2)
0		R/W	0x0	Connection Operation Start Setting 0: OFF 1: ON

CDIN_SET13
Connection Data 0 Setting
Offset : 0x34 , Reset : 0x00

Bits	Name	Direction	Reset	Description
31:0		R/W	0x0	Connection Data 0 Setting Connection setting of last data (i.e., the latest data) out of 3 pair data Make setting with {R ch[15:0], L ch[15:0]}.

CDIN_SET14
Connection Data 1 Setting
Offset : 0x38 , Reset : 0x00

Bits	Name	Direction	Reset	Description
31:0		R/W	0x0	Connection Data 1 Setting Connection setting of the middle data (i.e., data one before the latest) out of 3 pair data. Make setting with {R ch[15:0], L ch[15:0]}.

CDIN_SET15
Connection Data 2 Setting
Offset : 0x3C , Reset : 0x00

Bits	Name	Direction	Reset	Description
31:0		R/W	0x0	Connection Data 2 Setting Connection Setting of the first data (i.e., data two before the latest) out of 3 pair data. Make setting with {R ch[15:0], L ch[15:0]}.

CDIN_SET16
ECC/EDC Setting
Offset : 0x040 , Reset : 0x0E0000

Bits	Name	Direction	Reset	Description
20:16	wait_busreq	R/W	0x0E	AHB Bus Request Wait Cycle Sets the value of wait cycle upon issuance of hbusreq (Set value+2) × 2 sysclk. The default is 32 sysclk cycles.
15:12	max_pq_cnt	R/W	0x0	Number of Correction Times: 0 to 15 Times
11:9		-		
8	porq	R/W	0x0	Order of State P and State Q 0: From state P 1: From state Q
7:6		-		
5:4	edcmode	R/W	0x0	EDC Mode 1: MODE1 2: MODE2 FORM1 3: MODE2 FORM2
3		-		
2	dmaon	R/W	0x0	DMA ON/OFF for ECC/EDC 0: OFF 1: ON
1	eccon	R/W	0x0	ECC ON/OFF 0: ECC OFF 1: ECC ON
0	edcon	R/W	0x0	EDC ON/OFF 0: EDC OFF 1: EDC ON

CDIN_SET17
ECC/EDC DMA Start Address Setting
Offset : 0x44 , Reset : 0x00

Bits	Name	Direction	Reset	Description
19:0		R/W	0x0	ECC/EDC DMA Start Address Setting Lower 2 bits are set to 2'b00. Place sector data according to 4-byte boundary.

ECCSTART
ECC Start
Offset : 0x048 , Reset : 0x0

Bits	Name	Direction	Reset	Description
0		W	—	ECC starts up by write access.

EDCSTART
EDC Start
Offset : 0x04C , Reset : 0x0

Bits	Name	Direction	Reset	Description
0		W	—	EDC starts up by write access.

Irq_set0
Irqmask Setting
Offset : 0x60 , Reset : 0xFFFF

Bits	Name	Direction	Reset	Description
15:12		R/W	0xF	RX FIFO4 to 1 Sector Status Interrupt Mask 0: No Mask 1: Mask Interrupt
11		R/W	0x1	-
10		R/W	0x1	SUBQ Data Acquisition Completion Interrupt Mask 0: No Mask 1: Mask Interrupt
9		R/W	0x1	CD-Text Data Acquisition Completion Interrupt Mask 0: No Mask 1: Mask Interrupt
8		R/W	0x1	EDC Termination Interrupt Mask 0: No Mask 1: Mask Interrupt
7		R/W	0x1	ECC Termination Interrupt Mask 0: No Mask 1: Mask Interrupt
6		R/W	0x1	BFULLO Interrupt Mask When the BFULLO signal level rises to H: 0: No Mask 1: Mask Interrupt
5		R/W	0x1	RX Error 2 Interrupt Mask When data is written even if the amount of data has reached the set maximum FIFO size: 0: NoMask 1: Mask Interrupt
4		R/W	0x1	RX Error 1 Interrupt Mask When data is written even if the FIFO register is in FULL status: 0: No Mask 1: Mask Interrupt
3		R/W	0x1	RX FIFO4 Termination Interrupt Mask 0: No Mask 1: Mask Interrupt
2		R/W	0x1	RX FIFO3 Termination Interrupt Mask 0: Not Mask 1: Mask Interrupt
1		R/W	0x1	RX FIFO2 Termination Interrupt Mask 0: No Mask 1: Mask Interrupt
0		R/W	0x1	RX FIFO1 Termination Interrupt Mask 0: No Mask 1: Mask Interrupt

Irq_set1
Irqclear Setting
Offset : 0x64 , Reset : 0x0000

Bits	Name	Direction	Reset	Description
15:12		R/W	0x0	RXFIFO4 to 1 Sector Status Interrupt Clear The interrupt is cleared when “1” is written. The signal level becomes high only for one cycle.
11		R/W	0x0	-
10		R/W	0x0	SUBQ Data Acquisition Completion Interrupt Clear The interrupt is cleared when “1” is written. The signal level becomes high only for one cycle.
9		R/W	0x0	CD-TEXT Data Acquisition Completion Interrupt Clear The interrupt is cleared when “1” is written. The signal level becomes high only for one cycle.
8		R/W	0x0	EDC Termination Interrupt Clear The interrupt is cleared when “1” is written. The signal level becomes high only for one cycle.
7		R/W	0x0	ECC Termination Interrupt Clear The interrupt is cleared when “1” is written. The signal level becomes high only for one cycle.
6		R/W	0x0	BFULLO Interrupt Clear When the BFULLO signal level rises to H: The interrupt is cleared when “1” is written. The signal level becomes high only for one cycle.
5		R/W	0x0	RX Error 2 Interrupt Clear When data is written even if the data amount has reached the set maximum FIFO size: The interrupt is cleared when “1” is written. The signal level becomes high only for one cycle.
4		R/W	0x0	RX Error 1 Interrupt Clear When data is written even if the FIFO register is in a FULL status: The interrupt is cleared when “1” is written. The signal level becomes high only for one cycle.
3		R/W	0x0	RX FIFO4 Termination Interrupt Clear The interrupt is cleared when “1” is written. The signal level becomes high only for one cycle.
2		R/W	0x0	RX FIFO3 Termination Interrupt Clear The interrupt is cleared when “1” is written. The signal level becomes high only for one cycle.
1		R/W	0x0	RX FIFO2 Termination Interrupt Clear The interrupt is cleared when “1” is written. The signal level becomes high only for one cycle.
0		R/W	0x0	RX FIFO1 Termination Interrupt Clear The interrupt is cleared when “1” is written. The signal level becomes high only for one cycle.

Irq_set2
Irq Monitor
Offset : 0x68 , Reset : 0xFFFF

Bits	Name	Direction	Reset	Description
15:12		R	0xF	RX FIFO4 to 1 Sector Status Interrupt 0: Interrupt Generated 1: Interrupt Not Generated
11		R	0x1	-
10		R	0x1	SUBQ Data Acquisition Completion Interrupt 0: Interrupt Generated 1: Interrupt Not Generated
9		R	0x1	CD-Text Data Acquisition Completion Interrupt 0: Interrupt Generated 1: Interrupt Not Generated
8		R	0x1	EDC Termination Interrupt 0: Interrupt Generated 1: Interrupt Not Generated
7		R	0x1	ECC Termination Interrupt 0: Interrupt Generated 1: Interrupt Not Generated
6		R	0x1	BFULLO Interrupt This interrupt is generated when the BFULLO signal level rises to H. 0: Interrupt Generated 1: Interrupt Not Generated
5		R	0x1	RX Error 2 Interrupt This interrupt is generated when data is written even if the data amount has reached the set maximum FIFO size. 0: Interrupt Generated 1: Interrupt Not Generated
4		R	0x1	RX Error 1 Interrupt This interrupt is generated when data is written even if the FIFO register is in a FULL status. 0: Interrupt Generated 1: Interrupt Not Generated
3		R	0x1	RX FIFO4 Termination Interrupt 0: Interrupt Generated 1: Interrupt Not Generated
2		R	0x1	RX FIFO3 Termination Interrupt 0: Interrupt Generated 1: Interrupt Not Generated
1		R	0x1	RX FIFO2 Termination Interrupt 0: Interrupt Generated 1: Interrupt Not Generated
0		R	0x1	RX FIFO1 Termination Interrupt 0: Interrupt Generated 1: Interrupt Not Generated

MONI1
Monitor 1 Setting
Offset : 0x80 , Reset : 0x280

Bits	Name	Direction	Reset	Description
31:28		R	0x0	0
27:16		R	0x0	Previous Receive Count
15:12		R	0x0	0
11:10		R	0x0	0
9		R	0x1	BFULLO
8		R	0x0	DATAVALID
7		R	0x1	RX FIFO EMPTY
6		R	0x0	RX FIFO FULL
5		R	0x0	RX FIFO ERROR2
4		R	0x0	RX FIFO ERROR1
3		R	0x0	0
2		R	0x0	RX FINISH
1:0		R	0x0	Current FIFO No.

MONI2
Monitor 2 Setting
Offset : 0x84 , Reset : 0x0

Bits	Name	Direction	Reset	Description
31:28		R	0x0	-
27:16		R	0x0	Write Pointer
15:12		R	0x0	-
11:0		R	0x0	Read Pointer

MONI3
Monitor 3 Setting
Offset : 0x88 , Reset : 0x3FF0080

Bits	Name	Direction	Reset	Description
31:26		R	0x0	0
25:16		R	0x3FF	Number of Counts in Sector
15:13		R	0x0	Count State in Sector
12		R	0x0	Sector End
11		R	0x0	GOOD Sector
10		R	0x0	Interpolation Sector
9		R	0x0	Back-Gate Sector
8		R	0x0	Short Sector
7		R	0x1	Open Status
6		R	0x0	Sync Pattern Detection
5		R	0x0	Sync Pattern Detection
4		R	0x0	Sync Pattern Detection
3:0		R	0x0	Sector State

MONI3B
Monitor 3B Sector Status Monitor
Offset : 0x8C , Reset : 0x00

Bits	Name	Direction	Reset	Description
15:12		R	0x0	RX FIFO4 Sector Status
11:8		R	0x0	RX FIFO3 Sector Status
7:4		R	0x0	RX FIFO2 Sector Status
3:0		R	0x0	RX FIFO1 Sector Status 0x5:SYNC Lost (State0 ->Open) 0x4:Interpolation Sector 0x3: Back-Gate Sector 0x2:GOOD Sector 0x1: Short Sector 0x0: Undecided

MONI4
CD-ROM ECC Status
Offset : 0x90

Bits	Name	Direction	Reset	Description
27	ecc_busy	R		ECC Busy Flag
26:23	ecc_state	R		CD-ROM ECC State
22:18	p_state	R		CD-ROM ECC P State
17:13	q_state	R		CD-ROM ECC Q State
12	pq_corr_flag	R		Correction Made to State P/Q (Correction to State P/Q was made during execution of data correction)
11	pq_uncorr_flag	R		Uncorrectable State P/Q Detected (Data including uncorrectable state P/Q was detected during execution of data correction)
10	pucf_flag	R		Uncorrectable State P Detected 1'b0: No uncorrectable data detected 1'b1: Uncorrectable data detected (Uncorrectable data was detected during the last correction to state P)
9	qucf_flag	R		Uncorrectable State Q Detected 1'b0: No uncorrectable data detected 1'b1: Uncorrectable data detected (Uncorrectable data was detected during the last correction to state Q)
8	pqucf_flag	R		Uncorrectable data detected after completion of data correction 1'b0: No uncorrectable data detected 1'b1: Uncorrectable data detected (Uncorrectable data was detected during the last correction to state P/Q)
7	pquc1_flag	R		Uncorrectable data detected during the first data correction 1'b0: No uncorrectable data detected 1'b1: Uncorrectable data detected (Uncorrectable data was detected during the first correction to state P/Q)
6:4	pqc1_num	R		Number of times of corrections made during the first correction to state P/Q
3	pquc2_flag	R		Uncorrectable data detected during the second data correction 1'b0: No uncorrectable data detected 1'b1: Uncorrectable data detected (Uncorrectable data was detected during the second correction to state P/Q)
2:0	pqc2_num	R		Number of times of corrections made during the second correction to state P/Q

MONI5
CD-ROM EDC Status
offset : 0x94

Bits	Name	Direction	Reset	Description
5	edc_busy	R		EDC Busy Flag
4:1	edc_state	R		CD-ROM EDC State
0	edc_flag	R		EDC Result 1'b0: OK 1'b1: NG

INREQ
Input Request
Offset : 0x98 , Reset : 0x0

Bits	Name	Direction	Reset	Description
0	inreq	R/W	0x0	INREQ Flag 1'b0: Write disabled 1'b1: Write enabled

SUBQ1
SUBQ Data Acquisition Register 1
Offset : 0x9C , Reset : 0x00000000

Bits	Name	Direction	Reset	Description
31:0	SUBQ [95:64]	R	0x0000 0000	SUBQ Data [95:64]

SUBQ2
SUBQ Data Acquisition Register 2
Offset : 0xA0 , Reset : 0x00000000

Bits	Name	Direction	Reset	Description
31:0	SUBQ [63:32]	R	0x0000 0000	SUBQ Data [63:32]

SUBQ3
SUBQ Data Acquisition Register 3
Offset : 0xA4 , Reset : 0x00000000

Bits	Name	Direction	Reset	Description
31:0	SUBQ [31:0]	R	0x0000 0000	SUBQ Data [31:0]

CD-TEXT1
CD-TEXT Data Acquisition Register 1
Offset : 0xA8 , Reset : 0x00000000

Bits	Name	Direction	Reset	Description
31:0	CD-TEXT [143:112]	R	0x0000 0000	CD-Text Data [143:112]

CD-TEXT2
CD-TEXT Data Acquisition Register 2
Offset : 0xAC , Reset : 0x00000000

Bits	Name	Direction	Reset	Description
31:0	CD-TEXT [111:80]	R	0x0000 0000	CD-TEXT Data [111:80]

CD-TEXT3
CD-TEXT Data Acquisition Register 3
Offset : 0xB0 , Reset : 0x00000000

Bits	Name	Direction	Reset	Description
31:0	CD-TEXT [79:48]	R	0x0000 0000	CD-TEXT Data [79:48]

CD-TEXT4
CD-TEXT Data Acquisition Register 4
Offset : 0xB4 , Reset : 0x00000000

Bits	Name	Direction	Reset	Description
31:0	CD-TEXT [47:16]	R	0x0000 0000	CD-TEXT Data [47:16]

CD-TEXT5
CD-TEXT Data Acquisition Register 5
Offset : 0xB8 , Reset : 0x0000

Bits	Name	Direction	Reset	Description
15:0	CD-TEXT [15:0]	R	0x0000	CD-TEXT Data [15:0]

CHANSEL
Input Channel Setting Register
Offset : 0xBC , Reset : 0x0

Bits	Name	Direction	Reset	Description
1:0	CHANSEL	R/W	0x0	I2S Input Channel Setting 0x3: CD-DSP 0x2: Channel2 (PAD) 0x1: Channel1 (PAD) 0x0: CD-DSP

16. I2S Output I/F

16.1. Features

- 2.1-Ch Digital Audio Output (L-Ch + R-Ch + ADC)
- Supports output in I2S/EIAJ format
- Selectable sampling rate from 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz
  (When ADC input outputs it, the support of only 32k, 44.1k, 48k)
- Selectable data width from 16, 24, and 32 bits
- Supports bit clock of 64fs
- Supports pitch control (0.5× to 2.0× in 25 steps)

16.2. Description

16.2.1. Block Diagram

The following figure shows an I2S output controller block diagram.

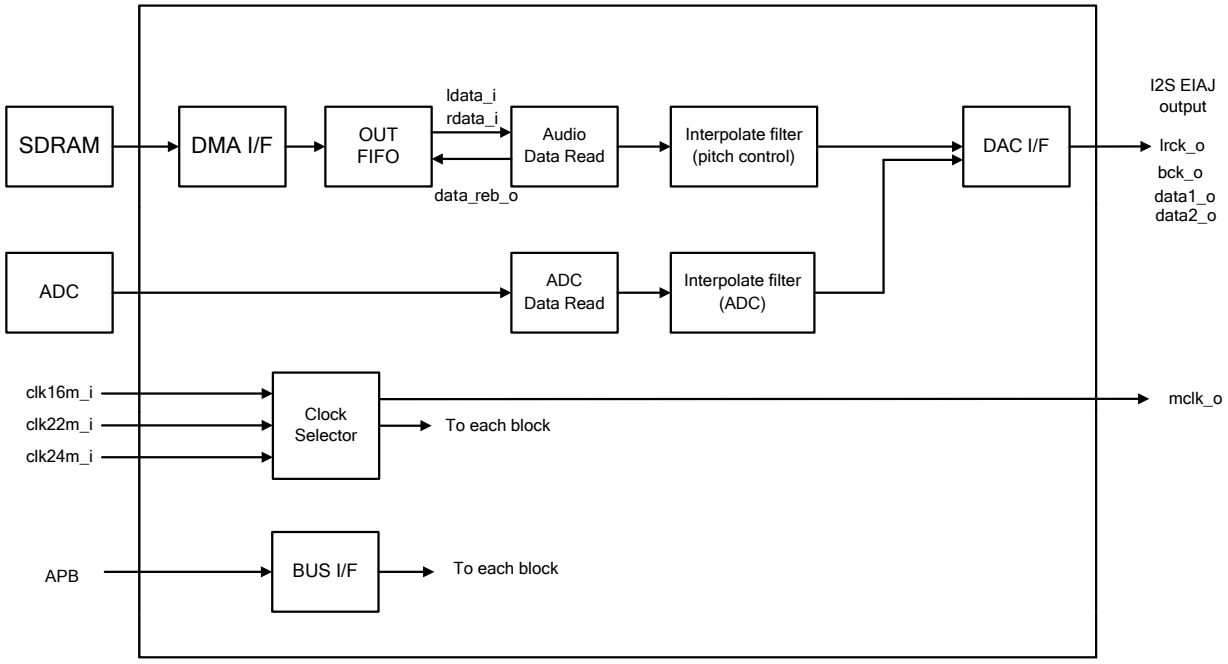


Figure 69. I2S Output Controller Block Diagram

16.2.2. DMA I/F

The DMA I/F block acquires input data from RAM and has four built-in FIFO areas.

Write data inputted in RAM according to the formats shown in the table below. (The formats shown are that in the tx0 area.) Four transfer areas, tx0 to tx3 can be set in RAM. Monaural data interpolates Rch data with hardware. The upper limit in each area for both stereo and monaural data is 1024 samples. When the last address is read, irq is generated. If the subsequent transfer area is ready, data is transferred to the subsequent area according to the setting of the tx fs register. DMA transfer repeats the cycle of tx0→tx1→tx2→tx3→tx0……

For 16-bit stereo data:

address	data[31:16]	data[15:0]
tx0startaddr	R(0)	L(0)
4	R(1)	L(1)
8	R(2)	L(2)
:	:	:
+ tx0size *4	R(tx0size)	L(tx0size)

For 24-bit stereo data:

address	data[31:24]	data[23:16]	data[15:8]	data[7:0]
tx0startaddr	R(0)	L(0)		
4	L(1)		R(0)	
8	R(1)			L(1)
:	:	:	:	:
+ tx0size *6 + 2	R(tx0size)			L(tx0size)

For 32-bit stereo data:

address	data[31:0]
tx0startaddr	L(0)
4	R(0)
8	L(1)
12	R(1)
:	:
+ tx0size *8	L(tx0size)
+ tx0size *8 + 4	R(tx0size)

For 16-bit monaural data (When the number of samples is an odd number.):

address	data[31:16]	data[15:0]
tx0startaddr	L(1)	L(0)
4	L(3)	L(2)
8	L(5)	L(4)
:	:	:
+ tx0size *2	-	L(tx0size)

For 24-bit monaural data (When the number of samples is an odd number.):

address	data[31:24]	data[23:16]	data[15:8]	data[7:0]
tx0startaddr	L(1)	L(0)		
4	L(2)		L(1)	
8	L(3)			L(2)
:	:	:	:	:
+ tx0size *3 + 2	-			L(tx0size)

For 32-bit monaural data (When the number of samples is an odd number.):

address	data[31:0]
tx0startaddr	L(0)
4	L(1)
8	L(2)
:	:
+ tx0size *4	L(tx0size)

Linear interpolation allows 2x and 4x interpolation.
The following table shows corresponding frequencies.

1x (dmaintpsel=0)	2x (dmaintpsel=1)	4x (dmaintpsel=2)
32 kHz	16 kHz	8 kHz
48 kHz	24 kHz	12 kHz
44.1 kHz	22.05 kHz	11.025 kHz

16.2.3. Clock selector

The clock selector block is used to generate MCLK frequency and consists of three types of clock input, dividers, and selectors.

The MCLK frequencies can be generated by a combination of clock input and divider.

		Divider		
		1	2	4
Clock source (MHz)	49.152	49.152	24.576	12.288
	45.1584	45.1584	22.5792	11.2896
	16.9344	16.9344	8.4672	4.2336

The following table shows combinations of sampling rates and MCLK frequencies of corresponding sound source.

		MCLK Fs						
		64fs	128fs	192fs	256fs	384fs	512fs	768fs
Music source Fs	32	-	-	-	-	12.288	-	24.576
	44.1	-	-	-	11.2896	16.9344	22.5792	-
	48	-	-	-	12.288	-	24.576	-
	88.2	-	11.2896	16.9344	22.5792	-	-	-
	96	-	12.288	-	24.576	-	-	-
	176.4	11.2896	22.5792	-	-	-	-	-
	192	12.288	24.576	-	-	-	-	-

16.2.4. I/O Bus Interface

The I/O bus interface is used to make settings for audio data output from the I/O bus and for digital audio interface. For details, refer to information in the chapter on registers.

16.2.5. Audio Data Read (I2S)

When an audio data read request signal “data_reb_o” is outputted to the output FIFO, L-channel audio data “ldata_i” and R-channel audio data “rdata_i” are inputted from the DMA I/F. Then, this block is used to make data read timing adjustment (0.5× to 2.0× in 12 steps) according to the pitch control setting.

16.2.6. Interpolating Filter

The interpolating filter is used to interpolate sample data when the pitch control is set to 0.5x to 1.0x.

16.2.7. Audio Data Read (ADC)

The downstream register in the ADC block reads data to output it to the interpolating filter (ADC).

When the sampling frequency of the sound source is set to 32, 44.1, or 48 kHz, data is acquired at the same timing as that of audio data read (I2S). Bigger sampling frequency than 48kHz isn't being supported.
The following table shows combinations of the sampling frequencies of sound source and frequencies at which the audio data read (ADC) block acquires data.

		Audio Data Read (ADC) Data read frequency
Music Source Fs	32kHz	32kHz
	44.1kHz	44.1kHz
	48kHz	48kHz

16.2.8. DAC I/F

The DAC interface is used to output data in I2S/EIAJ format. Data inputted from SDRAM and ADC are simultaneously outputted.

16.2.9. Output Waveforms

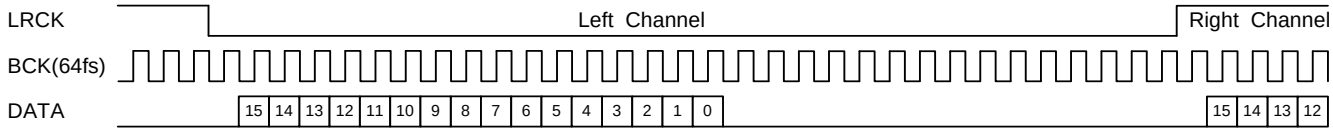


Figure 70. I2S Output Timing (64fs)

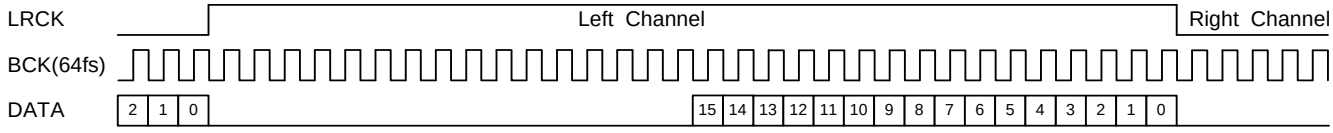


Figure 71. EIAJ Output Timing(64fs)

16.3. I/O Signals

Pin Name	I/O	Function	Destination
clk_i	In	APB BUS Clock	CLKCTR
rstb_i	In	Reset (Active Low)	RSTGEN
paddr_i	In	APB BUS Address	APB
penable_i	In	APB BUS Enable	APB
pwdata_i	In	APB BUS Write Data	APB
pwrite_i	In	APB BUS Write Enable	APB
psel_i	In	APB BUS Selector	APB
prdata _o	Out	APB BUS Read Data	APB
daout_test_mode_i	In	Test Mode Input	-
daout_test_ctr_i	In	Test Mode Register Setting	-
hgrant_i	In	Master X Bus Grant	PDMAC AHB
hrespm_i[1:0]	In	RAM Transport Response	PDMAC AHB
hreadymi_i	In	RAM Transport Finish	PDMAC AHB
hrdatam_i	In	RAM Read Data	PDMAC AHB
hbusreq_o	Out	Master X Bus Request	PDMAC AHB
htrans_o[1:0]	Out	Master X Transport Type	PDMAC AHB
hsize_o[1:0]	Out	Master X Transport Size	PDMAC AHB
hwrite_o	Out	Master X Transport Direction	PDMAC AHB
haddr_o[19:0]	Out	Master X Address	PDMAC AHB
hwdata_o[31:0]	Out	Master X Write Data	PDMAC AHB
lrck_o	Out	LR Clock Output	PAD
bck_o	Out	Bit Clock Output	PAD
data1_o	Out	Data Output	PAD
data2_o	In	Data Output (ADC)	PAD
mclk_o	Out	Master Clock Output	PAD

16.4. Register

16.4.1. Memory Map

Name	Description	Address Offset	Width	Reset
dacif_set0	Control	0x00	8	8'h00
dacif_set1	Output Format Setting	0x04	8	8'h72
dmacirq	DMA Interrupt	0x2C	32	32'h00000000
dmairqclr	DMA Interrupt Clear	0x30	8	-
sdmairqmsk	DMA Interrupt Mask	0x34	4	4'hFF
tx0startaddr	DMA tx0 Start Address	0x38	32	32'h00000000
tx0size	DMA tx0 Buffer Size	0x3C	16	16'h0000
tx0fs	DMA tx0 Sampling Frequency Setting	0x40	16	16'h0000
tx0ok	DMA tx0 Transfer Ready OK	0x44	8	16'h0000
tx1startaddr	DMA tx1 Start Address	0x48	32	32'h00000000
tx1size	DMA tx1 Buffer Size	0x4C	16	16'h0000
tx1fs	DMA tx1 Sampling Frequency Setting	0x50	16	16'h0000
tx1ok	DMA tx1 Transfer Ready OK	0x54	8	16'h0000
tx2startaddr	DMA tx2 Start Address	0x58	32	32'h00000000
tx2size	DMA tx2 Buffer Size	0x5C	16	16'h0000
tx2fs	DMA tx2 Sampling Frequency Setting	0x60	16	16'h0000
tx2ok	DMA tx2 Transfer Ready OK	0x64	8	16'h0000
tx3startaddr	DMA tx3 Start Address	0x68	32	32'h00000000
tx3size	DMA tx3 Buffer Size	0x6C	16	16'h0000
tx3fs	DMA tx3 Sampling Frequency Setting	0x70	16	16'h0000
tx3ok	DMA tx3 Transfer Ready OK	0x74	8	16'h0000
fsseqstart	DMA Transport Start Setting	0x78	8	8'h00
fsseqstop	DMA Transport Abort Setting	0x7C	8	8'b00
softreset	Software Reset	0x80	8	-
dmaflag	DMA Flag Monitor	0x84	10	8'h01
outfifoflash	Out FIFO Flash	0x88	1	16'h0000
outfifohold	Out FIFO Hold Setting	0x8C	1	16'h0000
outfifoflag	Out FIFO Full / Empty Flag	0x90	12	16'h0001

16.4.2. Register Detail

dacif_set0

Offset: 0x00

Width: 8 bits

Bits	Name	Direction	Reset	Description
3	din_test	R/W	0x0	(reserved)
2	adcout_on	R/W	0x0	ADC IF Block ON/OFF 0: OFF 1: ON
1	pause_on	R/W	0x0	DAC IF Block Pause Setting this register to “1” disables data to receive/transmit between outfifo and audrd. 0: Normal operation 1: Pause
0	daout_on	R/W	0x0	DAC IF Block ON/OFF Setting this register to OFF fix output of LRCK, BCK, and DATA to L level and disables data to receive/transmit between outfifo and audrd. 0: OFF 1: ON

dacif_set1

Offset: 0x04

Width: 8 bits

Bits	Name	Direction	Reset	Description
6:0		R/W	0x72	Output Format Selection 0x72: I2S 64fs Format 0x02: EIAJ 64fs Format

dacif_set8
Offset: 0x20
Width: 16 bits

Bits	Name	Direction	Reset	Description
[13:9]	pitchctrl	R/W	0x00	Pitch Controller Varies pitches in halftone steps of the equal temperature of 12 degrees. x0.5 – x2.0 25step 10100; x0.5 10101; x0.5229 10110; x0.5612 10111; x0.5946 11000; x0.6299 11001; x0.6674 11010; x0.7071 11011; x0.7491 11100; x0.7937 11101; x0.8407 11110; x0.8908 11111; x0.9438 00000; x1.0 00001; x1.0594 00010; x1.1224 00011; x1.1892 00100; x1.2599 00101; x1.3348 00110; x1.4142 00111; x1.4983 01000; x1.5874 01001; x1.6817 01010; x1.7817 01011; x1.1887 01100; x2.0
[8:5]	adc_atten	R/W	0x0	Adcrd Data Input Attenuation Attenuates data input from ADC Data input is variable in 16 stages in steps of 6dB. 0x0: 0dB 0x1:−6dB 0xF:−90dB
[4:0]	audrd_atten	R/W	0x0	Audrd Data Input Attenuation Attenuates data input from SDRAM Data input is variable in 32 stages in steps of 6dB. 0x0: 0dB 0x1:−6dB 0x1F: −190dB

dacif_set9
Offset: 0x24
Width: 4 bits

Bits	Name	Direction	Reset	Description
2	start_clksel	R/W	0x0	Clock Selection Start Selects clock according to the “clk_sel” register setting. When the “clk_sel” register setting is completed, write “H” to this register. (Detects the signal at the rising edge)
1:0	Clk_sel	R/W	0x0	Clock Domain Setting Makes clock setting to output I2S Select a sampling frequency for sound source to be played back. 0: 16.9344MHz 1: 45.1584MHz (Fs = 44.1, 88.2, 176.4 kHz) 2: 49.152MHz (Fs = 32, 48, 96, 192 kHz)

dacif_set10
Offset: 0x28
Width: 8 bits

Bits	Name	Direction	Reset	Description
4	start_clksel_mclk	R/W	0x0	Clock Select Start Selects MCLK according to the “Clk_se_mclk” and “ Div_sel_mclk” register settings. When the “Clk_se_mclk” and “Div_sel_mclk” register settings are completed, write “H” to this register. (Detects the signal at the rising edge)
3:2	Div_sel_mclk	R/W	0x0	MCLK Clock Division Setting 0: MCLK masked 1: 1 2: 1/2 3: 1/4
1:0	Clk_sel_mclk	R/W	0x0	MCLK Clock Domain Setting 0: 16.9344 MHz 1: 45.1584 MHz 2: 49.152 MHz

dmairq
Offset: 0x2C
Width: 32 bits

Bits	Name	Direction	Reset	Description
31:4		R	0x0	-
3	outfifo_error	R	0x0	Generated on receipt of read request from DAC IF when “outfifo” is set to Empty. The last data is continually outputted until “outfifo_flash” is executed. 0: No interrupt generated 1: Interrupt generated
2	outfifo_empty	R	0x0	Generated when “outfifo” is set to Empty 0: No interrupt generated 1: Interrupt generated
1		R	0x0	-
0	dma_final	R	0x0	Generated when the last data is read from dma 0: No interrupt generated 1: Interrupt generated

dmairqclr
Offset: 0x30
Width: 8 bits

Bits	Name	Direction	Reset	Description
3:0	dmairqclr	W	-	DMA Interrupt Clear Writing “1” to this register clears the corresponding bit of dmairq. Since the bit is continualy cleared during “1” is written to the register, write “0” to it after clearing the bit.

dmairqmsk
Offset: 0x34
Width: 8 bits

Bits	Name	Direction	Reset	Description
3:0	dmairqmsk	R/W	0xF	DMA Interrupt Cause Mask (0: Unmasked, 1: Masked) Masks the cause of interrupt of the corresponding bit of dmairq

tx0startaddr
Offset: 0x38
Width: 32 bits

Bits	Name	Direction	Reset	Description
32:0	tx0startaddr	R/W	0x0000	DMA tx0 Start Address (Specifies the start address as absolute address)

tx0size
Offset: 0x3C
Width: 16 bits

Bits	Name	Direction	Reset	Description
11:0	tx0size	R/W	0x000	DMA tx0 Buffer Size (Specifies “sample number – 1” up to a maximum of 1024 samples for L and R, respectively)

tx0fs
Offset: 0x40
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:5	dmaif_fs	R/W	0x0	Sampling Frequency Setting 0: 32 kHz 1: 44.1 kHz 2: 48 kHz 3: 88.2 kHz 4: 96 kHz 5: 176.4 kHz 6: 192 kHz 7: reserved Note: The output sampling frequency of DACIF should follow the set value of this bit. Apply the same to DMA interpolation.
4:3	dmaif_datawidth	R/W	0x0	Bit Width Setting 0: 16 bits 1: 24 bits 2: 32 bits
2	dmaif_mono	R/W	0x0	Monaural Interpolation Setting 0: Stereo data 1: Interpolated monaural data
1:0	dmaif_intp_sel	R/W	0x0	DMA Interpolation Setting 0: ×1 (32 kHz, 48 kHz, 44.1 kHz) 1: ×2 (16 kHz, 24 kHz, 22.05 kHz) 2: ×4 (8 kHz, 12 kHz, 11.025 kHz)

tx0ok
Offset: 0x44
Width: 8 bits

Bits	Name	Direction	Reset	Description
0	tx0ok	R/W	0x0	Write “1” to this bit when tx0 is ready. When “0” is written, DMA disables data acquisition. When data read for the set value of tx0size is completed or suspended by fsseqstop, this bit is set to “0”.

Note: The operation of the following registers conforms to that of the tx0 register aforementioned. DMA transfer repeats the cycle of tx0→tx1→tx2→tx3→tx0……
tx1startaddr, tx1size, tx1fs, tx1ok (Offset:; 0 x 48 to 0x54)
tx2startaddr, tx2size, tx2fs, tx2ok (Offset:; 0 x 58 to 0x64)
tx3startaddr, tx3size, tx3fs, tx3ok (Offset:; 0 x 68 to 0x74)

dmaseqstart
Offset: 0x78
Width: 16 bits

Bits	Name	Direction	Reset	Description
0		W	0x0	DMA Transfer Start Setting (Starts DMA transfer operation when write to the corresponding address is detected. Note: The transfer is accepted when the dma programmable controller is in an idle state and the subsequent transfer area is ready.)

dmaseqstop
Offset: 0x7C
Width: 16 bits

Bits	Name	Direction	Reset	Description
0		W	0x0	Forced DMA Transfer Stop Setting (Stops DMA transfer operation when write to the corresponding address is detected during DMA transfer is in progress.)

softreset
Offset: 0x80
Width: 16 bits

Bits	Name	Direction	Reset	Description
0		W	0x0	Software Resetting Initializes the DMA-FS switching programmable controller and flashes OUTFIFO when write to the corresponding address is detected. Note: All writable I/O registers return to their default to clear interrupts.

dmaflag
Offset: 0x84
Width: 16 bits

Bits	Name	Direction	Reset	Description
6:4	seq_cnt	R	0x0	Status Monitor of FS Switching Programmable Controller 0: Idle 1: Transfer 2: Continue 3: Ready 4: Stop
3:2	current_tx	R	0x0	Indicates currently busy transfer area number: tx fifo(tx0 to tx3) Note: Since this number is updated when switching or stopping data transfer, the subsequent transfer area number is indicated during data transfer stops.
1	dma_full	R	0x0	Set to “1” when FIFO in dmaif is full.
0	dma_empty	R	0x1	Set to “1” when FIFO in dmaif is empty.

outfifoflash
Offset: 0x88
Width: 16 bits

Bits	Name	Direction	Reset	Description
0		R/W	0x0	Initializes the DMA-FS switching programmable controller and flashes OUTFIFO when write to the corresponding address is detected. Note: All writable I/O registers return to their default to clear interrupts.

outfifohold
Offset: 0x8C
Width: 16 bits

Bits	Name	Direction	Reset	Description
0		R/W	0x0	Outfifo Preamble Hold Setting (0: Preamble hold OFF, 1: Preamble hold ON) Makes setting of data to be outputted on receipt of read request from DAC IF when outfifo is empty When preamble hold is set to ON, the last data is outputted. When it is set to OFF, “all 0” data is outputted.

dmaflag
Offset: 0x90
Width: 16 bits

Bits	Name	Direction	Reset	Description
1	outfifo_full	R	0x0	Set to “1” when outfifo is full.
0	outfifo_empty	R	0x1	Set to “1” when outfifo is empty.

17. CD Servo Controller

17.1. Features

- ■Supports rotation speed of CD up to 4×
- ■Built-in preservo amplifier with power save mode supports playback of CD-RW
- ■Allows independent offset adjustment of AC, BD, E, and F amplifiers
- ■Built-in auto tracking and focus adjustment function
- ■Built in PLL and CLV with a wide lock range
- ■Built-in asymmetry correction function

17.2. Description

17.2.1. Block Diagram

The following figure shows a CD-DSP block diagram.

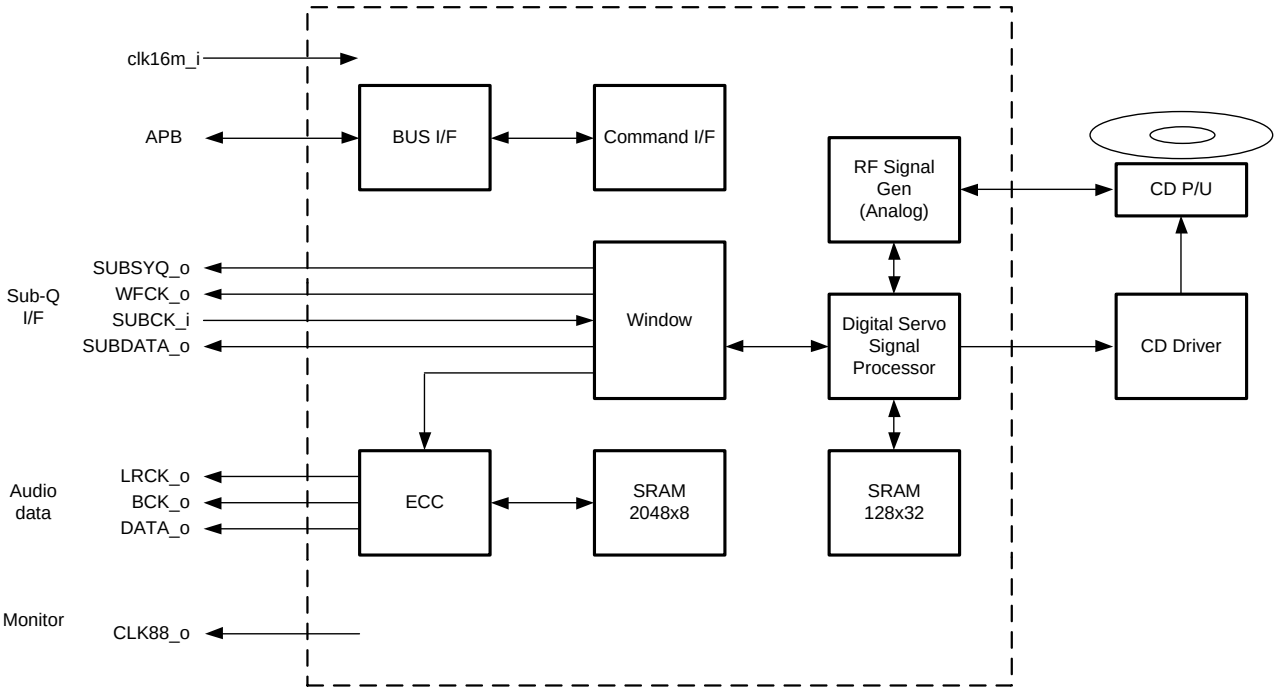


Figure 72. CD-DSP Block Diagram

17.2.2. Window

If a signal is regenerated, the frame sync signal may not be detected due to a DISC flaw or jitter, or other signals may be detected in error as a sync signal. If any sync signal is detected in error, all other signals will also be detected as a sync signal. This requires eliminating these wrong sync signals and generating new sync signals. Consequently, the window block internally executes the following operation:

(1) Detect sync signals: 11T, 11T, 2T (hereinafter called “SYNC”);
(2) Generate from SYNC a signal that is set to H level after PLCK counts 588 (hereinafter called “588T”);
(3) Set a ±9-count window with PLCK to 588T; and
(4) If SYNC is detected in this window, regard it as a correct sync signal.

If SYNC is not detected there, use 588T as SYNC up to 13 successive frames.
If SYNC is not detected in 13 or more successive frames, open the window to use SYNC detected first after that as a correct sync signal. In this case, if no sync signal is obtained from DISC in 3 successive frames, open the window again.

17.2.3. Error Detection and Correction (ECC) Block

The ECC block executes de-interleaving function and double C1/quad C2 error detection, correction, and flag processing. The correction capability is selectable with the command &hA1[4].
A super strategy is used for flag processing up to the double C1 and double C2 correction. Triple C2 correction is executed when there are three points to which no C1 correction can be made. Quad C2 correction is executed when there are found points to which no C1 correction can be made.
The ECC block also enables corrections to the EFM conversion table. This makes it possible to automatically correct T2 erroneously detected by switching the command &hAB[0] as T3.
16-kbit SRAM is used to absorb jitters for ±4 frames.
The frame counter is reset during tracking jump.
The ECC block supports CD-DA and CD-ROM modes selectable by the command &hA1[6].
The ECC block has the built-in mute and attenuation functions that are set by the command &hA0[5:4].
The function to automatically turn ON the mute function when the frame counter overflows is selectable by the command &hA1[5].
The ECC function supports normal mode and wide mode selectable by the command &h82[5:4].

Table 17.2.3.0 Control Commands in ECC Block

Setting Item	Command
Error Correction Capability	&hA1[4]
CD-DA / CD-ROM Mode	&hA1[6]
Audio Mute / −12dB Attenuation	&hA0[5:4]
Audio mute when the frame counter overflows	&hA1[5]
Normal / Wide Mode	&h82[5:4]

Table 17.2.3.1 C1 Group Flags in ECC Block

C1F1	C1F2	C1 Group Error Correction Status
0	0	No error
1	0	Single C1 correction succeeded correction
0	1	Double C1 correction succeeded correction
1	1	C1 correction disabled

Table17.2.3.2. C2 Group Flags in ECC Block

C2F1	C2F2	C2F3	C2FX	C2 Group Error Correction Status
0	0	0	0	No error
1	0	0	0	Single C2 correction succeeded correction
0	1	0	0	Double C2 correction succeeded correction
0	0	1	0	Triple C2 correction succeeded correction
1	0	1	0	Quad C2 correction succeeded correction
-	-	-	1	C2 correction disabled

17.3. RF Signal Gen (Analog) + Digital Servo Signal Processor

1.CLV and PLL
2.Servo-Type A/D Converter
3.ATS Comparator
4.TZC Comparator
5.COUT Signal Generation
6.Basic Block of Servo Filter Circuit
7.Focus Servo Filter
8.Tracking Servo Filter
9.Thread Servo Filter
10.Servo Controller
11.Focus Search
12.FZC Comparator
13.CD-RW Detection and Gain Setting
14.Tracking Jump
15.Tracking Half-Wave Brake Mode
16.Tracking Gain-Up Mode
17.Intermittent Thread Feed
18.Auto-Adjustment and Measurement
19.Flaw Detection and Countermeasure
20.Preservo Amplifier
21.YFLAG Generation
22.Directions for Pattern Layout of PCB (Recommended)

17.3.1. **CLV and PLL**

Below diagram shows the CLVPLL system components.

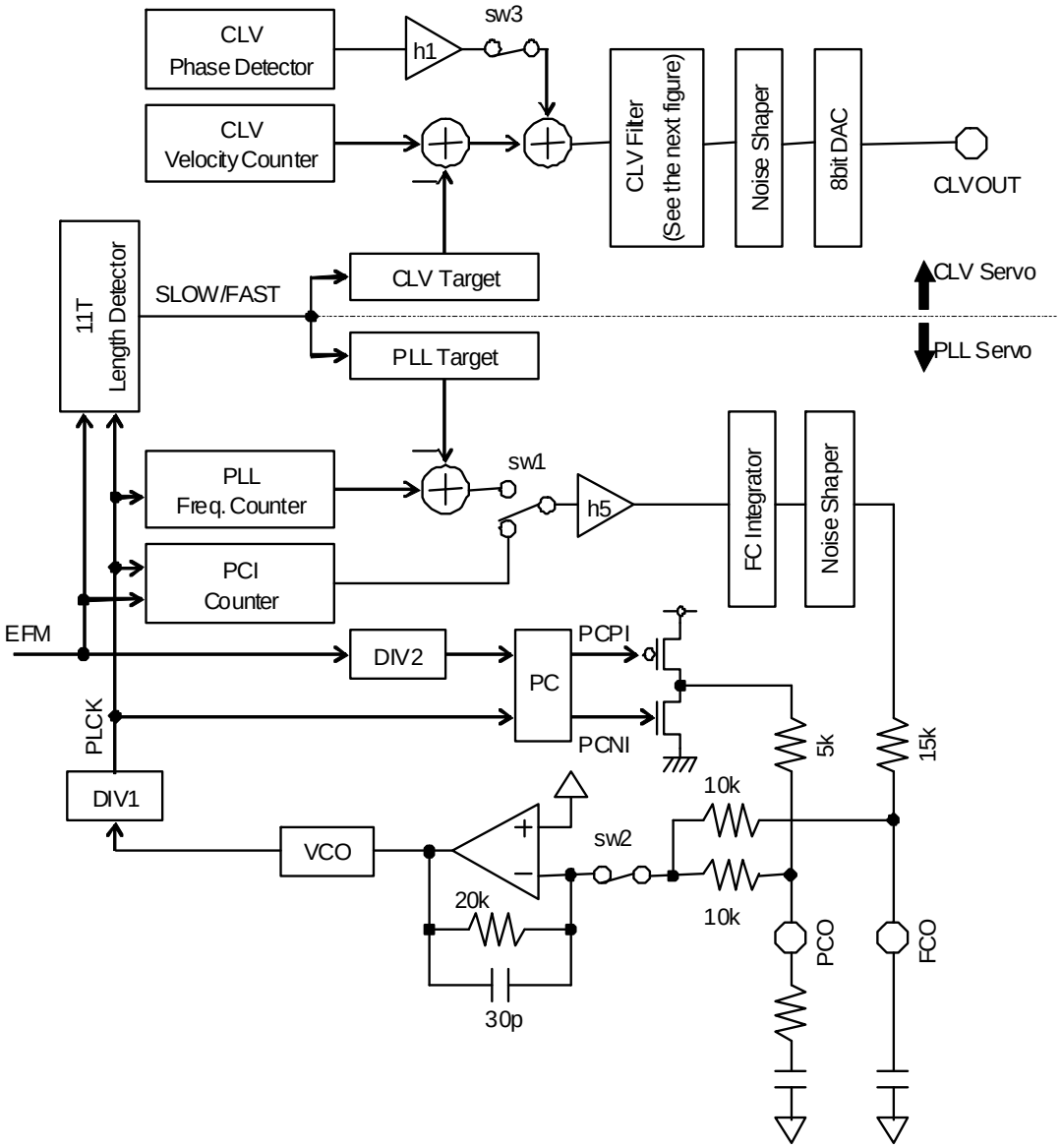


Figure 73. CLVPLL System Components

17.3.2. Functional description of each block

CLV phase detection
This block extends the output value from SRAM frame counter of the ECC by bit extension and thereby generates CLV phase error signal.
CLV speed counter
Under WIDE mode, ROUGH mode:
This counter count how often EFM edge comes during RFCK / 64 cycle.
Under SPEED PHASE mode:
This counter count how often PLCK comes during RFCK cycle.
Difference between the counted value by this counter and CLV target value is output as CLV speed error signal.
sw3, sw1
Either one is selected according to actual mode. For the detail, refer to the individual functional description of CLV and PLL.
11T length detection
This block counts EFM edge to edge length with PLCK at WFCK/4 cycle and measures maximum pulse width (detects pulse peak). The shortest pulse width at WFCK/32 cycle is detected from these measured values (detection of pulse bottom).
Under HIGH SPEED ROUGH mode, pulse peak is detected at WFCK/2 cycle and pulse bottom detected at WFCK/16 cycle.
Shift SLOW/FAST to L if counted pulth width value is 11T or less, and shift to H if the width value is larger than 11T.
PLL frequency counter
This block counts the number of PLCK/36 during RFCK/64 cycle.
Difference between this value and PLL target value is output as PLL frequency error signal.
PCI counter
This counter counts “UP” when EFM edge is earlier than startup of PLCK/2 and counts “DOWN” when it is later than startup of PLCK/2, deeming the value, which is given by &h89 command every RFCK cycle, as initial value.
Coefficient h1
This is set using command &h84[2:0].
Coefficient h5
This is set using &h83[2:0] command for PLL frequency counter and using &h84[6:4] command for PCI counter.
sw2
This is for test use, which is isolated by setting command &h63[7:4]=Eh and op-amp input data can be output from ANA_MONI0 terminal. This is to measure FC and PC loop characteristics.
DIV1
This is set using command &h50[7:6].
DIV2
This is set using command &h50[5:4].

VCO
The overall frequency characteristic of VCO can be changed by command &h9E[4:0], and tilt of the same linear characteristic be changed by command &h9F[3:0].

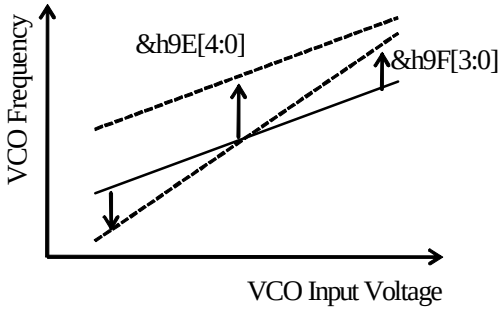


Figure 74. VCO characteristic control

CLV filter
Its shows composition of CLV filter system.

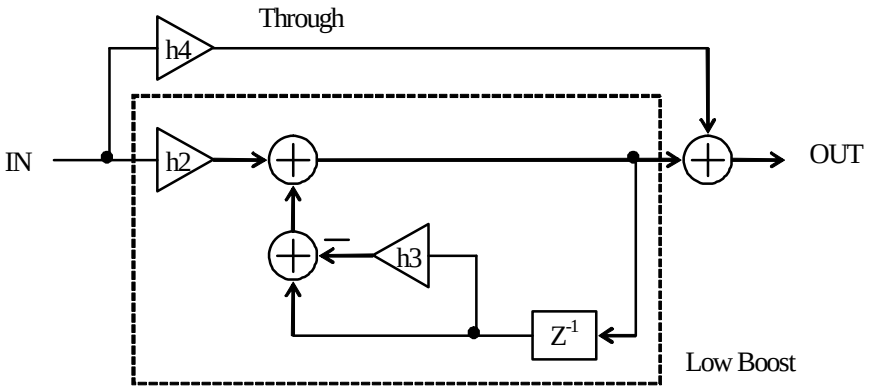


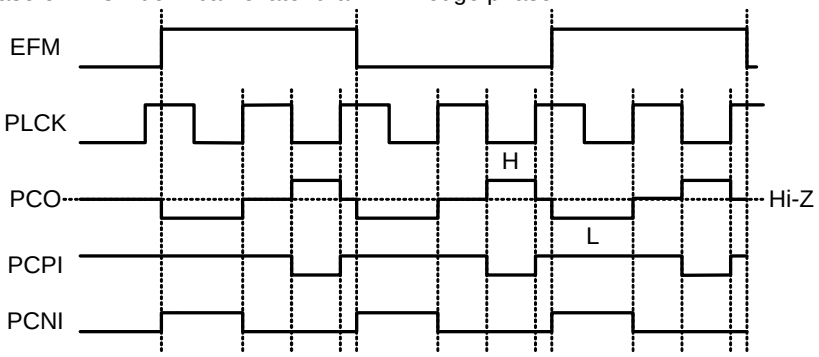
Figure 75. Composition of CLV filter system

Coefficient h2
This is set using command &h85[6:4] and &h86[6:4].
Coefficient h4
This is set using command &h85[2:0] and &h86[2:0].
Coefficient h3
Actually this is not coefficient, outputting +1LSB when input value (Z^{-1}) is positive and outputting -1LSB when it is negative.

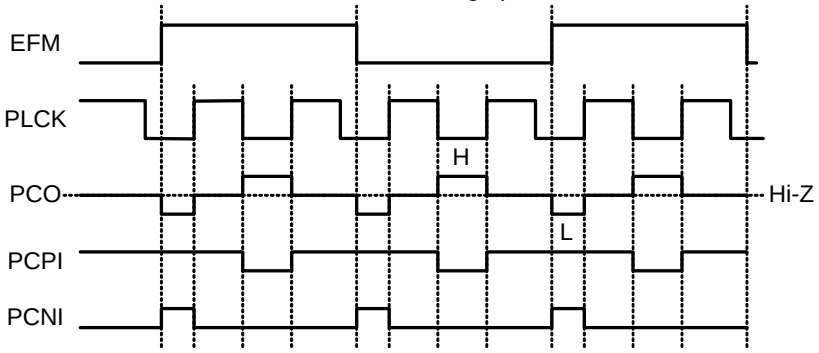
PC

This PC is intended for phase comparation of EFM edge with PLCK rise.
The diagrams below show the timing chart.

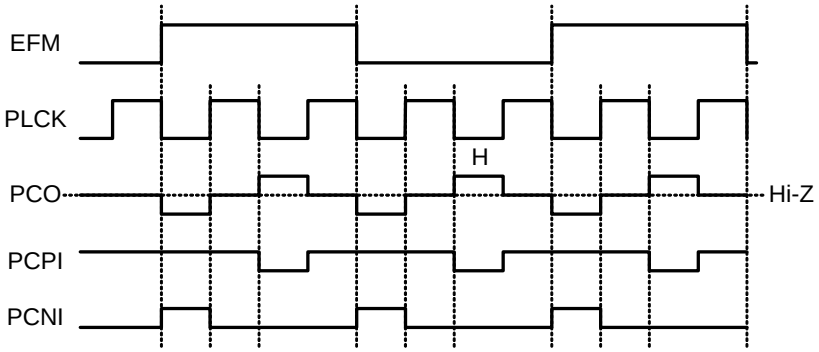
(1)Case of PLCK downcame later than EFM edge phase



(2)Case of PLCK downcame faster than EFM edge phase.



(3)Case of PLCK downcame simultaneous with EFM edge phase



PCO continues to output L until next PLCK rise from EFM edge.
And PCO outputs H throughout the first section of PLCK=L after Hi-Z.
Output from PCO is converted to LPF by built-in R and extermal C and the sign thereof is inverted by op-amp. For that, VCO acts to match both ends of EFM with PLCK downcome.

Further, when PLL is initialized, VCO/16 is input in plase of EFM, so that same value is output from PCO irrespective of positive value or negative value and the initializing function only by FCO is validated.
Furthermore, if EFM flaw is detected during usual playback, PC does same operation as initializing to theby prevents PLCK from deviating greatly from the lock.

17.3.3. Operation mode

17.3.3.1. CLV Operation mode

Table 17.3.3.1. summarizes the CLV operation mode, setting commands and conditions.

Operation mode	&h80[6:4] setup value	&h82[5:4] setup value	Description
OFF	0	-	OFF. Vc is output.
KICK	1	-	&h88[7:0] setup value is output (positive voltage)
BRAKE	2	-	2 complement to &h88[7:0] setup value is output. (negative voltage)
AUTO STOP	3	-	This is the mode to stop disc rotation automatically. At first, the operation mode is shifted to BRAKE mode and, then, BREAK mode is shifted to OFF mode when the CLV counter counted a value equivalent to 1/15 of usual value.
ON (AUTO)	4	0 or 1	The speed mode is automatically shifted to ROUGH mode against LOCK=L and to SPEED PHASE mode against LOCK=H.
SPEED PHASE	5	0 or 1	CLV target value is fixed to 588. The speed counter of CLV counts the number of PLCK during RFCK cycle and dirrerence between the two values is CLV speed error value. At the same time, sw3 turns ON and phase error value produced upon detection of CLV phase is added for control of the disc rotation.
ROUGH	6	0 or 1	CLV target value increments/decrements according to SLOW/FAST signal. When SLOW/FAST signal is L, the disc rotation is recognized as fast and consequently the CLV target value decrements. When SLOW/FAST signal is inversely H, the disc rotation is recognized as slow and consequently the target value increments. By this serch operation, the disc rotation is matched with the target value so PLL is locked. At this time, sw3 turns OFF and error component by detection of CLV phase is not added.
HIGH SPEED ROUGH	7	0 or 1	Under this mode, CLV operates similarly to ROUGH mode, but peak-bottom hold cycle for detection of 11T length shortens, which generates SLOW/FAST. This mode is used for search, etc.
WIDE	4 to 7	2	CLV target value is set using command &h81. CLV speed counter counts similarly to ROUGH mode. This WIDE mode enables to control the disc to any optional revolutions.

Table 17.3.3.1 **エラー! 参照元が見つかりません。**. Descroption of CLV operation modes

17.3.3.2. PLL operation mode

Table 17.3.3.2 summarizes the PLL operation mode, setting commands and conditions.

Operation mode	&h82[5:4] setting value	LOCK condition	Description
NORMAL INITIALIZE	0	-	Under this mode, sw1 is shifted to PLL frequency counter. PLL frequency counter counts the number of PLCK/32 during RFCK/64 cycle and aligned PLL center frequency to 4.3218MHz. This mode must be selected and executed without fail prior to usual playback.
NORMAL PC	1	-	Under this mode, FCO output terminal is held at the value under NORMAL INITIALIZE mode. And PLCK is locked to EFM signal by PCO output only. This condition is kept in reproducing in NORMAL mode.
WIDE FC	2	L	Under this mode, sw1 is shifted to PLL frequency counter. PLL frequency counter counts similarly to counting under NORMAL INITIAL mode, but PLL target value increments/decrements according to SLOW/FAST signal and PLCK frequency is changed so it matches the disc speed, whereby PLCK is enabled to follow and catch EFM frequency.
WIDE PCI	2	H	Under this mode, sw1 is shifted to PCI counter. PCI counter generates phase difference between EFM and PLCK. By using an integral value determined from this phase difference value as FCO output, PLCK can follow the disc rotation, even if it varies greatly, and continues to keep lock condition over the wide frequency band. In reproducing under WIDE mode, the PLL locks this condition at the frequency equivalent to disc speed of about ×0.5 to ×4.0 speed.

Table 17.3.3.2 Description of PLL operation modes

17.3.4. A/D Converter for Servo System

A/D convertor is samples each analog input signal from E, F, AC, BD AD_MONI0 and other terminals at time sharing and converts the sampled signals to digital value respectivery. The sampling frequency is 88.2kHz and comversion accuracy is 10bit. The conversion D-range is Vc ± 0.4*V_{DD}.
The Figure below is the input signals connection diagram for the A/D converter.

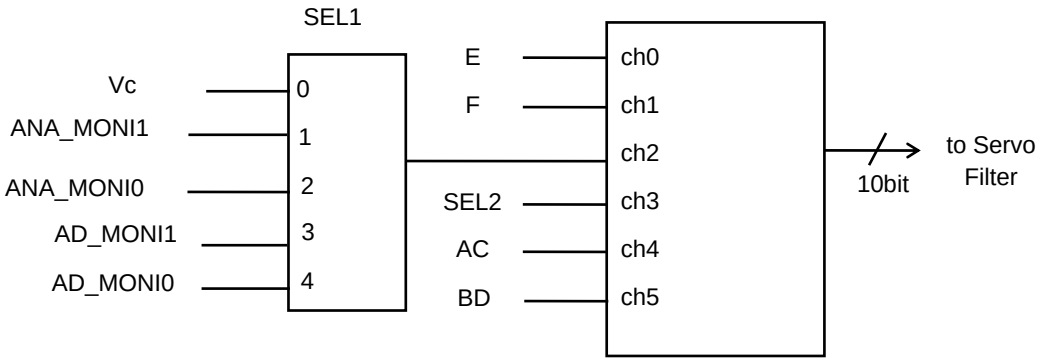


Figure 76. Input signal connection diagram for servo system ADC

The converted values from ch0, ch1, ch4 and ch5 are subtracted after conversion, and generate FE signal and TE signal. Thereafter, these signals converted value are always transferred to the sigital servo filter computing unit and used for control of each servo unit.
As for ch2 and ch3, the input signal is selected by command, and the converted value is output from DIN/DOUT and transferred to micro computer.
For the detailed operation, refer to Description of Individual Operation.
Alse, Figure 767 shows the timing chart.

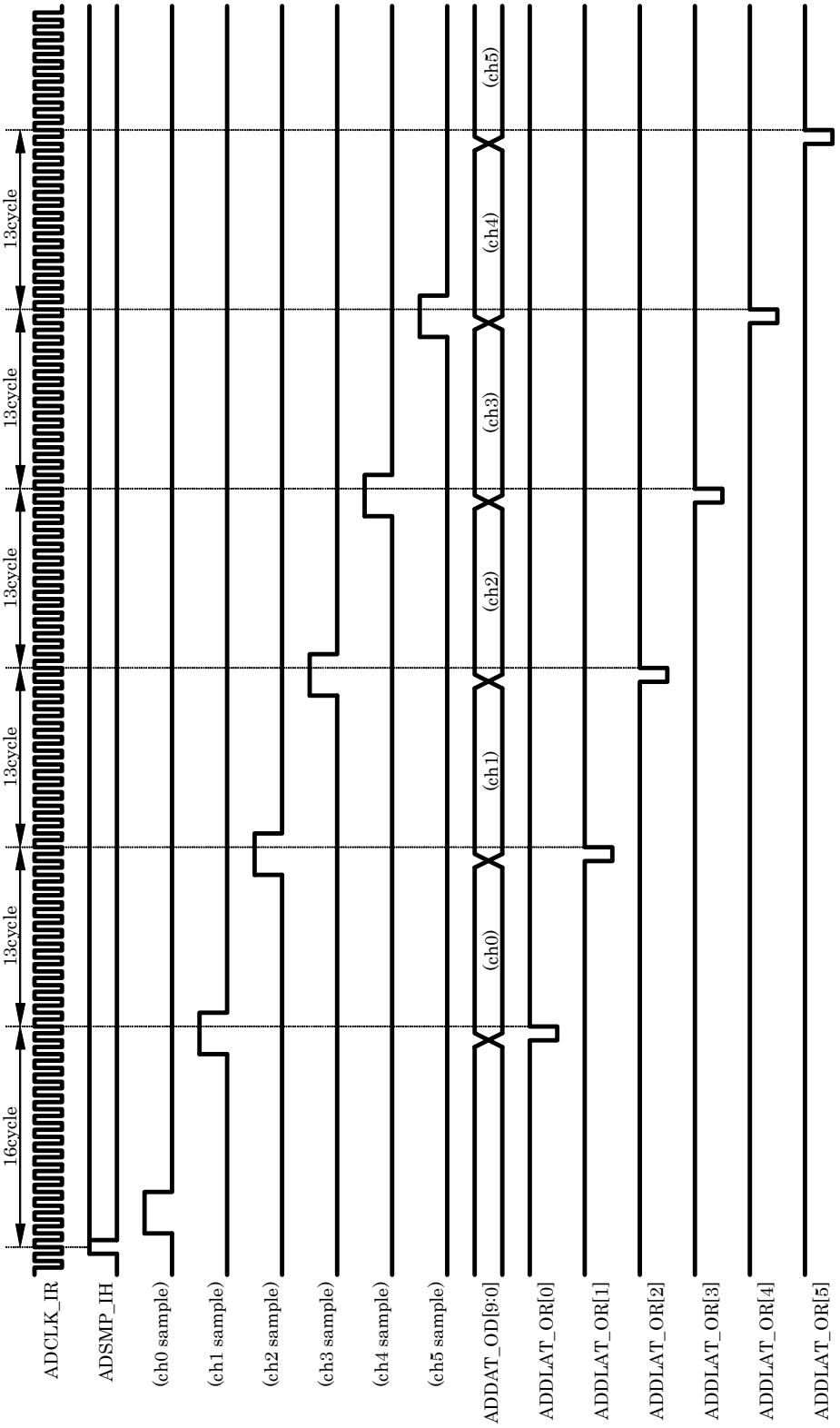


Figure 77. Servo system ADC operating timing chart

17.3.5. ATS Comparator

The Figure below is ATS comparator operation block diagram.

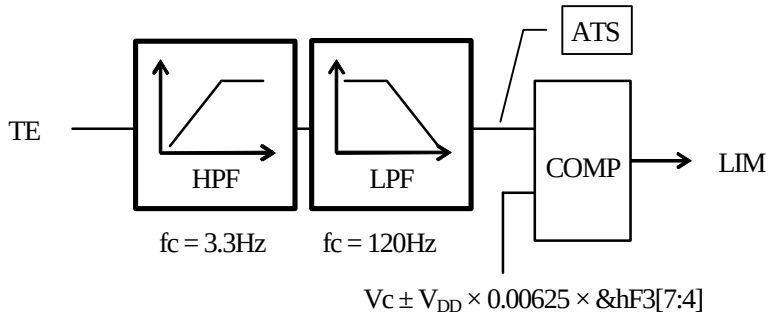


Figure 78. ATS comparator operation diagram

For usual playback, the TE signal is passed the band path filter and window comparation is excuted for the value.
The Figure below shows the I/O relation.

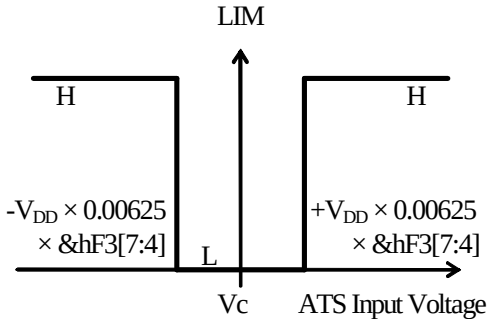


Figure 79. ATS comparator I/O characteristics

Output from the comparator (LIM) is L against the range of Vc±V_{DD}×0.00625×&hF3[7:4] and H against other than this range.
When amplitude of ATS input signal is wide, output from the comparator is H, which is deemed as shock detection condition. And tracking gain-up operation is executed to upgrade the anti-shock performance.
It is selectable by command &hCE[5] whether gain-up is executed or not by ATS.and it is selectable by command &h8C [6:4] that gain-up continued time.
For the gain-up operation detail, refer to Description of Tr jump.
It is impossible to monitor ATS comparator output itself. However, it is possible to do so, though indirect, by validating the anti-shock performance by &hCE[5]=0 and by outputting gain-up signal (TGUON) from FLAG2 terminal by &hB0[2:0]=Bh.

17.3.6. TZC Comparator

TZC comparator is comparator using digital filter and the threshold value thereof is Vc.
The Figure below shows the block diagram

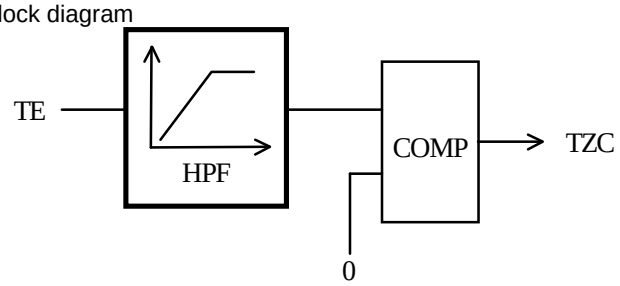


Figure 80. TZC comparator block diagram

The Cut-off frequency of HPF is selected by command &hF7[1:0].
Output data from the TZC comparator are used to count the number of tracks in track jumping.
These outputs can be monitored from FLAG2 treminal by command &hB0[2:0]=8h.

17.3.7. Generation of COUT Signal

COUT signal is a signal sampled from MIRROR signal at TZC change point, which is then used to detect moving direction of the pickup and to count the number of tracks.
The Figure below shows the timing chart for movement of the pickup in outward direction. At this time, TZC and COUT come to same phase.

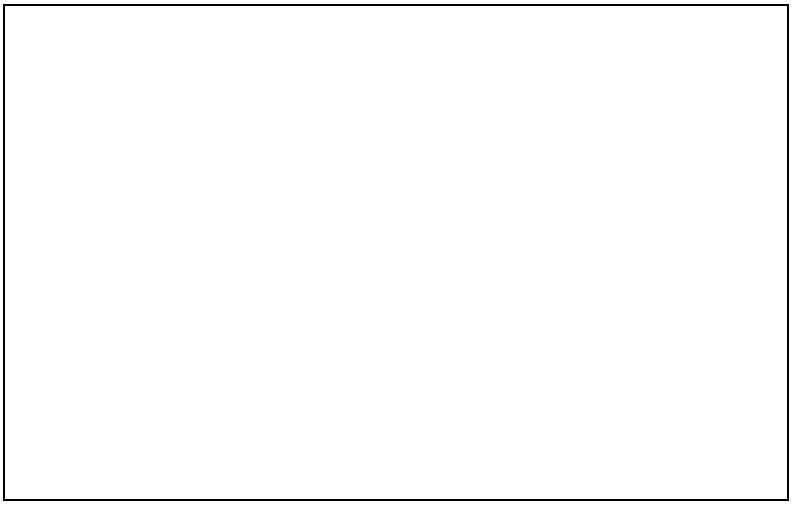


Figure 81. COUT signal-related diagram (when moving outward)

The figure below shows the timing chart for movement of the pickup in inward direction. At this time, TZC and COUT come to inverce phase to one another.

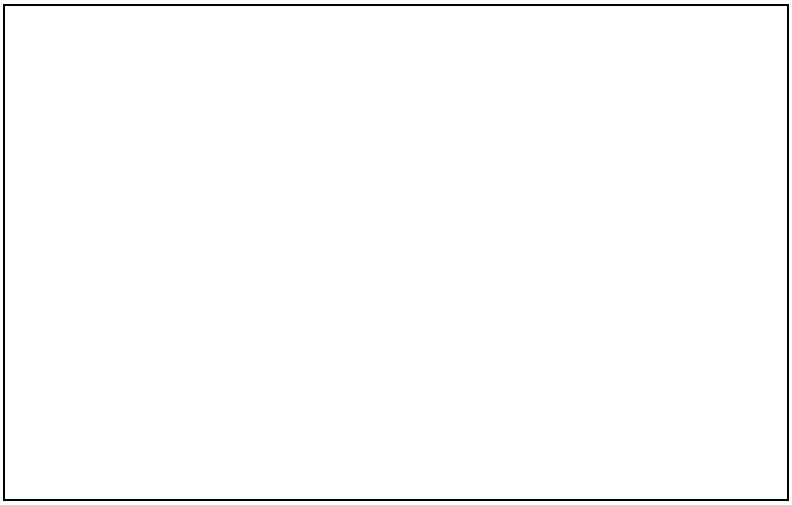


Figure 82. COUT signal-related diagram (when moving inward)

17.3.8. Basic Block of Servo Filter Circuit

This block is intended for computation of focus servo filter, tracking servo filter, sled servo filter, and band path filter and low path filter for auto adjustment, at time sharing.
The Figure below shows the basic IIR filter block composing the filter circuit.

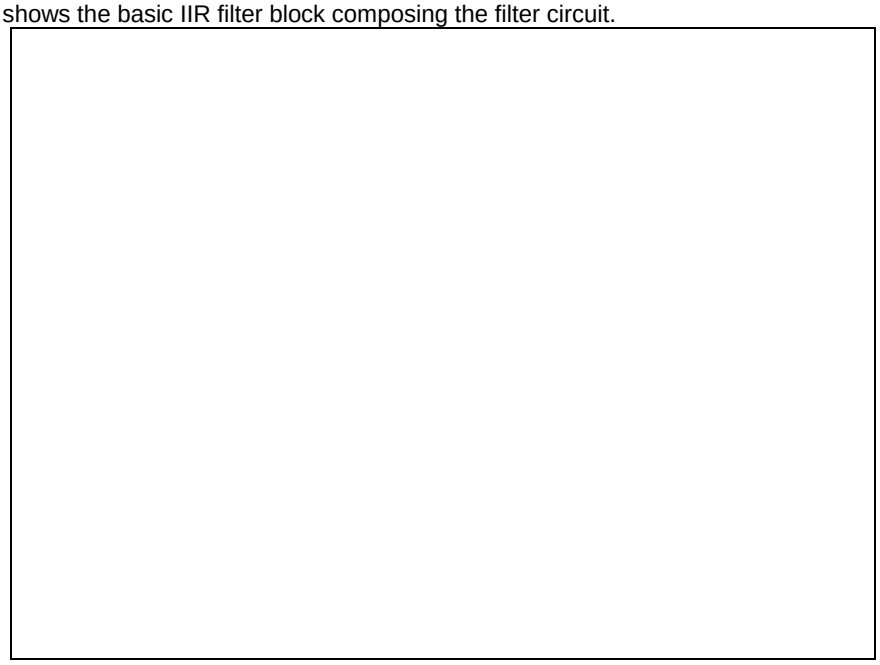


Figure 83. Basic IIR filter blocks in servo filter unit

This basic IIR filter works on sampling frequency 88.2kHz and can realize LPF and HPF by changing coefficients A1, B0, B1. Of servo filters and auto adjust filters, this basic IIR filter is used as LPF, LPS and HPF, and 3 different symbols in the above figure are used in the composition diagram for each filter to indicate the respective filter characteristic.

17.3.9. Focus Servo Filter

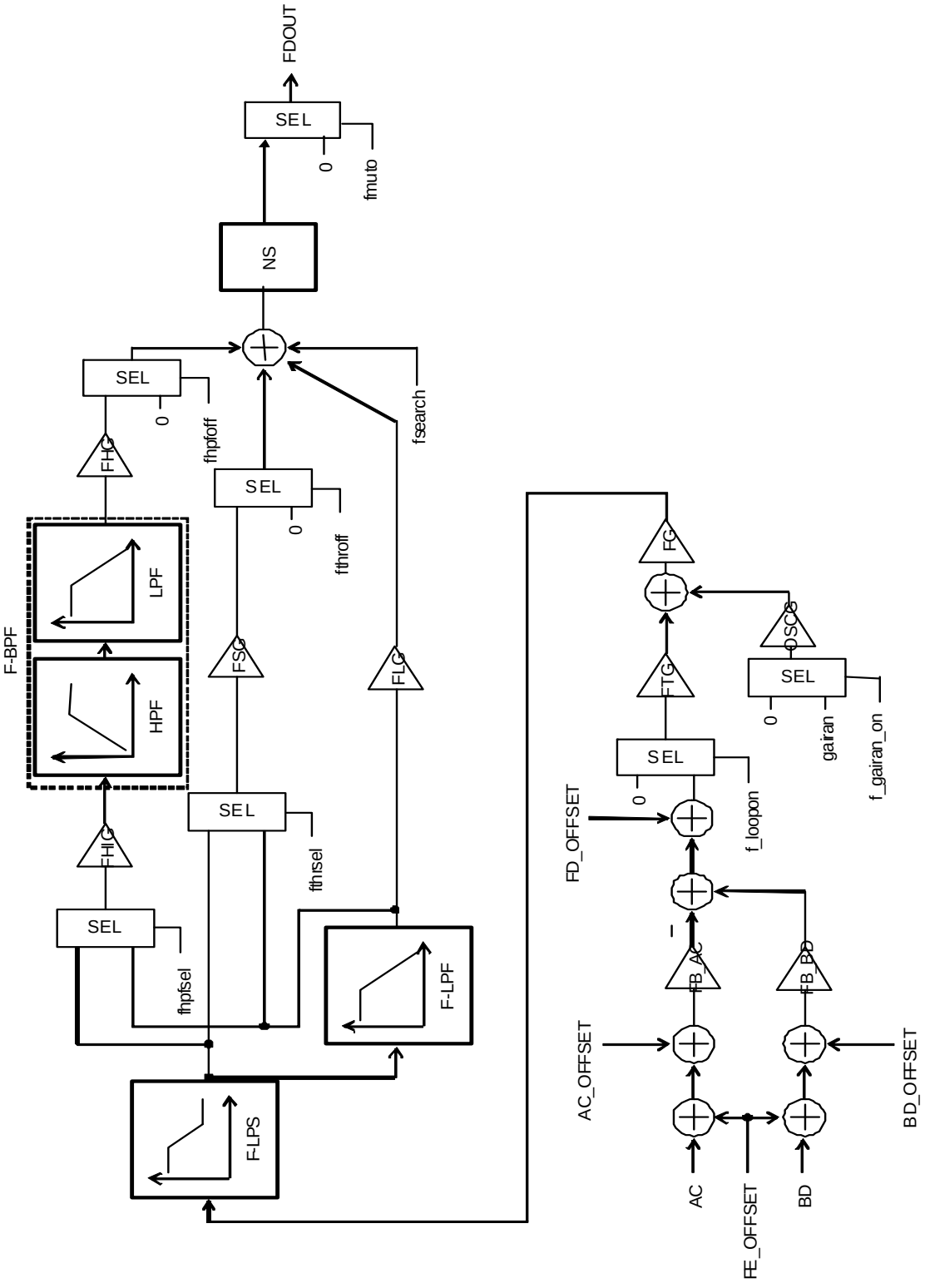


Figure 84. Focus servo filter block diagram

Input data AC,BD
Data converted from AC and BD input signal by 10bit AD converter.

FE_OFFSET
Offset value being setup by command &hF6[6:4].
AC_OFFSET, BD_OFFSET
Offset value being set up by command &h94[7:0] and &h95[7:0], which can be set up by auto adjustment sequence.
FB_AC, FB_BD
Offset value being set up by command &h98[7:0], which set up FE balance by changing AC and BD gain.
FD_OFFSET
Offset value being set up by command &h92[7:0], which can be set up by auto adjustment sequence.
f_loopon signal
Singal to turn ON Focus loop. At Command &hC0[5:4]=1 is used, this signal turns ON when the requirements is met upon focus serch. Also, when command &hC0[0]=1 is send, Focus loop is forcedly turned ON.
FTG
To set up input gain using command &hEC[3:2].
disturbance signal
Disturbance signal for auto adjustment use, being generated by servo controller. Not added in usual producing.
OSCG
To set up disturbance level using command &hED[5:0]. This disturbance level must be re-set optimally according to measured data, because it is common with the tracking filter.
f_disturbance_on signal
Add switch for disturbance, which is turned ON when measureing focus balance and gain.
FG
To set up overall gain. Command &h9A[5:0] is used for setting up. This gain can be set up per the auto adjust sequence.
F-LPS
Portion equivalent to lag lead filter in the conventional model. Cut-off and attenuation level are selected using command &hE9[7:4].
FSG, FHIG
Coefficient for gain-down operation against DEFECT and NEW_DEFECT. The operation mode is selectable by command &hD6[7:4] and gain-down level is selectable by command &hEF[4]. Furthermore, DEFECT mode can be force-selected by command &hC0[1]=1.
F-BPF
Filter unit composed of LPF+HPF, used for high-area phase compensation. Peak frequency is selectable by command &hE9[1:0].
FHG
F-BPF output addition gain, which can be set using command hE8[3:0].
F-LPF
Filter for servo band. Cut-off frequency is selected using command &hE9[3:2].
FLG
F-LPF output addition gain, which can be set using command &hE8[7:4].
fhpfsel,fthrsel,fhpfoff,fthroff signal
Switch to hold DC against DEFECT and NEW_DEFECT. This switch operation is selectable by command &hD6[7:4]. Hold system is selectable by command &hD7[5:4]. Furthermore, DEFECT mode can be force-selected by command &hC0[1]=1.
fsearch signal
Focus serch voltagel, generated by servo controller. This is fixed to a certain voltage during usual playback.
NS
This is noise shaper, which can be set using command hEF[2].
fmuto signal
Signal to turn OFF Focus loop.
Output to FDOUT terminal via servo 8bit DAC.

17.3.10. Tracking Servo Filter

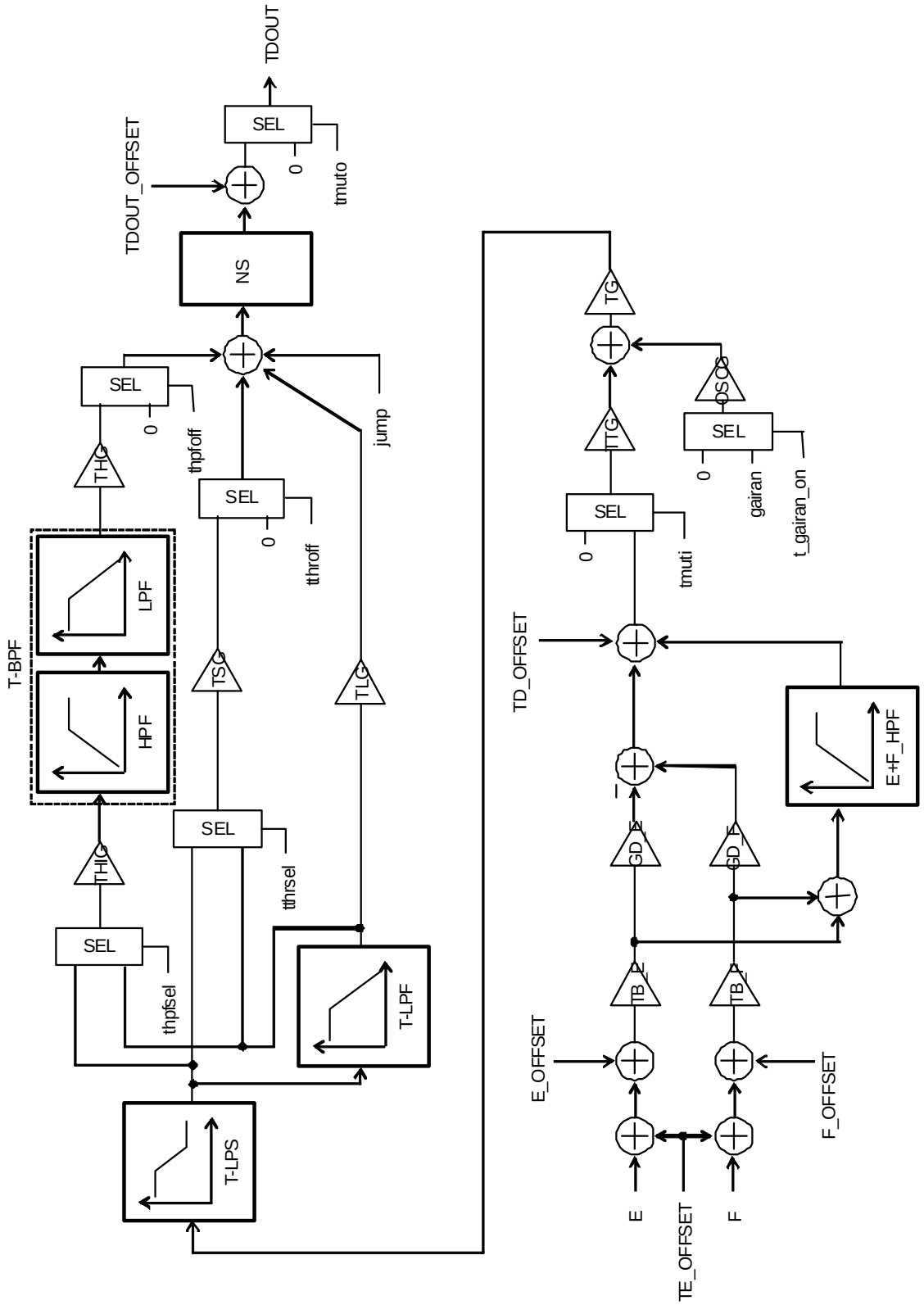


Figure 85. Tracking servo filter block diagram

Input data E,F
Data converted from E and F input signal by 10bit AD converter.
TE_OFFSET
Offset value being setup by command &hF6[2:0].
E_OFFSET, F_OFFSET
Offset value being set up by command &h96[7:0] and &h97[7:0], which can be set up by auto adjustment sequence.
TB_E, TB_F
Offset value being set up by command &h99[7:0], which set up TE balance by changing E and F gain.
E+F_HPF
High pass filter for (E+F) signal. Cut-off frequency is selectable by command &hF7[3:2].Gain is selectable by command &hF7[7:4]. Can be made reversed by command &h8D[0].
GD_E, GD_F
It is the gain for the time of gain-down operation.Gain-down level is selectable respectively by command &hF8[6:4] and &hF8[2:0].
TD_OFFSET
Offset value being set up by command &h93[7:0], which can be set up by auto adjustment sequence.
tmuti signal
Signal to turn OFF tracking loop. This signal turns OFF when the command is &hC1[5:4]=0 or during Tr jump, Sd move or when f_loopon signal is L. Also, when the command is &hC0[0]=1, &hC1[5:4] setup is force-validated.
TTG
To set up input gain using command &hEC[1:0].Gain-down level for the time of gain-down operation is selectable by command &hF9[5:4].
disturbance signal
Disturbance signal for auto adjustment use, being generated by servo controller. Not added in usual producing.
OSCG
To set up disturbance level using command &hED[5:0]. This disturbance level must be re-set optimally according to measured data, because it is common with the focus filter.
TG
To set up overall gain using Command &h9B[5:0]. This gain can be set up per the auto adjust sequence.
t_disturbance_on signal
ADD switch for disturbance, which is turned ON when measureing tracking gain.
T-LPS
It is the portion equivalent to lag lead filter in the conventional model. The Cut-off and attenuation level are selected using command &hEB[7:4].
TSG, THIG
It is the coefficient for the time of gain-down operation in the time of gain-up operation or DEFECT and NEW_DEFECT. High-area gain and through-gain can be changed by changing this gain. The operation mode is selectable by command &hD6[3:0]. The gain- up level is selectable by command &hEC[5:4] and gain-down level is selectable by command &hEC[7;6]. Furthermore, DEFECT mode can be force-selected by command &hC0[1]=1.
T-BPF
Filter unit composed of LPF+HPF, used for high-area phase compensation. Peak frequency is selectable by command &hEB[1:0].
THG
T-BPF output addition gain, which can be set using command &hEA[3:0].
T-LPF
Filter for servo band. Cut-off frequency is selected using command &hEB[3:2].
TLG
T-LPF output addition gain, which can be set using command &hEA[7:4].

thpfsel,tthrsel,thpfoff,tthroff signal
Switch to hold DC against DEFECT and NEW_DEFECT. This switch operation is selectable by command &hD6[3:0]. Hold system is selectable by command &hD7[6:4]. Furthermore, DEFECT mode can be force-selected by command &hC0[1]=1.
NS
This is noise shaper, which can be set using command &hEF[3].
TDOUT_OFFSET
Offset value being setup by command &hF9[3:0].
jump signal
Output selected when Tr jump.
tmuto signal
Signal to turn OFF the tracking loop. This signal turns OFF during Sd move or when the command is &hC1[5:4]=0 or when f_loopon signal is L. Also, when the command is &hC0[0]=1, &hC1[5:4] setup is force-validated.
Output data TDOUT
Output to TDOUT terminal via servo 8bit DAC.

17.3.11. Sled Servo Filter

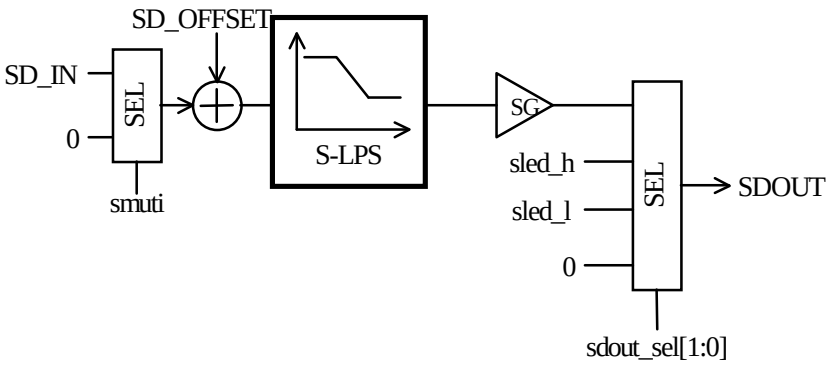


Figure 86. Sled servo filter block diagram

Input data
Output data from LPF of tracking servo filter.
smuti signal
Signal to turn OFF the sled loop.
SD_OFFSET
Offset value set up using command &h91[7:0], which can set up per auto adjustment sequence.
S-LPS
Lag lead filter. Attenuation level can be selected by command &hF5[2:0]. When the command is &hF5[2:0]=0, the filter comes to LPF, whose Cut-off frequency is 188Hz.
SG
Sled gain, selectable by command &hF4[7:0].
sled_h, sled_l
Output selected when the sled moves or multi Tr jump or command is &hC1[1:0]=2,3. Output value is set up using command hFE[7:4].
sdout_sel signal
Sled servo control signal, controlled by command &hC1[1:0] of controller. The servo ON precondition is &hC1[1:0]=1 and, in addition, GFS88 signal is H. In the case of &hC0[0]=1, &hC1[1:0] setup is force-validated.
Output data
Output to SDOUT terminal via servo 8bit DAC.

17.3.12. Servo controller

This is the control block to control focus search, track jump, sled intermittent feed, auto adjust function, etc.
For the detail, refer to the description of each control item.

17.3.13. Focus search

17.3.13.1. Focus ON operation

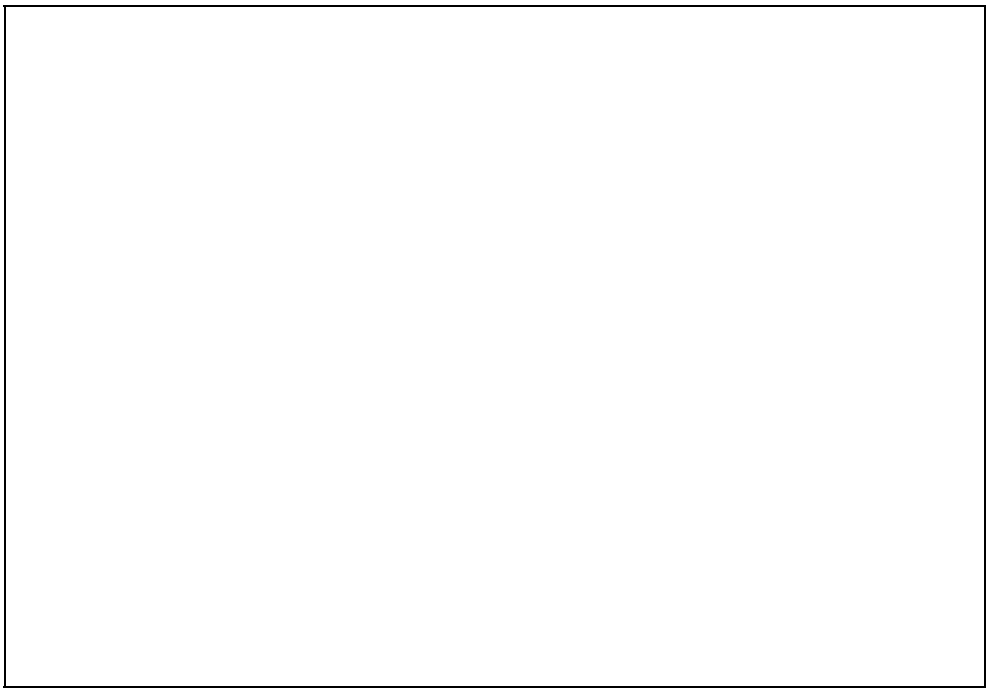


Figure 87. Focus ON operation timing chart

By using command &h60[4]=1, LON terminal gets H to allow laser ON and the focus search is started simultaneously. Initially F_LOOPON signal is L and the loop is in OFF. Fsearch voltage reduces once to minimum value (FSMIN) and thereafter, begins to increase toward maximum value (FSMAX). At this time, S-shaped curve appears in FEIN if the system is normal. FEIN is converted to FZC signal through FZC comparator. When this FZC signal downcome is detected, F_LOOPON signal comes to H to allow the loop close and, at this time, fsearch voltage is held. FSMIN is set by &hC8[3:0] and FSMAX set by &hC8[7:4] respectively. The fsearch voltage decremental speed rate is set up by &hC9[2:0] and the fsearch voltage incremental speed rate set up by &hC9[6:4]. Furthermore, inverted-S shaped curve appears on FEIN while fsearch voltage is decrementing. Under this inverted-S shape, it can be selectable whether the loop is turned ON or not, by &hC9[7].
If FZC signal is failed to be detected, fsearch voltage increments and decrements smoothly and repeatedly in the range of FSMIN to FSMAX. It can be discriminated whether fsearch voltage is incrementing or decrementing, by FSDOWN internal signal. Each signal of F_LOOPON and FSDOWN can be read as the internal status. For the detail refer to “Description of Command Interface”.

17.3.13.2. Focus recovery

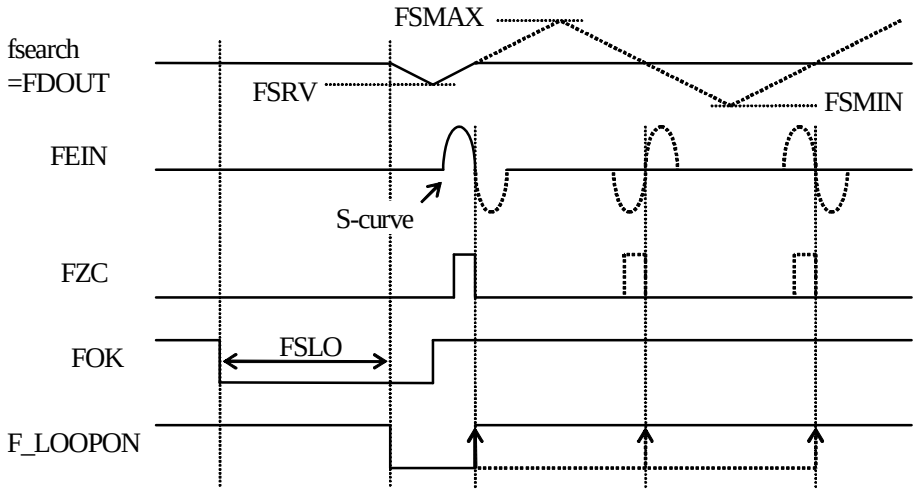


Figure 88. Focus recovery operation timing chart

This function is intended for focus re-searching in the case of focus failure during playback.
If FOK signal L level continues for FSLO time only, fsearch voltage decrements to the recovery start voltage (FSRV) and thereafter begins to increment toward FSMAX. Subsequently the same operation as focus search operation is executed and the loop turns ON. In addition, after this focus recovery operation, the tracking goes into gain-up + half-wave brake condition to quicken tracking completion. The precondition for resetting gain-up and half-brake is same as that for Tr jump. For the detail refer to Description of Tr jump.
Further, FSLO time is set up by &hCA[6:4] and FSRV voltage set up by &hCA[3:0].

17.3.14. FZC Comparator

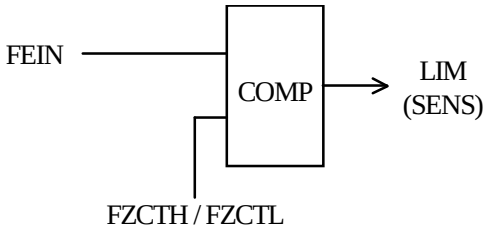


Figure 89. FZC comparator actuation block diagram

FZC comparator actuates upon comparison of the FEIN signal with the threshold value. FZC signal is used for detection of S-shaped focus as description in Focus Search.
The Figure below shows the timing chart (example).

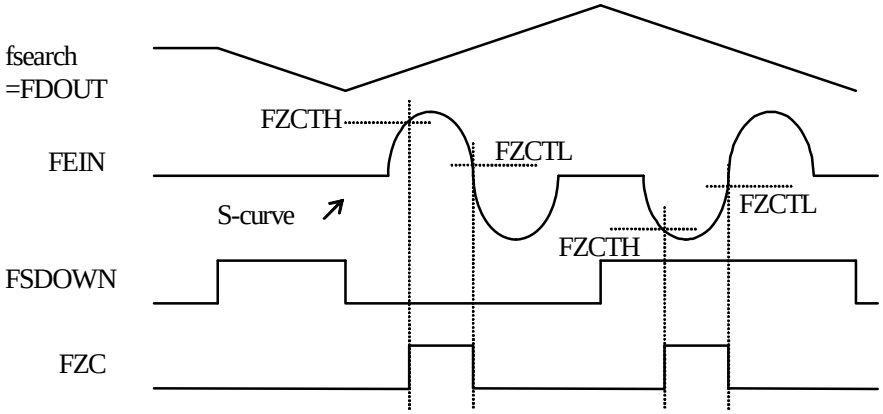


Figure 90. FZC comparator operation timing chart

The threshold value can be set individually for L→H (FZCTH) and H→L (FZCTL). The setting commands used are &hF2[7:4] and [3:0]. Also, the zone above S-shaped Vc is compared with the setup threshold value when f_search voltage is incrementing (FSDOWN is L), and the zone below S-shaped Vc is compared with the setup threshold value when f_search voltage is decrementing (FSDOWN is H).

17.3.15. CD-RW detection and Gain setting

FSFZC signal is used to detect CD-RW disc. This signal comes to H when FZC is detected even once during focus search, internal signal which returns to L after reset by issue of Focus OFF command.
Because of its reflectance lower than press disc and CD-R disc, CD-RW disc is held as FSFZC=L, if H-side comparate level is set properly by command &hF2[7:4], whereby present disc can be judged to be CD-RW disc.
FSFZC signal can be read from internal status.
Furthermore, at this time each gain in RF is increased by command &h61[5:4] and it is enable to get optimum gain setting for CD-RW.

17.3.16. Track Jump

Commands for jump in outer peripheral direction	Commands for jump in inner peripheral direction	Description
&hC400	&hC600	For 1 Tr jumping
&hC4XX	&hC6XX	For Tr jumping at setup value*2 when setup value is other than 00
&hC5XX	&hC7XX	Sled move on Tr at setup value*128

Table 17.3.16. Commands for jumping and description of each commands

17.3.16.1. Tr jump

This jump is effected when command &hC400 or &hC600 is issued.

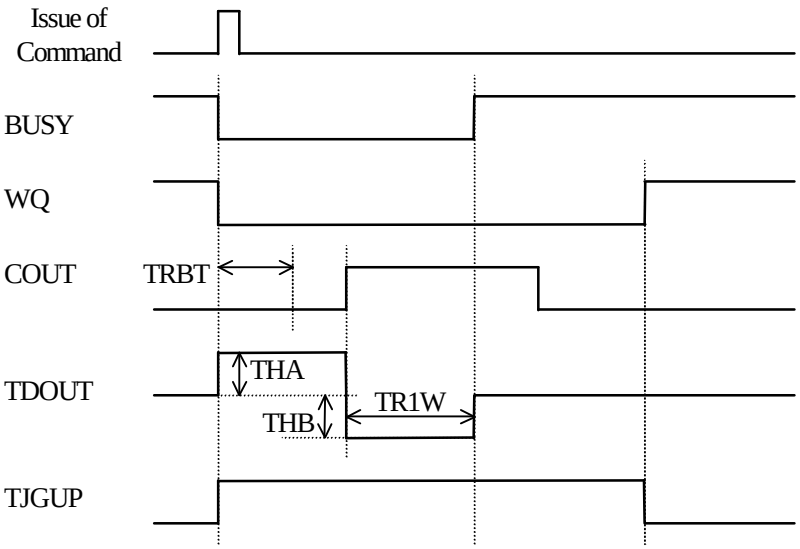


Figure 91. Tr jump (by issue of &hC400) timing chart

After issue of the command, BUSY signal comes to L. At this time, the tracking filter is put in DC HOLD condition and the data added acceleration pulse and LPF output is output from TDOUT terminal. The acceleration pulse height (THA) is set up using command &hFD[7:4].
The acceleration pulse is output continually until COUT signal rises after COUT signal had held L for a time longer than the blind time (TRBT). TRBT is set up using command &hCC[7:4].
Deceleration pulse is output from TDOUT terminal for the time of (acceleration pulse output time) × TR1W, commencing from the time point when the acceleration pulse output ended. The deceleration pulse height (THB) is set up by command &hFD[3:0] and TR1W set up by command &hCB[7:6].
Upon completion of the jump pulse output, BUSY signal comes to H, showing Tr jump ended. And the tracking filter goes into gain-up + half-wave brake condition. Return of the filter to the usual condition from this condition is effected when WQ has come to H. For the GAIN-UP mode and HALF-WAVE BRAKE mode, refer to the description of these modes given later separately.
Also, when jumped in inverted direction, TDOUT output positive and negative values are inverted.

17.3.16.2. The signal used for track number counting at Multi Tr jump/Sled move

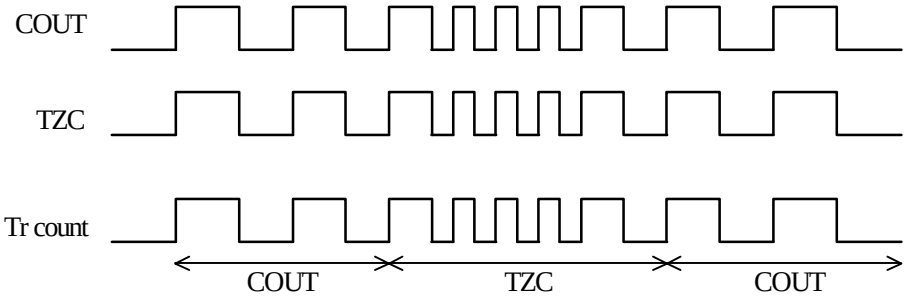


Figure 92. Relation of the signal used for track number counting at multi Tr jump

At multi Tr jump and Sled move, either COUT or TZC signal is selected for the signal used for Tr number counting by the period of signal. For this, COUT signal is used for Tr number counting signal when the period is slow and when the period is fast, TZC signal is used. It is enable to set the period to change the signal using for Tr number counting by command &hCB[3:0].

17.3.16.3. Multi Tr jump (1)

This multiple track jump is effected when the command is &hCB[5]=0, after issue of command &hC4XX or &hC6XX. (XX: other than 0)

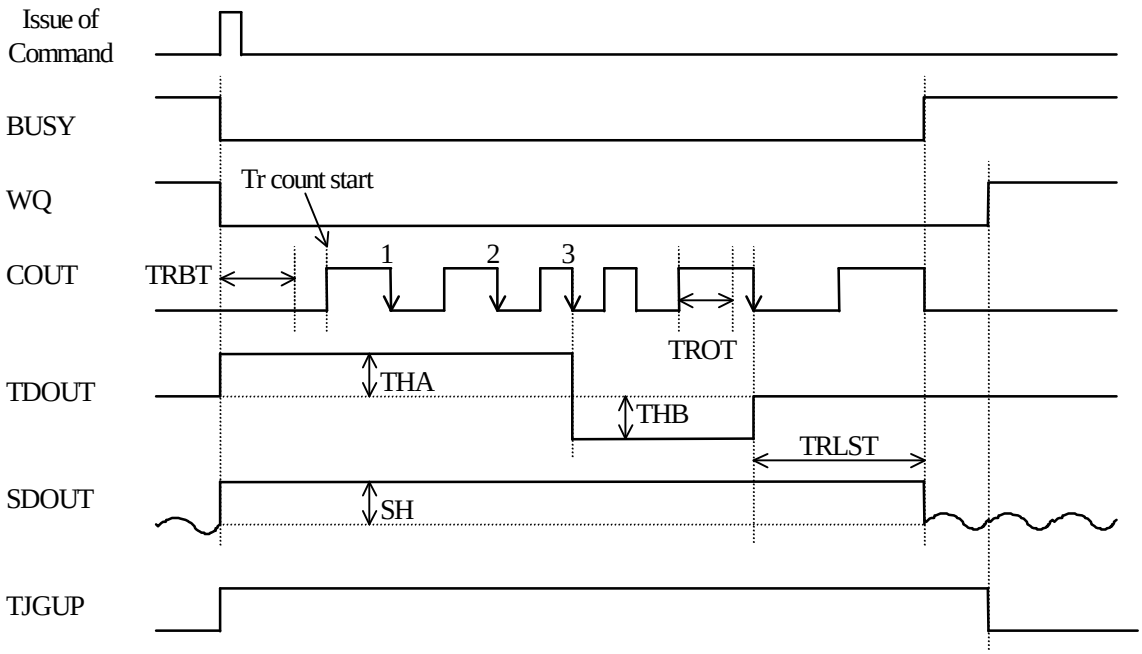


Figure 93. Multi Tr jump (1) (by issue of &C403) timing chart

After issue of the command, BUSY signal comes to L. At this time, the tracking filter is put in DC HOLD condition and the data added acceleration pulse and LPF output data is output from TDOUT terminal. The acceleration pulse height (THA) is set up using command &hFD[7:4]. Also, output of acceleration pulse from SDOUT terminal begins simultaneously, too. Sled pulse height (SH) set up using command &hFE[7:4].
Tr number counting begins with rise of COUT signal after COUT signal had held L for the time longer than blind time (TRBT). TRBT is set up by command &hCC[7:4]. Either COUT or TZC signal is selectable by command &hCB[4], as the signal useing for Tr number counting. When COUT signal is selected, by command &hCB[3:0], either COUT or TZC signal is changed for the signal using for Tr number counting by the period of Tr number counting.
The acceleration pulse from TDOUT terminal is output continually until Tr number counted value reaches the setup value. On the other hand, output of deceleration pulse from TDOUT terminal begins with end of the acceleration pulse output and is continued until COUT signal downcome after COUT signal had held H for the time longer than overflow time (TROT). This deceleration pulse height (THB) is set up by command &hFD[3:0] and TROT is set up by command &hCC[3:0].
Upon completion of the jump pulse output from TDOUT terminal, the tracking filter goes into gain-up + half-wave brake condition. Return of the filter to the usual condition from this condition is effected when WQ has come to H. For the GAIN-UP mode and HALF-WAVE BRAKE mode, refer to the description of these modes given later separately.
Acceleration pulse output from SDOUT terminal is continued excessively for TRLST time after completion of pulse output from TDOUT terminal. This is to enable adequate sled feed in executing Tr jumping because usually the sensitivity of sled motor sensor is lower than that of Tr actuator sensor. After completion of acceleration pulse output from SDOUT terminal, BUSY signal comes to H, showing that Tr jump ended. TRLST time is set up by command &hCD[6:0].
Also, when jumped in inverted direction, TDOUT and SDOUT output positive and negative values are inverted.

17.3.16.4. Multi Track Jump (2)

This multiple track jump is effected when the command is &hCB[5]=1, after issue of command &hC4XX or &hC6XX. (XX: other than 0)

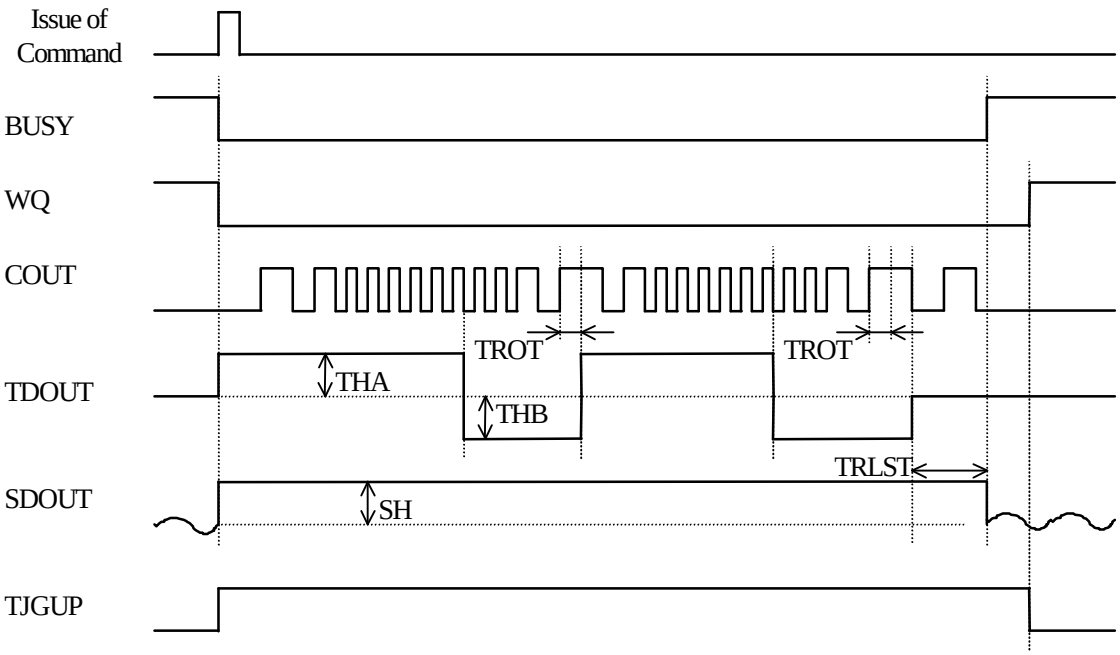


Figure 94. Multi Tr jump (2) (by issue of &hC410) timing chart

Under this mode, Tr jump similar to jumping by feed of &hC408 in Multi Tr Jump (1) mode is continued up to the cycles set up by &hC4[7:3]. However, the precondition for discontinuing deceleration pulse output from TDOUT terminal at the jump go-on point is not COUT signal downcome but the moment when H-section of COUT signal exceeded the blind time.
BUSY signal comes to H when Sled acceleration pulse output has ended.
Furthermore, in the case of this jump mode, it is prohibited to send such a command (ex. &hC403) that &hC4[7:4] comes to 0, except 1 Tr jump command.
Also, when jumped in inverted direction, TDOUT and SDOUT output positive and negative values are inverted.

17.3.16.5. Sled move

Mode effected when command &hC5XX or &hC7XX is issued.

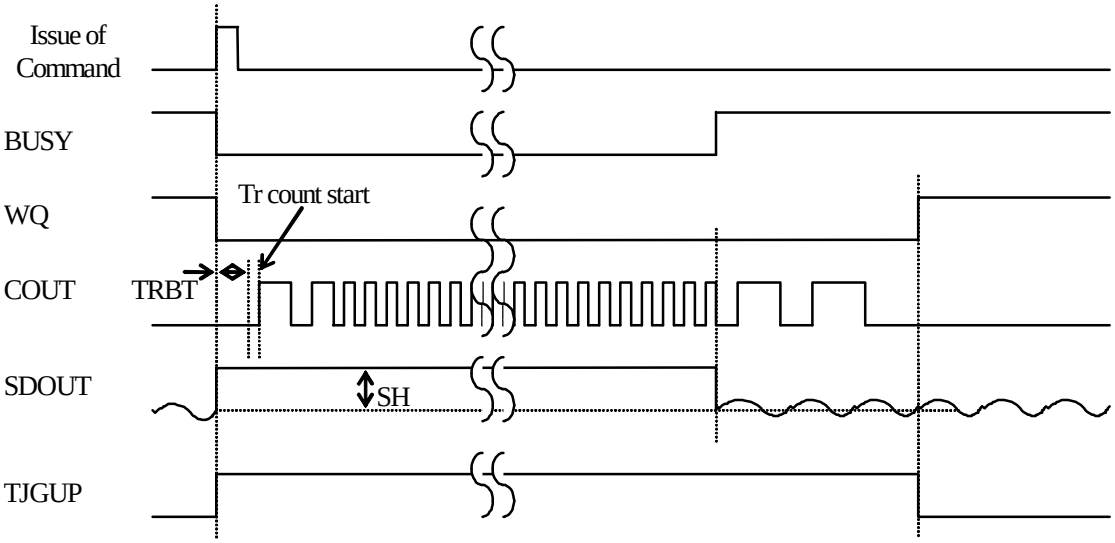


Figure 95. Sled move (by issue of &hC5XX) timing chart

After issue of the command, BUSY signal comes to L and acceleration pulse is output from TDOUT terminal. The sled pulse height (SH) is set up using command &hFE[7:4]. At this time, Vc is output from TDOUT terminal.
Tr number counting begins with rise of COUT signal after COUT signal had held L for the time longer than blind time (TRBT). TRBT is set up by command &hCC[7:4]. Either COUT or TZC signal is selectable by command &hCB[3:0], as the signal used for Tr number counting.
The acceleration pulse is output continually until Tr number counted value reaches the setup value*128.

Upon completion of the jump pulse output, the tracking filter stops Vc output and goes into gain-up + half-wave brake condition. Return of the filter to the usual condition from this condition is effected when WQ has come to H. For the GAIN-UP mode and HALF-WAVE BRAKE mode, refer to the description of these modes given later separately.
Upon completion of acceleration pulse output from SDOUT terminal, BUSY signal comes to H, showing that “sled move” has completed.
Also, when the sled moves in inverted direction, SDOUT output positive and negative values are inverted.

17.3.17. Tracking HALF-WAVE BRAKE Mode

The Figure below shows the brake timing chart in Tr half-brake mode in the case of jump in outward direction.

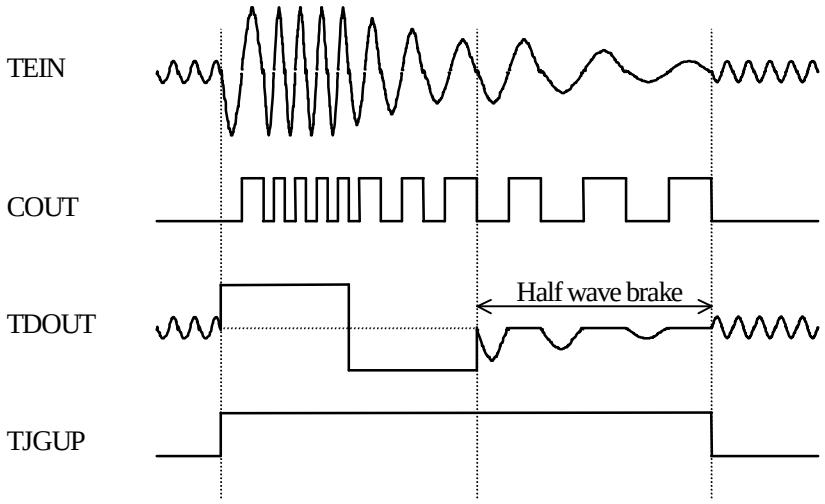


Figure 96. Brake timing chart in half-wave brake mode

After Tr jump pulse output ended, the pickup continues to move by its inertia. It is really difficult to stop the inertia movement, which then cause Tr guiding into Tr servo loop to get worse. At this time, if the Tr HALF-WAVE BRAKE mode turns ON, the COUT signal acts to turn ON Tr filter loop when the signal is in L section and acts to turn OFF the same loop when the signal is in H section. This means that braking is applied to jump directional movement of the pickup, whereby Tr servo can be reset earlier.
This mode is automatically turned ON after Tr jump and focus recovery using command &hCF[4], and reset when WQ=H. For delaying more the reset timing, reset this mode manually using command &hCE[7].
Further, when jumped in reverse direction, TEIN waveform and TDOUT output positive and negative values are inverted and Tr loop turns ON only when braking is applied in jumping direction.

17.3.18. Tracking Gain-Up Mode

This is the mode used to stabilize Tr earlier, where it is unstable. For that, Tr servol filter through (medium area) and BPF (high area) gains are increased by TGUP. TGUP is set up using command &hEC[5:4].
This mode turns ON simultaneously with Tr HALF-WAVE BRAKE mode after Tr jump and when focus recovery which is selected by command &hCF[4] is executed and the mode is reset when WQ=H. For delaying more the reset timing, however, reset this mode manually using command &hCE[7].
Also, on occasion this mode turns ON independently. It does so under ANTI-SHOCK mode. For the ANTI-SHOCK mode detail, refer to Description of ATS Comparator.

17.3.19. Sled Intermittent Feed

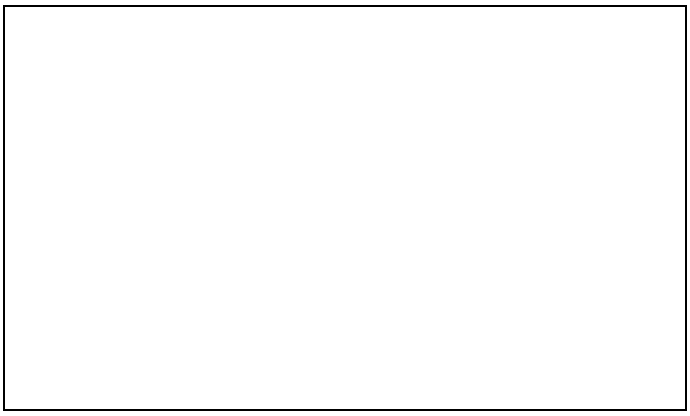


Figure 97. Sled intermittent feed timing chart

This function is intended to control ON/OFF of output to SDOUT terminal, based on the preset threshold value. Usually an insensible zone exists in the sled motor. Therefore, useless energy is consumed while the output is kept ON in the insensible zone. So, this function is turned ON to prevent useless power consumption.

COMPARATE level is set up individually for ON-side STH and OFF-side STL. STH is set up using command &hF0[6:0] and STL set up using command &hF1[6:0].
Furthermore, VALIDATE/INVALIDATE of this function can be selected using command &hCF[7].

17.3.20. Auto Adjustment and Measurement

This is the sequence to be followed after command &hD0XX was sent.
When the measurement has completed correctly, the measured result is read using command &hDE. As to how to read, refer to Description of Command Interface.
The table below lists respective commands and the measuring conditions, together with the commands used for adjustment of the respective values.

Command for measurement	Measuring items	Measuring conditions	Command for adjustment
&hD01X	SDOUT offset	Before Fo servo ON	&h91XX
&hD02X	FDOUT offset	Before Fo servo ON	&h92XX
&hD03X	TDOUT offset	Before Fo servo ON	&h93XX
&hD04X	AC offset	Before Fo servo ON	&h640X
			&h94XX
&hD05X	BD offset	Before Fo servo ON	&h650X
			&h95XX
&hD06X	E offset	Before Fo servo ON	&h660X
			&h96XX
&hD07X	F offset	Before Fo servo ON	&h670X
			&h97XX
&hD08X	Focus balance	(In case of using MAX/MIN) Fo servo OFF	&h98XX
		(In case of using RFRP) Fo servo ON, Tr servo ON	
&hD09X	Tracking balance	Fo servo ON, Tr servo OFF	&h99XX
&hD0AX	Focus gain	Fo servo ON, Tr servo ON	&h9AXX
&hD0BX	Tracking gain	Fo servo ON, Tr servo ON	&h9BXX
&hD0CX	RF offset	(At setting initial value) Fo servo OFF	&h9CXX
		(At playback) Fo servo ON, Tr servo ON	
&hD0CX	RF gain	Fo servo ON, Tr servo ON	&h9DXX
&hD0EX	VCO offset	Before Fo servo ON	&h9EXX
&hD0EX	VCO gain	Before Fo servo ON	&h9FXX

Table 17.3.20. Auto adjustment command and adjustment command

Design is so made that the larger measured data can be got correspondingly by setting up the adjustment commands at larger values.

The measuring procedure is described in detail hereunder.

17.3.20.1. Measurement of AC/BD/E/F Offset

These measurement are executed when either one of commands &hD04X to &hD07X is issued. AC/BD/E/F offset can be canceled by setting each offset value by applicable command.

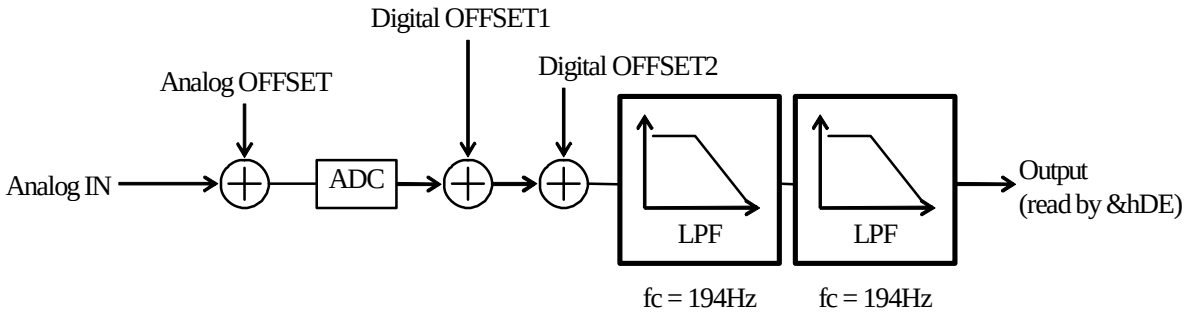


Figure 98. Block diagtam relating to AC/BD/E/F offset measurement

When the command to measure offset is issued, ADC selects an input signal and offset is added to output value. By Analog OFFSET, offset adjustment is executed roughly not to over the D-range of ADC. Digital OFFSET1 is added for making ADC output to Vc, and set up in proportion to the initial value of analog output. Digital OFFSET2 is for close offset adjustment.

	Commands for measurement	Analog OFFSET	Digital OFFSET1	Digital OFFSET2
AC offset	&hD04X	&h64[2:0]	&hF6[6:4]	&h94[7:0]
BD offset	&hD05X	&h65[2:0]	&hF6[6:4]	&h95[7:0]
E offset	&hD06X	&h66[2:0]	&hF6[2:0]	&h96[7:0]
F offset	&hD07X	&h67[2:0]	&hF6[2:0]	&h97[7:0]

Table 17.3.20.1. Commands for adjustment AC/BD/E/F offset

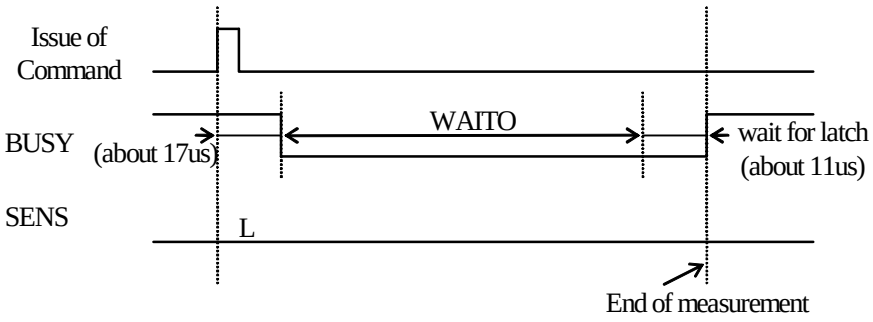


Figure 99. Timing chart relating to AC/BD/E/F offset measurement

BUSY signal comes to L in about 17us after issue of the command.
ADC output passes through primary LPF 2 stages after offset added. LPF output is latched at the time point when WAITO time has passed. Thereafter, the BUSY signal comes to H, showing the measurement ended. Read the result using command &hDE.
WAITO time is the waiting time until measurement stabilizes, which is set up using command &hD2[7:4].
Further, SENS=L remains unchanged in measuring AC/BD/E/F offset.

17.3.20.2. Measurement of FD/TD Offset

These measurements are executed when the command either &hD02X or &hD03X is issued. FD/TD offset can be canceled by setting each offset value by applicable command.

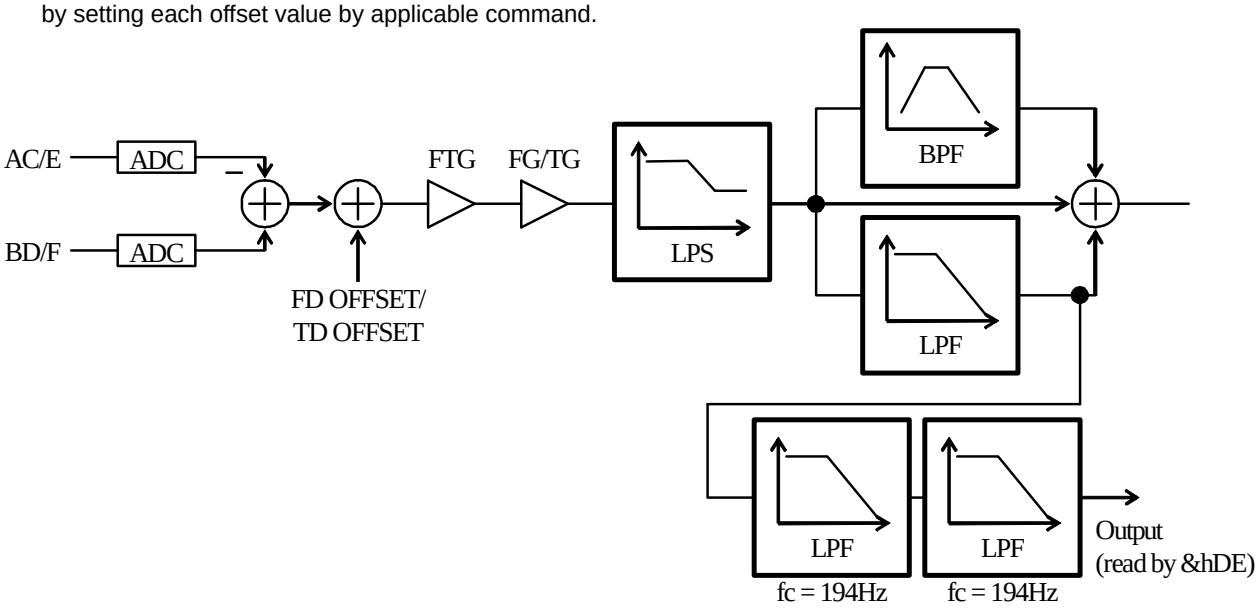


Figure 100. Block diagram relating to FD/TD offset measurement

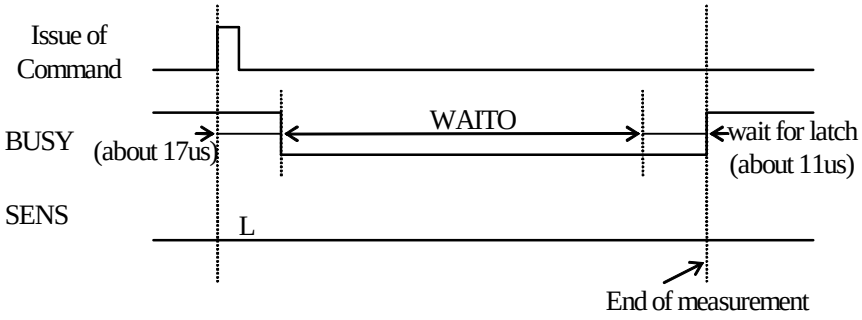


Figure 101. Timing chart relating to FD/TD offset measurement

	Commands for measurement	FD OFFSET/ TD OFFSET
FD offset	&hD02X	&h92[7:0]
TD offset	&hD03X	&h93[7:0]

Table 17.3.20.2. Command for adjustment FD/TD offset

BUSY signal comes to L in about 17us after issue of the command and measurement is started.
At this time, if command is &hD02X, input signals to ADC come to AC and BD signal and if command is &hD03X, come to E and F signal. ADC output passes through LPS and LPF of servo filter and primary LPF 2 stages after offset added. LPF output is latched at the time point when WAITO time has passed. Thereafter, the BUSY signal comes to H, showing the measurement ended. Read the result using command &hDE.
WAITO time is the waiting time until measurement stabilizes, which is set up using command &hD2[7:4].
Further, SENS=L remains unchanged in measuring FD/TD offset.

17.3.20.3. Measurement of SD offset

This measurement is excuted when command &hD01X is issued. SD offset can be canceled by setting offset value by applicable command.

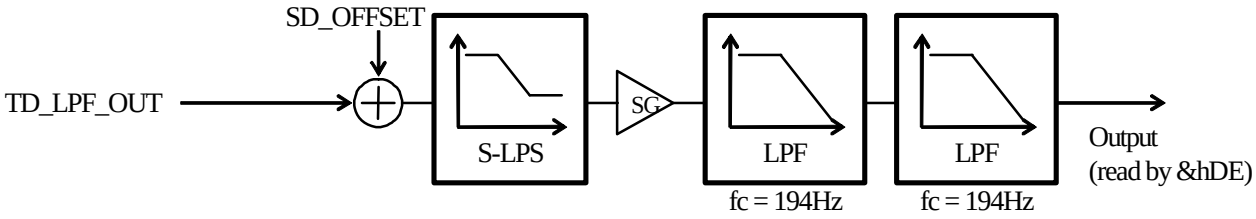


Figure 102. Block diagram rerating to SD offset measurement

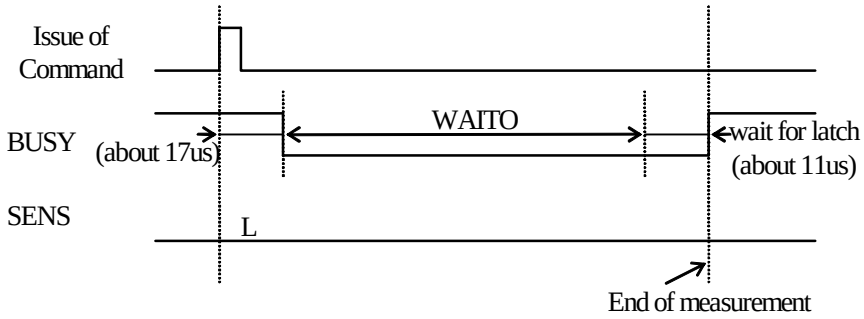


Figure 103. Timing chart relating to SD offset measurement

BUSY signal comes to L in about 17us after issue of the command and measurement is started. In the case of using digital sled filter, the input signal comes to LPF output signal of tracking filter and it passes through sled filter after offset added.After the signal passed sled filter, the output signal passes through primary LPF 2 stages. And LPF output is latched at the time point when WAITO time has passed. Thereafter, the BUSY signal comes to H, showing the measurement ended. Read the result using command &hDE.
SD_OFFSET is adjustable by the command &h91[7:0].
Further, SENS=L remains unchanged in measuring SD offset.

17.3.20.4. Measurement of tracking balance

(Method 1)
At command &hD4[1] is L, amplitude center of TE signal is measured by issue of command &hD09X. It is possible to cancel deviation from Vc by combining this function with the tracking balance adjust function.

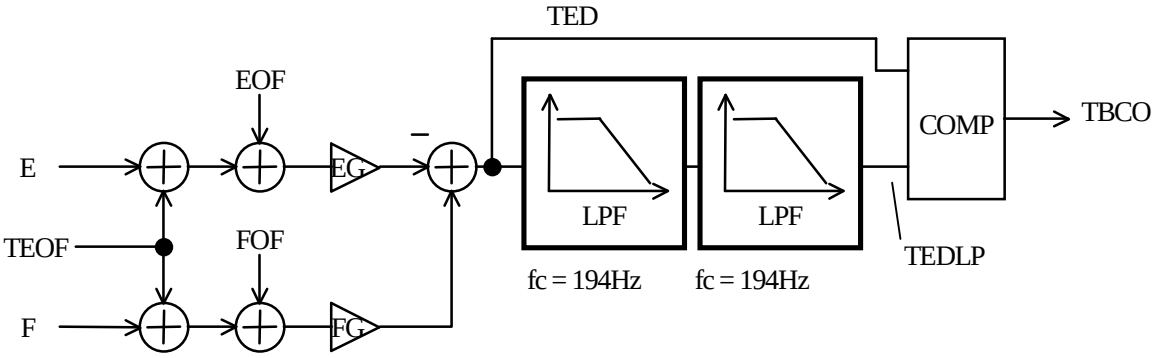


Figure 104. Tracking balance measuring block diagram (Method 1)

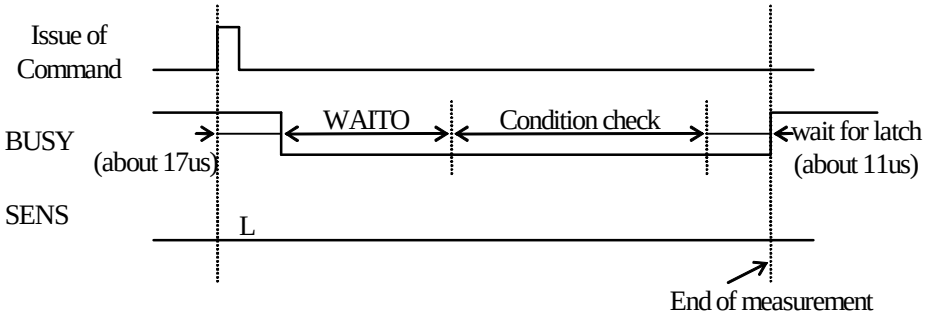


Figure 105. Tracking balance measuring timing chart (Method 1)

BUSY signal comes to L in about 17us after issue of the command, and measurement is started. At this time offset is added to each of E and F signals from ADC output, and by subtract these signals, TE signal is generated. Original signal (TED) is compared with TEDLP signal through LPF and consequently TBCO signal is ready for output. When measuring tracking balance, turn OFF tracking servo loop by command &hC1[5:4]=0. And according to cases, use sled move in combination with this function.
First of all this function is put in wait condition for WAITO time until E and F signals stabilizes, and thereafter discrimination of the preconditions for Measurement OK is started. The measurement is judged as OK when TBCO has continued by TBN cycles within the cycle range of TBMIN to TBMAX. Upon judgement of measurement OK, TEDLP value at that time is latched as the result. Thereafter, BUSY signal comes to H, showing completion of the measurement. Read the measured result using command &hDE. At this time, if SENS=L, it shows that the measurement was made correctly. If SENS=H, it shows that NG condition has took place during measurement, that is, showing that either FOK came to L (FOK=L) during measurement or measurement OK conditions failed to be met for 65ms (Time-out). In the case of SENS=L, read the result by command &hDE.
Set up WAITO by command &hD2[7:4], TBMIN by command &hD3[7:4], TBMAX by command &hD3[3:0], and TBN by command &hD4[7:4].

(Method 2)
At commancd &hD4[1] is H, MAX/MIN values of TE signal are measured by issue of command &hD09X. By this method, with adjustment the balance of upper and lower sides of tracking error signal, it is also possible to cancel deviation from Vc by combining this function with the tracking balance adjust function.

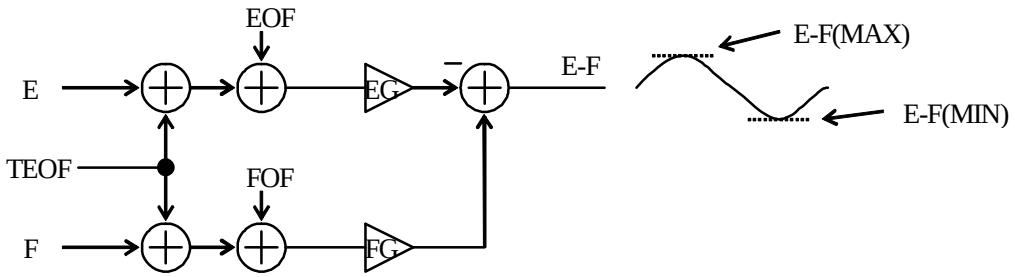


Figure 106. Tracking balance measuring block diagram (Method 2)

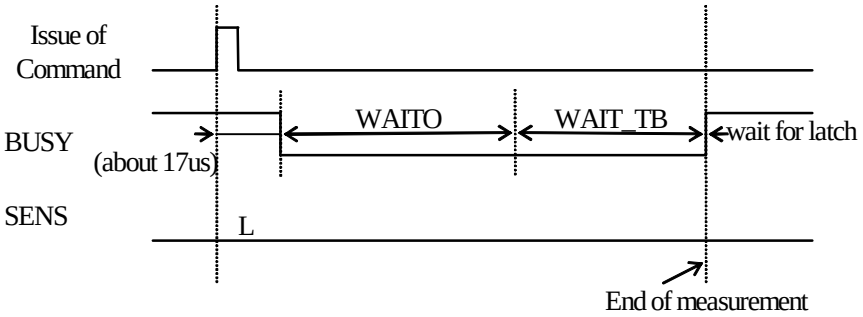


Figure 107. Tracking balance measuring timing chart (Method 2)

BUSY signal comes to L in about 17us after issue of the command, and measurement is started. At this time offset is added to each of E and F signals from ADC output, and by these signals, E-F signal is generated. The reading signal is selectable by command &hD5[1:0], MAX or MIN value of E-F signal can be selected. When measuring tracking balance, turn OFF tracking servo loop by command &hC1[5:4]=0.
First of all this function is put in wait condition for WAITO time until E and F signals stabilizes, and thereafter MAX and MIN values are measured during WAIT_TB time. These values at that time are latched as the result.Thereafter, BUSY signal comes to H, showing completion of the measurement. Read the measured result using command &hDE. At this time, if SENS=L, it shows that the measurement was made correctly. If SENS=H, it shows that NG condition has took place during measurement. NG condition is that FOK came to L (FOK=L) during measurement. In the case of SENS=L, read the result by command &hDE.
Set up WAITO by command &hD2[7:4], and WAIT_TB by command &hD2[3:0].

17.3.20.5. Measurement of focus balance

(Method 1)
At command &hD4[1] is L, RFRP deviation from its maximum amplitude point is measured by issue of command &hD08X. It is possible to get RF amplitude maximum point by combining this function with the focus balance adjusts function.

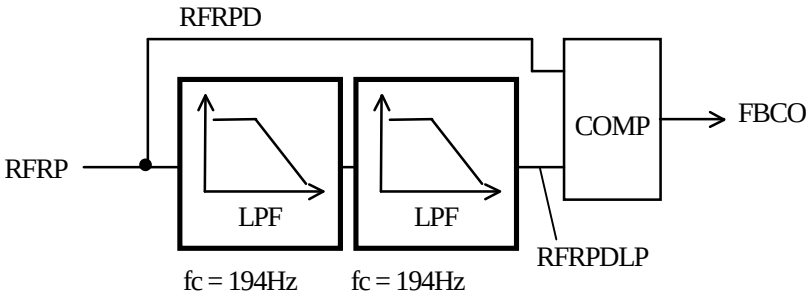


Figure 108. Focus balance measuring block diagram (Method 1)

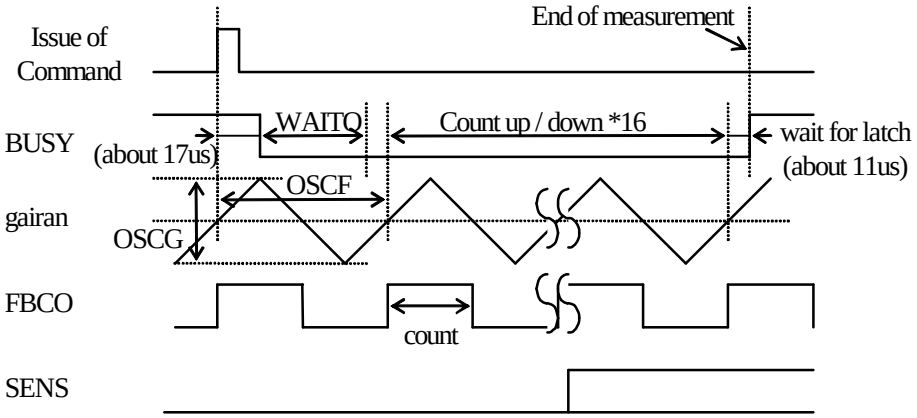


Figure 109. Focus balance measuring timing chart (Method 1)

BUSY signal comes to L in about 17us after issue of the command and at the same time measuring is started. At this time, original signal (RFRPD) is compared with RFRPDLP signal having passed through LPF and consequently FBCO is ready for output. On the other hand, Fo servo loop keeps as ON, but disturbance signal is as added automatically. It is possible to set up the height of this disturbance by command &hED[5:0] and frequency thereof by command &hED[7:6] respectively.
At first, this measurement function waits for WAITO time until RFRP stabilizes. Thereafter, this function starts measuring with initial rise of the disturbance signal. This measurement is effected by the counter operation. When disturbance is in positive section, the section of FBCO=H is counted up. Also, the section of FBCO=H is counted down when disturbance is in the negative section.
The measurement ends when such counter operation was repeated 16 times and the mean value of counter values is latched as the measured result.
Thereafter, BUSY signal comes to H, showing that the measurement ended. At this time, if SENS=L, it shows that the measurement was made correctly. If SENS=H, it shows that setup NG condition took place during measurement. As measurement NG condition, any one of LOCK=L or GFS88=L or nothing can be selected by command &hD4[3:2]. In the case of SENS=L, read the result by command &hDE.

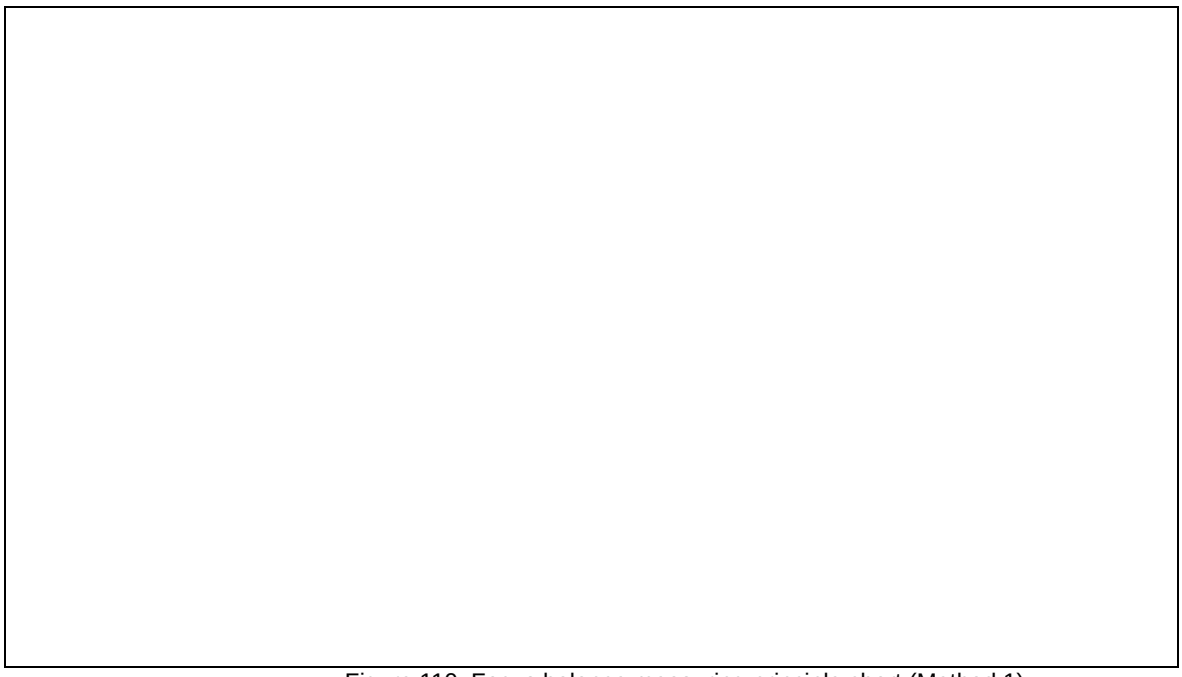


Figure 110. Focus balance measuring principle chart (Method 1)

When disturbance signal is added to FDOUT, RFRP response differs depending on which is the focal point of the focus, of a to e points. Herein, RFRP response characteristic is shown in graphs assuming the case of “no phase deviation”. As seen from the above graph, RFRP phase against disturbance in the case of focal point-a is reverse to that in the case of focal point-e.
This focus balance measuring function uses FBCO which is the comparative data of RFRP LPF component (=mean value) and RFRP. Hence, as prescribed it is possible to discriminate deviation direction of the focal point by comparing the time of FBCO=H under positive disturbance with the time of FBCO=H under negative disturbance.

The disturbance frequency is set to several hundred Hz because the focus sounds at high dB if the frequency comes to nearly 1kHz.

(Method 2)
At command &hD4[1] is H, MAX/MIN values of S-shaped curve at focus search are measured by issue of command &hD08X. By this method, it is excuted to adjustment the blance of upper and lower sides of S-shaped curve by combining with the focus balance adjust function.

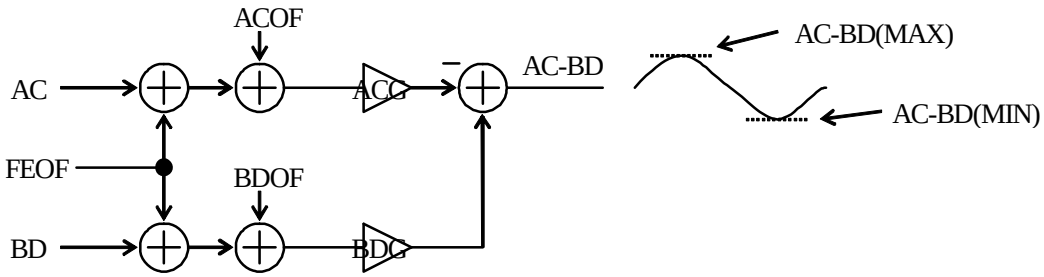


Figure 111. Focus balance measuring block diagram (Method 2)

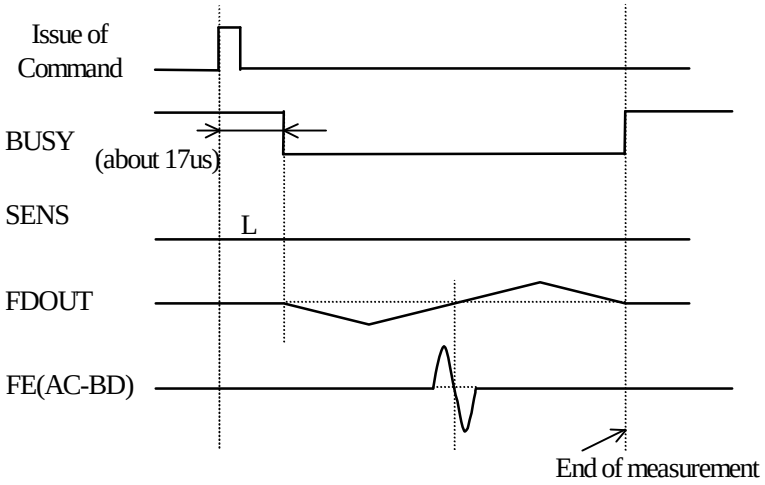


Figure 112. Focus balance measuring timing chart (Method 2)

BUSY signal comes to L in about 17us after issue of the command, and measurement is started. At this time offset is added to each of AC and BD signals from ADC output, and by these signals, AC-BD signal is generated. The reading signal is selectable by command &hD5[1:0], MAX or MIN value of AC-BD signal can be selected.
After measurement started, focus search is executed and in the meantime, MAX/MIN values of AC-BD signal are measured. Thereafter, BUSY signal comes to H, showing completion of the measurement. Read the measured result using command &hDE.
Further, SENS=L remains unchanged in measuring FD/TD offset.

17.3.20.6. Measurement of tracking gain and focus gain

This measuring function is effected by issue of either &hD0AX or &hD0BX, intended to measure phase difference between disturbance signal applied to the servo loop and TEIN/FEIN signal. Optimum gain can be set up by adjusting both of tracking gain and focus gain based on the measured result.

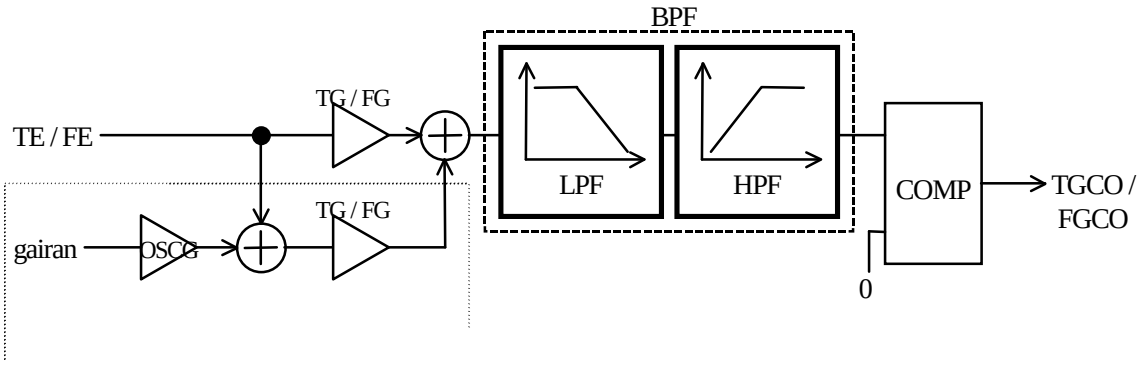


Figure 113. Tracking gain/focus gain measuring block diagram

The block enclosed with dotted line covers the internal portions of Tr servo filter /Fo servo filter.

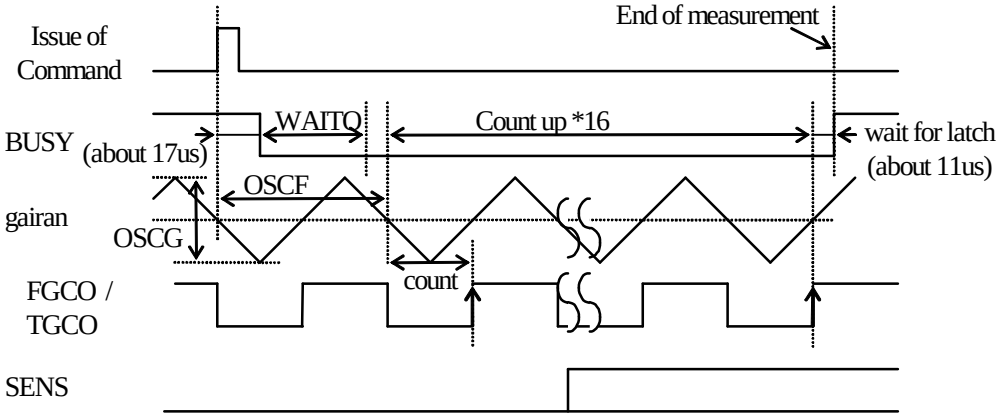


Figure 114. Tracking gain/focus gain measuring timing chart

BUSY signal comes to L in about 17us after issue of the command and at the same time measuring is started. At this time, the servo loop keeps ON, but disturbance signal is as added automatically. In addition, the signal having passed through BPF is compared with 0 and TGCO/FGCO is ready for output, as illustrated above. It is possible to set up the height of this disturbance by command &hED[5:0] and frequency thereof by command &hED[7:6] respectively. Furthermore, at this time the center frequency of BPF is changed according to the setup disturbance frequency.
At first, this measurement function waits for WAITO time until TE/FE stabilizes. Thereafter, this function starts measuring with initial downcome of the disturbance signal. This measurement is effected by the counter operation. The counter counts up for the time from change-over point from positive disturbance to negative disturbance until rise of TGCO/FGCO. The measurement ends when this cyclic operation is repeated 16 times and the mean value of the counter counted values is latched as the measured result.
Thereafter, BUSY signal comes to H, showing that the measurement ended. At this time, if SENS=L, it shows that the measurement was made correctly. If SENS=H, it shows that setup NG condition took place during measurement. As measurement NG condition, any of LOCK=L or GFS88=L or nothing can be selected by command &hD4[3:2]. In the case of SENS=L, read the result by command &hDE.

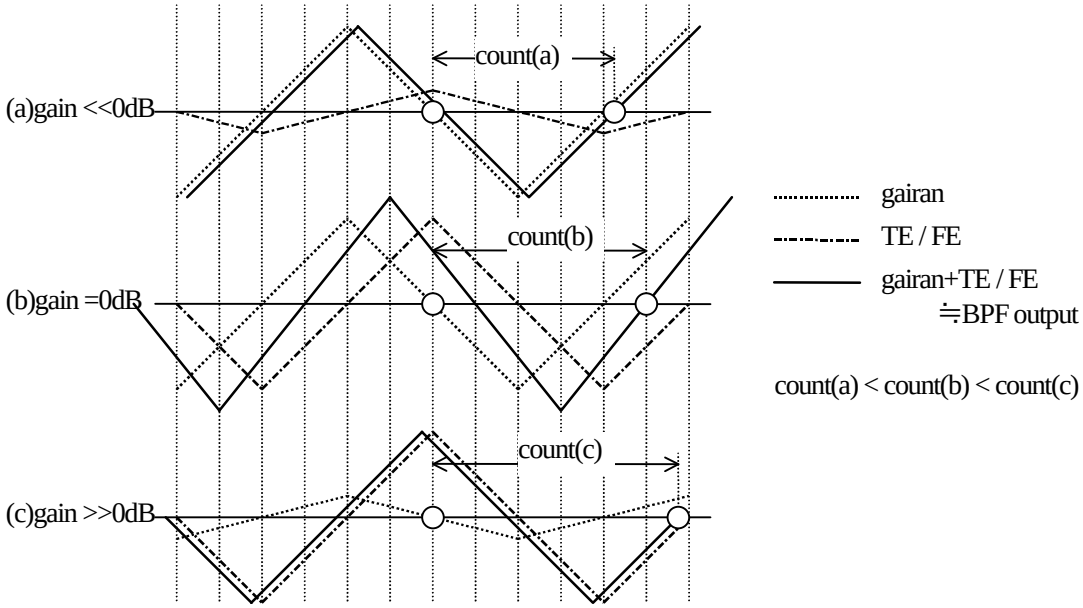


Figure 115. Tracking gain/focus gain measuring principle chart

The object of gain adjustment is to align the servo loop gain under 1kHz to 0dB.
In the above chart, disturbance is represented by dotted line, TE/FE represented by broken line, and BPF input signal represented by solid line. The peak frequency of BPF can be aligned to disturbance and, therefore, BPF output could be considered to be nearly same as BPF input.
Comparing the case of higher gain (than 0dB) with the case of lower gain (than 0dB), the result is as shown in the above chart. However, in (c) graph the vertical axis is compressed to express disturbance level so it gets smaller.
The counter counts from zero-cross point of disturbance downcome until zero-cross point of BPF output rise. Comparing this cycle count time, the result is as follows; count(a) <count(b)<count(c).
The gain measuring function uses this principle.

17.3.20.7. About RF amplitude measurement and the adjustment

Peak and bottom value of the amplitude of RF (EQO) signal are measured by excute out command &hD0CX. DC level and amplitude of RF signal can be adjusted by combining it with RF offset adjustment command &h9C0X and RF gain adjustment command &h9DXX. And, it can get the most suitable RF signal from the viewpoint of DC by combining it with FOK comparate level adjustment command &hAA[3:0]. (For the detail, refer to RF signal generator)

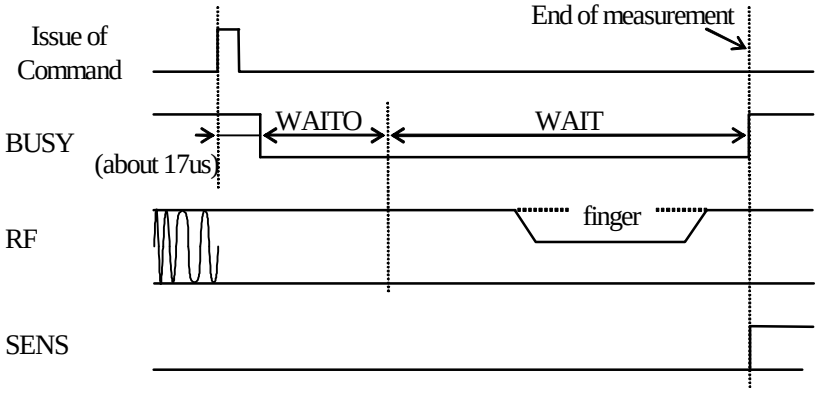


Figure 116. RF amplitude measuring timing chart

BUSY signal comes to L in about 17us after issue of the command, and measurement is started. The reading signal is selectable by command &hD5[1:0], MAX and MIN value can be selected.
First of all this function is put in wait condition for WAITO time until RF offset signal stabilizes, and thereafter MAX and MIN values are measured during WAIT time. These values measured at that time are latched as the result. Thereafter; BUSY signal comes to H, showing completion of the measurement. Read the measured result using command &hDE. At this time, if SENS=L, it shows that the measurement was made correctly. If SENS=H, it shows that NG condition has took place during measurement, that is, showing that either measurement NG conditions selected by command &hD4[3:2] are met or FOK came to L during measurement. In the case of SENS=L, read the result by command &hDE.
Set up WAITO by command &hD2[7:4], and WAIT command &hD2[3:0] with full time to pass through the finger and etc..
And, the case of measuring RF signal before focus servo turned ON, make command &hD4[1] to H.

17.3.20.8. Measurement of VCO

Frequency of VCO output signal is measured by issued command &hD0EX. At this time, VCO input voltage is selectable and it is possible to measure the frequency of VCO output signal at each case. By combining this result with the VCO offset/gain adjustment function, optimum offset/gain can be set up.

Figure 117. VCO measuring block diagram

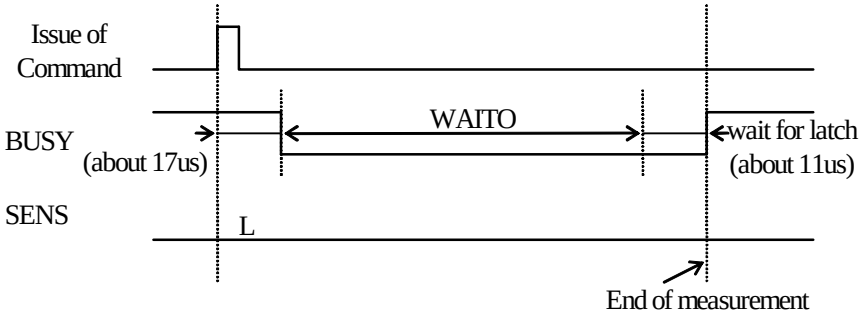


Figure 118. VCO measuring timing chart

BUSY signal comes to L in about 17us after issue of the command and at the same time measuring is started.
At command &h8A[6] is H, VCO input voltage can be set up by changing command &h8BXX. The frequency of VCO output is measured by a counter after divided and the frequency is latchd as the result. Thereafter, BUSY signal comes to H, showing that the measurement ended. So read the result by command &hDE.
WAITO time is a wait time set up by command &hD2[7:4] for VCO output is stabilized and the count value is latched. The division ratio of VCO output signal is possible to change by command &h50[7:6]. And when measuring, set up PLL measuring mode as for VCO measuring by command &h82[5:4]=h3.
Further, SENS=L remains unchanged in measuring VCO.

17.3.20.9. The case of sending continuously automatic adjustment and measurement commands

It is prohibited to send continuously different commands for automatic adjustment and measurement while one automatic adjustment and measurement command is ON. In such a case, send &hD00X without fail at once, and thereafter start new measurement.
On the other hand, where same measurement is repeated, wait time for each measurement is omitted and, hence, quick remeasurement is available.

17.3.21. Detection of defect disc and Countermeasures

On occasion flaw exists on disc to be reproduced. It is not allowed that the performance of each servo is disordered by disc flaw. To avoid such a phenomenon, disc surface must be detected and appropriate countermeasure be undertaken against it. Mainly 4 different flaws defined hereunder could exist on disc for evaluation of playability. Actual disc flaw may be considered to be a composite of these 4 different flaws.

17.3.21.1. Black Dot

This is a dot which is printed in ink on the read surface of disc, simulated from foreign matter adhered to disc and resin black dot in disc. Reflection light from disc is quite eliminated at black point.
DEFECT signal generated by RF is used for detection of such black dot. This signal is a signal which comes to H when eye level is low.
In the case of DEFECT=H, countermeasure for the focus and that for tacking are set up using command &hD6[7:6] and &hD6[3:2] respectively and each of them can be selected from three systems of NO COUNTERMEASURE, HOLD, and GAIN DOWN.

17.3.21.2. Interruption

This is a disc flaw which was simulated from pit interruption on flawed aluminum deposition surface. At this interruption spot, brightness-darkness difference in reflection light from disc depending on pitted surface is perfectly eliminated and, as a result, EYE signal comes to H. Hence, the prescribed DEFECT signal is kept as L (not detected).
NEW_DEFECT signal is used for detection of this disc interruption.
In the case of NEW_DEFECT=H, countermeasure for the focus and that for tracking are set up using command &hD6[5:4] and &hD6[1:0] respectively and each of them can be selected from three systems of NO COUNTERMEASURE, HOLD, and GAIN DOWN.

17.3.21.3. Fingerprint

Fingerprint means a fingerprint-like pattern, which was printed on disc read surface.
Such a disc flaw is not detected and also no countermeasure is taken for it.

17.3.21.4. Scratch

This scratch means a frictional flaw on disc read surface. Some of frictional flaws is called Red Band, which is flaw simulated from scratch.
In the case of this disc flaw, it is not specially detected and no special countermeasure is taken for it, but DEFECT and NEW_DEFECT could be detected though depending on amplitude level of RF.

17.3.21.5. PLL action in passing through flawed spot of disc

When DEFECT and NEW_DEFECT are H, the PLL circuit performs HOLD operation and prevents the frequency of PLCK deviating at the time of passing through flawed spot of a disk

17.3.22. Pre-Servo AMP

17.3.22.1. RF signal generator

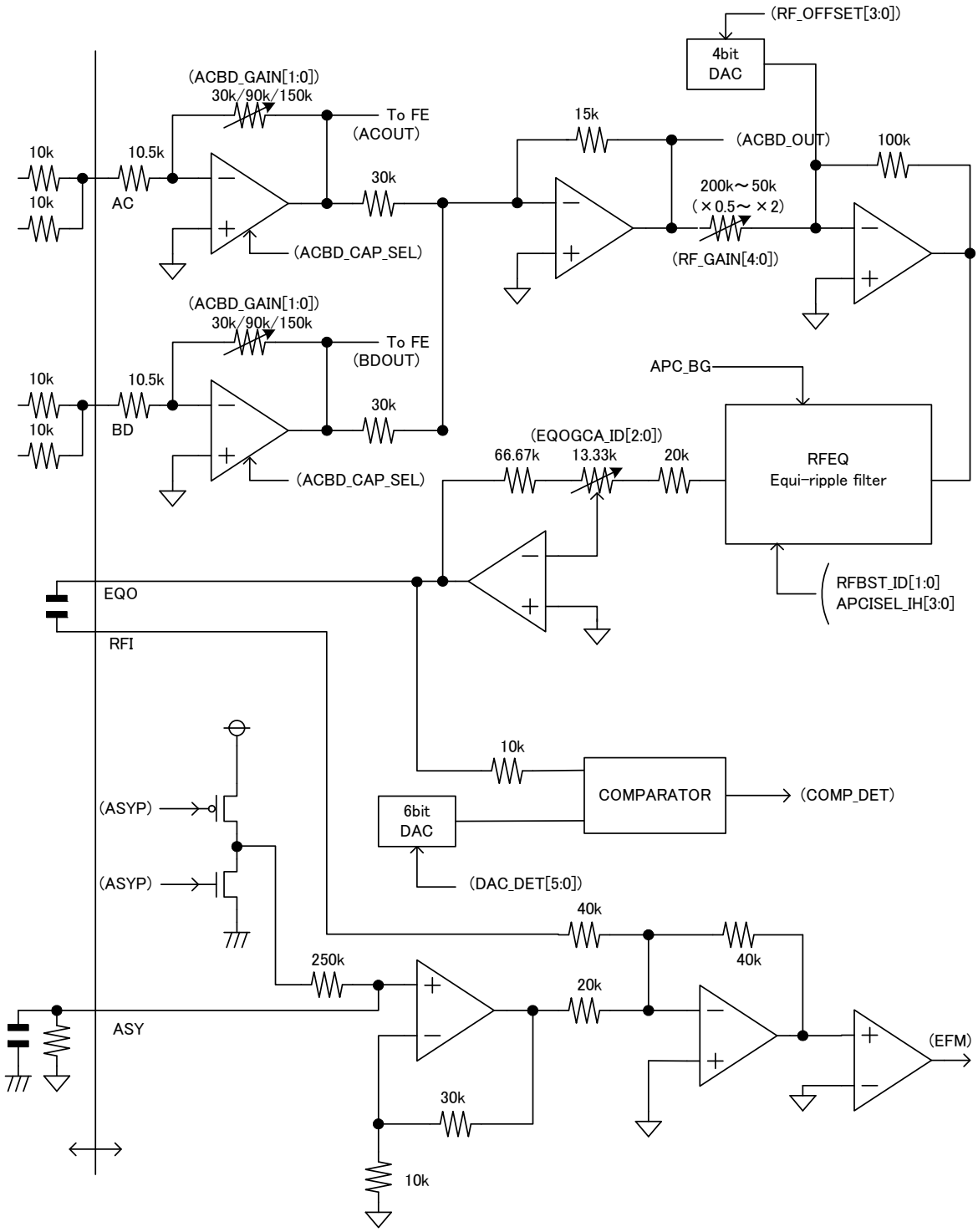


Figure 119. RF signal generator

This RF signal generator gets A+B+C+D from signals sent from the pickup and finally generates asymmetrically-corrected EFM signals.
Where reproduced disc is CD-R/W, the gain can be increased by +9.5dB or +14dB by setting CDRW_SEL to “1h” or “2h” as shown in table 17.3.22.1.0. respectively.
ACBD_CAP is capacitor for phase compensation. It is possible to set up as shown in Table 17.3.22.1.2
Asymmetrically-corrected EFM signal is output from EFM. ASY terminal is provided with a capacitor to get asymmetrically-corrected comparator slice level signal.
The equalizer (RFEQ) is structured with equi-ripple filter. Group delay is constant independ to boost level. The equalizer set as shown in Tables Table 17.3.22.1 **エラー! 参照元が見つかりません。**.3 – Table 17.3.22.1.5
The shift amount of base level of RF output (EQO) can be set at 16 steps by RF_OFFSET[3:0].(Table 17.3.22.1.6)
RF gain can be set at ±6dB by RF_GAIN[4:0].Please set the command to make EQO output voltage between 1.0Vp-p and 1.2Vp-p when EQOGCA_ID=4h.(Table17.3.22.1.1)
By being set as PWROFF_IH=“1”, the POWER DOWN mode to minimize consumption current is selected.

CDRW_SEL[1:0]	AC/BD Gain	E/F Gain
0h	0dB	0.0dB
1h	9.5dB	9.5dB
2h	14.0dB	9.5dB

Table17.3.22.1.0. CDRW_SEL setting values by command &h61[5:4]

Gain (dB)
G=20log[100/{(31-&h9D[4:0])×5+50}]

RF_GAIN[4:0]	RF Gain
01h	-6.0dB
15h	0.0dB
1Fh	6.0dB

Table17.3.22.1.1. RF_GAIN setting values by command &h9D[4:0]

ACBD_CAP_SEL	ACBD_CAP
0h	0.25 pF
1h	0.125 pF

Table17.3.22.1.2. ACBD_CAPA_SEL setting values by command &h60[1]

h62[5:4]	APCISEL_IH[3:0]	f_0	Speed
0h	1h	0.72MHz	x1
1h	2h	1.45MHz	x2
2h	4h	2.90MHz	x3 to x4
3h	8h	---	through

Table17.3.22.1.3. RF_CAPA_SEL setting values by command &h62[5:4]

h62[3:2]	EQOGCA_ID[2:0]	RFEQ total gain
0h	1h	6dB
1h	2h	9dB
2h	4h	12dB
3h	8h	---

Table 17.3.22.1.4. EQOGCA_ID setting values by command &h62[3:2]

RFBST_ID [1:0]	Boost	RFBST_ID [1:0]	Boost
0h	2dB	2h	6dB
1h	4dB	3h	8dB

Table 17.3.22.1.5. RFBST_ID setting values by command &h62[1:0]

RF_OFFSET [3:0]	EQO Basic level	RF_OFFSET [3:0]	EQO Basic level	RF_OFFSET [3:0]	EQO Basic level	RF_OFFSET [3:0]	EQO Basic level
00h	VC-2.00V	04h	VC-1.20	08h	VC-0.40V	0Ch	VC+0.40V
01h	VC-1.80V	05h	VC-1.00V	09h	VC-0.20V	0Dh	VC+0.60V
02h	VC-1.60V	06h	VC-0.80V	0Ah	VC	0Eh	VC+0.80V
03h	VC-1.40V	07h	VC-0.60V	0Bh	VC+0.20V	0Fh	VC+1.00V

Table 17.3.22.1.6. RF_OFFSET setting values by command not(&h9C[3:0])

17.3.22.2. FE/TE signal generator

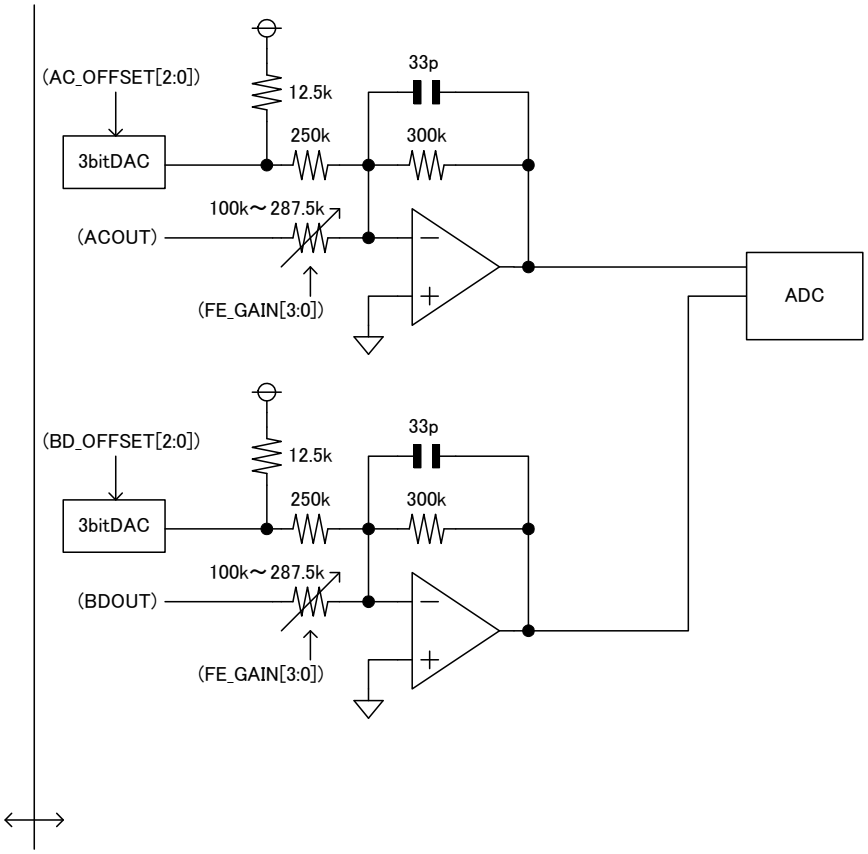


Figure 120. FE signal generator

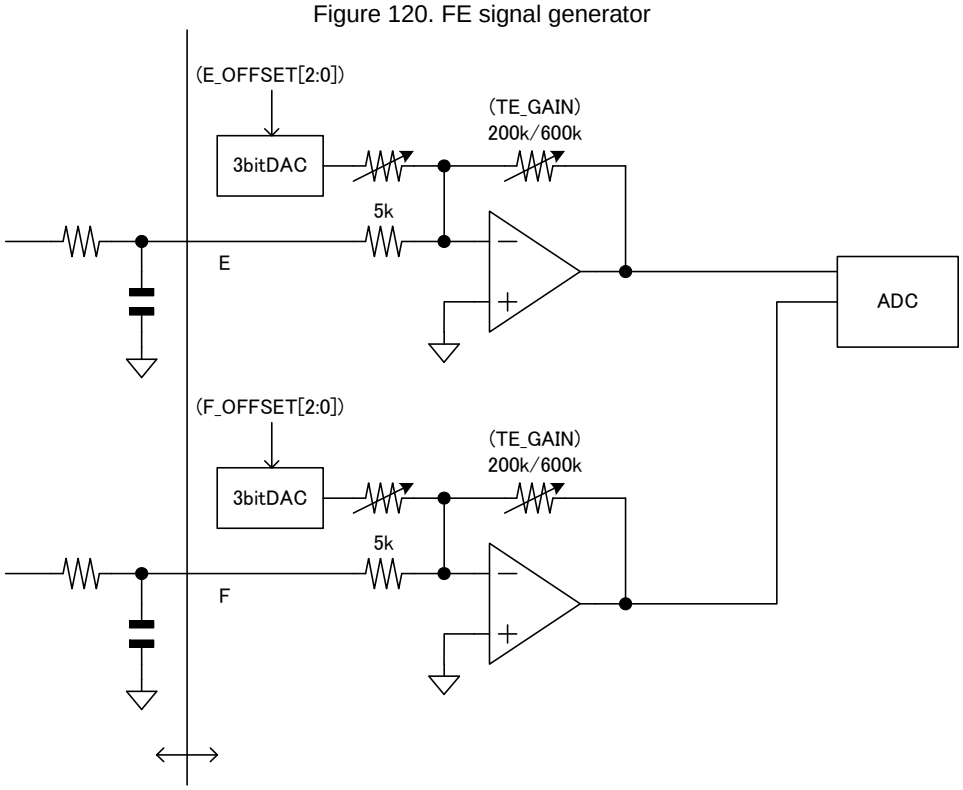


Figure 121. TE signal generator

At FE signal generator, it gets A+C, B+D signals being sent from the pickup and generates focus error signals A+B, B+D. At TE signal generator, it gets E, F signals being sent from the pickup and generates tracking error signals E, F. Thereafter, the focus signals and tracking signals are sent to ADC and after ADC, (A+C)-(B+D) signal and E-F signal are generated at digital block.
Be concerned about each of input A+C, B+D, E, F, offset adjustment can be made individually by setting AC_OFFSET, BD_OFFSET, E_OFFSET, F_OFFSET as shown in Table 17.3.22.2.0 and Table 17.3.22.2.1.
Where reproduced disc is CD-R/W, the FE gain can be increased by +9.5dB or +14dB and TE gain can be increased by +9.5dB by setting CDRW_SEL to “1h” or “2h” as shown in Table 17.3.22.2 **エラー! 参照元が見つかりません。**.0 respectively.
Moreover, by connecting resistances and capacitors to AC_GAIN terminal and BD_GAIN terminal of FE signal generator and to E, F input terminals of TE signal generator, adjustment of gain and cut-off frequency can be carried out by these constants.
TE signal generator can be change gain by setting FE_GAIN[3:0] as shown in Table 17.3.22.2.2
By being set as PWROFF_IH=“1”, the POWER DOWN mode to minimize consumption current is selected.

AC_OFFSET[2:0] BD_OFFSET[2:0]	DC Level	AC_OFFSET[2:0] BD_OFFSET[2:0]	DC Level
0h	Vc	4h	Vc-0.88V
1h	Vc-0.22V	5h	Vc-1.10V
2h	Vc-0.44V	6h	Vc-1.32V
3h	Vc-0.66V	7h	Vc-1.54V

Table 17.3.22.2.0. AC_OFFSET and BD_OFFSET setup values by command &h64[2:0], &h65[2:0] (Vcc=3.0V)

E_OFFSET[2:0] F_OFFSET[2:0]	DC Level	E_OFFSET[2:0] F_OFFSET[2:0]	DC Level
0h	Vc+1.54	4h	Vc+0.66V
1h	Vc+1.32V	5h	Vc+0.44V
2h	Vc+1.10V	6h	Vc+0.22V
3h	Vc+0.88V	7h	Vc

Table 17.3.22.2.1. E_OFFSET and F_OFFSET setup values by command &h66[2:0], &h67[2:0] (Vcc=3.0V)

FE_GAIN [3:0]	FE Gain[dB]	FE_GAIN [3:0]	FE Gain[dB]	FE_GAIN [3:0]	FE Gain[dB]	FE_GAIN [3:0]	FE Gain[dB]
00h	0.37	04h	2.03	08h	4.08	0Ch	6.77
01h	0.75	05h	2.50	09h	4.68	0Dh	7.60
02h	1.16	06h	3.00	0Ah	5.32	0Eh	8.32
03h	1.58	07h	3.50	0Bh	6.00	0Fh	9.54

Table 17.3.22.2.2. FE_GAIN setup values by command &h68[3:0] (Vcc=3.0V)

APC circuit

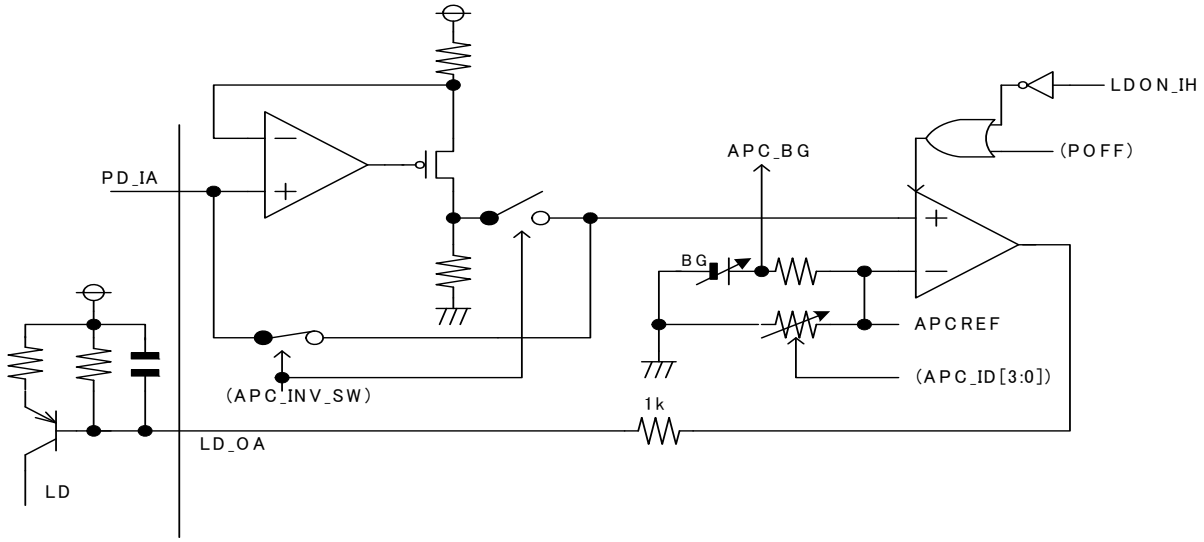


Figure 122. APC circuit

Laser power is automatically controlled by feeding back the detected power with signal from photo detector. By setting command &h60[4] to H, laser can be turned ON by setting LDON_IH to “1”. The reference level can be set by APC_ID[3:0] and Table 25.3.0 is showing the setup values.
By setting APC_INV_SW(command &h60[0]) to H, it invert Basic level(VCC level).
POWER DOWN mode to minimize consumption current is selected by setting PWROFF_IH to “H”.

APC_ID [3:0]	Level	APC_ID [3:0]	Level	APC_ID [3:0]	Level	APC_ID [3:0]	Level
0h	145mV	4h	165mV	8h	185mV	Ch	205mV
1h	150mV	5h	170mV	9h	190mV	Dh	210mV
2h	155mV	6h	175mV	Ah	195mV	Eh	215mV
3h	160mv	7h	180mV	Bh	200mV	Fh	220mV

Table 17.3.22.2.3. APC_ID setup value by command &h61[3:0]

17.3.22.3. DET circuit

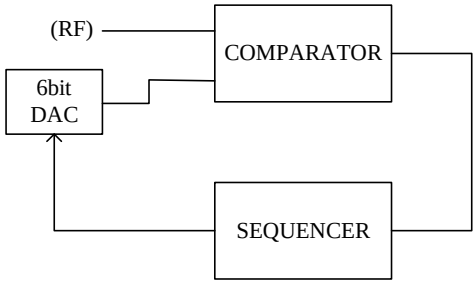


Figure 123. DET circuit

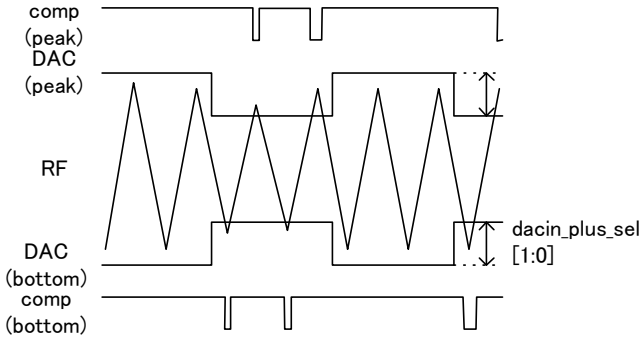
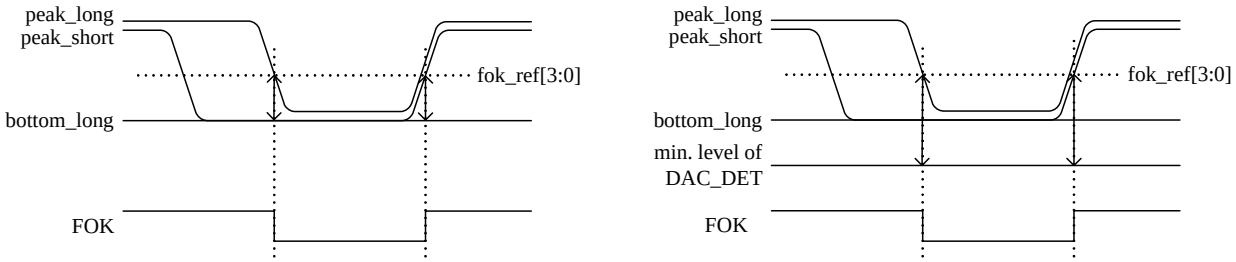


Figure 124. DET circuit operation principle

This detection circuit is to detect peak and bottom points of RF signal and by each long signal and short signal of those, FOK signal, mirror signal, defect signal and RF ripple signal are generated.
Detection of peak and bottom points is executed by referring to the comparison result of RF signal and 6bitDAC output voltage. Thereafter, the result is sent to sequencer and next input pattern to DAC is decided. The input pattern to DAC obtained by these ways becomes peak and bottom signals. Which between peak and bottom is detected, and which signal between a long signal and a short signal is detected are changed by sequence. Also the width of increase and decrease of DAC output value can be set by dacin_plus_sel[1:0] (command &hA8[5:4])
POWER DOWN mode to minimize consumption current is selected by setting PWROFF_IH to “1”.

17.3.22.3.1. FOK signal generator



Command &hAA[4]=H (amplitude judgement) Command &hAA[4]=L (peak_long level judgement)

Figure 125. FOK circuit operation principle

Generation of FOK signal is executed using peak_long signal, peak_short signal and bottom_long signal.
When focus is failed, peal_long signal increases. Then if peak_long signal becomes smaller than fok_ref[3:0] level, FOK signal turnes to L.
And when focus is recovered, peak_short signal becomes larger, and when peak_short signal becomes larger than fok_ref[3:0] level, FOK turns to H.
The base level used for judgement of the size of peak signal is selectable by command &hAA[4]. In the case of command &hAA[4]=H, the base level is bottom_long signal and FOK is judged by the amplitude of peak signal and bottom signal. In the case of command &hAA[4]=L, the base level is Min. level of DAC in DET circuit and FOK is judged by the value of peak_long to that level.
Moreover, the value of fok_ref[3:0] is possible to set by command &hAA[3:0].

17.3.22.3.2. DEFECT signal generator

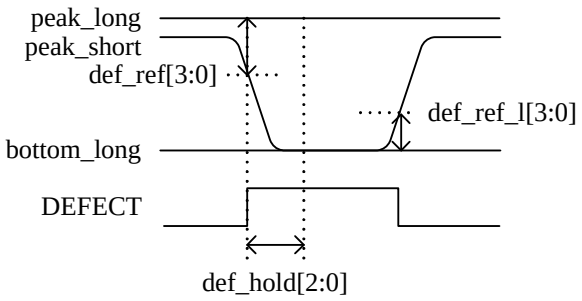


Figure 126. DEFECT circuit operation primciple

Generation of DEFECT signal is executed using peak_long signal, peak_short signal and bottom_long signal.
If flaws are in a disk, when passing through that, a peak short signal decreases. And if the difference between peak_long signal and peak_short signal comes to larger than def_ref[3:0] level, DEFECT signal turns to H. Then if peak_short signal does not recover while def_hold[2:0] time, DEFECT signal holds H as a flaw is detected.
Thereafter, when coming off from the flaw, peak_short signal recovers and increases. And the difference between peak_short signal and bottom_long signal becomes larger than def_ref_1[3:0] level, DEFECT signal turns to L.
It is possible to set def_ref[3:0] and def_ref_l[3:0] by commands &hA9[7:4] and &hA9[3:0] each other.
It is possible to set def_hold[2:0] by commands &hAB[2:0].

17.3.22.3.3. MIRROR signal generator

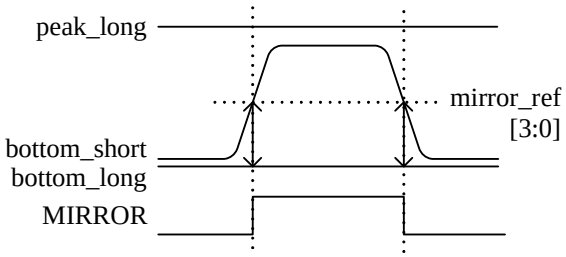


Figure 127. MIRROR circuit operation principle

Generation of MIRROR signal is excuted using peak_long signal, bottom_long signal and bottom_short signal.
When passing the mirror side, bottom_short signal increases because the reflection factor becomes higher at that section. Then when bottom_short signal exceeds the threshold level of mirror, MIRROR signal turns H as detected mirror side.
The threshold level of mirror is set by carrying out the multiplication of mirror_ref[3:0]/16 to the value which is the result of subtraction of a peak long signal and a bottom long signal. Mirror_ref[3:0] is set by command &hA8[3:0].

17.3.22.4. RFRP signal generator

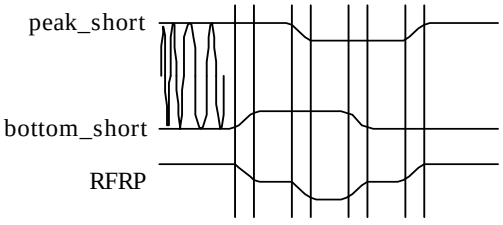


Figure 128. RFRP circuit operation principle

The RFRP signal is generated by subtraction of peak_short signal and bottom_short signal and used at focus Bias adjustment. For details, refer to the item of focus balance adjustment.

17.3.22.5. Bias voltage generation circuit

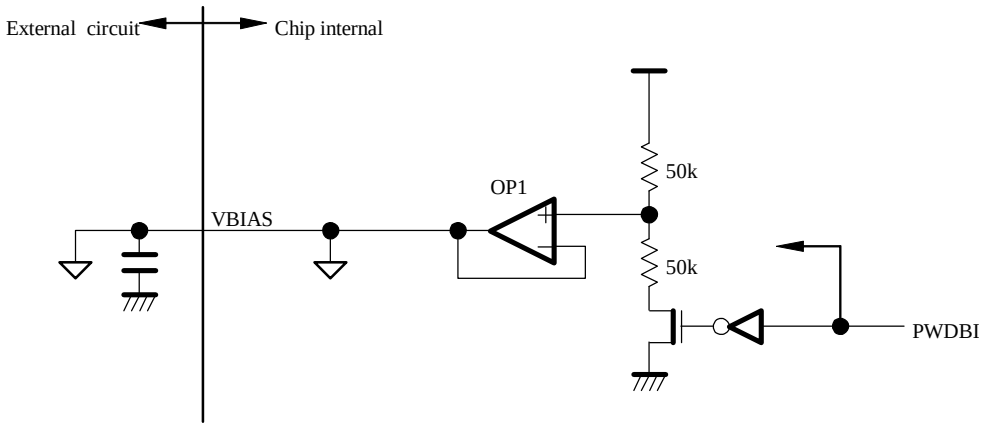


Figure 129. Bias voltage generation circuit

This circuit generates the bias voltage $V_{DD}/2$.
This block differs from other blocks, it becomes POWER DOWN mode to minimize consumption current by setting command &h40[6] PWDBI to“1”. For this, in case wanting to stabilize bias voltage level early when returning the power mode from POWER DOWN mode of command&h40[7] PWDRF= “1” to normal operation mode, or the case wanting to actuate other IC components which need bias voltage even under POWER DOWN mode, the bias voltage unit generates $V_{DD}/2$ by setting to PWDBI=“0”.

- Precautions

  Connect pass-control filter of about 10uF to VBIAS terminal without fail.

17.3.23. YFLAG generator

YFLAG is generated by comparision with counter value and threshold (h80).
This counter count up when counter enable signal is “H” and RFCK signal upcome is detect and C2FX signal is “H”, count down when counter enable signal is “H” and RFCK signal upcome is detect and C2FX signal is “L”.
The setting of this generator set up by command &h47[7:0].The upstep of This counter set up by command &h48[7:0]. The downstep of This counter set up by command &h49[7:0].

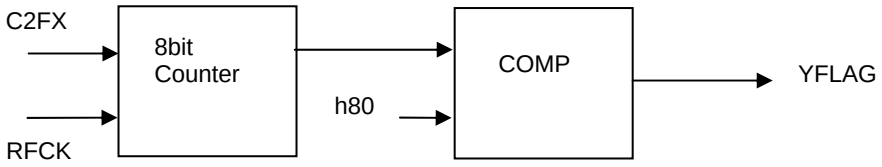


Figure 130. YFLAG generator block diagram

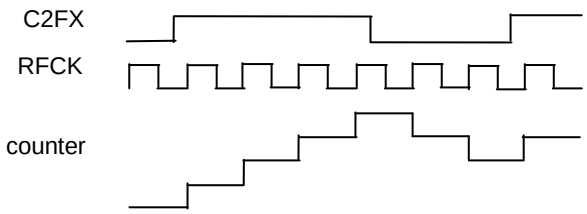


Figure 131. counter timing chart

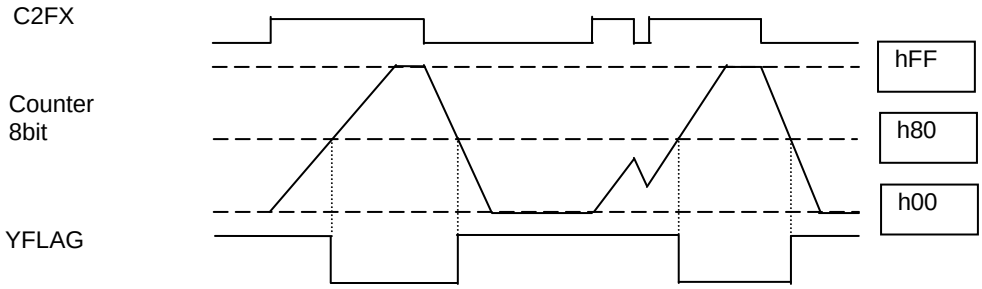
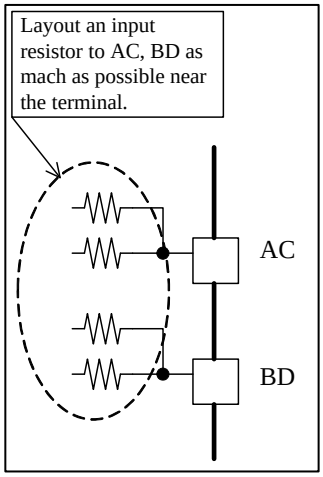
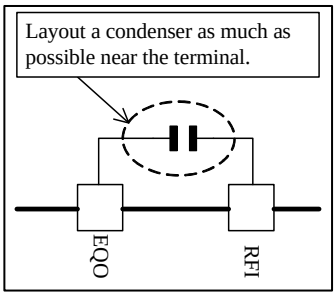


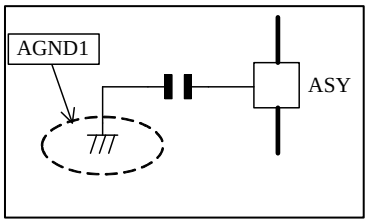
Figure 132. YFLAG timing chart

17.3.24. A precaution in PCB layout. (recommendation)

- Put on bypass condenser 0.1uF and about 10uF to 100uF in as close a position as possible between VDD which is a pair, and GND in the IC.
- Put on bypass condenser of about 10uF in the VBIAS terminal surely.
- Each VDD-GND of RF of the IC and DIGITAL surely separates, and does a ground one point from the supply cause of the power supply.
- Connect the parts with the outside connected with VDD and GND with VDD with the relations and GND.
- Show an attention point about pre-servo amplifier (RF) part and the AUDIO part in the bottom figure.







17.4. I/O Signals

Pin Name	I/O	Function	Destination
clk_i	In	APB BUS Clock	CLKCTR
rstb_i	In	Reset (Active Low)	RSTGEN
paddr_i	In	APB BUS Address	APB
penable_i	In	APB BUS Enable	APB
pwdata_i	In	APB BUS Write Data	APB
pwrite_i	In	APB BUS Write Enable	APB
psel_i	In	APB BUS Select	APB
prdata _o	Out	APB BUS Read Data	APB
AC	In	A + C Voltage Input	PAD
BD	In	B+D Voltage Input	PAD
VBIAS	Out	Bias Level	PAD
E	In	E Voltage Input	PAD
F	In	F Voltage Input	PAD
PD	In	APC Photo Detector Input	PAD
LD	Out	APC Laser Drive Output	PAD
ASY	Out	Asymmetric Correction	PAD
PCO	Out	PLL PCO Output	PAD
FCO	Out	PLL FCO-DAC Output	PAD
FDOUT	Out	Focus Drive Output	PAD
TDOUT	Out	Tracking Drive Output	PAD
SDOUT	Out	Sled Drive Output	PAD
CLVOUT	Out	CLV Drive Output	PAD
RFI	In	RF Output Capacitance Coupling Re-Input	PAD
EQO	Out	Output After RF Equalizer	PAD
AD_MONI0	Inout	Input & Monitor Signal Output	PAD
AD_MONI1	Inout	Input & Monitor Signal Output	PAD
ANA_MONI0	Inout	Input & Analog Monitor Output	PAD
ANA_MONI1	Inout	Input & Analog Monitor Output	PAD
cddsp_clk_i	In	CD-DSP Clock (16.9344 MHz)	CLKCTR
clr_i	In	CD-DSP Reset (Active High)	RSTGEN
lrck_o	Out	Signal used to switch between Lch and Rch for ECC data output	I2S_IN
bck_o	Out	Signal synchronized with data_o outputted from ECC	I2S_IN
data_o	Out	16-bit CD Data Outputted from ECC Block	I2S_IN
subsyq_o	Out	Subcode Block Sync Signal	I2S_IN
wfck_o	Out	Subcode Frame Sync Signal	I2S_IN
subck_i	In	Subcode Shift Clock Signal	I2S_IN
subdata_o	Out	Subcode Data Signal	I2S_IN
clk88_o	Out	Driver CLK and External Circuit CLK	PINCTR

17.5. Register

17.5.1. Memory Map

Name	Description	Address Offset	Width	Reset
cd-dsp_write_set	Set CD-DSP Write Command	0x00	16	16'h0000
cd-dsp_write_comp	Completion CD-DSP Write Command	0x04	32	32'h00000000
cd-dsp_read_set	Set CD-DSP Read Command	0x08	8	8'h00
cd-dsp_read_dat	Read Data CD-DSP Read Command	0x0C	32	32'h00000000
cd-dsp_status_set	Set CD-DSP Read Status 11 Byte	0x10	8	8'h00
cd-dsp_status_dat	Read Data CD-DSP Read Status	0x14	32	32'h00000000
cd-dsp_subq_set	Set CD-DSP Read Status and Subq	0x18	8	8'h00
cd-dsp_subq_dat0	Read Data CD-DSP Read Subq_0	0x1C	32	32'h00000000
cd-dsp_subq_dat1	Read Data CD-DSP Read subq_1	0x20	32	32'h00000000
cd-dsp_subq_dat2	Read Data CD-DSP Read subq_2	0x24	32	32'h00000000

For commands to CD-DSP, refer to "17.5.5 CD-DSP command".

17.5.2. Register Detail

Cd-dsp_write_set
Offset: 0x00
Width:16 bits

Bits	Name	Direction	Reset	Description
15:8	Write address	W	0x00	CD-DSP Write Address
7:0	Write data	W	0x00	CD-DSP Write Data

For commands to CD-DSP, refer to “17.5.5 CD-DSP command”.

Cd-dsp_write_comp
Offset: 0x04
Width:32 bits

Bits	Name	Direction	Reset	Description
31:17		R		0x00
16	Completion write	R	0x01	Command Write Completion Bit 0: Write not completed 1: Write completed
15:8	Wants to write address	R	0x00	CD-DSP Write Address
7:0	Wants to write data	R	0x00	CD-DSP Write Data

Cd-dsp_read_set
Offset: 0x08
Width: 8 bits

Bits	Name	Direction	Reset	Description
15:8	Read address	W	0x00	CD-DSP Read Address
7:0			0x00	

For commands to CD-DSP, refer to “17.5.5 CD-DSP command”.

Cd-dsp_read_dat
Offset: 0x0C
Width:32 bits

Bits	Name	Direction	Reset	Description
31:17		R		0x00
16	Completion read	R	0x01	Command Read Completion Bit 0: Data acquisition not completed 1: Data acquisition completed
15:8	Wants to read address	R	0x00	CD-DSP Read Address
7:0	Wants to read data	R	0x00	CD-DSP Read Data If data acquisition has not been completed, 0x00 is read.

Cd-dsp_status_set
Offset: 0x10
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:1			0x00	0x00
0	Read status	W	0x00	CD-DSP Read Status Execute only by write operation.

For CD-DSP statuses, refer to information in “17.5.3.Read CD-DSP status ”

Cd-dsp_ status _dat
Offset: 0x14
Width:32 bits

Bits	Name	Direction	Reset	Description
31			0x00	0x00
30	YFLAG	R	0x00	CD-DSP YFLAG Signal
29	SUBSYQ	R	0x00	CD-DSP SUBSYQ Signal
28	BUSY	R	0x00	CD-DSP BUSY Signal
27:25			0x00	
24	Completion status	R	0x01	Status Acquisition Completion Bit 0: Data acquisition not completed 1: Data acquisition completed
23:16	CD-DSP status	R	0x00	CD-DSP Status If data acquisition has not been completed, 0x00 is read.
15:0			0x00	

Cd-dsp_ subq _set
Offset: 0x18
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:1			0x00	0x00
0	Read status	W	0x00	When this bit is seto to “1”, read status and sub-Q from CD-DSP is executed. Execute only by write operation.

For CD-DSP statuses, refer to information in “17.5.3.Read CD-DSP status ”

Cd-dsp_ subq _dat0
Offset: 0x1C
Width:32 bits

Bits	Name	Direction	Reset	Description
31			0x00	0x00
30	YFLAG	R	0x00	CD-DSP YFLAG Signal
29	SUBSYQ	R	0x00	CD-DSP SUBSYQ Signal
28	BUSY	R	0x00	CD-DSP BUSY Signal
27:25			0x00	
24	Completion subq	R	0x01	Sub-Q Acquisition Completion Bit 0: Data acquisition not completed 1: Data acquisition completed
23:16	CD-DSP status	R	0x00	CD-DSP Status If data acquisition has not been completed, 0x00 is read.
15:8	Sub-Q 1	R	0x00	1st Byte of Sub-Q Data If data acquisition has not been completed, 0x00 is read.
7:0	Sub-Q 2	R	0x00	2nd Byte of Sub-Q Data If data acquisition has not been completed, 0x00 is read.

Cd-dsp_ subq _dat1
Offset: 0x20
Width:32 bits

Bits	Name	Direction	Reset	Description
31:24	Sub-Q 3	R	0x00	3rd Byte of Sub-Q Data If data acquisition has not been completed, 0x00 is read.
23:16	Sub-Q 4	R	0x00	4th Byte of Sub-Q Data If data acquisition has not been completed, 0x00 is read.
15:8	Sub-Q 5	R	0x00	5th Byte of Sub-Q Data If data acquisition has not been completed, 0x00 is read.
7:0	Sub-Q 6	R	0x00	6th Byte of Sub-Q Data If data acquisition has not been completed, 0x00 is read.

Cd-dsp_ subq _dat2
Offset: 0x24
Width:32 bits

Bits	Name	Direction	Reset	Description
31:24	Sub-Q 7	R	0x00	7th Byte of Sub-Q Data If data acquisition has not been completed, 0x00 is read.
23:16	Sub-Q 8	R	0x00	8th Byte of Sub-Q Data If data acquisition has not been completed, 0x00 is read.
15:8	Sub-Q 9	R	0x00	9th Byte of Sub-Q Data If data acquisition has not been completed, 0x00 is read.
7:0	Sub-Q 10	R	0x00	10th Byte of Sub-Q Data If data acquisition has not been completed, 0x00 is read.

17.5.3. CD-DSP Status

CD-DSP STATUS 8bit that it begins to be read by bit [23:16] of Cd-dsp_status_dat is shown in the following.

Bit	Name	Description
LSB	GFS	H if detected synchronously (11T, 11T, 2T)
1	FOK	H if focused perfectly
2	WQ	H if CRC check is OK
3	SENS	H if somewhat error is detected during measurement for auto adjustment
4	BUSY	L while measurening for auto adjustment and track jumping
5	F_LOOPON	H if focus loop closed
6	FSDOWN	H when search voltage is in the section of reduction in focus searching
MSB	FSFZC	H if FZC detected while focus search

17.5.4. Inside signal monitor output

43PIN ANA_MONI0
44PIN ANA_MONI1
47PIN AD_MONI0
48PIN AD_MONI1

The inout of the analog or digital inside signal of the CD-DSP block can be done more than upper 4 terminal.

Digital signal output switching

	Commnad	B0X0	B0X1	B0X2	B0X3
47	AD_MONI0	PCPI	WFCK	C2FX	C2FX
48	AD_MONI1	PCNI	RFCK	WQ	C1F2
43	ANA_MONI0	GFS	DISK_SYQ	SUBSYQ	C2F1
44	ANA_MONI1	RFCK	WQ	WFCK	C2F

	Commnad	B0X4	B0X5	B0X6	B0X7
47	AD_MONI0	LRCK(ECC)	-	FRAME[2]	SFPL
48	AD_MONI1	C2F	HOKAN_FLAG	FRAME[3]	FOK
43	ANA_MONI0	C2CLK	YFLAG	SLOW_FAST	BUSY
44	ANA_MONI1	HOKAN_FLAG	RFCK	SFPL	CLK3K

	Commnad	B0X8	B0X9	B0XA	B0XB
47	AD_MONI0	TJ_SIG	SCRTIMER	SENS	SFPL
48	AD_MONI1	BUSY	FOK	BUSY	FOK
43	ANA_MONI0	CLV_BUSY	COMP	DOUT	BUSY
44	ANA_MONI1	SCRTIMER	TGUON	SCRTIMER	SUBSYQ

	Commnad	B0XC	B0XD	B0XE	B0XF
47	AD_MONI0	SFPL	W_LATCH	C2FX	
48	AD_MONI1	FOK	C2FX	YFLAG	
43	ANA_MONI0	SLOW_FAST	STATUS_SEL	HOKAN_FLAG	
44	ANA_MONI1	MIRROR	EFM2	C2FX	

PCPI : PCPI is the signal to synchronize phases of the EFM signal and the PLCK signal. It makes PCO signal together with the PCNI signal. For the details, refer to the item of CLV and PLL.

PCNI : PCNI is the signal to synchronize phases of the EFM signal and the PLCK signal. It makes PCO signal together with the PCPI signal. For the details, refer to the item of CLV and PLL.

GFS : GFS is the signal to monitor whether the synchronizing signal of DISC was detected correctly. It turns to H if the synchronizing signal and 588 count of PLCK are in agreement. For the details, refer to the item of Window.

RFCK : RFCK is the frame clock generated on the basis of XIN. For the details, refer to the item of Window.

WFCK : WFCK is the frame clock generated on the basis of the EFM signal. For the details, refer to the item of Window.

DISC_SYQ : DISC_SYQ is the signal which turns to H when the synchronizing signal of DISC was detected.

WQ : WQ is the signal which turns to H when CRC check is OK. For the details, refer to the item of Reading Internal Status and Sub-Q Code.

C2FX : C2FX is the signal which turns to H when C2 series cannot be corrected by error correction of an one-frame unit.

C1F2 : Please refer to the error correction (ECC) part for C1 series correction flag.

C2F : C2F is the flag which shows the data interpolation situation of DOUTA. When C2F is H, it shows that the data is uncorrectable data. For the details, refer to the item of Error Correcter (ECC).

LRCK(ECC) : It is the signal for the Lch/Rch change at the time of the ECC data output. For the details, refer to the item of Error Correcter (ECC).

HOKAN_FLAG : It is the flag shows linear interpolation situation. If it is H, it is shown that the linear interpolation of the data is impossible for continuous correction impossible data from ECC output.

FRAME[3:0] : It is the signal for counting frames. For the details, refer to the item of Error Correcter (ECC).

SLOW/FAST : It shows the result of count between the edges of EFM in PLCK. It turns to L if counted value is no more than 11T and turns to H if counted value is more than 11T. For the details, refer to the item of CLV and PLL.

SFPL : SFPL is the signal which turns to L when the PLL operation mode is NORMAL INITIALIZE mode and turns to H when the mode is NORMAL PC mode or WIDE mode.

FOK : FOK is the signal which turns to H when focus suits. For the details, refer to the item of Focus Search.

SCRTIMER : SCRTIMER is the signal adding DEFECT and NEW_DEFECT. If it turns H, it turns to L after 4ms passed.

COMP : COMP is the output of the result of comparison at adjustment of balance and gain of tracking and focus.

TGUON : TGUON is the signal which turns to H when the gain of tracking filter increases at track jumping and etc.

SENS : SENS is the signal which turns to H if errors are exist during auto adjustment. For the details, refer to the item of Auto Adjustment and Measurement.

DOUT(SUBQ) : It is the signal to read internal status and Sub-Q code. For the details, refer to the item of Command Interface.

MIRROR : MIRROR is the signal which turns to H when laser passed through the mirror side. For the detailes, refer to the item of MIRROR signal generator.

(Analog Signal)
By command &h63[7:0], 43, 44pin are available for monitoring various internal signals and for inputting the test signal.

43pin ANA_MONI0

Command	Meaning
&h631X	DA output of digital signals
&h632X	ASY output
&h633X	AC amplifier output
&h634X	ACBD amplifier output
&h635X	ACBD input & separation
&h636X	DAC output of DET block
&h637X	FE(AC) output
&h638X	FE(BD) input & separation
&h639X	TE(E) output
&h63AX	TE(F) input & separation
&h63BX	APCREF output
&h63CX	BG output
&h63DX	ADPF amplifier output
&h63EX	ADPF input & separation
&h63FX	RVCO voltage output
&h6307	DAC output of ADC block

44pin ANA_MONI1

Command	Meaning
&h63X1	DA output of digital signals
&h63X2	BD amplifier output
&h63X3	FE(AC) input & separation
&h63X4	FE(BD) output
&h63X5	TE(E) input & separation
&h63X6	TE(F) output

43,44pin are I/O terminals with built-in pull-up resistor. Execute monitor setup for these terminals by the following commands.

&hB4[7:6] Change-over of monitor terminal Digital/Analog
&hB5[7:6] ON/OFF of pull-up resistor built in monitor terminal

The contents of each signal are as follows.
ASY output: It is the output of ASY block of RF block.
AC amplifier output: It is the output of the first amplifier by the side of AC input of the RF block.
ACBD amplifier output: It is the output of the addition amplifier of AC signal and BD signal.
ACBD input & separation: It separates the output of ACBD side AC, BD addition amplifier and it is made to input from the outside. By this, it is possible to input to RFGCA directly.
DAC output of DET block: It is the output of the 6bitDAC which becomes to threshold level of compersion at DET circuit in RF block.
FE(AC) output: It is the output of AC side FE amplifier.
FE(BD) input & separation: It separates the output of BD side FE amplifier and it is made to input from the outside. By this, it is possible to input to ADC directly.
TE(E) output: It is the output of E side of TE amplifier.
TE(F) input & separation: It separates the output of F side TE amplifier and it is made to input from the outside. By this, it is possible to input to ADC directly.
APCREF output: It outputs the REF voltage of APC circuit. It is possible to monitor the reference level of APC.
BG output: It outputs the BG voltage of APC circuit.
ADPF amplifier output: It is the output of the addition amplifier of PCO signal and FCO signal of the PLL block.
ADPF input & separation: It separates the input of the addition amplifier of PCO signal and FCO signal of the PLL block. It is possible to input to the addition amplifier from the outside directly.
RVCO voltage output: It outputs RVCO voltage of PLL block. This voltage is used for set value of VCO offset.
DAC output of ADC block: It is the output of the DAC for set up the reference voltage in A/D converter of servo system.
BD amplifier output: It is the output of the first amplifier by the side of BD input of the RF block.
FE(AC) input & separation: It separates the output of AC side FE amplifier and it is made to input from the outside. By this, it is possible to input to ADC directly.
FE(BD) output: It is the output of BD side FE amplifier.
TE(E) input & separation: It separates the output of E side TE amplifier and it is made to input from the outside. By this, it is possible to input to ADC directly.
TE(F) output: It is the output of F side TE amplifier.

(DA output of digital signals)
It is possible to monitor the signals calculated by the digital block from 43pin and 44pin by commands &h631X and &h63X1 as analog output through DAC.
The signal to monitor is selectable by command &hFA[3:0].

&hFA[3:0]	43pin ANA_MONI0	44pin ANA_MONI1
0h	FE	TE
1h	SLED_HPF	LPF
2h	RFRP	TZC
3h	BL	PL
4h	PS	BS
5h	PS	PL
6h	BL	BS
7h	TE	E+F_HPF
8h	-	SLED

43, 44pin are I/O terminals with built-in pull-up resistor. Execute monitor setup for these terminals by the following commands.

&hB4[7:6] Change-over of monitor terminal Digital/Analog
&hB5[7:6] ON/OFF of pull-up resistor built in monitor terminal
The contents of each signal are as follows.
FE: It is the focus error signal. It is made by subtracting with AC signal and BD signal.
SLED_HPF: It is the HPF componet of Sled signal. It is used for adjustment of sled gain.
RFRP: It is the signal made by subtracting peak_short signal and bottom_short signal of RF signal. For the details, refer to the item of RFRP signal generator.
BL: It is the bottom_logn signal of RF signal. For the details, refer to the item of DET circuit.
PS: It is the peak_short signal of RF signal. For the details, refer to the item of DET circuit.
TE: It is the tracking error signal. It is made by subtracting with E signal and F signal.
LPF: It is the output of each LPF and BPF used for auto adjustment. For the details, refer to the each item of Auto Adjustment and Measurement.
TZC: It is the HPF component of TE signal. TZC signal is generated by compared this signal with 0 and used for Tr number counting at the time of track jump.
PL: It is the peak_long signal of RF signal. For the details, refer to the item of DET circuit.
BS: It is the bottom_short signal of RF signal. For the details, refer to the item of DET circuit.
E+F_HPF: It is the HPF component of (E+F) signal.
SLED: It is the sled error signal.

17.5.5. CD-DSP Command

BM94801KUT Instruction Codes List

MSB/LSB		0	1	2	3	4	5	6	7
4	POWER DOWN	POWER DOWN	SYSTEM CLOCK						YFLAG COUNT1
5	PLL	VCO DEV EFM DEV	PLL Setting	PLL TEST Setting					
6	RF	Laser ON EQ APC	RF Gain APC REF	RF-EQ Setting	RF TEST Setting	RF-AC Offset	RF-BD Offset	RF-E Offset	RF-F Offset
7									
8	CLV PLL	CLV Mode Setting	CLV-W Target	PLL Mode Setting	CLV Setting FC Gain	PCI Gain CLV Gain	CLV-W Gain	CLV-N Gain	CLV, PLL T-Gain
9	OFFSET		Sled Offset	Focus Offset	Tracking Offset	AC amp Offset	BD amp Offset	E amp Offset	F amp Offset
A	CIRC	Audio ATT	ECC Status			DEFECT N-DEFECT	WIN, SUB TEST	SUBQ TEST	
B	MONI				MONI I/O Select	MONI D/A Select	MONI PU ON/OFF	PIO Setting	PIO OUT Register
C	SERVO SEQ	FON Servo TEST	Tr ON Sled ON			Tr Jump Forward	Sd Move Forward	Tr Jump Reverse	Sd Move Reverse
D	SERVO SEQ	ADJ GO	ADJ Sled Gain	ADJ Wait Time	Tr Error Min-Max	Tr Error Number	&hDE Read Setting	DFCT, N-DFCT Setting 1	DFCT, N-DFCT Setting 2
E	SERVO DF								
F	SERVO DF	Intermittent Sled ON	Intermittent Sled OFF	FZC Level	ATS Level	Sled Gain Setting	Sled LPS Setting	FE, TE Offset	TZC Filter

MSB/LSB		8	9	A	B	C	D	E	F
4	POWER DOWN	YFLAG COUNT2	YFLAG COUNT3						
5	PLL							ID Read	
6	RF	FE-Gain Setting	ADC Full Setting						
7									
8	CLV PLL	CLV Kick	PCI Counter	CLV, PLL Setting	CLV,PLL TEST-Reg	ATS TIME Setting	HPF(E+F) Setting		
9	OFFSET	Fo Balance Offset	Tr Balance Offset	Fo Total Gain	Tr Total Gain	RF Offset	RF Gain	VCO Center	VCO Gain
A	CIRC	RF-DET Setting 1	Deffect TH Level	FOK Setting	RF-DET Setting 2	RF-DET Setting 3			
B	MONI								
C	SERVO SEQ	Fo Serch Voltage	Focus Loop	Loop OFF Recovery	Tr Jump Setting	Tr Jump BT,OT	Tr Jump LS Kick T	ATS Setting	Servo Setting
D	SERVO SEQ	SEQ TEST	SEQ MONI					ADJ SQ STATUS	
E	SERVO DF	Fo LPF HPF Gain	Fo Filter Setting	Tr LPF HPF Gain	Tr Filter Setting	Fo, Tr Gain	Disturbance Setting	Monitor Setting	Gain Down Sled Select
F	SERVO DF	F/E Gain-Down	TDOUT Offset	Monitor Select	ASY Offset	Tr Jump Pulse ADD	Tr Jump Pulse-H	Sled Pulse-H	

Command : &h40
Meaning : POWER DOWN setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	PWDRF	RF POWER DOWN. (others than bias voltage generation circuit)	0 : Normal (Initial value) 1 : Power Down
6	PWDBI	RF bias voltage generation circuit POWER DOWN.	0 : Normal (Initial value) 1 : Power Down
5	PWDSE	SERVO POWER DOWN.	0 : Normal (Initial value) 1 : Power Down
4	PWDADC	ADC POWER DOWN.	0 : Normal (Initial value) 1 : Power Down
3	-		
2	-		
1	PWDADP	ADPFO POWER DOWN.	0 : Normal (Initial value) 1 : Power Down
LSB	PWDANA	AOUDIO LINEOUT POWER DOWN.	0 : Normal (Initial value) 1 : Power Down

Command : &h41
Meaning : SYSTEM CLOCK setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	DFCLK	DF system clock.	0 : Normal (Initial value) 1 : Stop
6	AUDCLK	AUDIO system clock.	0 : Normarl (Initial value) 1 : Stop
5	-		
4	ECCCLK	ECC system clock.	0 : Normal (Initial value) 1 : Stop
3	17MCLK	CLK17M system clock.	0 : Normal (Initial value) 1 : Stop
2	ADLCLK	ADC LOGIC system clock.	0 : Normal (Initial value) 1 : Stop
1	CLVCLK	CLV LOGIC system clock.	0 : Normal (Initial value) 1 : Stop
LSB	DELCLK	DET LOGIC system clock.	0 : Normal (Initial value) 1 : Stop

Command : &h47
Meaning : YFLAG COUNTER setting (Initial value : 08h)

Bit	Command code	Meaning	Status
MSB	CNTEN	To select YFLAG COUNTER enable.	0 : Counter OFF (Initial value) 1 : Counter ON
6	OUTEN	To select YFLAG OUTPUT invert.	0 : Normal (Initial value) 1 : Invert
5	FLG_SEL1	To select YFLAG OUTPUT.	0 : Counter (Initial value) 1 : HOKAN_FLAG 2 : C2FX 3 : External
4	FLG_SEL0		
3	HOUT	To fix OUTPUT to “H”.	0 : Normal 1 : H (Initial value)
2	LOUT	To fix OUTPUT to “L”.	0 : Normal (Initial value) 1 : L
1	-		
LSB	CNTIO_SEL	To input Counter signal from external terminal.	0 : Internal (C2FX) (Initial value) 1 : External

Command : &h48
Meaning : YFLAG COUNTER COUNT-UP setting (Initial value : 08h)

Bit	Command code	Meaning	Status
MSB	CNTUP7	To set YFLAG Counter Count up value.	(Initial value : 08h)
6	CNTUP6		
5	CNTUP5		
4	CNTUP4		
3	CNTUP3		
2	CNTUP2		
1	CNTUP1		
LSB	CNTUP0		

Command : &h49
Meaning : YFLAG COUNTER COUNT-DOWN settting (Initial value : 08h)

Bit	Command code	Meaning	Status
MSB	CNTDW7	To set YFLAG Conter Count down value.	(Initial value : 08h)
6	CNTDW6		
5	CNTDW5		
4	CNTDW4		
3	CNTDW3		
2	CNTDW2		
1	CNTDW1		
LSB	CNTDW0		

Command : &h50
Meaning : PLL setting, EFM dividing ratio (Initial value : 00h) → (Recommended value : 80h)

Bit	Command code	Meaning	Status
MSB	DVCO1	To set VCO-PC dividing ratio.	0 : 1/1 (Initial value) 1 : 1/2 2 : 1/4 3 : 1/8
6	DVCO0		
5	DEFM1	To set EFM dividing ratio.	0 : 1/1 (Initial value) 1 : 1/2 2 : 1/4 3 : 1/8
4	DEFM0		
3	-		
2	-		
1	-		
LSB	-		

Command : &h51
Meaning : Various setting items for PLL (Initial value : C2h) → (Recommended value : 00h)

Bit	Command code	Meaning	Status
MSB	SELX	To select external input for PLCK. Be sure to set up 0 when using normal operation.	0 : Normal 1 : External input (Initial value)
6	VCOSTP	To turn ON/OFF VCO transmitter. Be sure to set up 0 when using normal operation.	0 : ON 1 : OFF (Initial value)
5	PCOM1	PCO condition in DEFECT.	0 : With compensation (Initial value) 1 : Hi-z 2 : Without countermeasure
4	PCOM0		
3	VCO OUT	To input VCO output from AC terminal (MIRROR).	0 : Normal (Initial value) 1 : Test
2	PLCK REV	To invert PLCK input.	0 : Normal (Initial value) 1 : Invert
1	EFMEXT	External input for EFM. Be sure to set up 0 when using normal operation.	0 : Normal 1 : Input (Initial value)
LSB	DAC LOAD	To load the value of command &h91[7:0],&h92[7:6] to DAC of ADC block. (use only at the time of test)	0 : Normal (Initial value) 1 : Load

Command : &h52
Meaning : PLL test setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	SELFCO	To select FCO.	0 : ON (Initial value) 1 : Hiz
6	ASYOFS	To select ASY offset.	0 : Hiz (Initial value) 1 : ON
5	ASYHIZ	To select the condition which sets ASY to Hiz.	0 : When FOK is “L” (Initial value) 1 : When FOK is “L” or DEFECT is “H”
4	PLLPCH	To select the signal which holds PLL_PC.	0 : When NEW_DEFECT is “H” (Initial value) 1 : When DEFECT or NEW_DEFECT is ”H”
3	-		
2	-		
1	-		
LSB	PLLPCHL	To hold PLL_PC(PCPI=L,PCNI=L)	0:Normal (Initial value) 1:Hold

Command : &h5E
Meaning : Model ID (Exclusive for reading)

Bit	Command code	Meaning	Status
MSB	ID7	To read ID Number of application model.	In case of BM94801KUT 47h
6	ID6		
5	ID5		
4	ID4		
3	ID3		
2	ID2		
1	ID1		
LSB	ID0		

Command : &h60
Meaning : Laser ON (Initial value : 00h) → (Recommended value : 10h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	LON	To turn on the laser.	0 : Laser OFF (Initial value) 1 : Laser ON
3	-		
2	EQTEST	EQ test.	0 : Normal (Initial value) 1 : To change EQO terminal for input pin
1	RFFC_ SEL	To select RF amplifier (first step) phase Compensateing capacitors.	0 : 0.25pF (Initial value) 1 : 0.125pF
LSB	APCINV	To select APC polarity setting.	0 : Normal (Initial value) 1 : Invert

Command : &h61
Meaning : Focus/Tracking gain setting and APC REF voltage setting (Initial value : 07h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	CDRW_SEL1	To set focus/tracking gain.	(RF, FE / TE) 0 : Normal CD (×1/×1) (Initial value) 1 : RW high refracction (×3/×3) 2 : RW normal (×5/×3)
4	CDRW_SEL0		
3	APCREF_SEL3	To set APC REF Voltage.	&h61[3:0]×5+145 [mV] (Vcc=3.0V)
2	APCREF_SEL2		
1	APCREF_SEL1		
LSB	APCREF_SEL0		

Command : &h62
Meaning : Rf equalizer setting (Initial value : 09h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	EQF_SEL1	To set RF equalizer frequency.	0 : 0.72MHz (Initial value) 1 : 1.45MHz 2 : 2.90MHz 3 : EQ Through
4	EQF_SEL0		
3	EQG_SEL1	To set RF equalizer gain.	0 : 6dB 1 : 9dB 2 : 12dB (Initial value)
2	EQG_SEL0		
1	EQB_SEL1	To select RF equalizer boost level.	0 : 2dB 1 : 4dB (Initial value) 2 : 6dB 3 : 8dB
LSB	EQB_SEL0		

Command : &h63
Meaning : RF test setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	ANA_M 03	Used for RF chip test.(ANA-MONI0) 0h : Normal (Initial value) 1h : MONI0_TEST→(DA output of digital signals) 2h : ASY_TEST→ (ASY output) 3h : AC_TEST→ (AC amplifier output) 4h : ACBD_TEST→ (ACBD amplifier output) 5h : ACBD_TEST→ (ACBD input & separation) 6h : DET_TEST→ (DAC output of DET block) 7h : FE_TEST_AC→ (FE (AC) output) 8h : FE_CUT_BD→ (FE (BD) input & separation) 9h : TE_TEST_E→ (TE (E) output)	Ah:TE_CUT_F→ (TE (F) input & separation) Bh: APCREF_TEST→ (APCREF output) Ch: BG_TEST→ (BG output) Dh:LOOP_TEST[2] → (ADPF amplifier output) Eh:LOOP_TEST[1] → (ADPFinput & separation) Fh:LOOP_TEST[0] → (RVCO voltage block)
6	ANA_M 02		
5	ANA_M 01		
4	ANA_M 00		
3	-		&h6307h : ADC_TEST→ (DAC output of ADC block) →ANA_MONI0
2	ANA_M 12	Used for RF chip test.(ANA-MONI1) 0h : Normal (Initial value). 1h : MONI1_TEST→ (DA output of digital signals) 2h : BD_TEST→ (BD amplifier output) 3h : FE_CUT_AC→ (FE (AC) input & separation) 4h : FE_TEST_BD→ (FE (BD) amplifier output) 5h : TE_CUT_E→ (TE (E) input & separation)	6h : TE_TEST_F→ (TE (F) output)
1	ANA_M 11		
LSB	ANA_M 10		

Command : &h64
Meaning : AC amplifier offset adjustment (Initial value : 04h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	-		
3	-		
2	AC_OFF SET2	AC amplifier offset adjustment.	Vc-{&h64[2:0]×(-0.22)×V_{DD}/3} (Initial value : 04h)
1	AC_OFF SET1		
LSB	AC_OFF SET0		

Command : &h65
Meaning : BD amplifier offset adjustment (Initial value : 04h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	-		
3	-		
2	BD_OFF SET2	BD amplifier offset adjustment.	Vc-{&h65[2:0]×(-0.22)×V_{DD}/3} (Initial value : 04h)
1	BD_OFF SET1		
LSB	BD_OFF SET0		

Command : &h66
Meaning : E amplifier offset adjustment (Initial value : 04h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	-		
3	-		
2	E_OFF SET2	E amplifier offset adjustment.	Vc+{(7-&h66[2:0])×0.22×V_{DD}/3} (Initial value : 04h)
1	E_OFF SET1		
LSB	E_OFF SET0		

Command : &h67
Meaning : F amplifier offset adjustment (Initial value : 04h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	-		
3	-		
2	F_OFF SET2	F amplifier offset adjustment.	Vc+{(7-&h67[2:0])×0.22×V_{DD}/3} (Initial value : 04h)
1	F_OFF SET1		
LSB	F_OFF SET0		

Command : &h68
Meaning : Focus error gain setting (Initial value : 0Bh)

Bit	Command code	Meaning	Status	
MSB	-			
6	-			
5	-			
4	-			
3	FE_GA IN3	FE gain setting.	0h : 0.37[dB] 1h : 0.75[dB] 2h : 1.16[dB] 3h : 1.58[dB] 4h : 2.03[dB] 5h : 2.50[dB] 6h : 3.00[dB] 7h : 3.50[dB] 8h : 4.08[dB] 9h : 4.68[dB]	Ah : 5.32[dB] Bh : 6.00[dB] (Initial value) Ch : 6.77[dB] Dh : 7.60[dB] Eh : 8.32[dB] Fh : 9.54[dB]
2	FE_GA IN2			
1	FE_GA IN1			
LSB	FE_GA IN0			

Command : &h69
Meaning : ADC block Dynamic range select (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	ADCFR	ADC full range.	0 : Normal (Initial value) 1 : full range
6	ADCCH_SEL2	ADC full range channel.	0 : 0ch (Initial value) 1 : 1ch 2 : 2ch 3 : 3ch 4 : 4ch 5 : 5ch 6 : all 7 : Nothing
5	ADCCH_SEL1		
4	ADCCH_SEL0		
3	-		
2	-		
1	-		
LSB	-		

Command : &h80
Meaning : CLV servo mode setting (Initial value : 00h) → (Recommended value : 40h)

Bit	Command code	Meaning	Status
MSB	-		
6	CLV MODE2	To set CLV servo run mode.	0 : OFF (Initial value) 1 : Kick (&h88 setup value output. Positive voltage output) 2 : Brake (&h88 setup value output. Negative voltage output) 3 : Auto Stop 4 : ON (shift to AUTO) 5 : Phase mode 6 : Rough mode 7 : High speed rough mode
5	CLV MODE1		
4	CLV MODE0		
3	-		
2	-		
1	-		
LSB	-		

Command : &h81
Meaning : Target setting under CLV WIDE mode (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	TAR7	To set upper 8bits of target value under CLV WIDE mode.	(Approx. ×1 speed by 1Eh, Approx × speed by 3Dh,approx. ×4 speed by 7Ah.) (Initial value : 00h)
6	TAR6		
5	TAR5		
4	TAR4		
3	TAR3		
2	TAR2		
1	TAR1		
LSB	TAR0		

Command : &h82
Meaning : PLLmode setting (Initial value : 00h) → (Recommended value : 10h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	PLLMOD1	To set PLL run mode.	0 : Initialize mode (Initial value) 1 : Normal PC mode 2 : Wide mode 3 : ×4 speed mode (for VCO mesurement)
4	PLLMOD0		
3	-		
2	-		
1	-		
LSB	-		

Command : &h83
Meaning : CLV setting and FC integral gain (Initial value : 00h) → (Recommended value : 01h)

Bit	Command code	Meaning	Status
MSB	-		
6	HCOE	To turn ON/OFF “Half-wave CLV mode”.	0 : OFF (Initial value) 1 : ON
5	CLVHIT1	To set CLV height restrictions.	0 : No restriction (Initial value) 1 : 1/8 2 : 2/8 3 : 3/8
4	CLVHIT0		
3	-		
2	h5N2	FC integral gain.	2^{-n} (n : setup value) Initial value : 2^{-0}=1
1	h5N1		
LSB	h5N0		

Command : &h84
Meaning : PCI integral gain, CLV phase gain (Initial value : 00h) → (Recommended value : 53h)

Bit	Command code	Meaning	Status
MSB	-		
6	h5P2	PCI integral gain.	2^{-n} (n : setup value) Initial value : 2^{-0}=1
5	h5P1		
4	h5P0		
3	-		
2	h1N2	CLV phase gain.	2^{-n} (n : setup value) Initial value : 2^{-0}=1
1	h1N1		
LSB	h1N0		

Command : &h85
Meaning : Gain under CLV WIDE (Initial value : 00h) → (Recommended value : 34h)

Bit	Command code	Meaning	Status
MSB	-		
6	h2W2	Low boost gain under CLV_Wide.	2^{-n} (n : setup value) Initial value : 2^{-0}=1
5	h2W1		
4	h2W0		
3	-		
2	h4W2	Through gain under CLV_Wide.	2^{-n} (n : setup value) Initial value : 2^{-0}=1
1	h4W1		
LSB	h4W0		

Command : &h86
Meaning : Gain under CLV NORMAL (Initial value : 00h) → (Recommended value : 31h)

Bit	Command code	Meaning	Status
MSB	-		
6	h2N2	Low boost gain under CLV-Normal.	2^{-n} (n : setup value) Initial value : 2^{-0}=1
5	h2N1		
4	h2N0		
3	-		
2	h4N2	Through gain under CLV-Normal.	2^{-n} (n : setup value) Initial value : 2^{-0}=1
1	h4N1		
LSB	h4N0		

Command : &h87
Meaning : CLV and PLL total gain (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	CNG	Gain under CLV-Normal.	0 : ×1 (Initial value) 1 : ×0.75
6	CWG	Gain under CLV-Wide.	0 : ×1 (Initial value) 1 : ×0.75
5	CPG	CLV phase gain.	0 : ×1 (Initial value) 1 : ×0.75
4	FCG	FC gain.	0 : ×1 (Initial value) 1 : ×0.75
3	PCG	PCI gain.	0 : ×1 (Initial value) 1 : ×0.75
2	-		
1	-		
LSB	-		

Command : &h88
Meaning : CLV kick height (Initial value : 7Fh)

Bit	Command code	Meaning	Status
MSB	CVK7	CLV kick height (Value : complement for 2).	(Initial value : 7Fh)
6	CVK6		
5	CVK5		
4	CVK4		
3	CVK3		
2	CVK2		
1	CVK1		
LSB	CVK0		

Command : &h89
Meaning : PCI counter Initial value (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	PCINTV7	To set Initial value of PCI counter.	(Initial value : 00h)
6	PCINTV6		
5	PCINTV5		
4	PCINTV4		
3	PCINTV3		
2	PCINTV2		
1	PCINTV1		
LSB	PCINTV0		

Command : &h8A
Meaning : CLV,PLLStatus setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	SEL CLVH	CLV status against focusing failure.	0 : Vc output (Initial value) 1 : Without counter measure
6	INT_L	To load PLL integral register value.	0 : Normal (Initial value) 1 : &h8B[7 : 0] setup value is loaded
5	TOFS	To set whether to add offset to the change in target value.	0 : Add (Initial value) 1 : Don't add
4	-		
3	JCLVH	To set whether to carry out CLV hold at LOCK "H" and under Track jump.	0 : Don't add (Initial value) 1 : Add
2	DCLVH	To set whether to carry out CLV hold at LOCK "H" and under DEFECT "H".	0 : Don't add (Initial value) 1 : Add
1	NDCLV HM	To set whether to carry out CLV hold at LOCK "H" under NEW_DEFECT "H".	0 : Don't add (Initial value) 1 : Add
LSB	-		

Command : &h8B
Meaning : CLV and PLL test input register (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	CPTST7	To register CLV/PLL test inputs. (Center value : 00h)	(Initial value : 00h)
6	CPTST6		
5	CPTST5		
4	CPTST4		
3	CPTST3		
2	CPTST2		
1	CPTST1		
LSB	CPTST0		

Command : &h8C
Meaning : Gain up hold time setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	-		
6	GAINUP HLD2	To select hold time of Gain up when anti-shock.	0 : 0ms (Initial value) 1 : 20ms 2 : 50ms 3 : 100ms 4 : 200ms
5	GAINUP HLD1		
4	GAINUP HLD0		
3	-		
2	-		
1	-		
LSB	-		

Command : &h8D
Meaning : HPF(E+F) signal reverse setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB			
6			
5			
4			
3			
2			
1			
LSB	EAF REVER	HPF(E+F) signal reverse.	0 : Normal (Initial value) 1 : Reverse

Command : &h91
Meaning : Sled offset adjusting register (Initial value : 80h)

Bit	Command code	Meaning	Status
MSB	SDOFS7	To adjust sled offset. Center value is 80h because of offset binary.	(Initial value : 80h)
6	SDOFS6		
5	SDOFS5		
4	SDOFS4		
3	SDOFS3		
2	SDOFS2		
1	SDOFS1		
LSB	SDOFS0		

Command : &h92
Meaning : Focus offset adjusting register (Initial value : 80h)

Bit	Command code	Meaning	Status
MSB	FDOFS7	To adjust focus offset. Center value is 80h because of offset binary.	(Initial value : 80h)
6	FDOFS6		
5	FDOFS5		
4	FDOFS4		
3	FDOFS3		
2	FDOFS2		
1	FDOFS1		
LSB	FDOFS0		

Command : &h93
Meaning : Tracking offset adjusting register (Initial value : 80h)

Bit	Command code	Meaning	Status
MSB	TDOFS7	To adjust tracking offset. Center value is 80h because of offset binay.	(Initial value : 80h)
6	TDOFS6		
5	TDOFS5		
4	TDOFS4		
3	TDOFS3		
2	TDOFS2		
1	TDOFS1		
LSB	TDOFS0		

Command : &h94
Meaning : AC amplifier of RF block offset adjusting register (Initial value : 80h)

Bit	Command code	Meaning	Status
MSB	ACOFS7	To adjust offset of AC amplifier of RF block. Center value is 80h because of offset binary.	(Initial value : 80h)
6	ACOFS6		
5	ACOFS5		
4	ACOFS4		
3	ACOFS3		
2	ACOFS2		
1	ACOFS1		
LSB	ACOFS0		

Command : &h95
Meaning : BD amplifier of RF block offset adjusting register (Initial value : 80h)

Bit	Command code	Meaning	Status
MSB	BDOFS7	To adjust offset of BD amplifier of RF block. Center value is 80h because of offset binary.	(Initial value : 80h)
6	BDOFS6		
5	BDOFS5		
4	BDOFS4		
3	BDOFS3		
2	BDOFS2		
1	BDOFS1		
LSB	BDOFS0		

Command : &h96
Meaning : E amplifier of RF block offset adjusting register (Initial value : 80h)

Bit	Command code	Meaning	Status
MSB	RFEOFS7	To adjust offset of E amplifier of RF block. Center value is 80h because of offset binary.	(Initial value : 80h)
6	RFEOFS6		
5	RFEOFS5		
4	RFEOFS4		
3	RFEOFS3		
2	RFEOFS2		
1	RFEOFS1		
LSB	RFEOFS0		

Command : &h97
Meaning : F amplifier of RF block offset adjusting register (Initial value : 80h)

Bit	Command code	Meaning	Status
MSB	RFFOFS7	To adjust offset of F amplifier of RF block. Center value is 80h because of offset binary.	(Initial value : 80h)
6	RFFOFS6		
5	RFFOFS5		
4	RFFOFS4		
3	RFFOFS3		
2	RFFOFS2		
1	RFFOFS1		
LSB	RFFOFS0		

Command : &h98
Meaning : Focus balance offset adjusting register (Initial value : 80h)

Bit	Command code	Meaning	Status
MSB	FBOFS7	To adjust focus balance offset. Center value is 80h because of offset binary.	(Initial value : 80h)
6	FBOFS6		
5	FBOFS5		
4	FBOFS4		
3	FBOFS3		
2	FBOFS2		
1	FBOFS1		
LSB	FBOFS0		

Command : &h99
Meaning : Tracking balance offset adjusting register (Initial value : 80h)

Bit	Command code	Meaning	Status
MSB	TBOFS7	To adjust tracking balance offset. Center value is 80h because of offset binary.	(Initial value : 80h)
6	TBOFS6		
5	TBOFS5		
4	TBOFS4		
3	TBOFS3		
2	TBOFS2		
1	TBOFS1		
LSB	TBOFS0		

Command : &h9A
Meaning : Focus total gain adjusting register (Initial value : 10h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	FG5	To adjust focus total gain. Center value is 20h because of offset binary.	&h9A[5 : 0] multiple (Initial value : 10h)
4	FG4		
3	FG3		
2	FG2		
1	FG1		
LSB	FG0		

Command : &h9B
Meaning : Tracking total gain adjusting register (Initial value : 10h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	TG5	To adjust tracking total gain. Center value is 20h because of offset binary.	&h9B[5:0] multiple (Initial value : 10h)
4	TG4		
3	TG3		
2	TG2		
1	TG1		
LSB	TG0		

Command : &h9C
Meaning : RF offset adjusting register (Initial value : 08h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	-		
3	RFOFS3	To adjust RF offset (RF basic level).	Vc+((15-&h9C[3:0])×0.20-2.0)×V_{DD}/3 [V] (Initial value : 08h)
2	RFOFS2		
1	RFOFS1		
LSB	RFOFS0		

Command : &h9D
Meaning : RF gain adjusting register (Initial value : 1Ah)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	RFGAIN4	To adjust RF gain. However, the range which may be taken by &h9D[4 : 0] is taken as from 00h to 1Fh.	100/ ((31-&h9D[4:0])×5+50) multiple (Initial value : 1Ah)
3	RFGAIN3		
2	RFGAIN2		
1	RFGAIN1		
LSB	RFGAIN0		

Command : &h9E
Meaning : Resistance of center current of VCO setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	VCOOFS4	To set resistance of center current of VCO. (To adjust VCO offset.) On the whole, the frequency characteristic is carried up, so that the resistance is small.	(31-&h9E[4:0])×2.5k+2.5k [kΩ] (Initial value : 00h)
3	VCOOFS3		
2	VCOOFS2		
1	VCOOFS1		
LSB	VCOOFS0		

Command : &h9F
Meaning : Resistance of VCO gain setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	-		
3	VCOG3	To set resistance of VCO gain. The tilt of frequency characteristic. Becomes step, so that the resistance is small.	(15-&h9F[3:0])×5k+10k [kΩ] (Initial value : 0h)
2	VCOG2		
1	VCOG1		
LSB	VCOG0		

Command : &hA0
Meaning : ECC output data sound volume setting (Initial value : 00h) → (Recommended value : 20h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	ECCATT1	To set sound volume from ECC output data	0 : MUTE (Initial value) 1 : -12dB 2 : 0dB
4	ECCATT0		
3	-		
2	-		
1	-		
LSB	-		

Command : &hA1
Meaning : ECC Status setting and ECC test (Initial value : 80h) → (Recommended value : 00h)

Bit	Command code	Meaning	Status
MSB	RAMCLR	To clear RAM for ECC. Be sure to set up 0 when using normal operation.	0 : Normal 1 : Clear (Initial value)
6	CDROM	CD-ROM mode select.	0 : CD-DA (Initial value) 1 : CD-ROM
5	FCLR	To mute against overflow of frame counter.	0 : ON (Initial value) 1 : OFF
4	SELECC	To select ECC correction ability.	0 : C1_2word C2_4word (Initial value) 1 : C1_2word C2_2word
3	C12TST	C1 series 2 word correction test.	0 : Normal (Initial value) 1 : Test
2	-		
1	-		
LSB	-		

Command : &hA4
Meaning : DEFECT and NEW_DEFECT setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	MTND1	To select NEW_DEFECT masking time after DEFECT.	0 : 0ms (Initial value) 1 : 0.1ms 2 : 0.5ms 3 : 1.0ms
6	MTND0		
5	TNDS	To select the time until NEW_DEFECT is set up.	0 : 19T (Initial value) 1 : 35T
4	TNDRS	To select the time until NEW_DEFECT is reset.	0 : 96T (Initial value) 1 : 256T
3	WQOKT	To set the timing (SUBSYQ2) to judge WQOK at ESP.	0 : 50% (Initial value) 1 : 85%
2	IBC	To set EFM Reconversion ROM.	0 : Normal (Initial value) 1 : Convert to 2T.
1	-		
LSB	-		

Command : &hA5
Meaning : WINDOW and SUB test setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	GFSTST	To fix GFS to “H”.	0 : Normal (Initial value) 1 : Test
6	WQTST	To fix WQ to “H”.	0 : Normal (Initial value) 1 : Test
5	LOCK TST	To fix LOCK to “H”.	0 : Normal (Initial value) 1 : Test
4	GFS88 TST	To fix GFS88 to “H”.	0 : Normal (Initial value) 1 : Test
3	NDFTST	To fix NEW_DEFECT to “L”.	0 : Normal (Initial value) 1 : Test
2	WFCK TST	To input WFCK from MIRROR.	0 : Normal (Initial value) 1 : Test
1	SSYQ TST	To input SUBSYQ (2) from FOK.	0 : Normal (Initial value) 1 : Test
LSB	-		

Command : &hA6
Meaning : SUBQ test mode (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	SQTST3	To select SUBQ test mode.	0 : Normal (Initial value) Other : Test
6	SQTST2		
5	SQTST1		
4	SQTST0		
3	-		
2	-		
1	-		
LSB	-		

Command : &hA8
Meaning : DETECTOR of RF block setting1 (Initial value : 00h) → (Recommended value : 98h)

Bit	Command code	Meaning	Status
MSB	DETPOL	To set the polarity of DETECT block.	0 : Under EQO invert (Initial value) 1 : Under EQO un-invert
6	PBSBRT	To select the blind time of peak/bottom short measurement sequence.	0 : 1.06μsec (Initial value) 1 : 1.59μsec
5	PBSDAC1	To set the width of DAC increase/decrease for peak/bottom short measurement.	&hA8[5:4]+1 [STEP] 1STEP=V_{DD}×0.8/64 [V] (Initial value : 0h)
4	PBSDAC0		
3	MIRTHL3	To set the MIRROR threshold level	(PeakLong–Bottom Long) ×&hA8[3:0]/16 (Initial value : 0h)
2	MIRTHL2		
1	MIRTHL1		
LSB	MIRTHL0		

Command : &hA9
Meaning : Diffect threshold level setting (Initial value : 00h) → (Recommended value : AAh)

Bit	Command code	Meaning	Status
MSB	DSETTH3	To set the threshold level of DEFECT set side.	PeakLong–(&hA9[7:4]×V_{DD}×0.8/32) [V]. (Initial value : 0h)
6	DSETTH2		
5	DSETTH1		
4	DSETTH0		
3	DRSTTH3	To set the threshold level of DEFECT reset side.	BottomLong+(&hA9[3:0]×V_{DD}×0.8/32) [V]. (Initial value : 0h)
2	DRSTTH2		
1	DRSTTH1		
LSB	DRSTTH0		

Command : &hAA
Meaning : FOK setting (Initial value : 00h) → (Recommended value : 13h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	FOKD	To select the method of FOK judgement.	0 : Decided by Peak Long value (Initial value) 1 : Decided by Peak Long – Bottom Long (amplitude)
3	FOKTHL3	To set the FOK threshold level.	At &hAA[4]=0, FOK is set to “L” by PeakLong<(&hAA[3:0]-8)×V_{DD}×0.8/16. At &hAA[4]=1, FOK is set to “L” by (PeakLong–BottomLong)<&hAA[3:0] ×V_{DD}×0.8/16 (Initial value : 0h)
2	FOKTHL2		
1	FOKTHL1		
LSB	FOKTHL0		

Command : &hAB
Meaning : DETECTOR of RF block setting2 (Initial value : 00h) → (Recommended value : 03h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	BLHOLD	To select whether to hold Bottom Long.	0 : Don't hold (Initial value) 1 : Hold
3	-		
2	DFCTT2	To set the time of DEFECT sequence.	&hAB[2:0]×68μsec (Initial value : 0h)
1	DFCTT1		
LSB	DFCTT0		

Command : &hAC
Meaning : DETECTOR of RF block setting3 (Initial value : 10h) → (Recommended value : 00h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	DETDAC TEST	DETECTOR DAC test.	0 : Normal 1 : To load &hA9[5:0]
4	CMPOT	Test of COMP output. Be sure to set up 0 when using normal operation.	0 : Normal 1 : Input from ASYterminal (DFDCK) (Initial value)
3	FOKH	To fix FOK to "H".	0 : Normal (Initial value) 1 : Fix to "H"
2	DFCTL	To fix DEFECT to "L".	0 : Normal (Initial value) 1 : Fix to "L"
1	MIRRL	To fix MIRROR to "L".	0 : Normal (Initial value) 1 : Fix to "L"
LSB	FDMIN	To input FOK, DEFECT and MIRROR signal from external terminal.	0 : Use internal signal (Initial value) 1 : Input from external terminal

Command : &hB3
Meaning : Monitor terminals I/O select (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	ANAM1 IO	To select ANA_MONI1 I/O.	0 : Input (Initial value) 1 : Output
6	ANAM0 IO	To select ANA_MONI0 I/O.	0 : Input (Initial value) 1 : Output
5	ADM1 IO	To select AD_MONI1 I/O.	0 : Input (Initial value) 1 : Output
4	ADM0 IO	To select AD_MONI0 I/O.	0 : Input (Initial value) 1 : Output
3	-		
2	-		
1	-		
LSB	-		

Command : &hB4
Meaning : Monitor terminals analog/digital select (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	ANAM1 SEL	To select digital/analog of ANA_MONI1 terminal.	0 : Digital (Initial value) 1 : Analog
6	ANAM0 SEL	To select digital/analog of ANA_MONI0 terminals.	0 : Digital (Initial value) 1 : Analog
5	ADM1 SEL	To select digital/analog of AD_MONI1 terminal.	0 : Digital (Initial value) 1 : Analog
4	ADM0 SEL	To select digital/analog of AD_MONI0 terminal.	0 : Digital (Initial value) 1 : Analog
3	-		
2	-		
1	-		
LSB	-		

Command : &hB5
Meaning : ON/OFF of pull-up resistors built in monitor terminals (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	ANAM1 PU	To turn ON/OFF of pull-up resistor built in ANA_MONI1 terminal.	0 : ON (Initial value) 1 : OFF
6	ANAM0 PU	To turn ON/OFF of pull-up resistor built in ANA_MONI0 terminal.	0 : ON (Initial value) 1 : OFF
5	ADM1 PU	To turn ON/OFF of pull-up resistor built in AD_MONI1 terminal.	0 : ON (Initial value) 1 : OFF
4	ADM0 PU	To turn ON/OFF of pull-up resistor built in AD_MONI0 terminal.	0 : ON (Initial value) 1 : OFF
3	-		
2	-		
1	-		
LSB	-		

Command : &hB6
Meaning : Select to universal output port (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	SM4	To set ANA_MONI1 terminal to universal output port.	0 : Normal (Initial value) 1 : Output &hB7[7] content
6	SM3	To set ANA_MONI0 terminal to universal output port.	0 : Normal (Initial value) 1 : Output &hB7[6] content
5	SM2	To set AD_MONI1 terminal to universal output port.	0 : Normal (Initial value) 1 : Output &hB7[5] content
4	SM1	To set AD_MONI0 terminal to universal output port.	0 : Normal (Initial value) 1 : Output &hB7[4] content
3	-		
2	-		
1	-		
LSB	-		

Command : &hB7
Meaning : Universal output register (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	TM4	To output setup value to ANA_MONI1 terminal. (Effected at command &hB6[7]=1)	0 : Output"L" (Initial value) 1 : Output"H"
6	TM3	To output setup value to ANA_MONI0 terminal. (Effected at command &hB6[6]=1)	0 : Output"L" (Initial value) 1 : Output"H"
5	TM2	To output setup value to AD_MONI1 terminal. (Effected at command &hB6[5]=1)	0 : Output"L" (Initial value) 1 : Output"H"
4	TM1	To output setup value to AD_MONI1 terminal. (Effected at command &hB6[4]=1)	0 : Output"L" (Initial value) 1 : Output"H"
3	-		
2	-		
1	-		
LSB	-		

Command : &hB8
Meaning : Select of ADC for monitors (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	-		
6	ADC1 SEL2	To select of ADC for monitors.	0h : Vc (Initial value) 1h : ANA_MONI1 2h : ANA_MONI0 3h : AD_MONI1 4h : AD_MONI0
5	ADC1 SEL1		
4	ADC1 SEL0		
3	-		
2	-		
1	-		
LSB	ADC2 SEL0	To select of ADC for monitors2.	0 : AD_MONI0 (Initial value) 1 : AD_MONI1

Command : &hC0
Meaning : Focus ON and servo test setting (Initial value : 00h) → (Recommended value : 10h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	FON1	To execute focus ON.	0 : OFF (Initial value) 1 : ON 2 : Microcomputer control (with &hC8[7:0] comand)
4	FON0		
3	-		
2	-		
1	FDEFON	DEFECT forced ON/OFF. (To use for the test)	0 : OFF (Initial value) 1 : ON
LSB	FSERVON	Servo forced ON/OFF. (To use for the test)	0 : OFF (Initial value) 1 : ON

Command : &hC1
Meaning : Tracking ON and sled ON (Initial value : 00h) → (Recommended value : 11h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	TRM1	To execute tracking ON.	0 : OFF (Initial value) 1 : Tracking servo ON 2 : Forced foward 3 : Forced reverse
4	TRM0		
3	-		
2	-		
1	SDM1	To execute sled ON.	0 : OFF (Initial value) 1 : Sled servo ON 2 : Forced foward 3 : Forced reverse
LSB	SDM0		

Command : &hC4
Meaning : Execution of track jumping to the forward direction (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	TJF7	To execute track jumping to the forward direction. For the detail, refet to “Description of Tr Jump Sequence”. The related commands are as follows. &hCB[7:6] : to set brake pulse length per 1 track jump. &hCB[5] : to set multi-track jump mode. &hCB[4] : to set track number count signal under multi-track jump mode. &hCC[7:4] : to set blind time during track jump. &hCC[3:0] : to set over flow during track jump. &hCD[6:0] : to set long sled kick time during track jump. &hFD[7:4], [3:0] : to set track jump pulse height.	In the case of &hC4[7:0]=00h, 1 track jumping is executed. (Initial value) In other cases, multi-track jumping executed. When the command is &hCB[5]=0 (Mode1), accelerative pulse is outputted between &hC4[7:0] tracks. When the command is &hCB[5]=1 (Mode2), the jump to which accelerative pulse is outputted only between 8 tracks is repeated up to frequency which is set by &hC4[7:3].
6	TJF6		
5	TJF5		
4	TJF4		
3	TJF3		
2	TJF2		
1	TJF1		
LSB	TJF0		

Command : &hC5
Meaning : Execution of “sled move” to the forward direction (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	SJF7	To execute “sled move” to the forward direction. For the detail, refer to “Description of Sled Move Sequence”. The related commands are follows. &hCB[4] : to set track number count signal under multi-track jump mode. &hFE[7:4] : to set sled pulse height.	Accelerative pulse is outputted between the tracks set up by &hC5[7:0]×128.
6	SJF6		
5	SJF5		
4	SJF4		
3	SJF3		
2	SJF2		
1	SJF1		
LSB	SJF0		

Command : &hC6
Meaning : Execution of track jumping to the reverse direction (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	TJR7	To execute track jumping to the reverse direction. For the detail, refer to “Description of Tr Jump Sequence”. The related commands are as follows. &hCB[7:6] : to set brake pulse length per 1 track jump. &hCB[5] : to set multi-track jump mode. &hCB[4] : to set track number count signal under multi-track jump mode. &hCC[7:4] : to set blind time during track jump. &hCC[3:0] : to set over frow during track jump. &hCD[6:0] : to set long sled kick time during track jump. &hFD[7:4],[3:0] : to set track jump pulse height.	In the case of &hC6[7:0]=00h, 1 track jumping is executed. (Initial value) In other cases, multi-track jumping executed. When the command is &hCB[5]=0 (Mode1), decelerative pulse is outputted between &hC6[7:0] tracks. When the command is &hCB[5]=1 (Mode2), the jump to which decelerative pulse is outputted only between 8 tracks is repeated up to frequency which is set by &hC6[7:3].
6	TJR6		
5	TJR5		
4	TJR4		
3	TJR3		
2	TJR2		
1	TJR1		
LSB	TJR0		

Command : &hC7
Meaning : Execution of “Sled move” to the reverse direction (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	SJR7	To execution of “Sled move” to the reverse direction. For the detail, refer to “Description of Sled Move Sequence”. The related commands are follows. &hCB[4] : to set track number count signal under multi-track jump mode. &hFE[7:4] : to set sled pulse height.	Decelerative pulse is outputted between the tracks set up by &hC7[7:0]×128.
6	SJR6		
5	SJR5		
4	SJR4		
3	SJR3		
2	SJR2		
1	SJR1		
LSB	SJR0		

Command : &hC8
Meaning : Focus search voltage setting (Initial value : 00h) → (Recommended value : 48h)

Bit	Command code	Meaning	Status
MSB	FSMAX3	Max value of focus seach voltage (Vc standard, positive side).	&hC8[7:4] ×8×V_{DD}×0.8 / 256 [V] (Initial value : 0h)
6	FSMAX2		
5	FSMAX1		
4	FSMAX0		
3	FSMIN3	Minimum value of focus search voltage (Vc standard, negative side).	&hC8[3:0] ×8×V_{DD}×0.8 / 256 [V] (Initial value : 0h)
2	FSMIN2		
1	FSMIN1		
LSB	FSMIN0		

Command : &hC9
Meaning : Focus loop setting (Initial value : 00h) → (Recommended value : 33h)

Bit	Command code	Meaning	Status
MSB	FZCDM	Wherther to turn ON the focus loop by inverted S shape.	0 : Turn ON (Initial value) 1 : Not TurnON
6	FSTP2	The time spent for 1-step increment of search voltage.	&hC9[6:4] ×8×272 [µsec] (Initial value : 0h)
5	FSTP1		
4	FSTP0		
3	-		
2	FSTN2	The time spent for 1-step decrement of search voltage.	&hC9[2:0] ×8×272 [µsec] (Initial value : 0h)
1	FSTN1		
LSB	FSTN0		

Command : &hCA
Meaning : Focus loop and recomvery (Initial value : 00h) → (Recommended value : 26h)

Bit	Command code	Meaning	Status
MSB	-		
6	FSLO2	The time until focus loop turns OFF after FOK came to “L”.	&hCA[6:4] ×272 [µsec] (Warning)1h is prhibited (Initial value : 0h)
5	FSLO1		
4	FSLO0		
3	FSRV3	Focus recovery start voltage.	&hCA[3:0] ×4×V_{DD}×0.8/256 [V] (Initial value : 0h)
2	FSRV2		
1	FSRV1		
LSB	FSRV0		

Command : &hCB
Meaning : Track jump setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	TR1W1	The output time of the inverted voltage pulse at 1 track jump.	0 : ×0.5 (Initial value) 1 : ×0.625 2 : ×0.75 3 : ×1.0
6	TR1W0		
5	TRMM	To set multi-track jump mode.	0 : Mode 1 (Initial value) 1 : Mode 2
4	TRMCS	To select track number count signal in multi-track jumping.	0 : COUT (Initial value) 1 : TZC
3	TRTZC3	To set the time to switch track number count signal to TZC in track jumping.	&hCB[3:0] ×2×5.67 [µsec] (Initial value : 0h)
2	TRTZC2		
1	TRTZC1		
LSB	TRTZC0		

Command : &hCC
Meaning : Under track jump mode, blind time and overflow time setting (Initial value : 00h) → (Recommended value : 36h)

Bit	Command code	Meaning	Status
MSB	TRBT3	To set blind time under track jump mode.	&hCC[7:4]×2×5.67 [µsec] (Initial value : 0h)
6	TRBT2		
5	TRBT1		
4	TRBT0		
3	TROT3	Overflow time under track jump mode.	&hCC[3:0]×2×5.67 [µsec] (Initial value : 0h)
2	TROT2		
1	TROT1		
LSB	TROT0		

Command : &hCD
Meaning : Long sled kick time under track jump mode (Initial value : 00h) → (Recommended value : 20h)

Bit	Command code	Meaning	Status
MSB	-		
6	TRLST6	Long sled kick time under track jump mode.	&hCD[6:0] ×272 [µsec] (Initial value : 00h)
5	TRLST5		
4	TRLST4		
3	TRLST3		
2	TRLST2		
1	TRLST1		
LSB	TRLST0		

Command : &hCE
Meaning : Forced-brake, forced-gain-up and anti-shock setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	TJBRK	Forced brake ON or OFF	0 : OFF (Initial value) 1 : ON
6	TJGUP	Forced gain-up ON or OFF.	0 : OFF (Initial value) 1 : ON
5	ATS	Anti-shock mode ON or OFF.	0 : ON (Initial value) 1 : OFF
4	SLDCLR	Whether to clear sled filter at track jumping, sled OFF and focus failure.	0 : Clear (Initial value) 1 : Don't clear
3	MIRRSEL	Tracking OFF & LPF Reset, when MIRROR is "H".	0 : To be (Initial value) 1 : Not to be
2	-		
1	-		
LSB	-		

Command : &hCF
Meaning : Other servo setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	SDMODE	Intermittent sled ON/OFF	0 : ON (Initial value) 1 : OFF
6	SDGFSG	To select sled GFS guard.	0 : ON (Initial value) 1 : OFF
5	FSVC	Whether to clear focus search voltage	0 : Clear (Initial value) 1 : Don't clear
4	FRCBRK	Whether to brake after focus recovery.	0 : Don't brake (Initial value) 1 : Brake
3	FTR GAIRAN	Foced tracking gairan ON or OFF.	0 : OFF (Initial value) 1 : ON
2	-		
1	-		
LSB	-		

Command : &hD0
Meaning : Various measurement for auto adjustment (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	ADJ3	To execute each measurement.	0h : (Initial value) 1h : SDOUToffset measurement 2h : FDOUT offset measurement 3h : TDOUT offset measurement 4h : AC amplifier offset measurement 5h : BD amplifier offset measurement 6h : E amplifier offset measurement 7h : F amplifier offset measurement 8h : Focus balance measurement 9h : Tracking balance measurement Ah : Focus gain measurement Bh : Tracking gain measurement Ch : RF measurement Eh : VCO measurement
6	ADJ2		
5	ADJ1		
4	ADJ0		
3	-		
2	-		
1	-		
LSB	-		

Command : &hD1
Meaning : Sled gain measurement for auto adjustment. (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	SGADJ	To execute measurement of Sled gain.	0 : Normal (Initial value) 1 : Sled gain measurement
3	-		
2	-		
1	-		
LSB	-		

Command : &hD2
Meaning : Wait time for measurement for auto adjustment Initial value : 00h) → (Recommended value : FFh)

Bit	Command code	Meaning	Status
MSB	WAIT3	Wait time for auto adjustment.	&hD2[7:4] ×16×272 [µsec] (Initial value : 0h)
6	WAIT2		
5	WAIT1		
4	WAIT0		
3	ADJT3	MAX/MIN measurement time.	&hD2[3:0] ×16×272 [µsec] (Initial value : 0h)
2	ADJT2		
1	ADJT1		
LSB	ADJT0		

Command : &hD3
Meaning : Tracking error cycle setting, incurred by tracking balance measurement
(Initial value : 00h)) → (Recommended value : 38h)

Bit	Command code	Meaning	Status
MSB	TBMIN3	To set the lower limit of tracking error cycle when measurening tracking balance.	&hD3[7:4] ×8×5.67×2 [µsec] (Initial value : 0h)
6	TBMIN2		
5	TBMIN1		
4	TBMIN0		
3	TBMAX3	To set the upper limit of tracking error cycle when measurening tracking balance.	&hD3[3:0] ×8×5.67×2 [µsec] (Initial value : 0h)
2	TBMAX2		
1	TBMAX1		
LSB	TBMAX0		

Command : &hD4
Meaning : Number of tracking errors until the specific requirements are met, during tracking balance measuremet.
(Initial value : 00h) → (Recommended value : 30h)

Bit	Command code	Meaning	Status
MSB	TBN3	To set the lower limit of tracking error cycle when measuring tracking balance.	&hD4[7:4] ×8 (Initial value : 0h)
6	TBN2		
5	TBN1		
4	TBN0		
3	ADJNG1	To set measurement NG conditions. NG if signal selected herein comes to “L” during measurement.	0 : LOCK (Initial value) 1 : GFS88 2 : Nothing 3 : Nothing
2	ADJNG0		
1	MEGAIN	To select the measurement mode. (A)To set gain measurement section. (B)Rfmeasurement setting. (C)Balance measurement setting.	(A) 0 : Until “disturbance” down come 1 : Until “disturbance” rise (B) 0 : Disable at focus failure 1 : Enable at focus failure (C) 0 : Conventional method 1 : MAX/MIN measurement (&hD2[3 : 0])
LSB	TDON	Forced TDOUT mode.	0 : OFF (Initial value) 1 : ON

Command : &hD5
Meaning : Read signal by &hDE command selection (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	-		
3	-		
2	-		
1	DESEL1	To select the read signal by &hDE command.	0 : Normal (MAX) (Initial value) 1 : MIN 2 : (E+F)/ (AC+BD) (MAX) 3 : (E+F)/ (AC+BD) (MIN)
LSB	DESEL0		

Command : &hD6
Meaning : DEFECT,NEW_DEFECT setting 1 (Initial value : 00h) → (Recommended value : 66h)

Bit	Command code	Meaning	Status
MSB	FDEFM D1	To select FOCUS STATUS against DEFECT.	0 : No countermeasure (Initial value) 1 : Hold 2 : Gain down
6	FDEFM D0		
5	FNEFM D1	To select FOCUS STATUS against NEW_DEFECT.	0 : No countermeasure (Initial value) 1 : Hold 2 : Gain down
4	FNEFM D0		
3	TDEFM D1	To select TRACKING STATUS against DEFECT.	0 : No countermeasure (Initial value) 1 : Hold 2 : Gain down
2	TDEFM D0		
1	TNEFM D1	To select TRACKING STATUS against NEW_DEFECT.	0 : No countermeasure (Initial value) 1 : Hold 2 : Gain down
LSB	TNEFM D0		

Command : &hD7
Meaning : DEFECT,NEW_DEFECT setting 2 (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	-		
6	TJHSEL	To select HOLD at track jumping.	0 : BPF/Through OFF (Initial value) 1 : BPF OFF+Through ←LPF
5	HSEL1	To select HOLD against DEFECT/NEW_DEFECT.	0 : BPF/Through OFF (Initial value) 1 : BPF OFF+Through←LPF 2 : BPF/Through ←LPF 3 : BPF OFF+Through←LPF+LPF hold
4	HSEL0		
3	-		
2	-		
1	-		
LSB	-		

Command : &hD8
Meaning : Servo sequencer test setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	SQTST5	To set servo sequencer test.	0h : Normal Other : Test mode (Initial value : 0h)
4	SQTST4		
3	SQTST3		
2	SQTST2		
1	SQTST1		
LSB	SQTST0		

Command : &hD9
Meaning : Servo sequencer monitor signal select, counter test (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	-		
6	SQ MONI2	To select servo sequencer monitor signal [7:0]. It can be read using command &hDE. Furthermore, the monitor signals can be output from monitor terminals by selecting STATUS by command &hB0[7:4] and sending command &hDE01. (However, at this time, the commands used for output shall be &hEE00.) Send &hDE00 for returning to normal STATUS.	0 : cnt2 (&hD5=0),comp_reg2 (&hD5=1) comp_reg3 (&hD5=2),comp_reg4 (&hD5=3) 1 : fsearch_cnt 2 : 00,p_reg[5:0] 3 : fhpfoff,fhpfdown,fthroff,fhpfsel,fthrsel, flpf_hold,fmuto,f_gairan_on 4 : tmuti,thpfoff,thpfdown,tthroff,thpfsel, tthrsel,tlpf_hold,tmuto 5 : t_gairan_on,smuti,sfclr,00000 6 : tj_sel[1:0],sd_sel[1:0],fzc_frd,000
5	SQ MONI1		
4	SQ MONI0		
3	-		
2	-		
1	SQC TST1	Counter test of servo sequencer.	0 : Normal (Initial value) Other : Test mode
LSB	SQC TST0		

Command : &hDE
Meaning : Address for reading the result of measurement for auto adjustment and servo sequencer monitor signals (Exclusive for reading)

Bit	Command code	Meaning	Status
MSB	SQSTA7	Commands to read the result of measurement for auto adjustment which was executed by command &hD0[7:4] and &hD1[4] or moitor signals selected by command &hD9[6:4]. Furthermore, the monitor signals can be output from monitor terminals by selecting STATUS by command &hB0[7:4] and sending command &hDE01. (However, at this time the commands used for output shallbe &hEE00.) Send &hDE00 for returning to normal STATUS.	
6	SQSTA6		
5	SQSTA5		
4	SQSTA4		
3	SQSTA3		
2	SQSTA2		
1	SQSTA1		
LSB	SQSTA0		

Command : &hE8
Meaning : Focus LPF and HPF gain setting (Initial value : 00h) → (Recommended value : 4Bh)

Bit	Command code	Meaning	Status
MSB	FLG3	To set focus LPF gain.	&hE8[7:4]multiple (Initial value : 0h)
6	FLG2		
5	FLG1		
4	FLG0		
3	FHG3	To set focus HPF gain.	&hE8[3:0] ×2 (Initial value : 0h)
2	FHG2		
1	FHG1		
LSB	FHG0		

Command : &hE9
Meaning : Focus LPS setting, LPF cut-off, BPF peak setting (Initial value : 00h) → (Recommended value : 71h)

Bit	Command code	Meaning	Status
MSB	FLPSF1	To set focus LPS cut-off frequency.	0 : 15.4Hz (Initial value) 1 : 6.7Hz 2 : 3.41Hz
6	FLPSF0		
5	FLPSG1	To set focus LPS attenuation level.	0 : Through (Initial value) 1 : ×0.09 2 : ×0.18 3 : ×0.36
4	FLPSG0		
3	FLPFF1	To set focus LPF cut-off frequency.	0 : 188Hz (Initial value) 1 : 15.45Hz 2 : 6.87Hz 3 : 3.44Hz
2	FLPFF0		
1	FBPFF1	To set focus BPF peak frequency.	0 : 2kHz (Initial value) 1 : 1kHz 2 : 600Hz
LSB	FBPFF0		

Command : &hEA
Meaning : Tracking LPF and HPF gain setting (Initial value : 00h) → (Recommended value : 4Bh)

Bit	Command code	Meaning	Status
MSB	TLG3	To set tracking LPF gain.	&hEA[7:4] multiple (Initial value : 0h)
6	TLG2		
5	TLG1		
4	TLG0		
3	THG3	To set tracking HPF gain.	&hEA[3:0] ×2 multiple (Initial value : 0h)
2	THG2		
1	THG1		
LSB	THG0		

Command : &hEB
Meaning : Tracking LPS setting, LPF cut-off, and BPF peak setting
(Initial value : 00h) → (Recommended value : 41h)

Bit	Command code	Meaning	Status
MSB	TLPSF1	To set tracking LPS cut-off frequency.	0 : 15.4Hz (Initial value) 1 : 6.7Hz 2 : 3.41Hz
6	TLPSF0		
5	TLPSG1	To set tracking LPS attenuate level.	0 : Through (Initial value) 1 : ×0.09 2 : ×0.18 3 : ×0.36
4	TLPSG0		
3	TLPFF1	To set tracking LPF cut-off frequency.	0 : 188Hz (Initial value) 1 : 15.45Hz 2 : 6.87Hz 3 : 3.44Hz
2	TLPFF0		
1	TBPFF1	To set tracking BPF peak frequency.	0 : 2kHz (Initial value) 1 : 1kHz 2 : 600Hz
LSB	TBPFF0		

Command : &hEC
Meaning : Focus, tracking gain setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	TGDW1	To set tracking gain-down level.	0 : ×1 (Initial value) 1 : ×0.5 2 : ×0.25 3 : ×0
6	TGDW0		
5	TGUP1	To set tracking gain-up level.	0 : ×1 (Initial value) 1 : ×1.5 2 : ×2 3 : ×3
4	TGUP0		
3	FTG1	To set focus total gain.	0 : ×1 (Initial value) 1 : ×2 2 : ×4 3 : ×8
2	FTG0		
1	TTG1	To set tracking total gain.	0 : ×1 (Initial value) 1 : ×2 2 : ×4 3 : ×8
LSB	TTG0		

Command : &hED
Meaning : “Disturvance” setting (Initial value : 00h) → (Recommended value : 08h)

Bit	Command code	Meaning	Status
MSB	OSCF1	To select disturbance frequency. (For measurement gain/focus balance)	0 : 1kHz/500Hz (Initial value) 1 : 1.6kHz/660Hz 2 : 1.33kHz/350Hz 3 : 10Hz (Only using for tracking balance measurement)
6	OSCF0		
5	OSCG5	To set disturbance level.	&hED[5:0]/32 multiple (Initial value : 00h)
4	OSCG4		
3	OSCG3		
2	OSCG2		
1	OSCG1		
LSB	OSCG0		

Command : &hEE
Meaning : Addresses for reading servo and DF monitor signals (Exclusive reading)

Bit	Command code	Meaning	Status
MSB	DFSTA7	Commands to read signals [12:5] selected by command &hFA[7:4]. Furthermore, the monitor signals [12:0] can be output from monitor terminals by selecting STATUS by command &hB0[7:4] and sending command &hEE01. (However, at this time the commands used for output shall be &hDE00.) Send &hEE00 for returning to normal STATUS.	
6	DFSTA6		
5	DFSTA5		
4	DFSTA4		
3	DFSTA3		
2	DFSTA2		
1	DFSTA1		
LSB	DFSTA0		

Command : &hEF
Meaning : Servo DF RAM clear, AD converter input test , Disturbance clear, TE gain-down level,focus gain-down level, sled setting (Initial value : C0h) → (Recommended value : 00h)

Bit	Command code	Meaning	Status
MSB	RAM CLR	RAM clear. Be sure to set up 0 when using normal operation.	0 : Normal 1 : RAM clear (Initial value)
6	ADCTEST	AD converter input test. Be sure to set up 0 when using normal operation.	0 : Normal 1 : Test (Initial value)
5	GAIR CLR	Disturbance clear.	0 : Normal (Initial value) 1 : Disturbance clear.
4	SLEDF	Focus gain-down level.	0 : ×0.5 (Initial value) 1 : ×0
3	TSN	To select Tracking servo noise shiver.	0 : OFF (Initial value) 1 : ON
2	FSN	To select Tracking servo noise shiver.	0 : OFF (Initial value) 1 : ON
1	PBLP	To set the frequency of Peak/Bottom Long.	0 : 115Hz (Initial value) 1 : 230Hz
LSB	MDAC TEST	Monitor DAC test.	0 : Normal (Initial value) 1 : &h88[7 : 0] setup value is loaded

Command : &hF0
Meaning : Intermittent sled ON level setting (Initial value : 00h) → (Recommended value : 40h)

Bit	Command code	Meaning	Status
MSB	-		
6	STH6	To set intermittent sled ON level. Effective when command is &hCF[7]=0.	&hF0[6:0] ×V_{DD}×0.8 / 256 [V] (Initial value : 00h)
5	STH5		
4	STH4		
3	STH3		
2	STH2		
1	STH1		
LSB	STH0		

Command : &hF1
Meaning : Intermittent sled OFF level setting (Initial value : 00h) → (Recommended value : 30h)

Bit	Command code	Meaning	Status
MSB	-		
6	STL6	To set intermittent sled OFF level. Effective when command is &hCF[7]=0.	&hF1[6:0] $\times V_{DD} \times 0.8 / 256$ [V] (Initial value : 00h)
5	STL5		
4	STL4		
3	STL3		
2	STL2		
1	STL1		
LSB	STL0		

Command : &hF2
Meaning : FZC comparison level (Initial value : 00h) → (Recommended value : 63h)

Bit	Command code	Meaning	Status
MSB	FZCTH3	FZC H side comparison level.	&hF2[7:4] $\times 8 \times V_{DD} \times 0.8 / 256$ [V] (Initial value : 0h)
6	FZCTH2		
5	FZCTH1		
4	FZCTH0		
3	FZCTL3	FZC L side comparison level.	&hF2[3:0] $\times 8 \times V_{DD} \times 0.8 / 256$ [V] (Initial value : 0h)
2	FZCTL2		
1	FZCTL1		
LSB	FZCTL0		

Command : &hF3
Meaning : Anti-shock comparison level setting (Initial value : 00h) → (Recommended value : 40h)

Bit	Command code	Meaning	Status
MSB	ANT LEV3	To set anti-shock comparison level.	&hF3[7:4] ×2×V_{DD}×0.8/256 [V] (Initial value : 0h)
6	ANT LEV2		
5	ANT LEV1		
4	ANT LEV0		
3	-		
2	-		
1	TLPF RIMIT1	To set Tracking LPF rimit.	0 : Nothing(Initial value) 1 : 1/1 2 : 1/2 3 : 1/4
LSB	TLPF RIMIT0		

Command : &hF4
Meaning : Sled gain setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	SLG7	To set sled filter gain.	&hF4[7:0] /4 multiple (Initial value : 00h)
6	SLG6		
5	SLG5		
4	SLG4		
3	SLG3		
2	SLG2		
1	SLG1		
LSB	SLG0		

Command : &hF5
Meaning : Sled LPS setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	-		
4	-		
3	-		
2	SLPS2	To set sled filter LPS.	&hF5[2:0] × (-3dB) (At time of 0, it is 188Hz LPF) (Initial value : 0h)
1	SLPS1		
LSB	SLPS0		

Command : &hF6
Meaning : FE offset, TE offset setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	-		
6	FEOFS2	To set FE offset.	&hF6[6:4] ×V_{DD}×0.8/16 [V] (Initial value : 0h)
5	FEOFS1		
4	FEOFS0		
3	-		
2	TEOFS2	To set TE offset.	&hF6[2:0] ×V_{DD}×0.8/16 [V] (Initial value : 0h)
1	TEOFS1		
LSB	TEOFS0		

Command : &hF7
Meaning : TZC filter and HPF (E+F) settings (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	EAFG3	To set SBAD HPF (E+F) gain.	&hF7[7:4]/16 multiple (Initial value:0h)
6	EAFG2		
5	EAFG1		
4	EAFG0		
3	EAF1	To set HPF (E+F) cutoff frequency.	0 : 8kHz(Initial value) 1 : 4kHz 2 : 2kHz
2	EAF0		
1	TZC1	To set TZC filter.	0 : 4.51kHz (Initial value) 1 : 2.12kHz 2 : 0.96kHz
LSB	TZC0		

Command : &hF8
Meaning : EF gain-down setting (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	-		
6	EGDW2	E gain-down value under DEFECT.	-2×&hF8[6:4]dB However, if &hF8[6:4]=7, Gain-down value is ×0 multiple. (Initial value:0h)
5	EGDW1		
4	EGDW0		
3	-		
2	FGDW2	F gain-down value under DEFECT.	-2×&hF8[2:0]dB However, if &hF8[2:0]=7, Gain-down value is ×0 multiple. (Initial value:0h)
1	FGDW1		
LSB	FGDW0		

Command : &hF9
Meaning : TE gain-down setting (Initial value : 0Fh)

Bit	Command code	Meaning	Status
MSB	-		
6	-		
5	TEGDW1	TE gain down value under DEFECT.	0 : ×1(Initial value) 1 : ×0.5 2 : ×0
4	TEGDW0		
3	TDOFF3	To set TDOUT offset setting.	Add no offset at &hF9[3:0]=Fh. Add maximum offset at &hF9[3:0]=7h. Add minimum offset at &hF9[3:0]=8h. (Initial value:Fh)
2	TDOFF2		
1	TDOFF1		
LSB	TDOFF0		

Command : &hFA
Meaning : Monitor signal select (Initial value : 00h)

Bit	Command code	Meaning	Status
MSB	MONISG3	To select monitor signal.	0:adc_ch2_dlaatch_out[7:0],0_0000(Initial value) 1:dac_louta,dac_loutb,dac_routa,dac_routb,000 2:servodacin[7:0],0_0000 3:adout[9:0],ad_lat[5:3] 4:adout[9:0],ad_lat[2:0] 5:moni_in,0_0000 6:peak_long,000_0000 7:botm_long,000_0000 8:clv_cnt,00 9:pp_cnt,00 A:pc_cnt,00 B:pwm_in_1d[7], to pwm_iin_1d[6:0],0_0000 C:tlpf_latch[3:0],0_0000_0000 D:audio_test_moni[7:0],0_0000 (ref. &h4F[0]) E:adc_dlat_data[9:0],000
6	MONISG2		
5	MONISG1		
4	MONISG0		
3	ANADAC3	To select monitor signals form ANA_MONI1 and ANA_MONI0 terminal.	ANA_MONI1 / ANA_MONI0 0 : TE/FE (Initial value) 1 : LPF/SLED_HPF 2 : TZC/RFRP 3 : PL/BL 4 : BS/PS 5 : PL/PS 6 : BS/BL 7 : TE/HPF (E+F) 8 : - / SLED
2	ANADAC2		
1	ANADAC1		
LSB	ANADAC0		

Command : &hFB
Meaning : Asymmetry offset setting (Initial value : 80h)

Bit	Command code	Meaning	Status
MSB	ASYOFS 7	To set asymmetry offset. Center value 80h because of offset binary.	(Initial value : 80h)
6	ASYOFS 6		
5	ASYOFS 5		
4	ASYOFS 4		
3	ASYOFS 3		
2	ASYOFS 2		
1	ASYOFS 1		
LSB	ASYOFS 0		

Command : &hFC
Meaning : Track jump addition ratio (Initial value : 80h)

Bit	Command code	Meaning	Status
MSB	TJADD3	Track jump addition ratio.	&hFC[7:4]/8 multiple (Initial value : 8h)
6	TJADD2		
5	TJADD1		
4	TJADD0		
3	-		
2	-		
1	-		
LSB	-		

Command : &hFD
Meaning : Tracking jump height setting (Initial value : 00h) → (Recommended value : 44h)

Bit	Command code	Meaning	Status
MSB	THA3	Pulse height of tracking jump acceleration side (higher than Vc).	&hFD[7:4] ×8×V_{DD}×0.8 / 256 [V] (Initial value : 0h)
6	THA2		
5	THA1		
4	THA0		
3	THB3	Pulse height of tracking jump deceleration side (lower than Vc).	&hFD[3:0] ×8×V_{DD}×0.8 / 256 [V] (Initial value : 0h)
2	THB2		
1	THB1		
LSB	THB0		

Command : &hFE
Meaning : Sled pulse height setting (Initial value : 00h) → (Recommended value : 80h)

Bit	Command code	Meaning	Status
MSB	SH3	Sled pulse height.	&hFE[7:4] ×8×V_{DD}×0.8 / 256 [V] (Initial value : 0h)
6	SH2		
5	SH1		
4	SH0		
3	-		
2	-		
1	-		
LSB	-		

18. General-Purpose A/D Converter

18.1. Features

- ◇ Successive Approximation 10-bit ADC
- ◇ Analog Input Channels Up to 8 Channels
- ◇ Supports two data output formats (straight binary and binary 2's complement)
- ◇ Built-in Power-Down Function
- ◇ Analog Input Voltage Range: 0.75 ± 0.60V (Typ)
- ◇ Conversion Rate: 736 ksps (Max)
- ◇ DNL: ±5 LSB (Max), INL: ±5 LSB (Max)

18.2. Description

18.2.1. Block Diagram

The following figure shows a block diagram of this A/D converter.

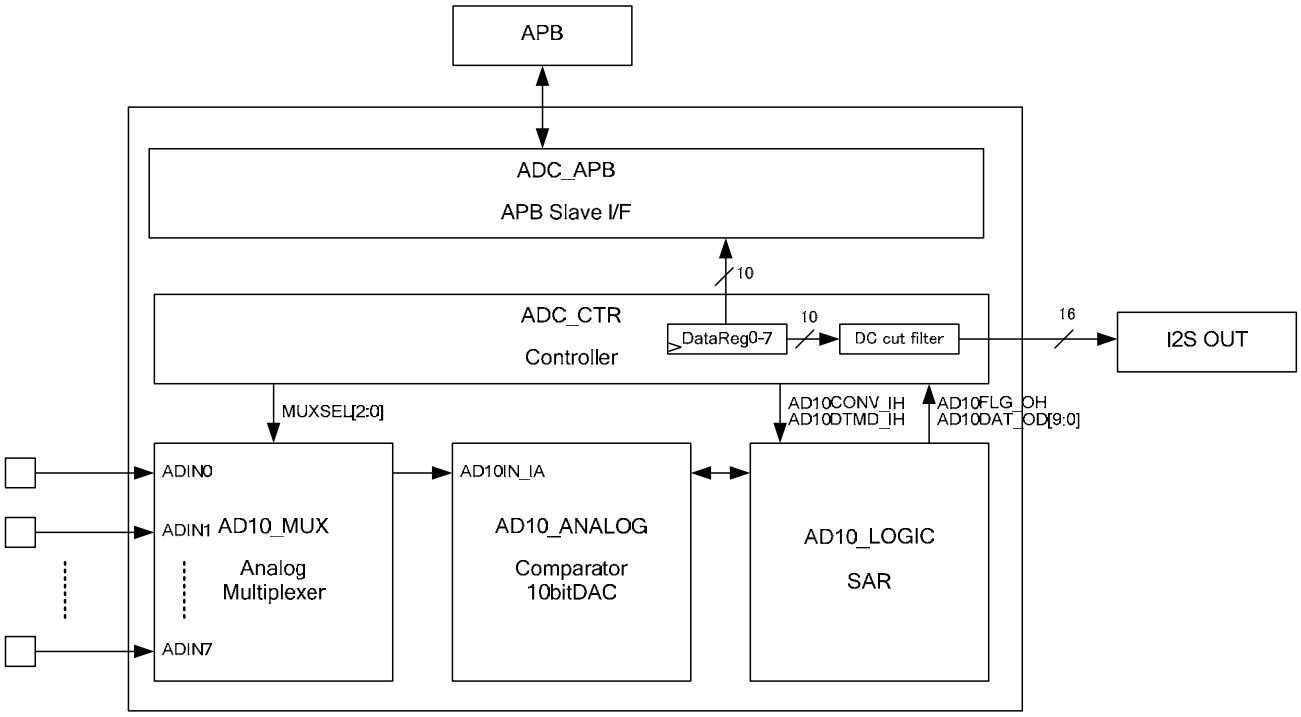


Figure 133. Block Diagram

18.2.2. Basic Operation

Operation setting is started from APB.
According to the control of the controller, the analog multiplexer selects input channels.
Data after A/D conversion is saved in the register (Data Reg) by input channel.
APB reads the data after A/D conversion.

18.2.3. Input Channel Setting

The controller conducts A/D conversions by repeating the conversion sequence from Conversion Slots 0 to 7.
The controller conducts a single A/D conversion per one conversion slot.
Input channel setting for each conversion slot can be made by making register setting.

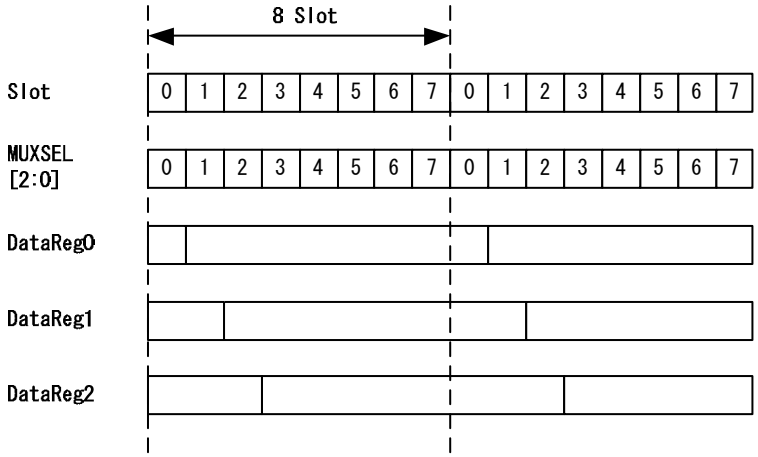


Figure 134

18.2.4. Data Output Coding Setting

Data output coding setting can be made by making register setting.
This A/D converter supports two data output formats (straight binary and binary 2's complement).
Figure 135 and Figure 136 show the theoretical transmission characteristics of the formats, respectively.

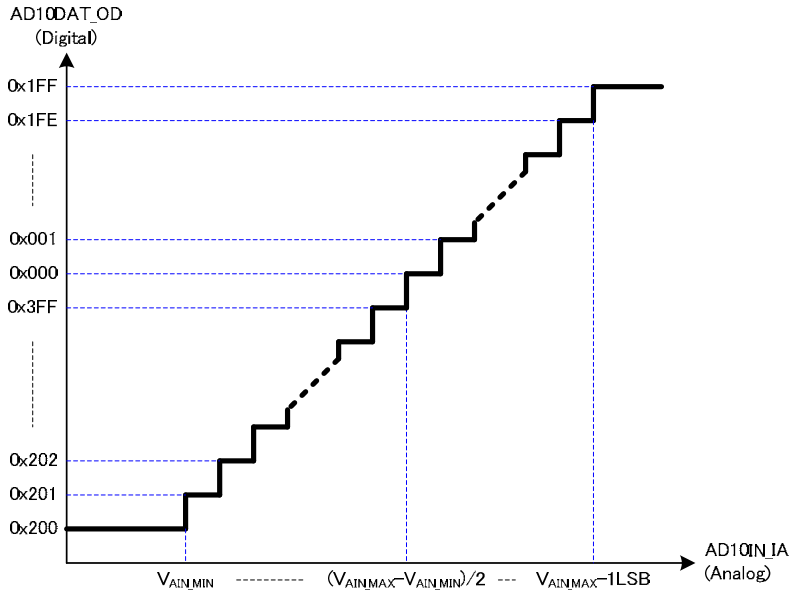


Figure 135. Transmission Characteristics of Binary 2's Complement (Midscale: 0x000)

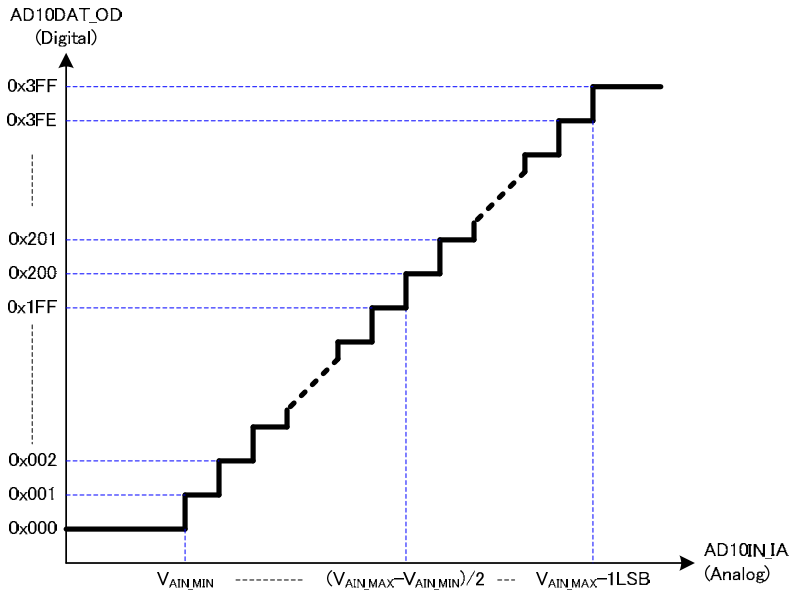


Figure 136. Transmission Characteristics of Straight Binary

18.2.5. Data Output to I2S Output Block

Data of Conversion Slots 0 and 4 out of the eight conversion slots are outputted to the DC cut filter one after another. Filtered 16-bit data are outputted to the I2S output block.

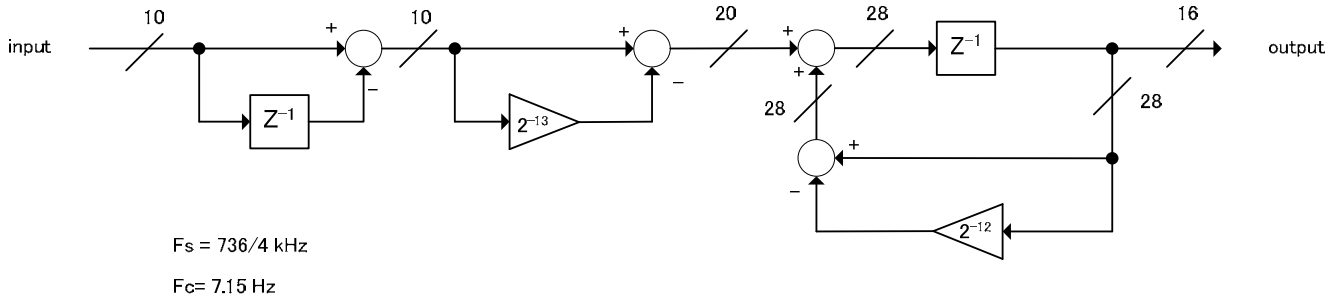


Figure 137. DC Cut Filter

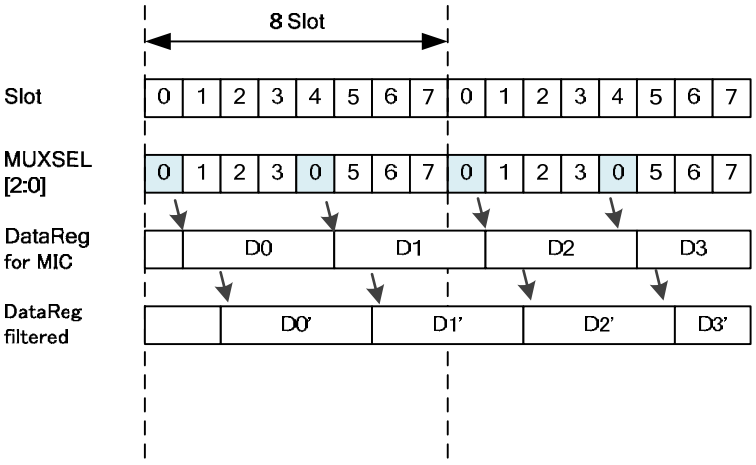


Figure 138. Data Output Sequence to the I2S Output Block

18.3. I/O Signals

Pin Name	I/O	Function	Destination
pclk	in	APB Clock	CLOCKGEN
presetn	in	APB Reset (Active Low)	RESETGEN
psel	in	APB Peripheral Select Signal	APB
paddr[7:0]	in	APB Address	APB
pwdata[31:0]	in	APB Write Data	APB
pwrite	in	APB Write Signal	APB
penable	in	APB Enable Signal	APB
prdata[31:0]	out	APB Read Data	APB
adcdata_reb	in	Data Read Request Signal	I2SOUT
adcdata_hold [15:0]	out	Add Data / Analog-Digital Data	I2SOUT
ADIN0	in	ADC Analog Input (0)	EXT I/O
ADIN1	in	ADC Analog Input (1)	EXT I/O
ADIN2	in	ADC Analog Input (2)	EXT I/O
ADIN3	in	ADC Analog Input (3)	EXT I/O
ADIN4	in	ADC Analog Input (4)	EXT I/O
ADIN5	in	ADC Analog Input (5)	EXT I/O
ADIN6	in	ADC Analog Input (6)	EXT I/O
ADIN7	in	ADC Analog Input (7)	EXT I/O
AD10CLK_IR	in	ADC Core Clock	CLOCKGEN
AD10PD_IL	in	ADC Core Power-Down	POWER
AD10RST_IL	in	ADC Core Reset	RESETGEN

18.4. Register

18.4.1. Memory Map

Name	Description	Address Offset	Width	Reset
SET_CTRL	Controller Operation Enable Setting	0x00	4	0
SET_CH	Input Channel Setting of Each Conversion Slot	0x04	32	0
SET_DTMD	Data Output Format Setting of Each Conversion Slot	0x08	8	0
SLOT0_DAT	Data of Each Conversion Slot After A/D Conversion	0x0C	10	0
SLOT1_DAT	Data of Each Conversion Slot After A/D Conversion	0x10	10	0
SLOT2_DAT	Data of Each Conversion Slot After A/D Conversion	0x14	10	0
SLOT3_DAT	Data of Each Conversion Slot After A/D Conversion	0x18	10	0
SLOT4_DAT	Data of Each Conversion Slot After A/D Conversion	0x1C	10	0
SLOT5_DAT	Data of Each Conversion Slot After A/D Conversion	0x20	10	0
SLOT6_DAT	Data of Each Conversion Slot After A/D Conversion	0x24	10	0
SLOT7_DAT	Data of Each Conversion Slot After A/D Conversion	0x28	10	0

18.4.2. Register Detail

SET_CTRL
Controller Operation Enable Setting
Offset: 0x00
Width: 4 bits

Bits	Name	Direction	Reset	Description
31:4	-	N/A	0x0	Reserved
3:2	filter_sel	R/W	0x0	Filter Selection 0x00: DC Cut Filter 0x01: 4-Sample Mean Filter 0x02: No Filter 0x03 : DC Cut Filter +4 Sample Average
1	out_sel	R/W	0x0	Data Output to the I2S Output Block 0: OFF 1: ON
0	adc_ctr	R/W	0x0	ADC_CTR Operation Control 0: Operation OFF 1: Operation ON

SET_CH
Input Channel Setting of Each Conversion Slot
Offset: 0x04
Width: 32 bits

Bits	Name	Direction	Reset	Description
31:28	set_ch7	R/W	0x0	Input Channel Setting of Conversion Slot 7
27:24	set_ch6	R/W	0x0	Input Channel Setting of Conversion Slot 6
23:20	set_ch5	R/W	0x0	Input Channel Setting of Conversion Slot 5
19:16	set_ch4	R/W	0x0	Input Channel Setting of Conversion Slot 4
15:12	set_ch3	R/W	0x0	Input Channel Setting of Conversion Slot 3
11:8	set_ch2	R/W	0x0	Input Channel Setting of Conversion Slot 2
7:4	set_ch1	R/W	0x0	Input Channel Setting of Conversion Slot 1
3:0	set_ch0	R/W	0x0	Input Channel Setting of Conversion Slot 0

SET_DTMD
Data Output Format Setting of Each Conversion Slot
Offset: 0x08
Width: 8bits

Bits	Name	Direction	Reset	Description
31:8	-	N/A	0x0	Reserved
7	set_dtmd7	R/W	0x0	Data Output Format Setting of Conversion Slot 7 0: Binary 2's complement 1: Straight binary
6	set_dtmd6	R/W	0x0	Data Output Format Setting of Conversion Slot 6 0: Binary 2's complement 1: Straight binary
5	set_dtmd5	R/W	0x0	Data Output Format Setting of Conversion Slot 5 0: Binary 2's complement 1: Straight binary
4	set_dtmd4	R/W	0x0	Data Output Format Setting of Conversion Slot 4 0: Binary 2's complement 1: Straight binary
3	set_dtmd3	R/W	0x0	Data Output Format Setting of Conversion Slot 3 0: Binary 2's complement 1: Straight binary
2	set_dtmd2	R/W	0x0	Data Output Format Setting of Conversion Slot 2 0: Binary 2's complement 1: Straight binary
1	set_dtmd1	R/W	0x0	Data Output Format Setting of Conversion Slot 1 0: Binary 2's complement 1: Straight binary
0	set_dtmd0	R/W	0x0	Data output format setting of Conversion Slot 0 0: Binary 2's complement 1: Straight binary

SLOTx_DAT (x=0-7)

Data of Each Conversion Slot After A/D Conversion

Offset: SLOT0_DAT - 0x0C
Offset: SLOT1_DAT - 0x10
Offset: SLOT2_DAT - 0x14
Offset: SLOT3_DAT - 0x18
Offset: SLOT4_DAT - 0x1C
Offset: SLOT5_DAT - 0x20
Offset: SLOT6_DAT - 0x24
Offset: SLOT7_DAT - 0x28

Width: 10 bits

Bits	Direction	Reset	Description
31:10	N/A	0x0	Reserved
9:0	R	0x0	Data of Conversion Slot x (x=0 to 7) After A/D conversion

19. Timer

19.1. Feature

- It has five independent programmable timers.
- The width of the counter of each timer is 32 bits.
- Two count modes are supported.
  Free orchis mode
  0xFFFFFFFF is set as the counter maximum value.
  User setting mode
  The given value is set to a counter maximum value.
- Out does the interrupt signal in each timer.
- The polarity of the interrupt signal is active low.
- Little-Endian

19.2. Description

19.2.1. Basic Operation

When timer counts down from the maximum value until 0, each timer generates interrupt. The width of each counter is 32 bits. As for each timer, the counter maximum value is set when timer is enabled. Initial value depends on the operation mode.

19.2.2. Operation Mode

Two counter modes are supported.
When the counter becomes 0, the value of the TimerN*LoadCount register is loaded as a counter maximum value in the user setting mode.
When the counter becomes 0, 0xFFFF_FFFF is loaded as a counter maximum value in the free orchis mode.

19.2.3. Interrupt Signal

When the counter reaches initial value from 0, internal interrupt signal is generated. As for the internal interrupt signal, output is done only at one clock cycle. To set external interrupt signal (timer_intr_n), the internal interrupt signal is sent to the system clock. The external interrupt signal is generated synchronized with the system clock.
The set interrupt signal is cleared by reading the TimerN*EOI register or the TimersEOI register when it is enabled. All the interrupt signals can be cleared clearing a specific interrupt signal by reading the TimerN*EOI register, and reading the TimersEOI register. The timing of clearing interrupts is synchronized with the system clock.
The external interrupt signal is generated because the interrupt generation has higher priority than clear interrupt when TimersEOI was led at the same time as generating the internal interrupt signal.
When timer is enabled, the interrupt signal is cleared synchronizing with the system clock.

19.3. I/O Signals

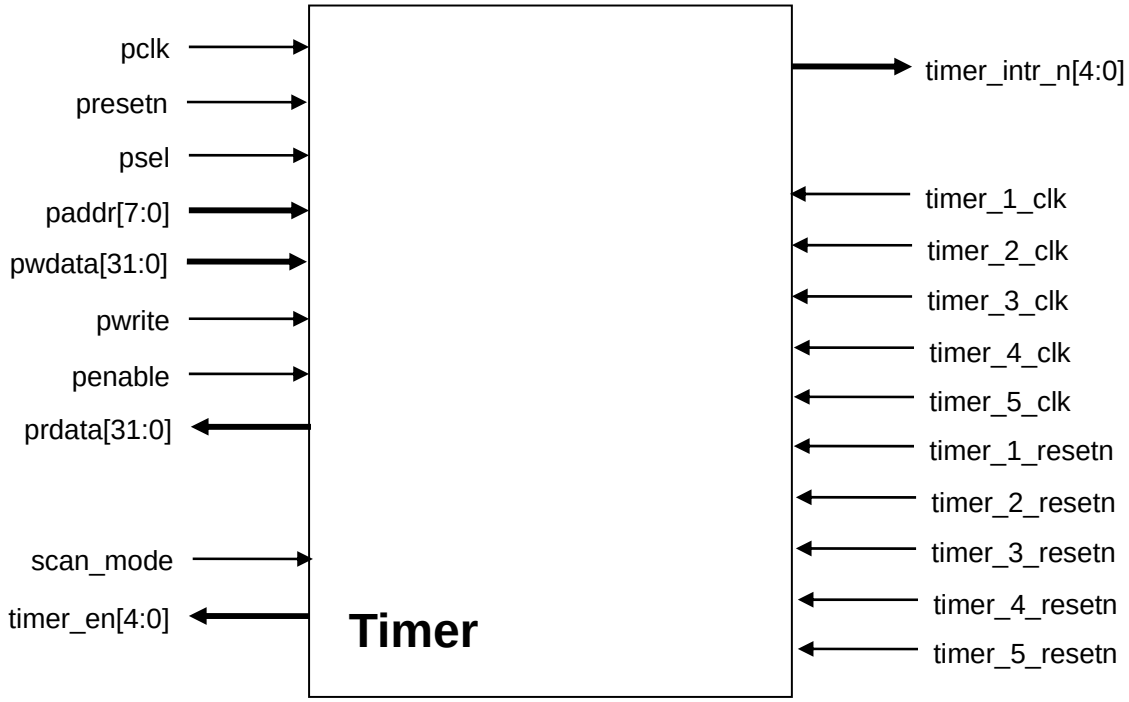


Figure 139. Timer Module

Terminal List of Timer Module

Terminal Name	I/O	Description	Connection
pclk	In	APB Clock	CLOCKGEN
presetn	In	APB Reset (Active Low)	RESETGEN
psel	In	APB Peripheral Selection Signal	APB
paddr[7:0]	In	APB Address	APB
pwdata[31:0]	In	APB Write Data	APB
pwrite	In	APB Write Signal	APB
penable	In	APB Enable Signal	APB
prdata[31:0]	Out	APB Read Data	APB
scan_mode	In	SCAN Mode Setting HI: Scan Mode LOW: Normal Mode	TESTDEC
timer_en[4:0]	Out	Timer Enable Signal. Each timer has corresponding enable signal. The clock generator uses these signals, and the timer clock can be generated. HI: Enabled State LOW: Disabled State	NC
timer_intr_n[4:0]	Out	Timer Interrupt Signal (Active Low) HI: Interrupt Disabled LOW: Interrupt Enabled	INTCTL
timer_1_clk	In	Clock Counter of Timer1	CLOCK_GEN
timer_2_clk	In	Clock Counter of Timer2	CLOCK_GEN
timer_3_clk	In	Clock Counter of Timer3	CLOCK_GEN
timer_4_clk	In	Clock Counter of Timer4	CLOCK_GEN
timer_5_clk	In	Clock Counter of Timer5	CLOCK_GEN
timer_1_resetn	In	Reset Signal of Timer1	RESET_GEN
timer_2_resetn	In	Reset Signal of Timer2	RESET_GEN
timer_3_resetn	In	Reset Signal of Timer3	RESET_GEN
timer_4_resetn	In	Reset Signal of Timer4	RESET_GEN
timer_5_resetn	In	Reset Signal of Timer5	RESET_GEN

19.4. Register

19.4.1. Memory Map

Name	Offset	R/W	Width Bit	Description
Timer1 Load Count	0x00	R/W	32	Timer1 Counter Initial Value Setting Register Initial Value: 0x0
Timer1 Current Value	0x04	R	32	Timer1 Counter Value Initial Value: 0x0
Timer1 Control Reg	0x08	R/W	3	Timer1 Control Register Initial Value: 0x0
Timer1 EOI	0x0C	R	1	Timer1 Interrupt Clear Register Initial Value: 0x0
Timer1 Int Status	0x10	R	1	Timer1 Interrupt Status Register Initial Value: 0x0
Timer2 Load Count	0x14	R/W	32	Timer2 Counter Initial Value Setting Register Initial Value: 0x0
Timer2 Current Value	0x18	R	32	Timer2 Counter Value Initial Value: 0x0
Timer2 Control Reg	0x1C	R/W	3	Timer2 Control Register Initial Value: 0x0
Timer2 EOI	0x20	R	1	Timer2 Interrupt Clear Register Initial Value: 0x0
Timer2 Int Status	0x24	R	1	Timer2 Interrupt Status Register Initial Value: 0x0
Timer3 Load Count	0x28	R/W	32	Timer3 Counter Initial Value Setting Register Initial Value: 0x0
Timer3 Current Value	0x2C	R	32	Timer3 Counter Value Initial Value: 0x0
Timer3 Control Reg	0x30	R/W	3	Timer3 Control Register Initial Value: 0x0
Timer3 EOI	0x34	R	1	Timer3 Interrupt Clear Register Initial Value: 0x0
Timer3 Int Status	0x38	R	1	Timer3 Interrupt Status Register Initial Value: 0x0
Timer4 Load Count	0x3C	R/W	32	Timer4 Counter Initial Value Setting Register Initial Value: 0x0
Timer4 Current Value	0x40	R	32	Timer4 Counter Value Initial Value: 0x0
Timer4 Control Reg	0x44	R/W	3	Timer4 Control Register Initial Value: 0x0
Timer4 EOI	0x48	R	1	Timer4 Interrupt Clear Register Initial Value: 0x0
Timer4 Int Status	0x4C	R	1	Timer4 Interrupt Status Register Initial Value: 0x0
Timer5 Load Count	0x50	R/W	32	Timer5 Counter Initial Value Setting Register Initial Value: 0x0
Timer5 Current Value	0x54	R	32	Timer5 Counter Value Initial Value: 0x0
Timer5 Control Reg	0x58	R/W	3	Timer5 Control Register Initial Value: 0x0
Timer5 EOI	0x5C	R	1	Timer5 Interrupt Clear Register Initial Value: 0x0
Timer5 Int Status	0x60	R	1	Timer5 Interrupt Status Register Initial Value: 0x0
Timers Int Status	0xA0	R	5	Timer Module Interrupt Status Register Initial Value: 0x0
Timers EOI	0xA4	R	5	Timer Module Interrupt Clear Register Initial Value: 0x0
Timers Raw IntStatus	0xA8	R	5	Timer Module Unmask Interrupt Status Register Initial Value: 0x0

19.4.2. Register Detail

TimerN Load Count
TimerN Counter Initial Value Setting Register
Address Offset : 0x00, 0x14, 0x28, 0x3C, 0x50
Reset : 0x0

Bit	Name	R/W	Reset	Description
31:0	TimerN Load Count	R/W	0x0	Initial value that starts the countdown of timer N is set.

TimerN Current Value
TimerN Counter Value Register
Address Offset : 0x04, 0x18, 0x2C, 0x40, 0x54
Reset : 0x0

Bit	Name	R/W	Reset	Description
31:0	TimerN* Current Value	R	0x0	CPU can read the current value of timer N.

TimerN Control Reg
TimerN Control Register
Address Offset : 0x08, 0x1C, 0x30, 0x44, 0x58
Reset : 0x0

Bit	Name	R/W	Reset	Description
2		R/W	0x0	Interrupt / Mask Enable 0 : Interrupt Enabled 1 :Mask Enabled
1		R/W	0x0	Timer N Mode Selection Register 0 : Free Running Mode 1 :User Setting Counter Mode
0		R/W	0x0	Timer N Enable Register Counter will only work if this bit is set to “1”. 0: Counter Disabled 1: Counter Enabled

TimerN EOI
TimerN Interrupt Clear Register
Address Offset : 0x0C, 0x20, 0x34, 0x48, 0x5C
Reset : 0x0

Bit	Name	R/W	Reset	Description
0	TimerN EOI	R	0x0	When this register is set to “1”, the interrupt of TimerN is cleared.

TimerN Int Status
TimerN Interrupt Status Register
Address Offset : 0x10, 0x24, 0x38, 0x4C, 0x60
Reset : 0x0

Bit	Name	R/W	Reset	Description
0	TimerN Int Status	R	0x0	Timer N Interrupt Status Register. 0 :Interrupt Disabled 1 :Interrupt Enabled

Timers Int Status
Timer Module Interrupt Status Register
Offset : 0xA0
Reset : 0x0

Bit	Name	R/W	Reset	Description
4:0	Timers Int Status	R	0x0	Interrupt Status Register Even if this register is set, the interrupt signal is never cleared. The bit position corresponds to the timer number. 0 : No Interrupt 1 :There is interrupt.

Timers EOI
Timer Module Interrupt Clear Register
Offset : 0xA4
Reset : 0x0

Bit	Name	R/W	Reset	Description
4:0	Timers EOI	R	0x0	When this register is read, all timers' interrupt signals are cleared. When read, it outputs "0".

Timers Raw Int Status
Timer Module Unmask Interrupt Status
Offset : 0xA8
Reset : 0x0

Bit	Name	R/W	Reset	Description
4:0	Timers Raw Int Status	R	0x0	When this register is read, all timers' interrupt signals are cleared. When read, it outputs "0".

20. Watchdog Timer

20.1. Feature

- Counter value can be set, which counts every cycle. It has time-out feature.
- The width of the counter is 32-bits.
- The counter counts down from a set value. Time-out occurs when counter value reaches “0”.
- The count rate can be controlled by the clock enable pin.
- The time-out response can be selected from the following:
  System Reset Generation.
  Interrupt Mode. When time out occurs, interrupt is generated. Once an interrupt happens due to first watchdog timer timeout, the second timeout will generate a system reset if the first interrupt is not cleared.
- The time-out cycle can be set to programmable.
- The pulse length of system reset can be set to programmable.

20.2. Description

20.2.1. Counter

WDT counter counts down from the set value to "0". When the counter value reaches "0", system reset or interrupt is generated depending on the selected response for time-out. Response Mode Bit (RMOD) of WDT Control Register controls this response. The counting continues even if system reset or interrupt is generated. When "0x76" is written in the WDT_CRR register, the counter is kicked.

◇ Interrupt

If RMOD=1 and WDT time-out occurs, interrupt is generated. If first interrupt is not cleared by the time the second interrupt arrives, system reset is generated. If the counter is reset to “0” due to kicking (writing “0x76” on WDT_CRR register), no interrupt will occur. The interrupt is cleared by WDT_EOI or if kicked.
Shown below is the timing diagram for interrupt generation and clearing of the interrupt signal.

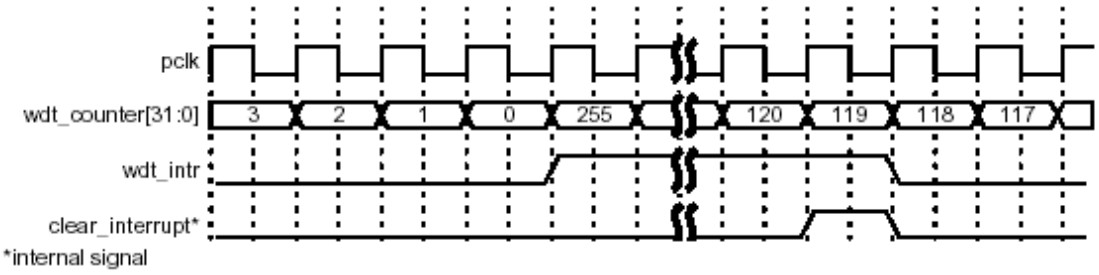


Figure 140. Interrupt generation timing chart

◇ System Reset

If RMOD=0 and WDT time-out occurs, system reset is generated. If the counter is reset to “0” due to kicking (writing “0x76” on WDT_CRR register), system reset will not occur.
The timing chart from the counter restart to the system reset generation is shown below.

Figure 141. Kick-system reset timing chart

20.2.2. Clock Enable

Clock enable (wdt_clk_en) is done to control the count rate of the counter and it can be done from the outside. It is executed by the following standing up when restart during clock-enable is " Low". If clock-enable is not "High", neither the interrupt nor system reset is generated. Clearing the interrupt is independent of enabling the clock.

20.2.3. Reset Pulse Length

The reset pulse length is set by integral multiples of the bus clock. When system reset is generated, it remains asserted until the entire system is reset . Restarting the counter after system reset is invalid.

20.3. I/O Signals

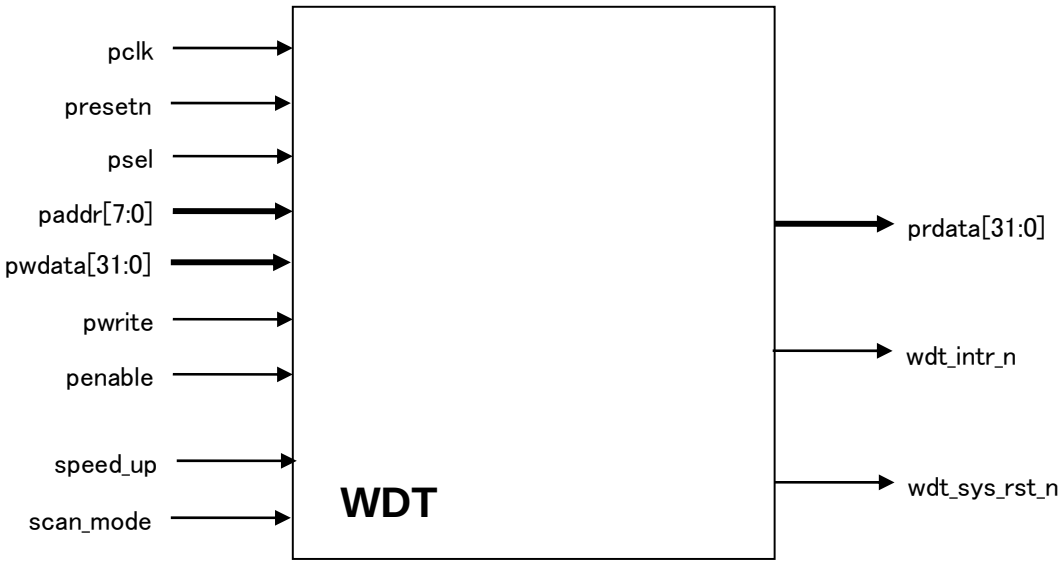


Figure 142. WDT Module

Terminal list of WDT module

Terminal name	I/O	Description	Connection
pclk	In	APB Clock	Clock Gen
presetn	In	APB Reset (Active Low)	Reset Gen
psel	In	APB Peripheral Select Signal	APB
paddr[7:0]	In	APB Address	APB
pwdata[31:0]	In	APB Write Data	APB
pwrite	In	APB Write Signal	APB
penable	In	APB Enable Signal	APB
prdata[31:0]	Out	APB Read Data	APB
wdt_clk_en	In	Count up by always pclk	Fixed to High
speed_up	In	This pin is used for testing. (Active High). The time-out cycle becomes 256 cycles regardless of the register value. If this pin is asserted, it shortens the time for testing. Time is usually fixed to low.	Fixed to Low
scan_mode	In	Scan Mode Signal (Active High) Time is usually fixed to low.	TEST_DEC
wdt_intr_n	Out	WDT Interrupt Output (Active Low)	INCTL
wdt_sys_rst_n	Out	WDT System Reset Output (Active Low)	Reset Gen

20.4. Register Map

20.4.1. Memory Map

Name	Offset	R/W	Bit Width	Description
WDT_CR	0x00	R/W	5	Control Register Initial value：0x12
WDT_TORR	0x04	R/W	4	Timeout Range Register Initial value：0xF
WDT_CCVR	0x08	R	32	Current Counter Value Register Initial value：0x7FFF_FFFF
WDT_CRR	0x0c	W	8	Counter Restart Register Initial value：0x0
WDT_STAT	0x10	R	1	Interrupt Status Register Initial value：0x0
WDT_EOI	0x14	R	1	Interrupt Clear Register Initial value：0x0

20.4.2. Register Detail

WDT_CR

WDT control register

Offset: 0x00 , Reset: 0x12

Bit	Name	R/W	Reset	Description
4 : 2	RPL	R/W	0x4	Reset Pulse Length Setting Register 0 – 2 pclk cycles 1 – 4 pclk cycles 2 – 8 pclk cycles 3 – 16 pclk cycles 4 – 32 pclk cycles 5 – 64 pclk cycles 6 – 128 pclk cycles 7 – 256 pclk cycles
1	RMOD	R/W	0x1	Timeout Response Select Register 0 :System reset generation 1 :System reset generation after interrupt is generated
0	WDT_EN	R/W	0x0	WDT Enable Setting If "1" is written, the watchdog timer is enabled. . "0" cannot be written when becoming effective one degree. It is nullified only by system reset.

WDT_TORR

Timeout cycle set register

Offset: 0x04 , Reset: 0xF

Bit	Name	R/W	Reset	Description
3 : 0	TOP	R/W	0xF	Timeout Cycle The cycle becomes 2(16 + TOP).

WDT_CCVR

Present WDT Count Value Reading Register

Offset ; 0x08 , reset ; 0x7FFF_FFFF

Bit	Name	R/W	Reset	Description
31 : 0	WDT_ CCVR	R	0x7FFF _FFFF	Present WDT Count Value

WDT_CRR
Register for Counter Kick
Offset: 0x0c , Reset: 0x0

Bit	Name	R/W	Reset	Description
7 : 0	WDT_ CRR	W	0x0	The counter is restarted by writing in this register. It becomes effective only when "0x76" is written to prevent a kick from happening by accident.

WDT_STAT
Interrupt State Register
Offset: 0x10 , Reset: 0x0

Bit	Name	R/W	Reset	Description
0	WDT_ STAT	R	0x0	Interrupt Status Register of WDT 0 :There is no interrupt. 1 :There is an interrupt.

WDT_EOI
Interrupt Clear Register
Offset: 0x14 , Reset: 0x0

Bit	Name	R/W	Reset	Description
0	WDT_ EOI	R	0x0	The interrupt of WDT is cleared. This is used when the clearing the interrupt without kicking the counter..

21. Real Time Clock

21.1. Feature

◇ 32-Bit Program Timer
◇ Increment Counter
◇ The counter value can be loaded from the register setting.
◇ When the value in which the register is set matches the counter value, it generates an interrupt.
◇ The interrupt signal is active low.
◇ External crystal output is 32.768kHz

21.2. Description

21.2.1. Clock

This block uses the following clocks.

	Bus clock pclk		Function part clock rtc_clk	
	Normal Mode	Power Down	Normal Mode	Power Down
RTC	SYSTEM (96MHz)	32.768kHz	8.192kHz (32.768/4 kHz)	

21.3. I/O Signal

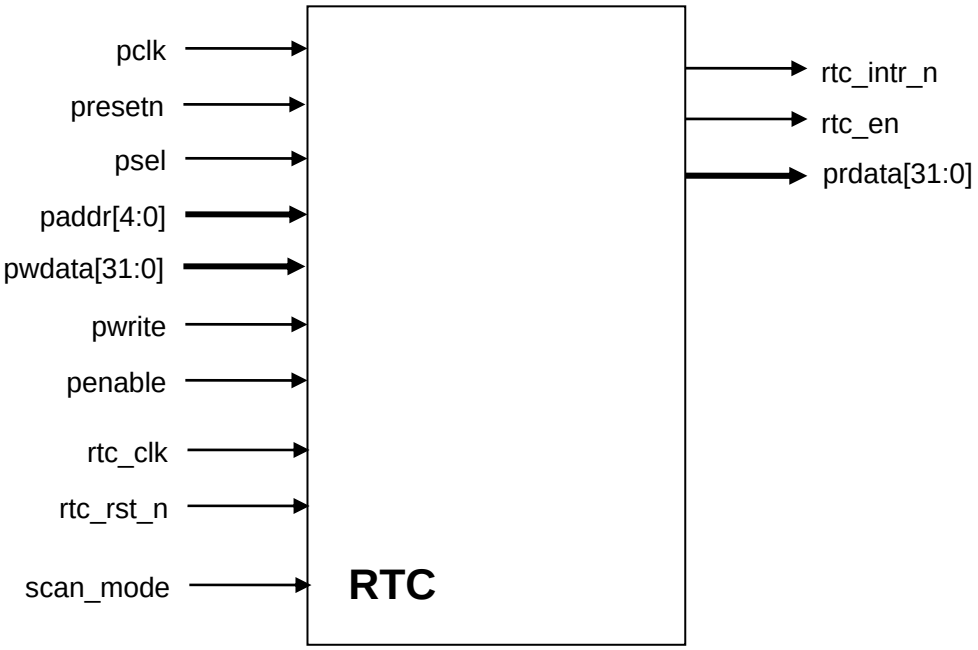


Figure 143. RTC Module

Terminal list of RTC module

Terminal Name	I/O	Description	Connection
pclk	In	APB Clock	CLOCKGEN
present	In	APB Reset	RESETGEN
psel	In	APB Peripheral Select Signal	APB
paddr[4:0]	In	APB Address	APB
pwdata[31:0]	In	APB Write Data	APB
pwrite	In	APB Write Signal	APB
penable	In	APB Enable Signal	APB
prdata[31:0]	Out	APB Read Data	APB
scan_mode	In	SCAN Mode Setting HI: Scan Mode LOW: Normal Mode	TESTDEC
rtc_clk	In	Realtime Clock Counter	CLOCKGEN
rtc_rst_n	In	Reset of Real Time Clock Counter	RESETGEN
rtc_intr_n	Out	Interrupt Signal (Active Low)	ICTL
rtc_en	Out	Free Rank Lock Demand Signal	Open

21.4. Register

21.4.1. Memory Map

Name	Description	Address Offset	R/W	Width	Reset
RTC_CCVR	Current Counter Value Register	0x00	R	32bit	0x0
RTC_CMR	Counter Match Register	0x04	R/W	32bit	0x0
RTC_CLR	Counter Load Register	0x08	R/W	32bit	0x0
RTC_CCR	Counter Control Register	0x0C	R/W	4bit	0x0
RTC_STAT	Interrupt Status Register	0x10	R	32bit	0x0
RTC_RSTAT	Interrupt Raw Status Register	0x14	R	32bit	0x0
RTC_EOI	End of Interrupt Register	0x18	R	32bit	0x0
RTC_COMP_VERSION	Component Version Register	0x1C	R	32bit	0x3230332A

21.4.2. Register Details

Current Counter Value Register
The current value of an internal counter
Address Offset : 0x00

Bits	Name	Direction	Reset	Description
31:0	Current Counter Value	R	0x0	Current value of internal counter

Counter Match Register
The interrupt match register
Address Offset : 0x04

Bits	Name	Direction	Reset	Description
31:0	Counter Match	R/W	0x0	When the internal counter matches the value of the corresponding register, interrupt is generated.

Counter Load Register
The counter loading register
Address Offset : 0x08

Bits	Name	Direction	Reset	Description
31:0	Counter Load	R/W	0x0	Value of this register is loaded into the counter

Counter Control Register
The counter control register
Address Offset : 0x0C

Bits	Name	Direction	Reset	Description
3	rtc_wen	R/W	0x0	When the match is generated instead of doing weight until the counter reaches the maximum value, the counter is wrapped. 0 = Wrap disabled 1 = Wrap enabled
2	rtc_en	R/W	0x0	The counter is controlled. 0 = Counter disabled 1 = Counter enabled
1	rtc_mask	R/W	0x0	Mask of interrupt 0: The mask is not done. 1: The mask is done.
0	rtc_ien	R/W	0x0	Interrupt generation permission 0: Interrupt is not possible. 1: Interrupt is possible.

Interrupt Status Register
The interrupt status register
Address Offset : 0x10

Bits	Name	Direction	Reset	Description
31:1	N/A	N/A	-	Reserved
0	rtc_stat	R	0x0	The register that does masking for interrupt status 0: Interrupt is not active 1: Interrupt is active

Interrupt Raw Status Register
Interrupt RAW status register
Address Offset : 0x14

Bits	Name	Direction	Reset	Description
31:1	N/A	N/A	-	Reserved
0	rtc_rstat	R	0x0	The interrupt status register that doesn't do the mask 0: Interrupt is not active 1: Interrupt is active

End of Interrupt Register
An interrupt clear register
Address Offset : 0x18

Bits	Name	Direction	Reset	Description
31:1	N/A	N/A	-	Reserved
0	rtc_eoi	R	0x0	When this register is set, the match interrupt is cleared.

Component Version Register
Component version
Address Offset : 0x1C

Bits	Name	Direction	Reset	Description
31:0	rtc_comp_version	R	0x3230332A	RTC Module Version Management Number

22. Remote Controller Receiver (RCR)

22.1. Features

- ◇ Converts infrared remote control signal into code
- ◇ Supports the AEHA communication format
- ◇ Generates interrupts (Leader signal, Data signal, End-of-frame, and Data error detection interrupts)
- ◇ Supports inversion of input signal polarity
- ◇ Has built-in de-noising circuit
- ◇ Allows H/L signal width setting

22.2. Description

22.2.1. Block Diagram

The following figure shows the block diagram of this remote control receiver.

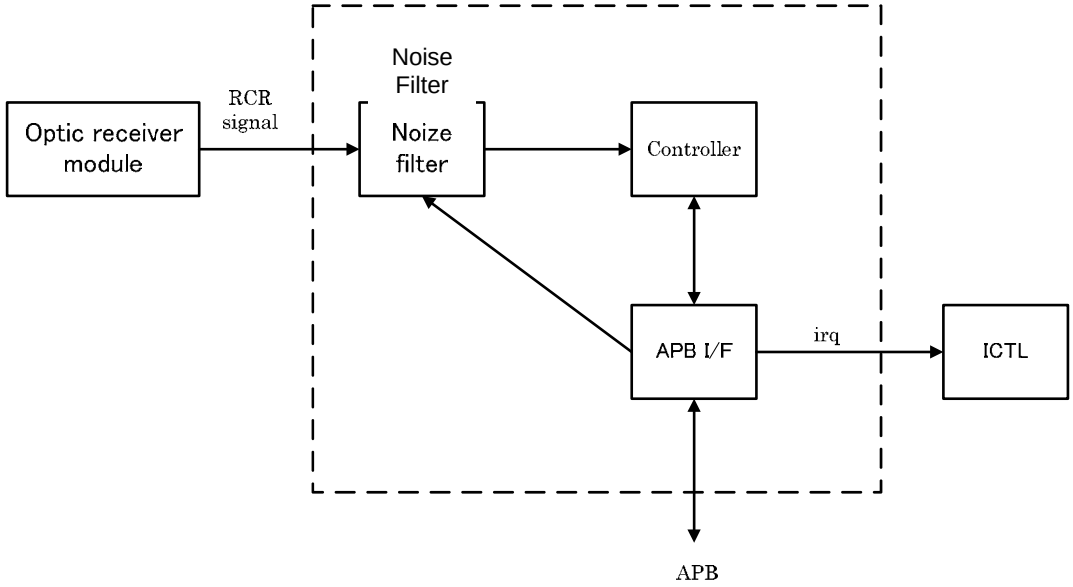
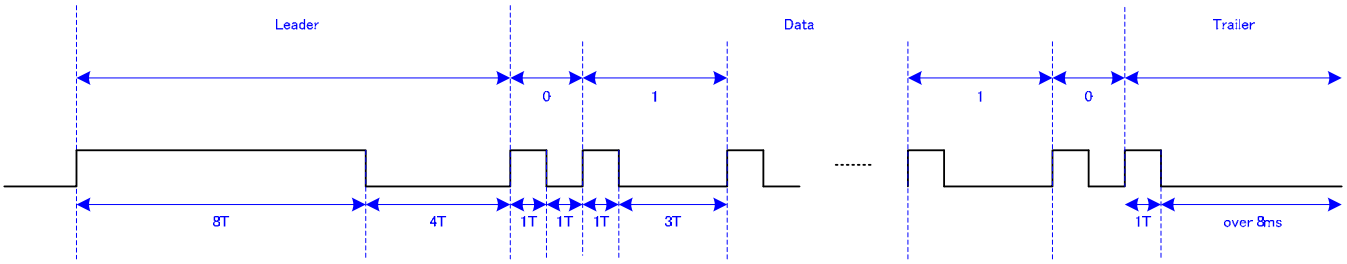


Figure 144. Block Diagram

22.2.2. AEHA Communication Format

The following section shows the waveform of the AEHA communication format that this RCR supports.



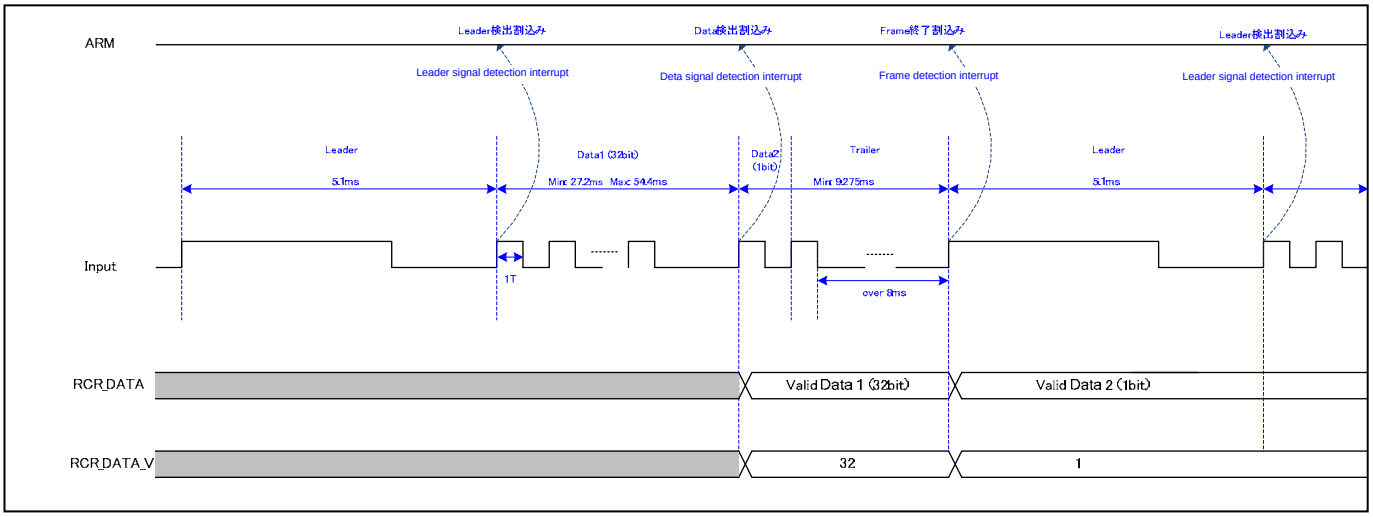
1T: 350 to 500us (typ: 425us)

Figure 145. AEHA communication format (for one frame)

22.2.3. Basic Operation

Set the register RCR_ON=1after completion of the settings for input signal polarity, denoising width, end-of-frame count, interrupt mask, and H-L signal. Thecomparison starts the signal counting and code conversion.
When a Leader signal, Data signal, or End-of frame is detected, an interrupt signal is generated and receive data register values are rewritten. After completion of data readout, clear the interrupt.
If an error is detected during data readout, a data error detection interrupt is generated. If a data error is detected, ignore data on the relevant frame.

Example for acquisition of leader + 33-bit data



(when 1T=425us)

Figure 146.

22.2.4. Operational Clock

The following table shows the operational clock of the RCR block. The clock operates at a frequency of 32.768 kHz at all times.

	Function	APB I/F
Standby Mode	32.768 kHz	32.768 kHz
Normal Mode	32.768 kHz	System clock

22.2.5. Inversion of Input Signal Polarity

The RCR inverts the polarity of an input signal, and then proceeds with subsequent processing.

22.2.6. Noise Filter

If a sampled signal level is maintained for the number of sampling times set with the register RCR_SET, the noise filter imports the said level. Signals that did not maintain the level for the set number of sampling times are ignored.

22.2.7. Pulse Width Measurement Counter

This counter is used to make measurement of pulse width. When the rising or falling edge of input signal is detected, the counter increments the pulse width until the subsequent rising or falling edge is detected.
Furthermore, this counter is also used to determine the end of frame and cleared at the end of frame.

22.2.8. Interrupts

- Leader signal detection interrupt: It is generated when the leader signal is detected. The detection is judged according to the set value of RCR_SET_L.
- Data signal detection interrupt: It is generated when data of 32 bits are detected.
- End-of-frame detection interrupt: It is generated when the value of the pulse with measurement counter reaches the set value of the register RCR_SET. The counter is cleared at the same time.
- Data error detection interrupt: It is generated when H/L width in the data section (1T or 3T) is not consistent with the set value of RCR_SET_D0/1.

22.2.9. Received Data

Data signal after 0/1 judgment is saved in the 0th bit of the temporary storage register. When the subsequent data is received, the saved data is shifted to upper bit in steps of 1 bit and new data is inputted in the 0th bit.
When data of 32 bits are received, the data are saved in the received data retention register (RCR_DATA) and the temporary storage register is cleared. At the end of frame, the temporary storage register value at the time is saved in RCR_DATA.
Since the register RCR_DATA_V is incremented by 1 every time it receives data after 0/1 judgment, the number of significant bits of data is indicated.
Ensure the number of effective bits at the same time when reading data.

22.2.10. Handling of Error Signal

- If the length of Leader signal is out of the set value of the register RCR_SET_L:
  Unless the Leader signal is normally detected, the data is not decoded. As a result, the value of the register RCR_DATA is not updated.
  Furthermore, no detection interrupt is generated.

- If the Leader signal is not detected, but the Data signal is only detected:
  Unless the Leader signal is normally detected, data is not decoded. As a result, the value of the register RCR_DATA is also not updated.
  Furthermore, no detection interrupt is generated.

- If the Leader signal is normally detected, but the length of the Data signal is out of the set value of the register RCR_SET_D0/1:
  Since the Leader signal was detected, the data is decoded. When any Data error is detected, a Data error detection interrupt is generated. Even if the Data error occurs, the value of the register RCR_DATA is updated when data of 32 bits are received or the end of frame is detected. As a result, data that can be read in this case becomes incorrect data. Data on the frame in which the Data error was detected should be ignored.

- If the subsequent frame is received in a period of time shorter than that to be taken for the judgment of the end of frame (RCR_SET [15:4]):
  If any signal change is made in a period of time shorter than that to be taken for the judgment of the end of frame, it is determined that Data error has been detected, resulting in the generation of Data error detection interrupt. In this case, handle the error in the same manner as that to be taken when a normal data error is detected.

22.3. I/O Signals

Pin Name	I/O	Function	Destination
pclk_i	in	APB Clock	CLOCKGEN
present	in	APB Reset (Active Low)	RESETGEN
psel	in	APB Peripheral Select Signal	APB
paddr [15:0]	in	APB Address	APB
pwdata [31:0]	in	APB Write Data	APB
pwrite	in	APB Write Signal	APB
penable	in	APB Enable Signal	APB
prdata [31:0]	out	APB Read Data	APB
pclk_fun_i	in	RCR Function Clock (32.768 KHz)	CLOCKGEN
rcrdata_org	in	RCR Data Input	PAD
rcr_irq_o	out	Interrupt Request Signal	ICTL

22.4. Register

22.4.1. Memory Map

Name	Description	Address Offset	Width	Reset
RCR_ON	RCR Operation Enable Setting	0x00	1	0x0
RCR_SET	Input Signal Processing Setting	0x04	4	0x4
RCR_SET_L	Leader Section Setting	0x08	32	0x0
RCR_SET_D0	Data 0 Section Setting	0x0C	32	0x0
RCR_SET_D1	Data 1 Section Setting	0x10	16	0x0
RCR_DATA	Received Data	0x14	32	0x0
RCR_DATA_V	Number of Significant Bits of Received Data	0x18	6	0x0
RCR_IRQ	Interrupt	0x1C	4	0x0
RCR_IRQ_CL	Interrupt Clear	0x20	4	0x0
RCR_IRQ_MSK	Mask for Cause of Interrupt	0x24	4	0xF

22.4.2. Register Detail

RCR_ON
RCR Operation Enable Setting
Offset: 0x00
Width: 1 bit

Bits	Name	Direction	Reset	Description
0	rcr_on	R/W	0x0	RCR Operation Control Setting 1 to this bit after completion of setting of registers RCR_SET, RCR_SET_L, RCR_SET_D0, and RCR_SET_D1 starts the RCR operation. 0: Operation OFF 1: Operation ON

RCR_SET
Input Signal Processing Setting
Offset: 0x04
Width: 4 bits

Bits	Name	Direction	Reset	Description
15:4	set_end		0x0	End-of-Frame Judgment Count Setting Sets the length of section in which no bit changes are made to judge the end of frame Judgment time = (1 ÷ 32 .768kHz) × Set value Max: 125 ms (Set value: 0xFFF)
3:1	set_fltr	R/W	0x2	Denoising Width Setting 0: reserved 1: 30.5 us 2: 61.0 us 3: 91.5 us 4: 122 us 5: 153 us 6: 183 us 7: 214 us
0	set_inv	R/W	0x0	Input Signal Polarity Setting 0: Normal, 1: Inversed

RCR_SET_L
Leader Section Setting
Offset: 0x08
Width: 32 bits

Bits	Name	Direction	Reset	Description
31:24	set_ldh_max	R/W	0x0	Maximum Count Setting in the H Section of Leader Signal Set this register so that MIN will be equal to or smaller than MAX. (Max.: 7.781ms, 1T equivalent: 972us)
23:16	set_ldh_min	R/W	0x0	Minimum Count Setting in the H Section of Leader Signal
15:8	set_ldl_max	R/W	0x0	Maximum Count Setting in the L Section of Leader Signal set this register so that MIN will be equal to or smaller than MAX.
7:0	set_ldl_min	R/W	0x0	Minimum Count Setting in the L Section of Leader Signal

RCR_SET_D0
Data Section Setting
Offset: 0x0C
Width: 32 bits

Bits	Name	Direction	Reset	Description
31:24	set_dth_max	R/W	0x0	Maximum Count Setting in the H Section when Data = 0/1 Set this register so that MIN will be equal to or smaller than MAX.
23:16	set_dth_min	R/W	0x0	Minimum Count Setting in the H Section when Data = 0/1
15:8	set_dtl_max	R/W	0x0	Maximum Count Setting in the L Section when Data = 0 Set this register so that MIN will be equal to or smaller than MAX.
7:0	set_dtl_min	R/W	0x0	Minimum Count Setting in the L Section when Data = 0

RCR_SET_D1
Data Section Setting
Offset: 0x10
Width: 32 bits

Bits	Name	Direction	Reset	Description
15:8	set_dtl_max	R/W	0x0	Maximum Count Setting in the L Section when Data = 1 Set this register so that MIN will be equal to or smaller than MAX.
7:0	set_dtl_min	R/W	0x0	Minimum Count Setting in the L Section when Data = 1

RCR_DATA
Received Data
Offset: 0x14
Width: 32 bits

Bits	Name	Direction	Reset	Description
31:0	rcv_data	R/W	0x0	32-bit Received Data

RCR_DATA_V
Number of Significant Bits of Received Data
Offset: 0x18
Width: 6 bits

Bits	Name	Direction	Reset	Description
5:0	varid_bit	R/W	0x0	Number of Significant Bits

RCR_IRQ
Interrupt
Offset: 0x1C
Width: 4 bits

Bits	Name	Direction	Reset	Description
3	irq_dat	R	0x0	Data Error Detection Interrupt 0: No interrupt generated 1: Interrupt generated
2	irq_frm	R	0x0	End of Frame Detection Interrupt 0: No interrupt generated 1: Interrupt generated
1	irq_dat	R	0x0	Data Signal Detection Interrupt 0: No interrupt generated 1: Interrupt generated
0	irq_ldr	R	0x0	Leader Signal Detection Interrupt 0: No interrupt generated 1: Interrupt generated

RCR_IRQ_CL
Interrupt Clear
Offset: 0x20
Width: 4 bits

Bits	Name	Direction	Reset	Description
3	rcr_irq_cl[3]	R/W	0x0	Data Error Detection Interrupt Clear 1: Interrupt Cleared
2	rcr_irq_cl[2]	R/W	0x0	End of Frame Detection Interrupt Clear 1: Interrupt Cleared
1	rcr_irq_cl[1]	R/W	0x0	Data Signal Detection Interrupt Clear 1: Interrupt Cleared
0	rcr_irq_cl[0]	R/W	0x0	Leader Signal Detection Interrupt Clear 1: Interrupt Cleared

RCR_IRQ_MSK
Mask for Cause of Interrupt
Offset: 0x24
Width: 4 bits

Bits	Name	Direction	Reset	Description
3	rcr_irq_msk[3]	R/W	0x1	Data Error Detection Interrupt Mask 0: Unmasked, 1: Masked
2	rcr_irq_msk[2]	R/W	0x1	End of Frame Detection Interrupt Mask 0: Unmasked, 1: Masked
1	rcr_irq_msk[1]	R/W	0x1	Data Signal Detection Interrupt Mask 0: Unmasked, 1: Masked
0	rcr_irq_msk[0]	R/W	0x1	Leader Signal Detection Interrupt Mask 0: Unmasked, 1: Masked

23. Clock Generator

23.1. Features

- ◇ Designed to supply clocks to internal blocks
- ◇ Allows the ON/OFF control of clocks for the blocks
- ◇ Generates an audio master clock
- ◇ Supports Power-Down Mode

23.2. Description

23.2.1. Block Diagram

The following figure shows the CLKGEN controller block diagram.

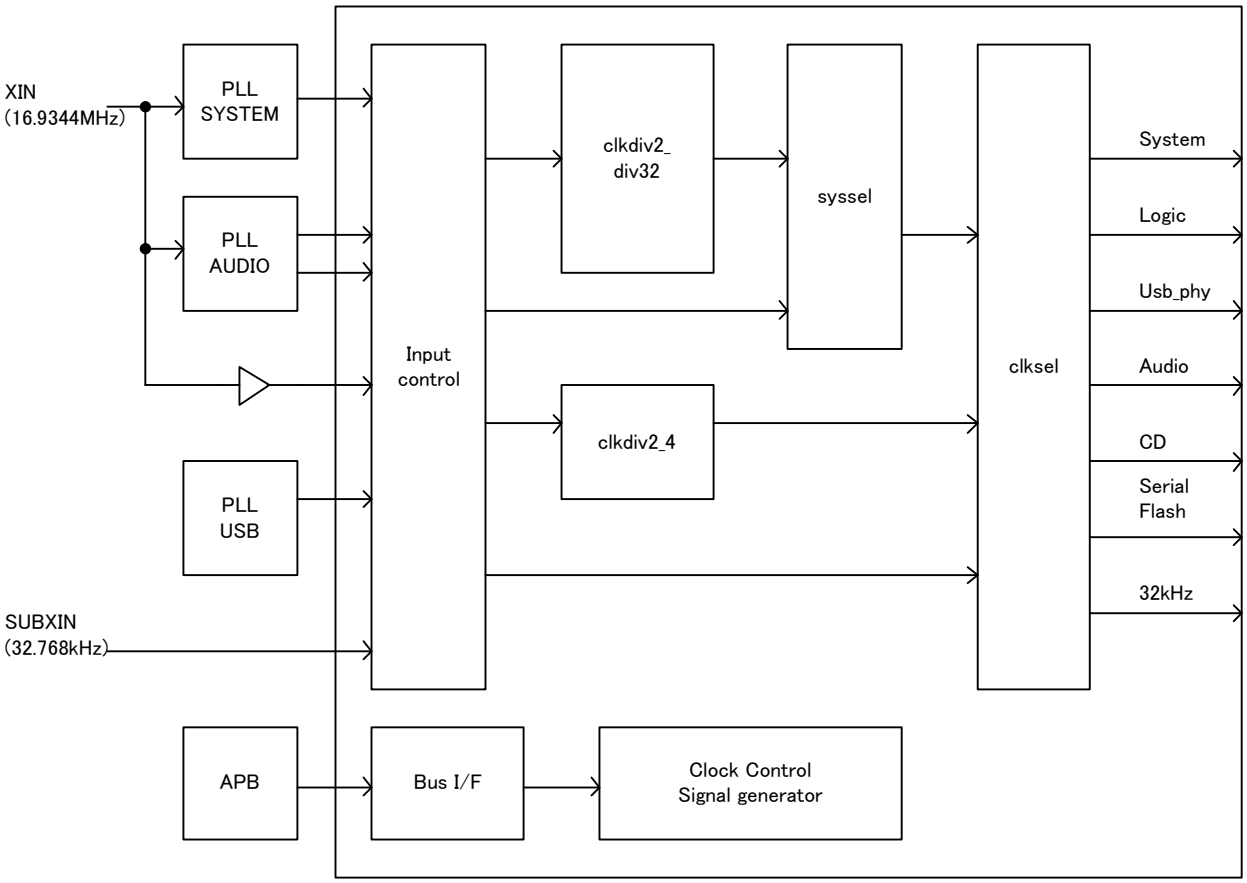


Figure 147. CLKGEN Controller Block Diagram

23.2.2. Input Control Block

This block selects between PLL or Test clock for clock input to blocks.

23.2.3. Clkdiv2_div32 and Clkdiv2_4 Blocks

These blocks are used to divide PLL clock frequency from 2 to 32.
PLL clock frequency for audio is divided by 2, 4, 3, and 6.

23.2.4. Syssel Block

This block is used to shift to system clock set with software.
The system clock is selectable according to Normal Mode (96 MHz) or Power-Down Mode (32 kHz).

23.2.5. Clksel Block

This block is used to enable or disable clocks to individual blocks according to clock enable signal set with software.

23.2.6. Clock Control Signal Generator

This block is used to generate clock control signals set with software.
This signal generator allows selecting of system clock to operate ARM9 to normal mode (96 MHz) and power-down mode (32 kHz) accordingly.
The signal generator also allows the following settings:

- Frequency dividing setting by clock to be supplied to each clock
- Clock supply stop/start setting by clock to be supplied to each block
- Analog block stop/start setting
- Oscillation circuit stop/start setting

23.2.7. Power-Down Mode

For power management, normal mode and power-down mode for power saving are provided.

Normal Mode: The system clock operates at a frequency of 96 MHz.
Power-Down Mode: The system clock operates at a frequency of 32.768 kHz inputted from SUBXIN.

Switching between normal mode and power-down mode is enabled by software register setting.
By switching to power-down mode, input clocks to unnecessary blocks are disabled. Thus, power consumption is reduced.

23.2.8. Clocks in Logic Block

The following table lists clocks in the Logic block.

	Bus Clock		Clock in Function Block		
Block	Normal mode	Power-Down mode	Normal mode	MHz	Power-Down mode
ARM9	-	-	SYSTEM	96	32.768K
AMBA	SYSTEM	32.768K	-	96	-
Serial Flash I/F	SYSTEM	32.768K	SFR	73.728	32.768K
	-	-	SFR	73.728 (Inverted)	32.768K (Inverted)
WDT	SYSTEM	32.768K	-	-	-
Timer1	SYSTEM	32.768K	SYSTEM (Note 1)	96	32.768K
Timer2	-	-	SYSTEM (Note 1)	96	32.768K
Timer3	-	-	SYSTEM (Note 1)	96	32.768K
Timer4	-	-	SYSTEM (Note 1)	96	32.768K
Timer5	-	-	SYSTEM (Note 1)	96	32.768K
Clock Controller	SYSTEM	32.768K	-	-	-
PIN Controller	SYSTEM	32.768K	-	-	-
RTC	SYSTEM	32.768K	RTC	8.192K	8.192K
UART0	SYSTEM	32.768K	SYSTEM (Note 1)	96	32.768K
UART1	SYSTEM	32.768K	SYSTEM (Note 1)	96	32.768K
SPI0	SYSTEM	32.768K	SYSTEM (Note 1)	96	32.768K
SPI1	SYSTEM	32.768K	SYSTEM (Note 1)	96	32.768K
I2C0	SYSTEM	32.768K	SYSTEM (Note 1)	96	32.768K
I2C1	SYSTEM	32.768K	SYSTEM v	96	32.768K
I2S Output	SYSTEM	32.768K	AUDIO	AUDIO	32.768K

Clocks in Logic Blocks – continued

	Bus Clock		Clock in Function Block		
CD-DSP	SYSTEM	32.768K	XIN	16.9344	32.768K
ADC	SYSTEM	32.768K	XIN	16.9344	32.768K
REMAP	SYSTEM	32.768K	-	-	-
RCR	SYSTEM	32.768K	RCR	32.768K	32.768K
GPIO0	SYSTEM	32.768K	SYSTEM (Note 1)	96	32.768K
GPIO1	SYSTEM	32.768K	SYSTEM (Note 1)	96	32.768K
DMAC	SYSTEM	32.768K	-	-	-
I2SIN/CD-ROM	SYSTEM	32.768K	SYSTEM (Note 1)	96	32.768K
SDIO I/F	SYSTEM	32.768K	SYSTEM	96	32.768K
USB Controller	SYSTEM	32.768K	USB	60	32.768K
USB Connect Detector	SYSTEM	32.768K	SYSTEM	32.768K	32.768K
USB PHY	-	-	PHY	12M	32.768K
ICTL	SYSTEM	32.768K	-	-	-

(Note 1) Available for selection of frequency-dividing clock

23.2.9. SDRAM Clocks

Block	Signal Name	Normal mode	MHz	Power-Down Mode
SDRAM Controller: Used for bus and controller	sdrc_hclk_o	SYSTEM	96	32.768 kHz
SDRAM Controller: Used for WRITEPIPE	sdrc_hclkb_o	Used to invert sdrc_hclk_o		
Clock for output to SDRAM	osdram_clk_o	Used for delay selection and output of sdrc_hclk_o		
Clock for capture from SDRAM	isdram_clk_o	Used for delay selection and output of isdram_clk_i		

23.2.10. Audio Clocks

The following clocks are supplied as Audio output clocks.

Sampling Frequency	256 fs	96 fs	Unit
192 kHz (48-kHz system)	49.152	-	MHz
176.4 kHz (44.1-kHz system)	45.1584	16.9344	MHz

23.3. I/O Signals

Pin Name	I/O	Function	Destination
sys_clk_i	In	APB BUS Clock	CLKCTR
rstb_i	In	Reset (Active Low)	RSTGEN
paddr_i	In	APB BUS Address	APB
penable_i	In	APB BUS Enable	APB
pwdata_i	In	APB BUS Write Data	APB
pwrite_i	In	APB BUS Write Enable	APB
psel_i	In	APB BUS Selector	APB
prdata _o	Out	APB BUS Read Data	APB
xinmain_clk_i	In	XIN Clock Input	PAD
xinsub_clk_i	In	SUB Clock Input	PAD
pllsys_clk_i	In	PLL(SYSTEM) Clock Input	PLL
pllaud1_clk_i	In	PLL(AUDIO) Clock Input	PLL
pllaud2_clk_i	In	PLL(AUDIO) Clock Input	PLL
pllusb_clk_i	In	PLL(USB) Clock Input	PLL
isdram_clk_i	In	Clock for Capture from SDRAM Return Clock for PAD_***.CIN	PAD
sys_clk_o	Out	System Clock	Logic
phy12m_clk_o	Out	USB-PHY 12M Clock	USB-PHY
usbx_clk_o	Out	USB 60M Clock	USB
wdt_clk_o	Out	WDT Clock	Logic
tm1_clk_o	Out	Timer1 Clock	Logic
tm2_clk_o	Out	Timer2 Clock	Logic
tm3_clk_o	Out	Timer3 Clock	Logic
tm4_clk_o	Out	Timer4 Clock	Logic
tm5_clk_o	Out	Timer5 Clock	Logic
rtc_clk_o	Out	RTC Clock	Logic
uart0_clk_o	Out	UART Clock	Logic
uart1_clk_o	Out	UART Clock	Logic
spi0_clk_o	Out	SPI1 Clock	Logic
spi1_clk_o	Out	SPI2 Clock	Logic
i2c0_clk_o	Out	I2C1 Clock	Logic
i2c1_clk_o	Out	I2C2 Clock	Logic
gpio_clk_o	Out	GPIO Clock	Logic
dmac_clk_o	Out	DMAC Clock	Logic
pdm_clk_o	Out	PERI DMAC Clock	Logic
cdr_clk_o	Out	CD-ROM Clock	Logic
sdrc_hclk_o	Out	SDRAM Controller: Used for bus and controller	Logic
sdrc_hclkb_o	Out	SDRAM Controller: Used for WRITEPIPE	Logic
qspi_clk_o	Out	QUAD-SPI Clock	Logic
sdio_clk_o	Out	SDIO Clock	Logic

I/O Signals – continued

Pin Name	I/O	Function	Destination
usbd_clk_o	Out	USB DMA Clock	Logic
sdw_clk_o	Out	SHADOW Clock	Logic
sfr_clk_o	Out	SERIAL FLACH Clock	Logic
sdr_clk_o	Out	SD-RAM Clock	Logic
aud1_clk_o	Out	AUDIO Clock (45.1584MHz)	Logic
aud2_clk_o	Out	AUDIO Clock (33.8688MHz)	OPEN
aud3_clk_o	Out	AUDIO Clock (49.152MHz)	Logic
aud4_clk_o	Out	AUDIO Clock (36.864MHz)	OPEN
aud5_clk_o	Out	AUDIO Clock (16.9344MHz)	Logic
cdd_clk_o	Out	CD-DSP Clock	Logic
adc_clk_o	Out	ADC Clock	Logic
osdram_clk_o	Out	Clock for output to SD-RAM	Logic
isdram_clk_o	Out	Clock for capture from SD-RAM	Logic

23.4. Register

23.4.1. Memory Map

Name	Description	Address Offset	Width	Reset
clk_ctl0	System Clock Control	0x00	32	32'h00000000
clk_ctl1	Clock Divider Control	0x04	32	32'h00000000
clk_ctl2	Clock Divider Control	0x08	32	32'h00000000
clk_ctl3	Clock Divider Control	0x0C	32	32'h00000000
clk_ctl5	Clock Enable Control	0x14	32	32'h00000000
clk_ctl6	Clock Enable Control	0x18	32	32'h00000000
clk_ctl7	Clock Enable Control	0x1C	32	32'h00000000
clk_ctl8	Clock Enable Control	0x20	32	32'h00000000
SDRAM_INCLK_DELAY	SDRAM In Clock Delay Register	0x24	8	16'h0000
SDRAM_OUTCLK_ DELAY	SDRAM Out Clock Delay Register	0x28	8	16'h0000

23.4.2. Register Detail

clk_set0
Offset: 0x00
Width: 32 bits

Bits	Name	Direction	Reset	Description
15		R/W	0x0	-
14		R/W	0x0	-
13		R/W	0x0	-
12		R/W	0x0	Selects operation mode of CD (ANALOG) 0: Power ON 1: Power OFF
11		R/W	0x0	Selects operation mode of ADC 0: Power ON 1: Power OFF
10		R/W	0x0	Selects operation mode of PLL AUDIO2 0: Power ON 1: Power OFF
9		R/W	0x0	Selects operation mode of PLL AUDIO1 0: Power ON 1: Power OFF
8		R/W	0x0	Selects operation mode of PLL SYSTEM 0: Power ON 1: Power OFF
7:6		R/W	0x0	-
5		R/W	0x0	-
4		R/W	0x0	Selects operation mode of oscillation circuit for MAIN clock input 0: Start operation 1: Stop operation
3:1		R/W	0x0	-
0		R/W	0x0	Selects system clock (ARM9 operation clock) 0: 96 MHz 1: 32 kHz (Power-Down)

clk_set1
Offset: 0x04
Width: 32 bits

Bits	Name	Direction	Reset	Description
31:28		R/W	0x0	GPIO1 Settings (GPIO clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
27:24		R/W	0x0	GPIO0 Settings (GPIO clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
23:20		R/W	0x0	TIM5 Settings (Timer5 clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
19:16		R/W	0x0	TIM4 Settings (Timer4 clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
15:12		R/W	0x0	TIM3 Settings (Timer3 clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
11:8		R/W	0x0	TIM2 Settings (Timer2 clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
7:4		R/W	0x0	TIM1 Settings (Timer1 clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
3:0		R/W	0x0	-

clk_set2
Offset: 0x08
Width: 32 bits

Bits	Name	Direction	Reset	Description
31:28		R/W	0x0	-
27:24		R/W	0x0	-
23:20		R/W	0x0	I2C1 Settings (I2C clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
19:16		R/W	0x0	I2C0 Settings (I2C clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
15:12		R/W	0x0	SPI1 Settings (SPI1 clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
11:8		R/W	0x0	SPI0 Settings (SPI0 clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
7:4		R/W	0x0	UART1 Settings (UART1 clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
3:0		R/W	0x0	UART0 Settings (UART0 clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided

clk_set3
Offset: 0x0c
Width: 32 bits

Bits	Name	Direction	Reset	Description
31:24		R/W	0x0	-
23:20		R/W	0x0	SDIO Settings (SDIO clock) 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
19:16		R/W	0x0	SFROM Settings (serial flash ROM clock) 4'h0 : 73.73 MHz inverted 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
15:12		R/W	0x0	-
11:8		R/W	0x0	CD-ROM Settings (CD-ROM clock). 4'h0: System clock / 1/1 frequency-divided 4'h1: System clock / 1/2 frequency-divided 4'h2: System clock / 1/4 frequency-divided 4'h3: System clock / 1/8 frequency-divided
7:0		R/W	0x0	-

clk_set5
Offset: 0x14
Width: 32 bits

<table>
<tr><th>Bits</th><th>Name</th><th>Direction</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:0</td><td></td><td>R/W</td><td>0x0</td><td>Enables or disables clock supply to each function block
1’b0: Clock supply in progress
1’b1: Clock supply stopped

Refer to the table shown below for correspondence between bits and blocks.
<table>
<tr><th>Bit</th><th>Block</th></tr>
<tr><td>0</td><td>-</td></tr>
<tr><td>1</td><td>SD-RAM I/F</td></tr>
<tr><td>2</td><td>-</td></tr>
<tr><td>3</td><td>Timer1</td></tr>
<tr><td>4</td><td>Timer2</td></tr>
<tr><td>5</td><td>Timer3</td></tr>
<tr><td>6</td><td>Timer4</td></tr>
<tr><td>7</td><td>Timer5</td></tr>
<tr><td>8</td><td>-</td></tr>
<tr><td>9</td><td>-</td></tr>
<tr><td>10</td><td>UART0</td></tr>
<tr><td>11</td><td>UART1</td></tr>
<tr><td>12</td><td>SPI0</td></tr>
<tr><td>13</td><td>SPI1</td></tr>
<tr><td>14</td><td>I2C0</td></tr>
<tr><td>15</td><td>I2C1</td></tr>
<tr><td>16</td><td>-</td></tr>
<tr><td>17</td><td>GPIO0</td></tr>
<tr><td>18</td><td>GPIO1</td></tr>
<tr><td>19</td><td>-</td></tr>
<tr><td>20</td><td>-</td></tr>
<tr><td>21</td><td>CD-ROM</td></tr>
<tr><td>22</td><td>SDRAM Controller
sdrc_hclkb_o</td></tr>
<tr><td>23</td><td>Serial Flash I/F Inverted</td></tr>
<tr><td>24</td><td>SDIO I/F</td></tr>
<tr><td>25</td><td>USB Connect Detector</td></tr>
<tr><td>26</td><td>-</td></tr>
</table></td></tr>
</table>

clk_set6
Offset: 0x18
Width: 32 bits

<table>
<tr><th>Bits</th><th>Name</th><th>Direction</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:0</td><td></td><td>R/W</td><td>0x0</td><td>Enables or disables clock supply to each function block
1’b0: Clock supply in progress
1’b1: Clock supply stopped

Refer to the table shown below for correspondence between bits and blocks.
<table>
<tr><th>BIT</th><th>Block</th></tr>
<tr><td>0</td><td>Serial Flash I/F</td></tr>
<tr><td>1</td><td>RTC</td></tr>
<tr><td>2</td><td>I2S output - 45.1584 MHz</td></tr>
<tr><td>3</td><td>-</td></tr>
<tr><td>4</td><td>I2S output - 49.152 MHz</td></tr>
<tr><td>5</td><td>-</td></tr>
<tr><td>6</td><td>I2S output - 16.9344 MHz</td></tr>
<tr><td>7</td><td>CD-DSP</td></tr>
<tr><td>8</td><td>ADC</td></tr>
<tr><td>9</td><td>RCR</td></tr>
<tr><td>10</td><td>-</td></tr>
<tr><td>11</td><td>USB Controller</td></tr>
<tr><td>12</td><td>USB PHY</td></tr>
</table></td></tr>
</table>

clk_set7
Offset: 0x1C
Width: 32 bits

<table>
<tr><th>Bits</th><th>Name</th><th>Direction</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:0</td><td></td><td>R/W</td><td>0x0</td><td>
Enables or disables clock supply to the AMBA bus of each block
1’b0: Clock supply in progress
1’b1: Clock supply stopped

Refer to the table shown below for correspondence between bits and blocks.
<table>
<tr><th>BIT</th><th>BUS Block</th></tr>
<tr><td>0</td><td>-</td></tr>
<tr><td>1</td><td>SD-RAM I/F</td></tr>
<tr><td>2</td><td>WDT</td></tr>
<tr><td>3</td><td>Timer1-5</td></tr>
<tr><td>4-7</td><td>-</td></tr>
<tr><td>8</td><td>Clock Controller</td></tr>
<tr><td>9</td><td>PIN Controller</td></tr>
<tr><td>10</td><td>UART0</td></tr>
<tr><td>11</td><td>UART1</td></tr>
<tr><td>12</td><td>SPI0</td></tr>
<tr><td>13</td><td>SPI1</td></tr>
<tr><td>14</td><td>I2C0</td></tr>
<tr><td>15</td><td>I2C1</td></tr>
<tr><td>16</td><td>REMAP</td></tr>
<tr><td>17</td><td>GPIO0</td></tr>
<tr><td>18</td><td>GPIO1</td></tr>
<tr><td>19</td><td>DMAC</td></tr>
<tr><td>20</td><td>-</td></tr>
<tr><td>21</td><td>CD-ROM</td></tr>
<tr><td>22</td><td>SDRAM Controller sdrc_hclk_o</td></tr>
<tr><td>23</td><td>-</td></tr>
<tr><td>24</td><td>SDIO I/F</td></tr>
<tr><td>25</td><td>USB Connect Detector</td></tr>
<tr><td>26</td><td>ICTL</td></tr>
</table>

Clocks of WDT, DMAC, SD-RAM Controller, and ICTL function blocks are shared with the AMBA bus. Consequently, when stopping the clock supply to the AMBA bus, the clock inputs to the function blocks are also stopped.
</td></tr>
</table>

clk_set8
Offset: 0x20
Width: 32 bits

<table>
<tr><th>Bits</th><th>Name</th><th>Direction</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:0</td><td></td><td>R/W</td><td>0x0</td><td>Enables or disables clock supply to the AMBA bus of each function block
1’b0: Clock supply in progress
1’b1: Clock supply stopped

Refer to the table shown below for correspondence between bits and blocks.
<table>
<tr><th>BIT</th><th>BUS Block</th></tr>
<tr><td>0</td><td>Serial Flash I/F</td></tr>
<tr><td>1</td><td>RTC</td></tr>
<tr><td>2</td><td>I2S Output</td></tr>
<tr><td>3-6</td><td>-</td></tr>
<tr><td>7</td><td>CD-DSP</td></tr>
<tr><td>8</td><td>ADC</td></tr>
<tr><td>9</td><td>RCR</td></tr>
<tr><td>10</td><td>-</td></tr>
<tr><td>11</td><td>USB Controller</td></tr>
<tr><td>12</td><td>USB PHY</td></tr>
</table>
</td></tr>
</table>

SDRAM_INCLK_DELAY
Offset: 0x24
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:0	-	R/W	0x0	Selects the clock to be used in capturing data inputted from SDRAM (selects delay time to input clock returned from PAD.CIN) When [7] is set to 1, clock is inverted. When [7] is set to 0, a value from 0 to 20 is set. Please use this bit with a Reset value.

SDRAM_OUTCLK _DELAY
Offset: 0x28
Width: 8 bits

Bits	Name	Direction	Reset	Description
7:0	-	R/W	0x0	Selects the clock to be used in outputting data to SDRAM (selects delay time to output data from system clock) When [7] is set to 1, clock is inverted. When [7] is set to 0, a value from 0 to 20 is set. Please use this bit with a Reset value.

24. Reset Generator

24.1. Features

- ◇ Designed to generate reset signals to be supplied to blocks
- ◇ Has a built-in circuit used to denoise the reset signals
- ◇ Has a built-in timer used to reset the system

24.2. Description

24.2.1. Outline Circuit Diagram

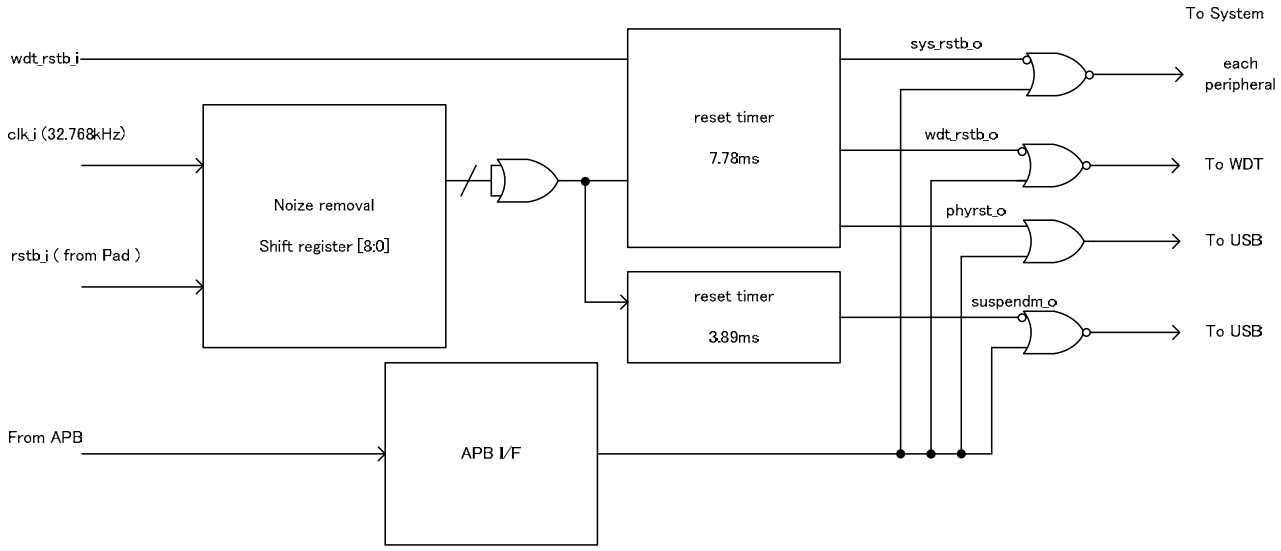


Figure 148. Rstgen Module

24.2.2. Description

24.2.3. Timing Chart

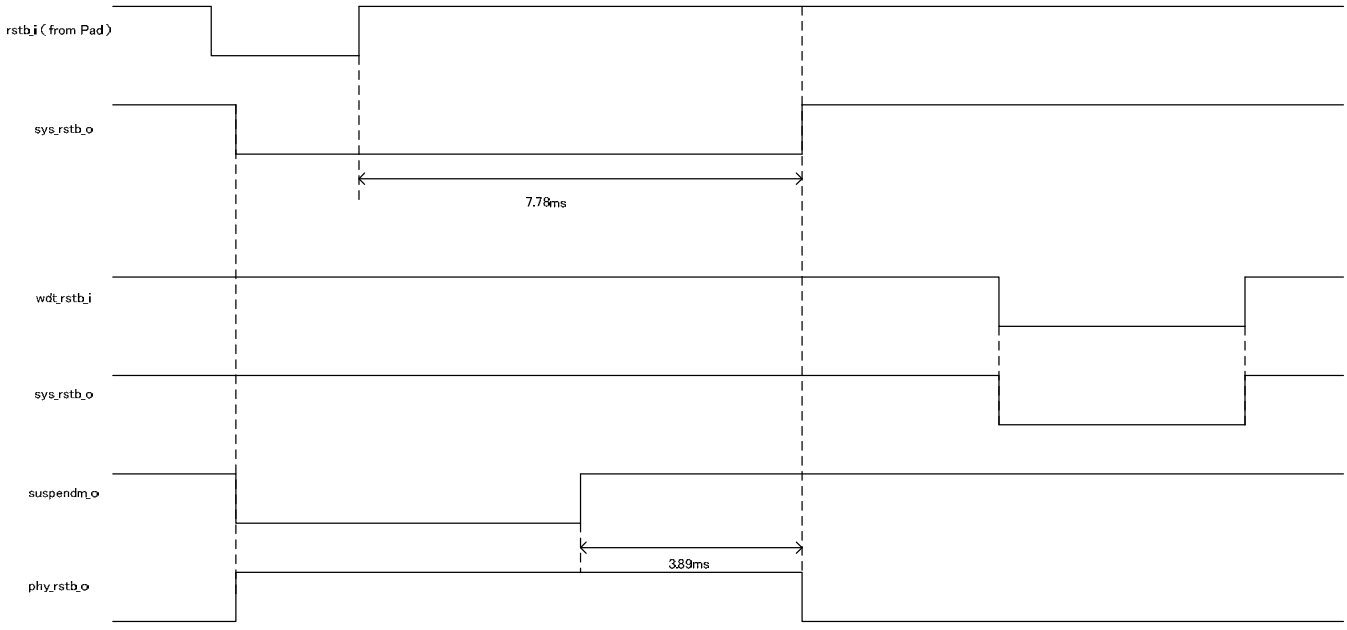


Figure 149.

24.2.4. Denoising Circuit

For denoising reset signals, input a reset signal in a 9-bit shift register and use OR for output.
32.768-kHz clock is used for denoising. Consequently, reset input to PAD should be held at least for a period of 300 us in order to detect the reset signal.

24.2.5. System Reset Counter

Internal system reset signal is maintained at the L level for a period of 7.78 ms after denoised reset signal reaches the H level.

24.2.6. PHY Reset Counter

PHY reset signal in the USB block and a signal to SuspendM are outputted as shown in the above timing chart.

24.2.7. WDT Reset

Connecting reset output signal from WDT block directly to the reset pin of the WDT block via the reset generator will stop WDT output operation in progress. As a result, a reset signal due to WDT timeout is not outputted to the WDT block itself. The WDT block is reset independently by inputting a signal from PAD or making register setting.

24.3. I/O Signals

Pin Name	I/O	Function	Destination
clk_i	In	Clock (32.768 kHz)	CLKGEN
sys_clk_i	In	Internal System Clock	CLKGEN
asyrstb_i	In	Reset (Active Low from PIN)	PAD
tmode_i	In	TMODE Pin	PAD
wdtrstb_i	In	Reset (Active Low from WDT)	WDT
paddr	In	APB Address	APB
pwdata	In	APB Write Data	APB
pwrite	In	APB Write Enable	APB
penable	In	APB W/R Enable	APB
psel	In	APB Slave Select	APB
pdata	Out	APB Data Out	APB
syn_rstb_o	Out	Internal System Reset Output	ARM,AMBA
wdt_rstn_o	Out	Reset to WDT	WDT
timer1_rstn_o	Out	Timer1-5 Reset Output	Timer
clkgen_rstn_o	Out	Clkgen Reset Output	Clkgen
pinctrl_rstn_o	Out	PIN Controller Reset Output	PIN controller
rtc_rstn_o	Out	RTC Reset Output	RTC
uart0_rstn_o	Out	UART0 Reset Output	UART0
uart1_rstn_o	Out	UART1 Reset Output	UART1
spi0_rstn_o	Out	SPI0 Reset Output	SPI0
spi1_rstn_o	Out	SPI1 Reset Output	SPI1
i2c0_rstn_o	Out	I2C0 Reset Output	I2C0
i2c1_rstn_o	Out	I2C1 Reset Output	I2C1
i2sout_rstn_o	Out	I2S Output Reset Output	I2S output
cdd_rstn_o	Out	CD DSP Reset Output	CD DSP
adc_rstn_o	Out	ADC Reset Output	ADC
remap_rstn_o	Out	REMAP Reset Output	REMAP
rcr_rstn_o		RCR Reset Output	RCR
gpio0_rstn_o	Out	GPIO0 Reset Output	GPIO0
gpio1_rstn_o	Out	GPIO1 Reset Output	GPIO1
dmac_rstn_o	Out	DMAC Reset Output	DMAC
cdr_rstn_o	Out	CD-ROM Reset Output	CD-ROM
sdrc_rstn_o	Out	SDRAM Controller Reset Output	SDRAM controller
qspi_rstn_o	Out	Quad SPI Reset Output	Open
sdio_rstn_o	Out	SDIO Reset Output	SDIO
sdw_rstn_o	Out	Shadow RAM Reset Output	Open
sfl_rstn_o	Out	Serial Flash Reset Output	Serial flash
sdr_rstn_o	Out	SDRAM Reset Output	OPEN
usbd_rstn_o	Out	USB Reset Output	USB
usbc_rstn_o	Out	USB Controller Reset Output	USB controller
usbphy_rst_o	Out	USB PHY Reset Output	USB PHY
usb_suspendm_o	Out	USB Suspend (3.89 ms ount)	USB PHY

24.4. Register

24.4.1. Memory Map

Name	Description	Address Offset	Width	Reset
SOFTRST_CTRL0	Software Reset Control	0x00	32bit	0x0
SOFTRST_CTRL1	Software Reset Control	0x04	32bit	0x0

24.4.2. Register Detail

SOFTRST_CTRL0
This register is used to make software reset setting.
Offset: 0x00

Bits	Name	Direction	Reset	Description
0	wdt_rst	R/W	0	WDT Block 0: Reset cleared (Normal operation) 1: Reset set The sample bit logic applies to the following reset setting.
1	timer1_rst	R/W	0	Timer1 to 5
2-5	-	R/W	0	Reserved
6	clkgen_rst	R/W	0	Clock Controller
7	pinctrl_rst	R/W	0	PIN Controller
8	rtc_rst	R/W	0	RTC
9	uart0_rst	R/W	0	UART0
10	uart1_rst	R/W	0	UART1
11	spi0_rst	R/W	0	SPI0
12	spi1_rst	R/W	0	SPI1
13	i2c0_rst	R/W	0	I2C0
14	i2c1_rst	R/W	0	I2C1
15	i2sout_rst	R/W	0	I2S Output
16	cdd_rst	R/W	0	CD-DSP
17	adc_rst	R/W	0	ADC
18	remap_rst	R/W	0	REMAP
19	rcr_rst	R/W	0	RCR
20	gpio0_rst	R/W	0	GPIO0
21	gpio1_rst	R/W	0	GPIO1
22	dmac_rst	R/W	0	DMAC
23	cdr_rst	R/W	0	CD-ROM
24	sdrc_rst	R/W	0	SDRAM Controller
25	-	R/W	0	Reserved
26	sdio_rst	R/W	0	SDIO I/F
27	-	R/W	0	Reserved
28	sfl_rst	R/W	0	Serial Flash I/F
29	-	R/W	0	Reserved
30	-	R/W	0	Reserved

SOFTRST_CTRL1
This register is used to make software reset setting.
Offset: 0x04

Bits	Name	Direction	Reset	Description
0	usbd_rst	R/W	0	USB Connect Detector 0: Reset cleared (Normal operation) 1: Reset set
1	usbc_rst	R/W	0	USB Controller 0: Reset cleared (Normal operation) 1: Reset set
2	usbphy_rst	R/W	0	USB PHY 0: Reset cleared (Normal operation) 1: Reset set
3	usb_suspend	R/W	0	USB suspend 0 : Suspend cleared (Normal operation) 1 : Suspend set

Operational Notes

1. Power on Reset
   Please keep the terminal RESETX at the Low level when the power supply starts. After completely starting up 3.3V system power supply, afterwards, please make the terminal RESETX High level after 300us after the 32.768KHz and 16.9344MHz oscillation is steady. Moreover, please make the terminal RESETX Low level during 300us or more when resetting it while operating.

2. About Compatibility in USB Memory Device and SD Memory Card
   According to the file structure and communication speed of USB memory, SD memory card, this LSI might not play back correctly.

3. About Compatibility in Bluetooth Device
   According to the Bluetooth device, this LSI might not play back correctly.

4. About Turning On the Power Supply
   Current rush might flow momentarily by the order of turning on the power supply and the delay in IC with two or more power supplies, and note the capacity of the power supply coupling, the power supply, and width and drawing the GND pattern wiring.

5. About Absolute Maximum Rating
   When the absolute maximum rating such as the applied voltage and the ranges of the operating temperature is exceeded, LSI might be destroyed. Please do not apply eithervoltage or temperature that exceeds the absolute maximum rating. Please execute physical measures for safety such as fuse when it is thought to exceed the absolute maximum rating, and examine it so that the condition to exceed the absolute maximum rating is not applied to LSI.

6. Power Supply
   Power and Ground line must be designed as low impedance in the PCB. Print patterns if digital power supply and analog power supply must be separated even if these have same voltage level. Print patterns for ground must be designed as same as power supply. These considerations avoid analog circuits from the digital circuit noise. All pair of power supply and ground must have their own de-coupling capacitor. Those capacitor should be checked about their specification, etc. (nominal electrolytic capacitor degrades its capacity at low temperature) and choose the constant of an electrolytic capacitor.

7. About GND Voltage
   In any state of operation, it must be the lowest voltage about the voltage of the terminal GND. Please actually confirm the voltage of each terminal is not a voltage that is lower than the terminal GND including excessive phenomenon.

8. About Design of Overheating Malfunction Preventive Circuit
   Please design overheating malfunction preventive circuit with an enough margin in consideration of a permissible loss in actual usage.

9. About the Short Between Terminals and the Mounting by Mistake
   Please note that the direction and the gap of position of LSI must be enough when you mount on the substrate. LSI might be destroyed when mounting by mistake and energizing. Moreover, LSI might be destroyed when short-circuited by entering of the foreign substances between the terminal and GND, between terminals, between the terminal and the power supply of LSI.

10. About Operation in Strong Electromagnetic Field
    LSI might malfunction when operating in strong magnetic fiels. Please evaluate before usage.

11. About 2X Speed Recording
    Recording to a memory with slow access speed may require data connection operation.
    2X speed recording to all the memories cannot be guaranteed.

12. Power OFF or Memory Disconnection Under Memory Writing
    The sudden power off or memory disconnection during recording or file write operation to a memory may break the data in a memory.

13. Browsing Operation
    With a memory with slow access speed, browsing operation during music playing may generate skipping.

Operational Notes – continued

14. CD-ROM Playing
CD-ROM playing operation is premised on data being inputted so that an internal data buffer may not become empty. When an input does not meet the deadline and internal data buffers become empty, skipping occurs.

15. Playing Time of MP3 File
The playing time when MP3 file playing may shift when fast forward playing, rewind playing, and VBR playing.

16. Write-In Operation Exceeding Memory Size
Writing to a file when memory size is exceeded is not supported.

17. Write-In Operation of the File Size Exceeding FAT Specification
Writing to a file when file size is exceeded is not supported.

18. About I^2C Format I/F
Although this LSI has adopted the I^2C format, the level shifter circuit is not built in.
For this reason, level shifter is needed for connection with the device besides the range of operating power supply voltage of this LSI.

Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority

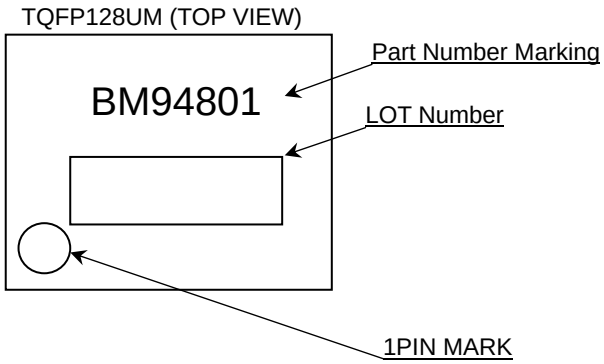
Ordering Information

B	M	9	4	8	0	1	K	U	T	-	Z

Part Number

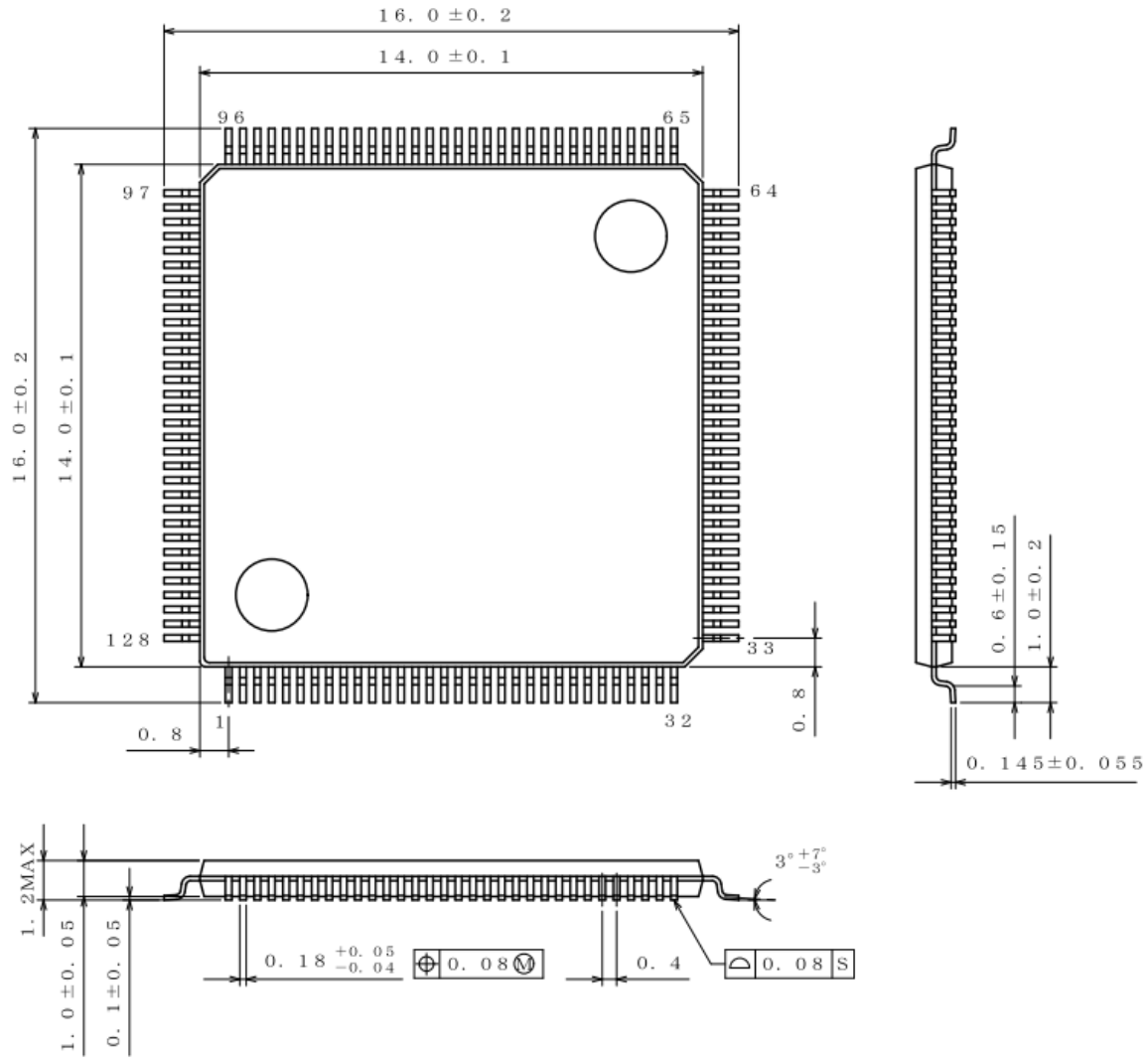
Package
TQFP128UM , supply with tray

Marking Diagram



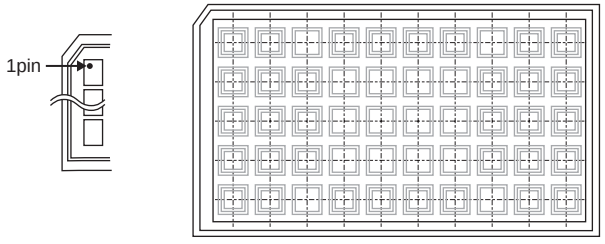
Physical Dimension, Tape and Reel Information

Package Name	TQFP128UM



<Tape and Reel information>

Container	Tray (with dry pack)
Quantity	500pcs
Direction of feed	Direction of product is fixed in a tray



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
6.Sep.2013	001	New Release
1.Oct.2013	002	P. 186 : Removed about the correspondence beyond 88.2kHz P. 186 : Removed 16.2.8 Interpolating Filter (ADC) P. 275 : CD-DSP command:&h85[2:0] is modified to h4W2, h4W1, h4W0 P. 284 : CD-DSP command:&h9C[3:0] modified RFoffset equation to Vc+((15-&h9C[3:0]).0.20-2.0).VDD/3 P. 304 : CD-DSP command:&hD4[3:0] "3: Nothing" is added P. 333 : WDT_CCVR register initial value is modified to 0x7FFF_FFFF P. 338 : Component Version Register register initial value is modified to 0x3230332A P. 353 : clk_set3 register bit [3:0] is modified to the un-use The addition of other details explanations and indication composition become proper.
18.Apr.2014	003	P.008 : The addition of the Function explanations about No.100 USB REXTI. P.009 - P010 : The addition of the Electrical Characteristics Measurement Condition about REXTI Pin's external resistance.

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1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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