

The LS3N165 is a monolithic dual enhancement mode P-Channel Mosfet

The LS3N165 is a dual enhancement mode P-Channel Mosfet and is ideal for space constrained applications and those requiring tight electrical matching.

The hermetically sealed TO-78 package is well suited for high reliability and harsh environment applications.

(See Packaging Information).

LS3N165 Features:

- Very high Input Impedance
- Low Capacitance
- High Gain
- High Gate Breakdown Voltage
- Low Threshold Voltage

FEATURES

DIRECT REPLACEMENT FOR INTERSIL LS3N165

ABSOLUTE MAXIMUM RATINGS¹ @ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Maximum Power Dissipation

Continuous Power Dissipation (one side)	300mW
Total Derating above 25°C	4.2 mW/°C

MAXIMUM CURRENT

Drain Current	50mA
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MAXIMUM VOLTAGES

Drain to Gate or Drain to Source ²	-40V
Peak Gate to Source ³	±125V
Gate-Gate Voltage	±80V

LS3N165 ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	TYP.	MAX	UNITS	CONDITIONS
I _{GSSR}	Gate Reverse Leakage Current	--	--	10	pA	V _{GS} = -0V
I _{GSSF}	Gate Forward Current	T _A = +125°C	--	-10		V _{GS} = -40V
			--	-25		
I _{DSS}	Drain to Source Leakage Current	--	--	-200	mA	V _{DS} = -20V
I _{SDS}	Source to Drain Leakage Current	--	--	-400		V _{SD} = -20V V _{DB} = 0
I _{D(on)}	Drain Current "On"	-5.0	--	-30	mV	V _{DS} = -15V, V _{GS} = -10V
V _{GS(th)}	Gate to Source Threshold Voltage	-2.0	--	-5.0		V _{DS} = -15V, I _D = -10μA
r _{DS(on)}	Drain to Source "On" Resistance	--	--	300	Ω	V _{GS} = -20V, I _D = -100μA
		--	--	300		V _{DS} = -15V, I _D = -10mA, f = 1kHz
g _{fs}	Forward Transconductance	1500	--	3000	pF	V _{DS} = -15V, I _D = -10mA, f = 1MHz ⁴
g _{os}	Output Admittance	--	--	300		
C _{iss}	Input Capacitance	--	--	3		
C _{rss}	Reverse Transfer Capacitance	--	--	0.7		
C _{oss}	Output Capacitance	--	--	3.0	μS	V _{DS} = -15V, I _D = -10mA, f = 100MHz ⁴
R _E (Y _{fs})	Common Source Forward Transconductance	1200	--	--		

MATCHING CHARACTERISTICS LS3N165

SYMBOL	CHARACTERISTIC	LIMITS		UNITS	CONDITIONS
		MIN	MAX		
Y _{fs1} /Y _{fs2}	Forward Transconductance Ratio	0.90	1.0	ns	V _{DS} = -15V, I _D = -500μA, f = MHz ⁴
V _{GS1-2}	Gate Source Threshold Voltage Differential	--	100	mV	V _{DS} = -15V, I _D = -500μA
ΔV _{GS1-2} /ΔT	Gate Source Threshold Voltage Differential Change with Temperature	--	100	μV/°C	V _{DS} = -15V, I _D = -500μA T _A = -55°C to +25°C

Note 1 - Absolute maximum ratings are limiting values above which LS3N165 serviceability may be impaired.

Note 2 - Per Transistor

Note 3 - Device must not be tested at ±125V more than once or longer than 300ms.

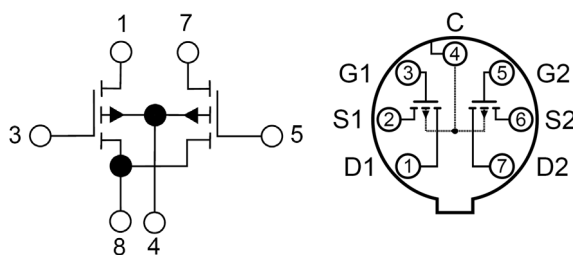
Available Packages:

LS3N165 in TO-72
LS3N165 in bare die.

Please contact Micross for full package and die dimensions

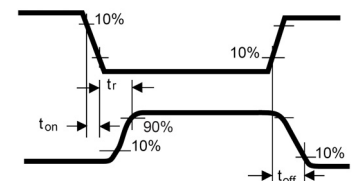
Device Schematic

TO-78 (Bottom View)



*To avoid possible damage to the device while wiring, testing, or in actual operation, follow these procedures: To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used. Avoid unnecessary handling. Pick up devices by the case instead of the leads. Do not insert or remove devices from circuits with the power on, as transient voltages may cause permanent damage to the devices.

SWITCHING WAVEFORM & TEST CIRCUIT



INPUT PULSE

Rise Time ≤ 2ns
Pulse Width ≥ 200ns

SAMPLING SCOPE

T_r ≤ 0.2ns
C_{IN} ≤ 2pF
R_N = 10M

