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SJA2020

ARM7 microcontroller with CAN and LIN controllers

Rev. 01 — 5 April 2006 Objective data sheet

1. Introduction

1.1 About this document

This document lists detailed information about the SJA2020 device. It focuses on factual information like pin information, register views, characteristics etc. Short descriptions are used to outline the concept of the features and functions. More details and background on developing applications for this device is given in the SJA2020 User manual (see Ref. 1). No explicit references are made to the User manual.

Please refer to the SJA2020 Application note ‘Known issues’ (see Ref. 2) for corrections and additional product information.

1.2 Intended audience

This document is written for engineers evaluating and/or developing systems, hard- and/or software for the SJA2020. Some basic knowledge of ARM processors and architecture and ARM7 in particular is assumed (see Ref. 3).

2. General description

2.1 Architectural overview

The SJA2020 consists of an ARM7TDMI-S processor with real-time emulation support, the AMBA Advanced High-performance Bus (AHB) for interface to the on-chip memory controllers, a DTL bus (a universal Philips interface) for interface to the interrupt controller and three VLSI Peripheral Buses (VPB - a compatible superset of ARMs AMBA advanced peripheral bus) for connection to the on-chip peripherals clustered in so-called subsystems. The SJA2020 configures the ARM7TDMI-S processor in little endian byte order. All peripherals run on the same system clock frequency as the ARM7TDMI-S processor to minimize the access latency time. The AHB2VPB bridge used in the subsystems contain a write-ahead buffer of 1 deep. This implies that when the ARM7 writes to a register located at the VPB side of the bridge, it will continue even though the actual write may not yet have taken place. Completion of a second write to the same subsystem will not be executed until the first write is finished.

2.2 ARM7TDMI-S processor

The ARM7TDMI-S is a general purpose 32-bit processor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective controller core.

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Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- Standard 32-bit ARM set
- 16-bit Thumb set

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit controller using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM controller connected to a 16-bit memory system.

The ARM7TDMI-S processor is described in detail in the ARM7TDMI-S data sheet (see Ref. 3).

2.3 On-chip flash memory system

The SJA2020 includes up to 384 kB flash memory system. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed in-system via a serial port, like e.g. CAN. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field upgrades.

2.4 On-chip static RAM

The SJA2020 includes a 24 kB static RAM memory that may be used for code and/or data storage.

3. Features

3.1 General

- ARM7TDMI-S processor at 60 MHz maximum
- Up to 384 kB on-chip flash program memory
- 24 kB static RAM
- One 550 UART with 16 bytes TX and RX FIFO depths
- Three full-duplex SPIs with 16 bits wide, 8 locations deep TX FIFO and RX FIFO
- Four 32-bit timers containing each four capture and compare registers linked to I/Os
- 10-bit, 400 ksample/s, 4-channel ADC with external trigger start option
- Real time clock with on-chip 32 kHz crystal oscillator and (battery) supply
- 32-bit watchdog with timer change protection

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- 94 general purpose I/O pins with programmable pull-up
- Vectored interrupt controller with 16 priority levels
- External 8-bit, 16-bit or 32-bit bus with four memory banks
- Standard ARM test and debug interface with real-time in-circuit emulator
- Dual power supply:
  - CPU operating voltage: 1.8 V ± 5 %
  - I/O operating voltage: 3.3 V
  - 5 V tolerant port pins (without pull-up)
- Configurable system power management
- Twelve level sensitive external interrupt pins
- Processor wake-up from power down via external interrupt pins, CAN or LIN activity
- On-chip low power ring-oscillator with operating range from 25 kHz to 1 MHz
- On-chip crystal oscillator with operating range from 10 MHz to 20 MHz
- On-chip PLL allows CPU operation up to maximum CPU rate of 60 MHz
- Automotive product qualification according AEC-Q100 Rev-F:
  - Temperature grade 2 compliant; ambient operating temperature from –40 °C to +105 °C
- Boundary scan test supported
- Small 144-pin LQFP package

3.2 Flash memory

- Consisting of sectors of 8 kB
- Supporting in-system and in-application programming
- Fast programming capability at 4 Mbit/s
- Provisions against over-burning and over-erasing
- Source code protection

3.3 CAN gateway

- Six CAN controllers
- Full CAN mode for message reception
- Triple transmit buffers with automatic priority scheduling
- Extensive global CAN acceptance filter for high performance gateway functionality

3.4 LIN master controller

- Four dedicated LIN master controllers
- Four standard 450 UARTs with LIN enhancement for LIN slaves or general purposes

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
SJA2020HL/623[1]	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

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[1] SJA2020HL/623 has 384 kB flash consisting of 48 sectors of 8 kB.

5. Block diagram

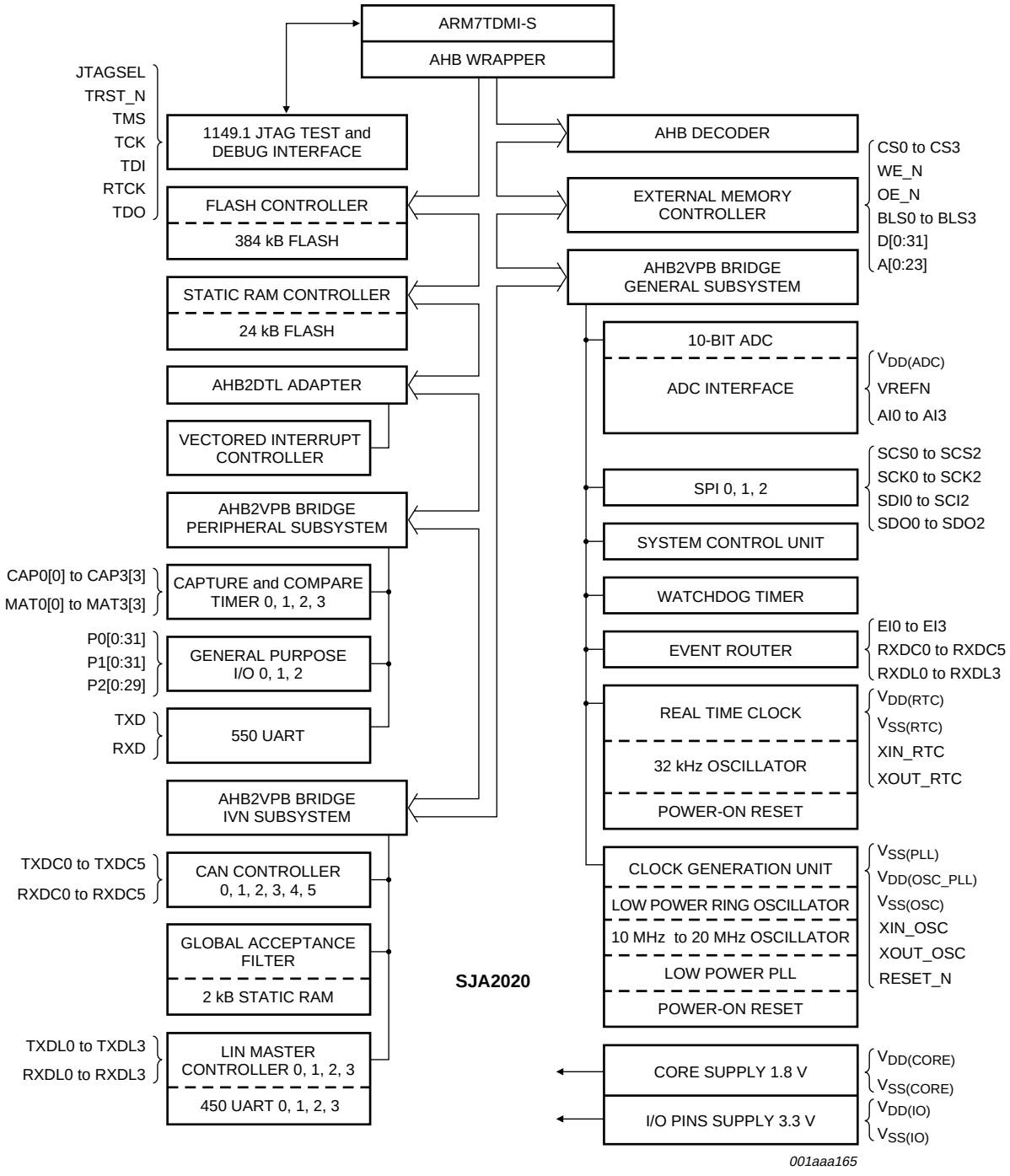

Fig 1. Block diagram

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6. Pinning information

6.1 Pinning

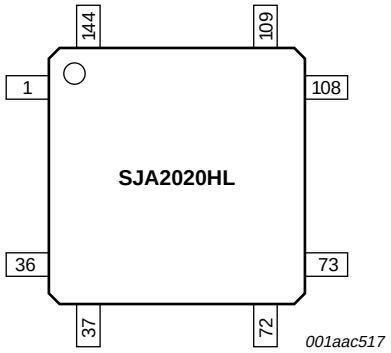

Fig 2. Pin configuration for SOT486-1

6.2 Pin description

Table 2: LQFP144 pin assignment

Symbol	Pin	Description			
		Default function	Function 1	Function 2	Function 3
JTAGSEL	1	TAP controller select input; LOW level selects ARM debug mode and HIGH level selects boundary scan and flash programming; pulled-up internally			
RESET_N	2	external reset input; pulled-up internally (active LOW)			
$V_{SS(RTC)}$	3	real time clock oscillator ground			
XOUT_RTC	4	real time clock crystal output			
XIN_RTC	5	real time clock crystal input or external clock input			
$V_{DD(RTC)}$	6	real time clock oscillator supply voltage			
$V_{SS(OSC)}$	7	oscillator ground			
XOUT_OSC	8	oscillator crystal output			
XIN_OSC	9	oscillator crystal input or external clock input			
$V_{DD(OSC\_PLL)}$	10	oscillator and PLL supply voltage			
$V_{SS(PLL)}$	11	PLL ground			
P0[31]/SDO0	12	GPIO 0; pin 31	GPIO 0; pin 31	SPI0 SDO	SPI0 SDO
P0[30]/SDI0	13	GPIO 0; pin 30	GPIO 0; pin 30	SPI0 SDI	SPI0 SDI
P0[29]/SCK0	14	GPIO 0; pin 29	GPIO 0; pin 29	SPI0 SCK	SPI0 SCK
P0[28]/SCS0	15	GPIO 0; pin 28	GPIO 0; pin 28	SPI0 SCS	SPI0 SCS
$V_{SS(IO)}$	16	I/O pins ground			
P0[27]/SDO1	17	GPIO 0; pin 27	GPIO 0; pin 27	SPI1 SDO	SPI1 SDO
$V_{DD(CORE)}$	18	core supply voltage 1.8 V			
$V_{SS(CORE)}$	19	digital core ground			
P0[26]/SDI1	20	GPIO 0; pin 26	GPIO 0; pin 26	SPI1 SDI	SPI1 SDI
P0[25]/SCK1	21	GPIO 0; pin 25	GPIO 0; pin 25	SPI1 SCK	SPI1 SCK

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Table 2: LQFP144 pin assignment *...continued*

Symbol	Pin	Description			
		Default function	Function 1	Function 2	Function 3
P0[24]/SCS1	22	GPIO 0; pin 24	GPIO 0; pin 24	SPI1 SCS	SPI1 SCS
$V_{DD(IO)}$	23	I/O pins supply voltage 3.3 V			
P0[23]/SDO2/A[23]	24	GPIO 0; pin 23	SPI2 SDO	EXT BUS A23	EXT BUS A23
P0[22]/SDI2/A[22]	25	GPIO 0; pin 22	SPI2 SDI	EXT BUS A22	EXT BUS A22
P0[21]/SCK2/A[21]	26	GPIO 0; pin 21	SPI2 SCK	EXT BUS A21	EXT BUS A21
P0[20]/SCS2/A[20]	26	GPIO 0; pin 20	SPI2 SCS	EXT BUS A20	EXT BUS A20
$V_{SS(IO)}$	28	I/O pins ground			
P0[19]/A[19]	29	GPIO 0; pin 19	GPIO 0; pin 19	EXT BUS A19	EXT BUS A19
P0[18]/A[18]	30	GPIO 0; pin 18	GPIO 0; pin 18	EXT BUS A18	EXT BUS A18
P0[17]/A[17]	31	GPIO 0; pin 17	GPIO 0; pin 17	EXT BUS A17	EXT BUS A17
P0[16]/A[16]	32	GPIO 0; pin 16	GPIO 0; pin 16	EXT BUS A16	EXT BUS A16
$V_{DD(IO)}$	33	I/O pins supply voltage 3.3 V			
P0[15]/A[15]	34	GPIO 0; pin 15	GPIO 0; pin 15	EXT BUS A15	EXT BUS A15
P0[14]/A[14]	35	GPIO 0; pin 14	GPIO 0; pin 14	EXT BUS A14	EXT BUS A14
TDI	36	test data input; pulled-up internally			
TDO	37	test data output			
P0[13]/A[13]	38	GPIO 0; pin 13	GPIO 0; pin 13	EXT BUS A13	EXT BUS A13
P0[12]/A[12]	39	GPIO 0; pin 12	GPIO 0; pin 12	EXT BUS A12	EXT BUS A12
$V_{SS(IO)}$	40	I/O pins ground			
P0[11]/A[11]	41	GPIO 0; pin 11	GPIO 0; pin 11	EXT BUS A11	EXT BUS A11
P0[10]/A[10]	42	GPIO 0; pin 10	GPIO 0; pin 10	EXT BUS A10	EXT BUS A10
P0[9]/A[9]	43	GPIO 0; pin 9	GPIO 0; pin 9	EXT BUS A9	EXT BUS A9
P0[8]/A[8]	44	GPIO 0; pin 8	GPIO 0; pin 8	EXT BUS A8	EXT BUS A8
$V_{DD(IO)}$	45	I/O pins supply voltage 3.3 V			
P0[7]/A[7]	46	GPIO 0; pin 7	GPIO 0; pin 7	EXT BUS A7	EXT BUS A7
P0[6]/A[6]	47	GPIO 0; pin 6	GPIO 0; pin 6	EXT BUS A6	EXT BUS A6
P0[5]/A[5]	48	GPIO 0; pin 5	GPIO 0; pin 5	EXT BUS A5	EXT BUS A5
P0[4]/A[4]	49	GPIO 0; pin 4	GPIO 0; pin 4	EXT BUS A4	EXT BUS A4
$V_{SS(IO)}$	50	I/O pins ground			
P0[3]/A[3]	51	GPIO 0; pin 3	GPIO 0; pin 3	EXT BUS A3	EXT BUS A3
P0[2]/A[2]	52	GPIO 0; pin 2	GPIO 0; pin 2	EXT BUS A2	EXT BUS A2
P0[1]/A[1]	53	GPIO 0; pin 1	GPIO 0; pin 1	EXT BUS A1	EXT BUS A1
$V_{SS(CORE)}$	54	digital core ground			
$V_{DD(CORE)}$	55	core supply voltage 1.8 V			
P0[0]/A[0]	56	GPIO 0; pin 0	GPIO 0; pin 0	EXT BUS A0	EXT BUS A0
$V_{DD(IO)}$	57	I/O pins supply voltage 3.3 V			
P2[29]/CS0	58	GPIO 2; pin 29	GPIO 2; pin 29	EXT BUS CS0	EXT BUS CS0
P2[28]/CS1	59	GPIO 2; pin 28	GPIO 2; pin 28	EXT BUS CS1	EXT BUS CS1
P2[27]/EI3/CS2	60	GPIO 2; pin 27	EXTINT3	EXT BUS CS2	EXT BUS CS2
P2[26]/EI2/CS3	61	GPIO 2; pin 26	EXTINT2	EXT BUS CS3	EXT BUS CS3

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Table 2: LQFP144 pin assignment *...continued*

Symbol	Pin	Description			
		Default function	Function 1	Function 2	Function 3
P2[25]/EI1	62	GPIO 2; pin 25	GPIO 2; pin 25	EXTINT1	EXTINT1
P2[24]/EI0	63	GPIO 2; pin 24	GPIO 2; pin 24	EXTINT0	EXTINT0
P2[23]/CAP1[0]/MAT1[0]	64	GPIO 2; pin 23	GPIO 2; pin 23	TIMER1 CAP0	TIMER1 MAT0
P2[22]/CAP2[0]/MAT2[0]	65	GPIO 2; pin 22	GPIO 2; pin 22	TIMER2 CAP0	TIMER2 MAT0
$V_{DD(ADC)}$	66	ADC supply voltage and high reference level			
VREFN	67	ADC low reference level			
AI3	68	analog input for channel 3 and channel 7			
AI2	69	analog input for channel 2 and channel 6			
AI1	70	analog input for channel 1 and channel 5			
AI0	71	analog input for channel 0 and channel 4			
TRST_N	72	test reset input; pulled-up internally (active LOW)			
$V_{SS(IO)}$	73	I/O pins ground			
P2[21]/RXDL0	74	GPIO 2; pin 21	GPIO 2; pin 21	LIN0 RXDL	LIN0 RXDL
P2[20]/TXDL0	75	GPIO 2; pin 20	GPIO 2; pin 20	LIN0 TXDL	LIN0 TXDL
P2[19]/RXD/RXDL1	76	GPIO 2; pin 19	UART RXD	LIN1 RXDL	LIN1 RXDL
P2[18]/TXD/TXDL1	77	GPIO 2; pin 18	UART TXD	LIN1 TXDL	LIN1 TXDL
P2[17]/RXDL2/RXDC5	78	GPIO 2; pin 17	LIN2 RXDL	CAN5 RXDC	CAN5 RXDC
P2[16]/TXDL2/TXDC5	79	GPIO 2; pin 16	LIN2 TXDL	CAN5 TXDC	CAN5 TXDC
P2[15]/RXDL3/RXDC4	80	GPIO 2; pin 15	LIN3 RXDL	CAN4 RXDC	CAN4 RXDC
P2[14]/TXDL3/TXDC4	81	GPIO 2; pin 14	LIN3 TXDL	CAN4 TXDC	CAN4 TXDC
$V_{DD(IO)}$	82	I/O pins supply voltage 3.3 V			
P2[13]/RXDC3	83	GPIO 2; pin 13	GPIO 2; pin 13	CAN3 RXDC	CAN3 RXDC
P2[12]/TXDC3	84	GPIO 2; pin 12	GPIO 2; pin 12	CAN3 TXDC	CAN3 TXDC
P2[11]/RXDC2	85	GPIO 2; pin 11	GPIO 2; pin 11	CAN2 RXDC	CAN2 RXDC
P2[10]/TXDC2	86	GPIO 2; pin 10	GPIO 2; pin 10	CAN2 TXDC	CAN2 TXDC
P2[9]/RXDC1	87	GPIO 2; pin 9	GPIO 2; pin 9	CAN1 RXDC	CAN1 RXDC
P2[8]/TXDC1	88	GPIO 2; pin 8	GPIO 2; pin 8	CAN1 TXDC	CAN1 TXDC
P2[7]/RXDC0	89	GPIO 2; pin 7	GPIO 2; pin 7	CAN0 RXDC	CAN0 RXDC
$V_{SS(CORE)}$	90	digital core ground			
$V_{DD(CORE)}$	91	core supply voltage 1.8 V			
P2[6]/TXDC0	92	GPIO 2; pin 6	GPIO 2; pin 6	CAN0 TXDC	CAN0 TXDC
$V_{SS(IO)}$	93	I/O pins ground			
P2[5]/BLS3	94	GPIO 2; pin 5	GPIO 2; pin 5	EXT BUS BLS3	EXT BUS BLS3
P2[4]/BLS2	95	GPIO 2; pin 4	GPIO 2; pin 4	EXT BUS BLS2	EXT BUS BLS2
P2[3]/BLS1	96	GPIO 2; pin 3	GPIO 2; pin 3	EXT BUS BLS1	EXT BUS BLS1
P2[2]/BLS0	97	GPIO 2; pin 2	GPIO 2; pin 2	EXT BUS BLS0	EXT BUS BLS0
P2[1]/WE_N	98	GPIO 2; pin 1	GPIO 2; pin 1	EXT BUS WEN	EXT BUS WEN
P2[0]/OE_N	99	GPIO 2; pin 0	GPIO 2; pin 0	EXT BUS OEN	EXT BUS OEN
$V_{DD(IO)}$	100	I/O pins supply voltage 3.3 V			
P1[0]/D[0]	101	GPIO 1; pin 0	GPIO 1; pin 0	EXT BUS D0	EXT BUS D0

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Table 2: LQFP144 pin assignment *...continued*

Symbol	Pin	Description			
		Default function	Function 1	Function 2	Function 3
P1[1]/D[1]	102	GPIO 1; pin 1	GPIO 1; pin 1	EXT BUS D1	EXT BUS D1
P1[2]/D[2]	103	GPIO 1; pin 2	GPIO 1; pin 2	EXT BUS D2	EXT BUS D2
P1[3]/D[3]	104	GPIO 1; pin 3	GPIO 1; pin 3	EXT BUS D3	EXT BUS D3
$V_{SS(IO)}$	105	I/O pins ground			
P1[4]/D[4]	106	GPIO 1; pin 4	GPIO 1; pin 4	EXT BUS D4	EXT BUS D4
P1[5]/D[5]	107	GPIO 1; pin 5	GPIO 1; pin 5	EXT BUS D5	EXT BUS D5
TMS	108	test mode select input; pulled-up internally			
TCK	109	test clock input			
P1[6]/D[6]	110	GPIO 1; pin 6	GPIO 1; pin 6	EXT BUS D6	EXT BUS D6
P1[7]/D[7]	111	GPIO 1; pin 7	GPIO 1; pin 7	EXT BUS D7	EXT BUS D7
$V_{DD(IO)}$	112	I/O pins supply voltage 3.3 V			
P1[8]/D[8]	113	GPIO 1; pin 8	GPIO 1; pin 8	EXT BUS D8	EXT BUS D8
P1[9]/D[9]	114	GPIO 1; pin 9	GPIO 1; pin 9	EXT BUS D9	EXT BUS D9
P1[10]/D[10]	115	GPIO 1; pin 10	GPIO 1; pin 10	EXT BUS D10	EXT BUS D10
P1[11]/D[11]	116	GPIO 1; pin 11	GPIO 1; pin 11	EXT BUS D11	EXT BUS D11
$V_{SS(IO)}$	117	I/O pins ground			
P1[12]/D[12]	118	GPIO 1; pin 12	GPIO 1; pin 12	EXT BUS D12	EXT BUS D12
P1[13]/D[13]	119	GPIO 1; pin 13	GPIO 1; pin 13	EXT BUS D13	EXT BUS D13
P1[14]/D[14]	120	GPIO 1; pin 14	GPIO 1; pin 14	EXT BUS D14	EXT BUS D14
P1[15]/D[15]	121	GPIO 1; pin 15	GPIO 1; pin 15	EXT BUS D15	EXT BUS D15
$V_{DD(IO)}$	122	I/O pins supply voltage 3.3 V			
P1[16]/CAP3[3]/D[16]/MAT3[3]	123	GPIO 1; pin 16	TIMER3 CAP3	EXT BUS D16	TIMER3 MAT3
P1[17]/CAP3[2]/D[17]/MAT3[2]	124	GPIO 1; pin 17	TIMER3 CAP2	EXT BUS D17	TIMER3 MAT2
P1[18]/CAP3[1]/D[18]/MAT3[1]	125	GPIO 1; pin 18	TIMER3 CAP1	EXT BUS D18	TIMER3 MAT1
$V_{DD(CORE)}$	126	core supply voltage 1.8 V			
$V_{SS(CORE)}$	127	digital core ground			
P1[19]/CAP3[0]/D[19]/MAT3[0]	128	GPIO 1; pin 19	TIMER3 CAP0	EXT BUS D19	TIMER3 MAT0
$V_{SS(IO)}$	129	I/O pins ground			
P1[20]/CAP2[3]/D[20]/MAT2[3]	130	GPIO 1; pin 20	TIMER2 CAP3	EXT BUS D20	TIMER2 MAT3
P1[21]/CAP2[2]/D[21]/MAT2[2]	131	GPIO 1; pin 21	TIMER2 CAP2	EXT BUS D21	TIMER2 MAT2
P1[22]/CAP2[1]/D[22]/MAT2[1]	132	GPIO 1; pin 22	TIMER2 CAP1	EXT BUS D22	TIMER2 MAT1
P1[23]/CAP1[3]/D[23]/MAT1[3]	133	GPIO 1; pin 23	TIMER1 CAP3	EXT BUS D23	TIMER1 MAT3
$V_{DD(IO)}$	134	I/O pins supply voltage 3.3 V			
P1[24]/CAP1[2]/D[24]/MAT1[2]	134	GPIO 1; pin 24	TIMER1 CAP2	EXT BUS D24	TIMER1 MAT2
P1[25]/CAP1[1]/D[25]/MAT1[1]	136	GPIO 1; pin 25	TIMER1 CAP1	EXT BUS D25	TIMER1 MAT1
P1[26]/CAP0[3]/D[26]/MAT0[3]	137	GPIO 1; pin 26	TIMER0 CAP3	EXT BUS D26	TIMER0 MAT3
P1[27]/CAP0[2]/D[27]/MAT0[2]	138	GPIO 1; pin 27	TIMER0 CAP2	EXT BUS D27	TIMER0 MAT2
$V_{SS(IO)}$	139	I/O pins ground			
P1[28]/CAP0[1]/D[28]/MAT0[1]	140	GPIO 1; pin 28	TIMER0 CAP1	EXT BUS D28	TIMER0 MAT1
P1[29]/CAP0[0]/D[29]/MAT0[0]	141	GPIO 1; pin 29	TIMER0 CAP0	EXT BUS D29	TIMER0 MAT0

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Table 2: LQFP144 pin assignment *...continued*

Symbol	Pin	Description			
		Default function	Function 1	Function 2	Function 3
P1[30]/RTCK/D[30]	142	GPIO 1; pin 30	RTCK	EXT BUS D30	EXT BUS D30
P1[31]/D[31]	143	GPIO 1; pin 31	GPIO 1; pin 31	EXT BUS D31	EXT BUS D31
$V_{DD(IO)}$	144	I/O pins supply voltage 3.3 V			

7. Functional description

7.1 Reset and power-up behavior

The SJA2020 contains an external reset input and an internal power-up reset circuitry. This circuitry ensures a reset is internally extended until oscillators, PLL and Flash have reached a stable state. See Section 12 for characteristics of the several start-up and initialization times. Table 3 shows the reset pin.

Table 3: Reset pin

Symbol	Direction	Description
RESET_N	IN	external reset input, active LOW; pulled-up internally

7.2 JTAG interface and debug pins

The SJA2020 contains boundary scan test logic according to IEEE 1149.1, in this document further referred to as 'JTAG'. The JTAG pins can be used to connect a debugger probe for the embedded ARM processor. Pin JTAGSEL selects between the boundary scan mode and debug mode. See User manual for more information (see Ref. 1). Table 4 shows the JTAG pins.

Table 4: JTAG and debug interface

Symbol	Direction	Description
JTAGSEL	IN	TAP controller select input; LOW level selects ARM debug mode and HIGH level selects boundary scan and flash programming; pulled-up internally
TRST_N	IN	test reset input; pulled-up internally (active LOW)
TMS	IN	test mode select input; pulled-up internally
TDI	IN	test data input, pulled-up internally
TDO	OUT	test data output
TCK	IN	test clock input
RTCK	OUT	synchronized ARM debug return clock output (multiplexed with other functions on a device pin, see Section 6)

7.3 Power supply pins description

Table 5 shows the power supply pins. See User manual (see Ref. 1) for more information on physical constraints and board design issues.

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Table 5: Power supplies

Symbol	Description
$V_{DD(CORE)}$	core supply voltage 1.8 V
$V_{SS(CORE)}$	core ground
$V_{DD(IO)}$	I/O supply voltage 3.3 V
$V_{SS(IO)}$	I/O ground
$V_{DD(OSC\_PLL)}$	oscillator and PLL supply voltage 1.8 V
$V_{SS(OSC)}$	oscillator ground
$V_{DD(RTC)}$	real time clock oscillator supply voltage 1.8 V
$V_{SS(RTC)}$	real time clock oscillator ground
$V_{DD(ADC)}$	ADC supply voltage 3.3 V
$V_{SS(PLL)}$	PLL ground

7.4 Clock architecture

As can be seen in Figure 3, the SJA2020 is partitioned into so called subsystems or blocks. The subsystems concept allows the several functional parts to be configured individually with respect to the power mode that is used in each of them. Subsystems and or blocks are grouped into ‘clock-domains’. In this way clocks can be switched on or off and the response to sleep/wake-up events can be set per clock domain. In Section 8.3.1 these features are described in more detail.

Figure 3 gives a simplified view of how the SJA2020 is split into several ‘clock-domains’.

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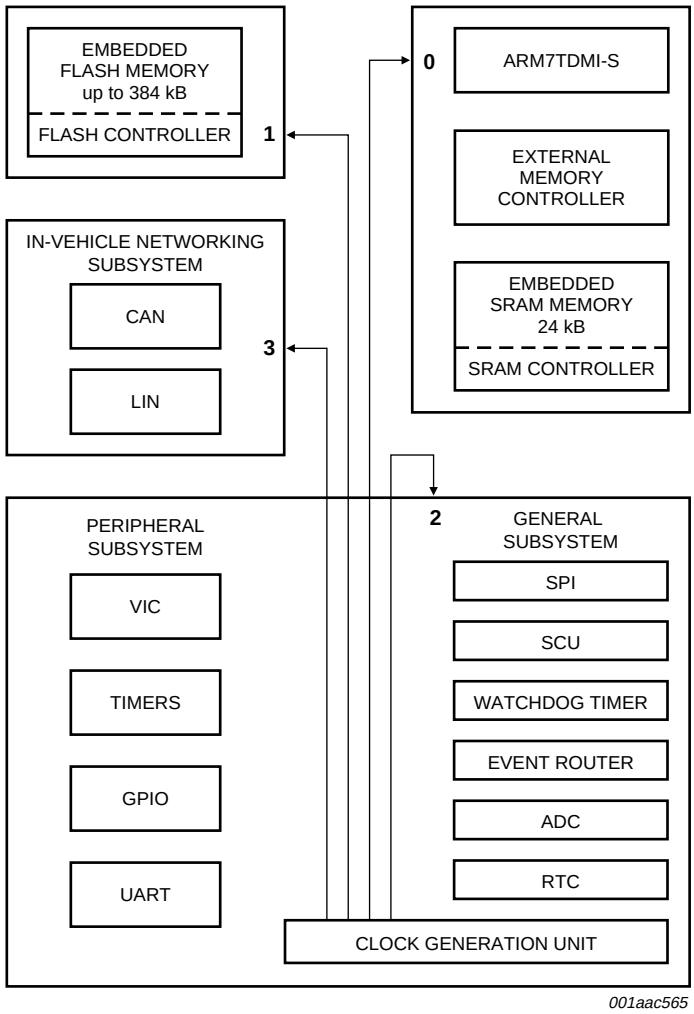

Fig 3. Clock domains in the SJA2020

7.5 Memory maps

ARM7 processors have 4 GB address space. The SJA2020 has divided this memory space into 8 regions of 512 MB each. Each region is used for a dedicated purpose.

An exception to this is region 0; several of the other regions (or a part of it) can be shadowed in the memory map at this region. This shadowing can be controlled by software via the programmable re-mapping registers.

Figure 4 gives a graphical overview of the SJA2020 memory map.

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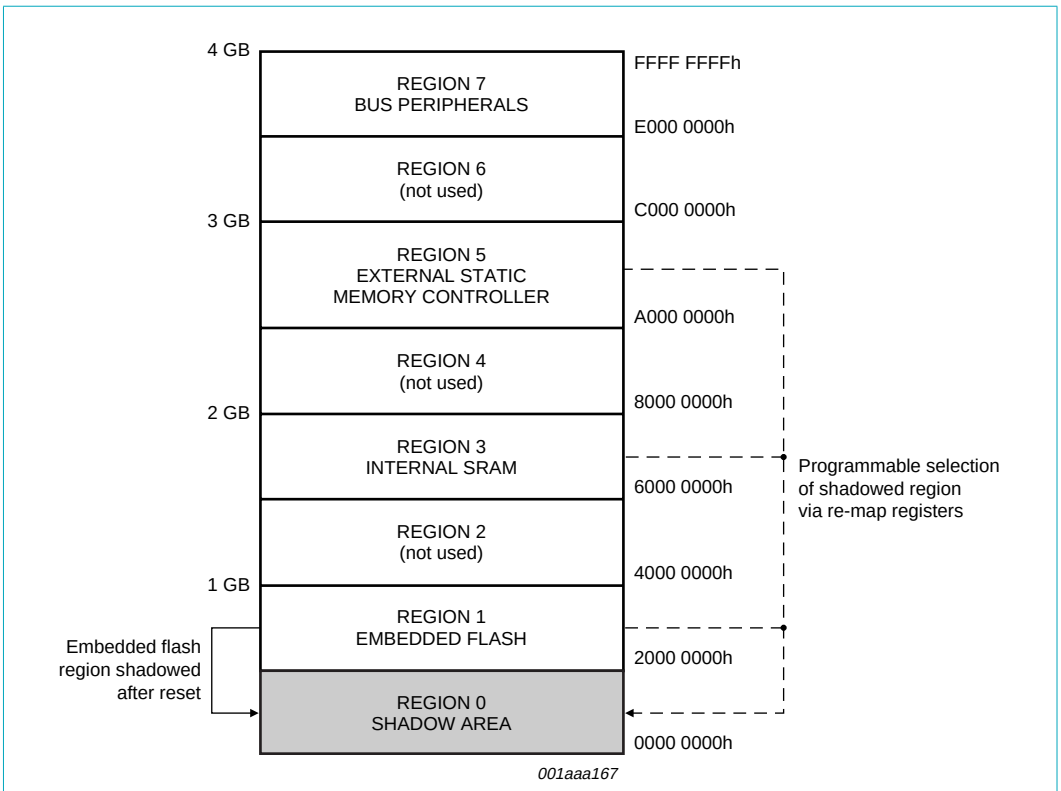

Fig 4. AHB system memory map graphical overview

7.5.1 Region 0: remap area

The ARM7TDMI-S processor has its exception vectors located at address logic 0. Since flash is the only non-volatile memory available in the SJA2020, the exception vectors in the flash must be located at address logic 0 after reset. Memory re-mapping from flash to SRAM is therefore introduced to improve performance.

To enable memory re-mapping, the SJA2020 AHB system memory map provides a shadow area (region 0) starting at address logic 0. This is a virtual memory region, i.e. no actual memory is present at the shadow area addresses. A selectable region of the AHB system memory map is, apart from its own specific region, also accessible via this shadow area region.

After reset, the region 1 embedded flash area is always available at the shadow area. After booting, any other region of the AHB system memory map (e.g. internal SRAM) can be re-mapped to region 0 by means of the shadow memory mapping register. For more details about the shadow area see Section 8.3.2.4.

7.5.2 Region 1: embedded flash area

Figure 5 gives a graphical overview of the embedded flash memory map.

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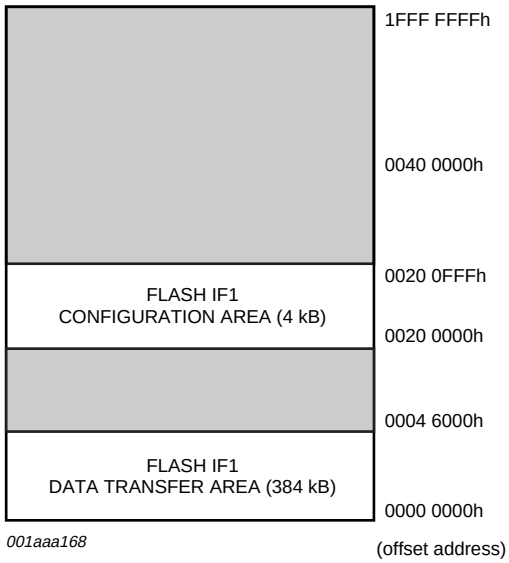

Address: 2000 0000h to 3FFF FFFFh.

Fig 5. Region 1 embedded flash memory

Region 1 is reserved for the embedded flash. For each embedded flash instance a data area of 2 MB (to be prepared for larger flash memory instance) and a configuration area of 4 kB are reserved. Although the SJA2020 contains only one embedded flash instance, the memory aperture per embedded flash instance is defined at 4 MB.

7.5.3 Region 2: not used

7.5.4 Region 3: internal SRAM area

Figure 6 gives a graphical overview of the internal SRAM memory map.

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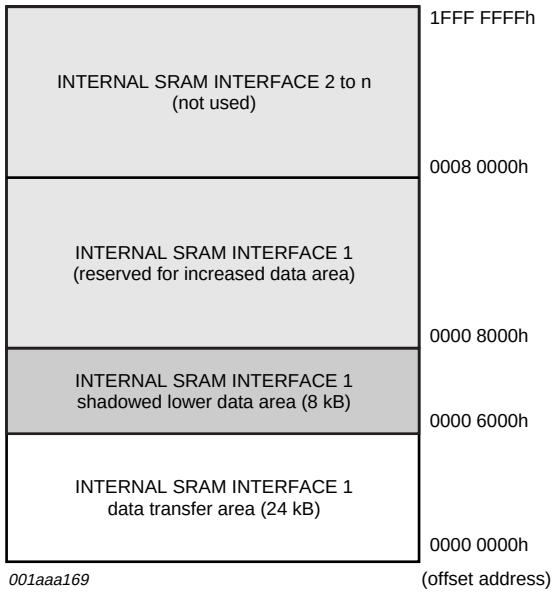

Address: 6000 0000h to 7FFF FFFFh.

Fig 6. Region 3 internal SRAM memory

Region 3 is reserved for internal SRAM. For each internal SRAM instance a data area of 512 kB is reserved. Although the SJA2020 has only one internal SRAM instance, the memory aperture per internal SRAM instance is defined at 512 kB.

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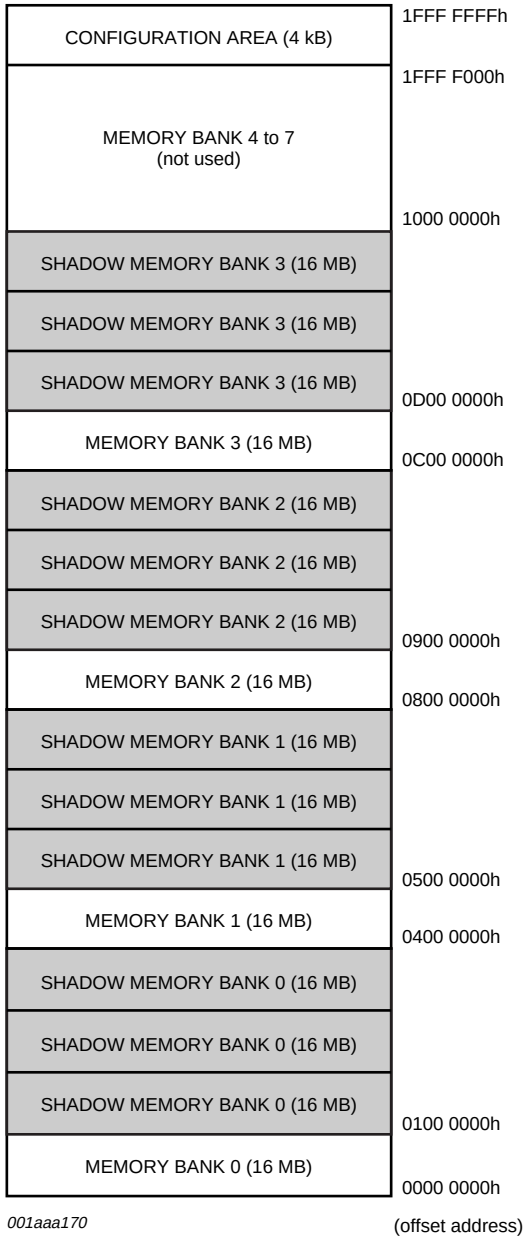
7.5.5 Region 4: not used

7.5.6 Region 5: static memory controller area



Address: A000 0000h to BFFF FFFFh.

Fig 7. Region 5 static memory controller

Figure 7 gives a graphical overview of the static memory controller memory map.

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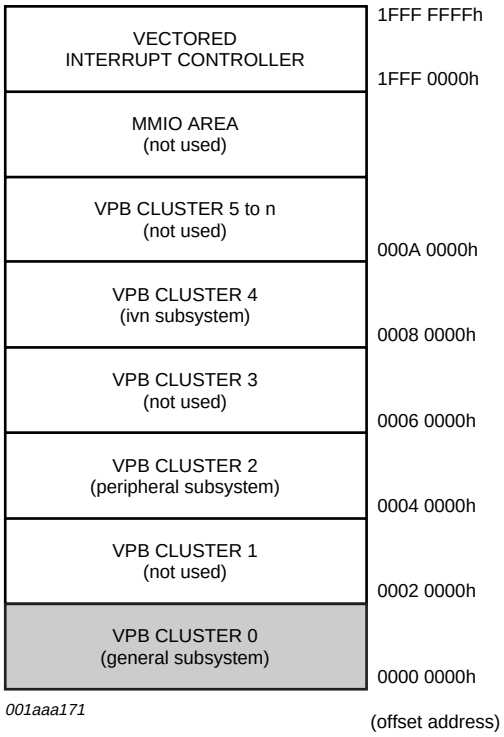
Region 5 is reserved for the static memory controller. The SJA2020 provides I/O pins for 4 bank select signals and 24 address lines. This implies that 4 memory banks of 16 MB each can be externally addressed. Due to the static memory controller hardware configuration, each bank of 16 MB data area is mirrored four times in a 64 MB region memory map.

The static memory controller configuration area is located on top of region 5.

7.5.7 Region 6: not used

7.5.8 Region 7: bus peripherals area

Figure 8 gives a graphical overview of the bus peripherals area memory map.



Address: E000 0000h to FFFF FFFFh.

Fig 8. Region 7 bus peripherals area memory

Region 7 is reserved for all ‘stand-alone’ memory mapped register interfaces. Examples of such peripherals are DTL target modules connected to the AHB bus via AHB2DTL adapters and VPB peripherals connected via AHB2VPB bridges.

The lower part of region 7 is again divided into VPB clusters. A VPB cluster is typically used as the address space for a set of VPB peripherals connected to a single AHB2VPB bridge, the slave on the AHB system bus. The clusters are aligned on 128 kB boundaries. In the SJA2020 three VPB clusters are in use. The VPB peripherals are aligned on 4 kB boundaries inside the VPB clusters.

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The upper part of region 7 is used as the memory area where memory mapped register interfaces of 'stand-alone' AHB peripherals reside. Each of these peripherals will be a slave on the AHB system bus. In the SJA2020 only one of such slave is present: the interrupt controller. It is a DTL target connected to the AHB system bus via an AHB2DTL adapter.

7.5.9 Memory map concepts operation

The basic concept on the SJA2020 is that each memory area has a 'natural' location in the memory map. This is the address range for which code residing in that area is written. Each memory space remains permanently fixed in the same location, eliminating the need to have portions of the code designed to run in different address ranges.

Because of the location of the interrupt vectors on the ARM7 processor (at addresses 0000 0000h through 0000 001Ch) (see Table 6), the embedded flash, internal SRAM or even external memories can be re-mapped to the shadow memory area in order to allow alternative uses of interrupts in the different operating modes. After reset, the embedded flash is re-mapped into the shadow memory area by default.

The SJA2020 generates the appropriate bus cycle abort exception if an access is attempted for an address that is in a reserved or not used address region and unassigned peripheral spaces. For these areas, both attempted data access and instruction fetch generate an exception. Note that write access address should be word aligned in ARM code or halfword aligned in Thumb code. Byte aligned writes are performed as word or halfword aligned writes without error signalling.

Within the address space of an existing peripheral, a data abort exception is not generated in response to an access to an undefined address. Address decoding within each peripheral is limited to that needed to distinguish defined registers within the peripheral itself. Details of address aliasing within a peripheral space are not defined in the SJA2020 documentation and are not a supported feature.

Note that the ARM stores the prefetch abort flag along with the associated instruction (which will be meaningless) in the pipeline and processes the abort only if an attempt is made to execute the instruction fetched from the illegal address. This prevents accidental aborts that could be caused by prefetches that occur when code is executed very near a memory boundary.

Table 7 gives the base address overview of all peripherals.

Table 6: Interrupt vectors address table

Address	Exception
0000 0000h	reset
0000 0004h	undefined instruction
0000 0008h	software interrupt
0000 000Ch	prefetch abort (instruction fetch memory fault)
0000 0010h	data abort (data access memory fault)
0000 0014h	reserved
0000 0018h	IRQ
0000 001Ch	FIQ

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Table 7: Peripherals base address overview

Base address	Base name	AHB peripherals
Memory region 0 to 6		
0000 0000h		shadow area memory
2000 0000h		embedded flash memory
2020 0000h	FMC RegBase	embedded flash controller configuration registers
6000 0000h		internal SRAM memory
A000 0000h		external static memory
BFFF F000h	SMC RegBase	static memory controller configuration registers
VPB cluster 0: general subsystem		
E000 0000h	CGU RegBase	clock generation unit
E000 1000h	SCU RegBase	system control unit
E000 2000h	SPI RegBase	SPI 0
E000 3000h	SPI RegBase	SPI 1
E000 4000h	SPI RegBase	SPI 2
E000 5000h	ADC RegBase	ADC
E000 6000h	WD RegBase	watchdog
E000 8000h	ER RegBase	event router
E000 A000h	RTC RegBase	real time clock
VPB cluster 2: peripheral subsystem		
E004 0000h	TIMER RegBase	timer 0
E004 1000h	TIMER RegBase	timer 1
E004 2000h	TIMER RegBase	timer 2
E004 3000h	TIMER RegBase	timer 3
E004 4000h	UART RegBase	16C550 UART
E004 5000h	GPIO RegBase	general purpose I/O 0
E004 6000h	GPIO RegBase	general purpose I/O 1
E004 7000h	GPIO RegBase	general purpose I/O 2
VPB cluster 4: in-vehicle networking subsystem		
E008 0000h	CANC RegBase	CAN controller 0
E008 1000h	CANC RegBase	CAN controller 1
E008 2000h	CANC RegBase	CAN controller 2
E008 3000h	CANC RegBase	CAN controller 3
E008 4000h	CANC RegBase	CAN controller 4
E008 5000h	CANC RegBase	CAN controller 5
E008 6000h	CANAFM RegBase	CAN ID-look-up table memory
E008 7000h	CANAFR RegBase	CAN acceptance filter registers
E008 8000h	CANCS RegBase	CAN central status registers
E008 9000h	LIN RegBase	LIN master controller 0
E008 A000h	LIN RegBase	LIN master controller 1
E008 B000h	LIN RegBase	LIN master controller 2

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Table 7: Peripherals base address overview *…continued*

Base address	Base name	AHB peripherals
E008 C000h	LIN RegBase	LIN master controller 3
Vector interrupt controller		
FFFF F000h	VIC RegBase	vectored interrupt controller

8. Block description

8.1 Flash memory controller

8.1.1 Overview

The Flash Memory Controller (FMC) interfaces to the embedded flash memory with two tasks:

- Providing memory data transfer
- Memory configuration via triggering, programming and erasing

The flash memory has a 128-bit wide data interface and the flash controller offers two 128-bit buffer lines to improve the system performance. Initially, the flash has to be programmed via JTAG. In-system programming must be supported by the boot loader. In-application programming is possible. The flash memory contents can be protected by disabling the JTAG access. Suspending of burning or erasing is not supported.

The key features are:

- Programming by CPU via AHB
- Programming by external programmer via JTAG
- JTAG access protection
- Burn-finished and erased-finished interrupt

After reset, the flash initialization is started which takes t_{init} time. During this initialization flash access is not possible and AHB transfers to the flash are stalled, thus blocking the AHB bus.

During the flash initialization, the index sector is read to identify the status of the JTAG access protection and sector security. In case the JTAG access protection is active, the flash is not accessible via JTAG anymore and the ARM debug facilities have been disabled to protect the flash memory contents against unwanted reading out externally. If the sector security is active, the concerning sector is read only.

The flash can be read synchronously or asynchronously to the system clock. In synchronous operation, the flash goes into standby after returning the read data. Started reads cannot be stopped and therefore speculative reading and dual buffering is not supported.

With asynchronous reading, the transfer of the address to the flash, and read data from the flash are done asynchronously, yielding in the fastest possible response time. Started reads can be stopped and therefore speculative reading and dual buffering is supported.

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Buffering is offered because the flash has a 128-bit wide data interface, while the AHB interface has only 32 bits. With buffering, a buffer line holds the complete 128 bits flash word, from which 4 words can be read. Without buffering, every AHB data port read starts a flash read. A flash read is a slow process compared to the minimum AHB cycle time. With buffering, the average read time is reduced which can improve the system performance.

With single buffering, the most recently read flash word stays available until the next flash read. When an AHB data port read transfer requires data from the same flash word as the previous read transfer, no new flash read is done, and the read data is given without wait cycles.

When an AHB data port read transfer requires data from a different flash word as the previous read transfer, a new flash read is done, and wait states are given until the new read data is available.

With dual buffering, a secondary buffer line is used. The output of the flash is considered as the primary buffer. On a primary buffer hit, data can be copied to the secondary buffer line, which allows the flash to start a speculative read of the next flash word.

Both buffer lines are invalidated after:

- Initialization
- Configuration register access
- Data latch reading
- Index sector reading

The modes of operation are listed in Table 8.

Table 8: Flash read modes

Buffering	Configuration bit				Characteristics and features
	FS_DCR	FS_CACHEBYP	CACHE2EN	Special ways	
Synchronous timing					
No buffer line	0	1	X	X	for single (non linear) reads, one flash word read per word read
Single buffer line	0	0	X	X	default mode of operation; most recently read flash word is kept until another flash word is required
Asynchronous timing					
No buffer line	1	1	X	X	one flash word read per word read
Single buffer line	1	0	0	X	most recently read flash word is kept until another flash word is required
Dual buffer line, single speculative	1	0	1	0	on a buffer miss, a flash read is done, followed by at most one speculative read; optimized for execution of code with small loops (< 8 words) from flash
Dual buffer line, always speculative	1	0	1	1	most recently used flash word is copied into second buffer line, next flash word read is started; highest performance for linear reads

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8.1.2 Flash memory controller pin description

The flash memory controller has no external pins.

8.1.3 Flash memory layout

The ARM processor can program the flash for ISP and IAP. Note that the flash always has to be programmed by flash words (of 128-bit).

The flash memory is organized in equal sectors of 8 kB that must be erased before data can be written into them. The flash memory also has sector wise protection. Writing occurs per page which consists of 4096 bits (32 flash words). Thus a sector contains 16 pages.

Table 9 and Table 10 give an overview of the flash sector and page addressing.

Table 9: Flash sector overview

Sector number	Sector base address
0	0000 0000h
1	0000 2000h
2	0000 4000h
3	0000 6000h
4	0000 8000h
5	0000 A000h
6	0000 C000h
7	0000 E000h
8	0001 0000h
9	0001 2000h
10	0001 4000h
11	0001 6000h
12	0001 8000h
13	0001 A000h
14	0001 C000h
15	0001 E000h
16	0002 0000h
17	0002 2000h
18	0002 4000h
19	0002 6000h
20	0002 8000h
21	0002 A000h
22	0002 C000h
23	0002 E000h
24	0003 0000h
25	0003 2000h
26	0003 4000h
27	0003 6000h
28	0003 8000h

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Table 9: Flash sector overview *...continued*

Sector number	Sector base address
29	0003 A000h
30	0003 C000h
31	0003 E000h
32	0004 0000h
33	0004 2000h
34	0004 4000h
35	0004 6000h
36	0004 8000h
37	0004 A000h
38	0004 C000h
39	0004 E000h
40	0005 0000h
41	0005 2000h
42	0005 4000h
43	0005 6000h
44	0005 8000h
45	0005 A000h
46	0005 C000h
47	0005 E000h

Table 10: Page addressing overview

Page number	Page base address
0	0000 0000h
1	0000 0200h
2	0000 0400h
3	0000 0600h
4	0000 0800h
5	0000 0A00h
6	0000 0C00h
7	0000 0E00h
8	0000 1000h
9	0000 1200h
10	0000 1400h
11	0000 1600h
12	0000 1800h
13	0000 1A00h
14	0000 1C00h
15	0000 1E00h

The index sector is a special sector in which the JTAG access protection and sector security are located. The address space becomes visible by setting the FS_ISS bit and overlaps the regular flash sectors address space.

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Note that the index sector can not be erased and access to index sector has to be performed via code outside the flash.

8.1.4 Register mapping

The flash memory controller registers are shown in Table 11. The flash memory controller registers have an offset to the base address FMC RegBase which can be found in the memory map (see Table 7).

Table 11: Flash memory controller register summary

Address offset	Type	Reset value	Name	Description	Reference
000h	R/W	0005h	FCTR	flash control register	see Table 12
004h	-	-	reserved	reserved register; do not modify	
008h	R/W	0000h	FPTR	flash program time register	see Table 13
00Ch	-	-	reserved	reserved register; do not modify	
010h	R/W	C004h	FBWST	flash bridge wait state register	see Table 14
014h	-	-	reserved	reserved register; do not modify	
018h	-	-	reserved	reserved register; do not modify	
01Ch	R/W	000h	FCRA	flash clock divider register	see Table 15
020h	R/W	0000h	FMSSTART	flash BIST start address register	see Table 16
024h	R/W	0 0000h	FMSSTOP	flash BIST stop address register	see Table 17
028h	-	-	reserved	reserved register; do not modify	
02Ch	R	-	FMSW0	flash 128-bit signature word 0 register	see Table 18
030h	R	-	FMSW1	flash 128-bit signature word 1 register	see Table 19
034h	R	-	FMSW2	flash 128-bit signature word 2 register	see Table 20
038h	R	-	FMSW3	flash 128-bit signature word 3 register	see Table 21
FD8h	W	-	INT_CLR_ENABLE	flash clear interrupt enable register	see Table 27
FDCh	W	-	INT_SET_ENABLE	flash set interrupt enable register	see Table 26
FE0h	R	0h	INT_STATUS	flash interrupt status register	see Table 22
FE4h	R	0h	INT_ENABLE	flash interrupt enable register	see Table 25
FE8h	W	-	INT_CLR_STATUS	flash clear interrupt status register	see Table 24
FECh	W	-	INT_SET_STATUS	flash set interrupt status register	see Table 23

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8.1.5 Flash control register (FCTR)

The flash control register is used to select read modes, and to control the programming of the flash memory.

The flash has data latches to store the data that is to be programmed into the flash. Instead of reading the flash contents, the data latch contents of the flash can be read. Data latch reading is always done without buffering, with the programmed number of wait states (WST) on every beat of the burst. Data latch reading can be done both synchronously and asynchronously. Data latch reading is selected with the FS_RLD bit.

Index sector reading is always done without buffering, with the programmed number of wait states (WST) on every beat of the burst. Index sector reading can be done both synchronously and asynchronously. Index sector reading is selected with the FS_ISS bit.

Table 12 shows the bit assignment of the FCTR register.

Table 12. FCTR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 16	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
15	FS_LOADREQ	R/W		data load request
			1	the flash is written if FS_WRE has been set; the data load is automatically triggered after the last word was written to the load register; this bit is automatically cleared and thus always read as logic 0
			0*	
14	FS_CACHECLR	R/W		buffer line clear
			1	all bits of the data transfer register are set
			0*	
13	FS_CACHEBYP	R/W		buffering bypass
			1	reading from flash is without buffering
			0*	the read buffering is active
12	FS_PROGREQ	R/W		programming request
			1	flash programming is requested
			0*	
11	FS_RLS	R/W		select sector latches for reading
			1	the sector latches are read
			0*	the flash array is read
10	FS_PDL	R/W		preset data latches
			1	all bits in the data latches are set
			0*	
9	FS_PD	R/W		power down
			1	the flash is in power down
			0*	the flash is not in power down
8	reserved	-	-	reserved; do not modify, write as logic 0, read as logic 0

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Table 12. FCTR register bit description *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7	FS_WPB	R/W		program and erase protection
			1	program and erase have been enabled
			0*	program and erase have been disabled
6	FS_ISS	R/W		index sector selection
			1	the index sector will be read
			0*	the flash array will be read
5	FS_RLD	R/W		read data latches
			1	the data latches are read for verification of data that is loaded to be programmed
			0*	the flash array is read
4	FS_DCR	R/W		DC read mode
			1	asynchronous reading has been selected
			0*	synchronous reading has been selected
3	reserved	-	-	reserved; do not modify, write as logic 0, read as logic 0
2	FS_WEB	R/W		program and erase enable
			1*	program and erase have been disabled
			0	program and erase have been enabled
1	FS_WRE	R/W		program and erase selection
			1	program and data load have been selected
			0*	erase has been selected
0	FS_CS	R/W		flash chip select
			1*	the flash is active
			0	the flash is in standby

8.1.6 Flash program time register (FPTR)

The flash program time register controls the timer for burning and erasing the flash memory. It also allows to read the remaining burn or erase time.

The erase time to be programmed can be calculated from the following formula:

$$TR = \frac{t_{er(sect)}}{512 \times t_{clk(sys)}}$$

The burn time to be programmed can be calculated from the following formula:

$$TR = \frac{t_{wr(pg)}}{512 \times t_{clk(sys)}}$$

Table 13 shows the bit assignment of the FPTR register.

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Table 13. FPTR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 16	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
15	EN_T	R/W		program timer enable
			1	the flash program timer has been enabled
			0*	the flash program timer has been disabled
14 to 0	TR[14:0]	R/W	0000h*	program timer; the (remaining) burn and erase time is 512 × TR clock cycles

8.1.7 Flash bridge wait states register (FBWST)

The flash bridge wait states register controls the number of wait states that is inserted for flash read transfers. This register also controls the second buffer line for asynchronous reading.

To eliminate the delay that is associated with synchronizing the flash read data, a predefined number of wait states has to be programmed which depends on the flash response time and the system clock period. The minimum wait states value WST can be calculated with the following formulas:

- Synchronous reading: $WST > \frac{t_{a(clk)}}{t_{clk(sys)}} - 1$
- Asynchronous reading: $WST > \frac{t_{a(A)}}{t_{clk(sys)}} - 1$

In case the programmed number of wait states is more than three, flash data reading cannot be performed at full speed if speculative reading is active.

Table 14 shows the bit assignment of the FBWST register.

Table 14. FBWST register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 16	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
15	CACHE2EN	R/W		dual buffering enable
			1*	the second buffer line has been enabled
			0	the second buffer line has been disabled
14	SPECALWAYS	R/W		speculative reading
			1*	always speculative reading is performed
			0	single speculative reading is performed
13 to 8	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
7 to 0	WST[7:0]	R/W	04h*	number of wait states; contains the number of wait states to be inserted for flash reading; the minimum calculated value must be programmed for proper flash read operation

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8.1.8 Flash clock divider register (FCRA)

The flash clock divider register controls the clock divider for the flash program and erase clock CRA. This clock should be programmed to 66 kHz during burning or erasing.

The CRA clock frequency fed to the flash memory is the system clock frequency divided by 3 × (FCRA + 1). The programmed value must result in a CRA clock frequency of 66 kHz ± 20 %.

Table 15 shows the bit assignment of the FCRA register.

Table 15. FCRA register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 12	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
11 to 0	FCRA[11:0]	R/W	000h*	clock divider setting; when logic 0, no CRA clock is fed to the flash memory

8.1.9 Flash BIST control registers (FMSSTART and FMSSTOP)

The flash BIST control registers control the embedded BIST signature generation via the BIST start address register FMSSTART and the BIST stop address register FMSSTOP.

A signature can be generated for any part of the flash contents. The address range to be used for the generation is defined by writing the start address to the BIST start address register and the stop address to the BIST stop address register. The BIST start and stop addresses must be flash word aligned and can be derived from the AHB byte addresses through division by 16. The signature generation is started by setting the BIST start bit in the BIST stop address register. Setting the BIST start bit is typically combined with defining the signature stop address.

Note that the flash access is blocked during the BIST signature calculation. The duration of the flash BIST is $t_{BIST} = (t_{fl(BIST)} + 3 \times t_{clk(sys)}) \times (FMSSTOP - FMSSTART + 1)$

See Section 12 for $t_{fl(BIST)}$.

Table 16 and Table 17 show the bit assignment of the FMSSTART and FMSSTOP registers, respectively.

Table 16. FMSSTART register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 17	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
16 to 0	FMSSTART[16:0]	R/W	0 0000h*	BIST start address (corresponds to AHB byte address [20:4])

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Table 17. FMSSTOP register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 18	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
17	MISR_START	R/W		BIST start
			1	the BIST signatures generation is initiated
			0*	
16 to 0	FMSSTOP[16:0]	R/W	0 0000h*	BIST stop address (corresponds to AHB byte address [20:4])

8.1.10 Flash BIST signature registers (FMSW0, FMSW1, FMSW2 and FMSW3)

The flash BIST signature registers return the signatures as produced by the embedded signature generator. There is a a 128-bit signature reflected by the four registers FMSW0, FMSW1, FMSW2 and FMSW3.

The generated signature by the flash can be used to verify the flash contents. The generated signature can be compared with an expected signature and makes the more time and code consuming procedure of reading back all contents superfluous.

Table 18, Table 19, Table 20 and Table 21 show the bit assignment of the FMSW0 and FMSW1, FMSW2, FMSW3 registers, respectively.

Table 18. FMSW0 register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	FMSW0[31:0]	R	-	flash BIST 128-bit signature (bits 31 to 0)

Table 19. FMSW1 register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	FMSW1[63:32]	R	-	flash BIST 128-bit signature (bits 63 to 32)

Table 20. FMSW2 register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	FMSW2[95:64]	R	-	flash BIST 128-bit signature (bits 95 to 64)

Table 21. FMSW3 register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	FMSW3[127:96]	R	-	flash BIST 128-bit signature (bits 127 to 96)

8.1.11 Flash interrupt status register (INT_STATUS)

The flash interrupt status register shows the active interrupt requests. The corresponding interrupt enable needs to be set.

The INT_STATUS is read only. Table 22 shows the bit assignment of the INT_STATUS register.

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Table 22. INT_STATUS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 3	reserved	-	-	reserved; do not modify, read as logic 0
2	END_OF_MISR	R		signature interrupt
			1	the BIST signature generation has finished or logic 1 is written to bit INT_SET_STATUS[2]
			0*	no interrupt is pending or logic 1 is written to bit INT_CLR_STATUS[2]
1	END_OF_BURN	R		burn interrupt
			1	the page burning has finished or logic 1 is written to bit INT_SET_STATUS[1]
			0*	no interrupt is pending or logic 1 is written to bit INT_CLR_STATUS[1]
0	END_OF_ERASE	R		erase interrupt
			1	the erasing of one or more sectors has finished or logic 1 is written to bit INT_SET_STATUS[0]
			0*	no interrupt is pending or logic 1 is written to bit INT_CLR_STATUS[0]

8.1.12 Flash set interrupt status (INT_SET_STATUS)

The flash set interrupt status register sets the bits in the flash interrupt status register.

The INT_SET_STATUS register is write only. Table 23 shows the bit assignment of the INT_SET_STATUS register.

Table 23. INT_SET_STATUS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 3	reserved	-	-	reserved; do not modify, read as write
2 to 0	INT_SET_STATUS[2:0]	W	-	
			1	the corresponding bit in the flash interrupt status register is set
			0	the corresponding bit in the flash interrupt status register is unchanged

8.1.13 Flash clear interrupt status (INT_CLR_STATUS)

The flash clear interrupt status register clears the bits in the flash interrupt status register.

The INT_CLR_STATUS register is write only. Table 24 shows the bit assignment of the INT_CLR_STATUS register.

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Table 24. INT_CLR_STATUS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 3	reserved	-	-	reserved; do not modify, read as write
2 to 0	INT_CLR_STATUS[2:0]	W	-	
			1	the corresponding bit in the flash interrupt status register is cleared
			0	the corresponding bit in the flash interrupt status register is unchanged

8.1.14 Flash interrupt enable (INT_ENABLE)

The flash interrupt enable register determines when the flash interface gives an interrupt request if the corresponding interrupt enable has been set.

The INT_ENABLE register is read only. Table 25 shows the bit assignment of the INT_ENABLE register.

Table 25. INT_ENABLE register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 3	reserved	-	-	reserved; do not modify, read as logic 0
2	END_OF_MISR	R		BIST signature interrupt enable
			1	bit INT_SET_ENABLE[2] is set to enable the BIST signature interrupt
			0*	bit INT_CLR_ENABLE[2] is reset to disable the interrupt
1	END_OF_BURN	R		BIST signature interrupt enable
			1	bit INT_SET_ENABLE[1] is set to enable the BIST signature interrupt
			0*	bit INT_CLR_ENABLE[1] is reset to disable the interrupt
0	END_OF_ERASE	R		BIST signature interrupt enable
			1	bit INT_SET_ENABLE[0] is set to enable the BIST signature interrupt
			0*	bit INT_CLR_ENABLE[0] is reset to disable the interrupt

8.1.15 Flash set interrupt enable (INT_SET_ENABLE)

The flash set interrupt enable register sets the bits in the flash interrupt enable register.

The INT_SET_ENABLE register is write only. Table 26 shows the bit assignment of the INT_SET_ENABLE register.

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Table 26. INT_SET_ENABLE register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 3	reserved	-	-	reserved; do not modify, read as write
2 to 0	SET_ENABLE[2:0]	W	-	
			1	the corresponding bit in the flash interrupt enable register is set
			0	the corresponding bit in the flash interrupt enable register is unchanged

8.1.16 Flash clear interrupt enable (INT_CLR_ENABLE)

The flash clear interrupt enable register clears the bits in the flash interrupt enable register.

The INT_CLR_ENABLE register is write only. Table 27 shows the bit assignment of the INT_CLR_ENABLE register.

Table 27. INT_CLR_ENABLE register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 3	reserved	-	-	reserved; do not modify, read as write
2 to 0	CLR_ENABLE[2:0]	W	-	
			1	the corresponding bit in the flash interrupt enable register is cleared
			0	the corresponding bit in the flash interrupt enable register is unchanged

8.2 Static memory controller

8.2.1 Overview

The static Static Memory Controller (SMC) provides an interface for external (off-chip) memory devices.

The key features are:

- Supports static memory-mapped devices including RAM, ROM, flash, burst ROM and external I/O devices
- Asynchronous page mode read operation in non-clocked memory subsystems
- Asynchronous burst mode read access to burst mode ROM devices
- Independent configuration for up to 4 banks, each up to 16 MB
- Programmable bus turnaround (idle) cycles (1 to 16)
- Programmable read and write wait states (up to 32), for static RAM devices
- Programmable initial and subsequent burst read wait state, for burst ROM devices
- Programmable write protection
- Programmable burst mode operation
- Programmable external data width: 8 bits, 16 bits or 32 bits
- Programmable read byte lane enable control

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The static memory controller supports up to four independently configurable memory banks simultaneously. Each memory bank can be 8 bits, 16 bits or 32 bits wide and is capable of supporting SRAM, ROM, flash EPROM, burst ROM memory or external I/O devices.

A separate chip select output is available for each bank. The chip select lines are configurable to be active HIGH or LOW. The memory bank selection is controlled by memory addressing. Table 28 shows the address mapping for the external memory banks; see also Figure 7.

Table 28. External memory bank address bit description

Bit	Symbol	Description
31 to 29	BA[2:0]	external static memory base address; the base address can be found in the memory map (see Table 7).
28	-	reserved; write as logic 0
27 to 26	CS[1:0]	chip select address space for 4 memory banks
		00: bank 0
		01: bank 1
		10: bank 2
		11: bank 3
25 to 24	-	reserved; write as logic 0
23 to 0	A[23:0]	16 MB memory banks address space

8.2.2 External memory controller pin description

The external memory controller module in the SJA2020 has the following pins. The pins are combined with other functions on the port pins of the SJA2020, see Section 8.3.2. Table 29 shows the external memory controller pins.

Table 29: External memory controller pins

Symbol	Direction	Description
EXTBUS CSx	OUT	memory bank x select, x runs from 0 to 3
EXTBUS BLSy	OUT	byte lane select y, y runs from 0 to 3
EXTBUS WE_N	OUT	write enable (active LOW)
EXTBUS OE_N	OUT	output enable (active LOW)
EXTBUS A[23:0]	OUT	address bus
EXTBUS D[31:0]	IN/OUT	data bus

8.2.3 Register mapping

The static memory controller memory banks configuration registers are shown in Table 30.

The memory banks configuration registers have an offset to the base address SMC RegBase which can be found in the memory map (see Table 7).

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Table 30: Static memory controller register summary

Address offset	Type	Width	Reset value	Name	Description	Reference
Bank 0						
000h	R/W	4	Fh	SMBIDCYR0	idle cycle control register for memory bank 0	see Table 31
004h	R/W	5	1Fh	SMBWST1R0	wait state 1 control register for memory bank 0	see Table 32
008h	R/W	5	1Fh	SMBWST2R0	wait state 2 control register for memory bank 0	see Table 33
00Ch	R/W	4	0h	SMBWSTOENR0	output enable assertion delay control register for memory bank 0	see Table 34
010h	R/W	4	1h	SMBWSTWENR0	write enable assertion delay control register for memory bank 0	see Table 35
014h	R/W	8	80h	SMBCR0	configuration register for memory bank 0	see Table 36
018h	R/W	2	0h	SMBSR0	status register for memory bank 0	see Table 37
Bank 1						
01Ch	R/W	4	Fh	SMBIDCYR1	idle cycle control register for memory bank 1	see Table 31
020h	R/W	5	1Fh	SMBWST1R1	wait state 1 control register for memory bank 1	see Table 32
024h	R/W	5	1Fh	SMBWST2R1	wait state 2 control register for memory bank 1	see Table 33
028h	R/W	4	0h	SMBWSTOENR1	output enable assertion delay control register for memory bank 1	see Table 34
02Ch	R/W	4	1h	SMBWSTWENR1	write enable assertion delay control register for memory bank 1	see Table 35
030h	R/W	8	00h	SMBCR1	configuration register for memory bank 1	see Table 36
034h	R/W	2	0h	SMBSR1	status register for memory bank 1	see Table 37
Bank 2						
038h	R/W	4	Fh	SMBIDCYR2	idle cycle control register for memory bank 2	see Table 31
03Ch	R/W	5	1Fh	SMBWST1R2	wait state 1 control register for memory bank 2	see Table 32
040h	R/W	5	1Fh	SMBWST2R2	wait state 2 control register for memory bank 2	see Table 33
044h	R/W	4	0h	SMBWSTOENR2	output enable assertion delay control register for memory bank 2	see Table 34
048h	R/W	4	1h	SMBWSTWENR2	write enable assertion delay control register for memory bank 2	see Table 35
04Ch	R/W	8	40h	SMBCR2	configuration register for memory bank 2	see Table 36
050h	R/W	2	0h	SMBSR2	status register for memory bank 2	see Table 37
Bank 3						
054h	R/W	4	Fh	SMBIDCYR3	idle cycle control register for memory bank 3	see Table 31
058h	R/W	5	1Fh	SMBWST1R3	wait state 1 control register for memory bank 3	see Table 32
05Ch	R/W	5	1Fh	SMBWST2R3	wait state 2 control register for memory bank 3	see Table 33
060h	R/W	4	0h	SMBWSTOENR3	output enable assertion delay control register for memory bank 3	see Table 34
064h	R/W	4	1h	SMBWSTWENR3	write enable assertion delay control register for memory bank 3	see Table 35
068h	R/W	8	00h	SMBCR3	configuration register for memory bank 3	see Table 36
06Ch	R/W	2	0h	SMBSR3	status register for memory bank 3	see Table 37

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8.2.4 Bank idle cycle control registers (SMBIDCYR)

The bank idle cycle control register configures the external bus turn around cycles between read and write memory accesses to avoid bus contention on the external memory data bus. The bus turn-around wait time is inserted between external bus transfers in case of:

- Read-to-read, to different memory banks
- Read-to-write, to the same memory bank
- Read-to-write, to different memory banks

Table 31 shows the bit assignment of the SMBIDCYR0 to SMBIDCYR3 registers.

Table 31. SMBIDCYRn register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 4	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
3 to 0	IDCY[3:0]	R/W	Fh*	idle or turn-around cycles; this register contains the number of bus turn-around cycles added between read and write accesses; the turn-round time is the programmed number of cycles times the system clock period

8.2.5 Bank wait state 1 control registers (SMBWST1R)

The bank wait state 1 control register configures the external transfer wait states in read accesses. The bank configuration register contains the enable and polarity setting for the external wait.

The minimum wait states value WST1 can be calculated from the following formula:

$$WST1 = \frac{t_{a(R)int} + t_{d(R)em}}{t_{clk(sys)}} - 1$$

Where:

$t_{a(R)int}$ = internal read access time, see Section 12.

$t_{d(R)em}$ = external memory read delay.

Table 32 shows the bit assignment of the SMBWST1R0 to SMBWST1R3 registers.

Table 32. SMBWST1Rn register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 5	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
4 to 0	WST1[4:0]	R/W	1Fh*	wait state 1; this register contains the length of read accesses, except for burst ROM where it defines the length of the first read access only; the read access time is the programmed number of wait states times the system clock period

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8.2.6 Bank wait state 2 control registers (SMBWST2R)

The bank wait state 2 control register configures the external transfer wait states in write accesses or the external transfer wait states in burst read accesses. The bank configuration register contains the enable and polarity setting for the external wait.

Sequential access burst reads from burst flash devices of the same type of as for burst ROM are supported. Due to sharing of the SMBWST2R register between write and burst read transfers, it is only possible to have one setting at a time for burst flash, either write delay or the burst read delay. This means that for write transfer the SMBWST2R register must be programmed with the write delay value, and for a burst read transfer the SMBWST2R register must be programmed with the burst access delay.

The minimum wait states value WST2 can be calculated from the following formula:

$$WST2 = \frac{t_{a(W)int} + t_{d(W)em}}{t_{clk(sys)}} - 1$$

Where:

$t_{a(W)int}$ = internal write access time, see Section 12.

$t_{d(W)em}$ = external memory write delay.

Table 33 shows the bit assignment of the SMBWST2R0 to SMBWST2R3 registers.

Table 33. SMBWST2Rn register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 5	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
4 to 0	WST2[4:0]	R/W	1Fh*	wait state 2; this register contains the length of write accesses, except for burst ROM where it defines the length of the burst read accesses; the write access time c.q. the burst ROM read access time is the programmed number of wait states times the system clock period

8.2.7 Bank output enable assertion delay control register (SMBWSTOENR)

The bank output enable assertion delay control register configures the delay between the assertion of the chip select and the output enable. This delay is used to reduce the power consumption for memories that are not able to provide valid data immediately after the chip select is asserted. The programmed value must be equal to, or less than the bank wait state 1 programmed value, as the access is timed by the wait states. The output enable is always de-asserted at the same time as the chip select, at the end of the transfer. The bank configuration register contains the enable for output assertion delay.

Table 34 shows the bit assignment of the SMBWSTOENR register.

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Table 34. SMBWSTOENR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 4	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
3 to 0	WSTOEN	R/W	0h*	output enable assertion delay; this register contains the length of the output enable delay after the chip select assertion; the output enable assertion delay time is the programmed number of wait states times the system clock period

8.2.8 Bank write enable assertion delay control register (SMBWSTWENR)

The bank write enable assertion delay control register configures the delay between the assertion of the chip select and the write enable. This delay is used to reduce the power consumption for memories. The programmed value must be equal to, or less than the bank wait state 2 programmed value, as the access is timed by the wait states. The write enable is asserted half a system clock cycle after the assertion of the chip select for logic 0 wait states. The write enable is de-asserted half a system clock cycle before the chip select, at the end of the transfer. The byte lane select outputs have the same timing as the write enable output for writes to 8-bit devices that use the byte lane selects instead of the write enables. The bank configuration register contains the enable for output assertion delay.

Table 35 shows the bit assignment of the SMBWSTWENR register.

Table 35. SMBWSTWENR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 4	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
3 to 0	WSTWEN	R/W	1h*	write enable assertion delay; this register contains the length of the write enable delay after the chip select assertion; the write enable assertion delay time is the programmed number of wait states times the system clock period

8.2.9 Bank configuration register (SMBCR)

The bank configuration register defines the memory bank access for the connected memory device.

It is allowed to initiate a wider data transfer to the external memory than the width of the external memory data bus. In this case the external transfer is automatically split up into several transfers to complete.

Table 36 shows the bit assignment of the SMBCR register.

Table 36. SMBCR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

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Table 36. SMBCR register bit description *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 6	MW[1:0]	R/W	bank default*	memory width; memory width configuration including the default memory width after reset
			00	8-bit, bank 3 and bank 1 reset (default)
			01	16-bit, bank 2 reset (default)
			10	32-bit, bank 0 reset (default)
			11	reserved
5	BM	R/W		burst mode
			1	sequential access burst reads to a maximum of four consecutive locations is supported to increase the bandwidth by using reduced access time; however, bursts crossing quad boundaries are split up so that the first transfer after the boundary uses the slow wait state 1 read timing
			0*	the memory bank is configured for nonburst memory
4	WP	R/W		write protect
			1	the connected device is write protected e.g. (burst) ROM, read only flash, or SRAM
			0*	no write protection is required e.g. SRAM or write enabled flash
3	CSPOL	R/W		chip select polarity
			1	the chip select input is active HIGH
			0*	the chip select input is active LOW
2 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	RBLE	R/W		read byte lane enable
			1	the byte lane select pins are held asserted (logic 0) during a read access; this is for 16-bit or 32-bit devices where the separate write enable signal is used and the byte lane selects must be held asserted during a read; the write enable pin WEN is used as the write enable in this configuration
			0*	the byte lane select pins BLSn are all de-asserted (logic 1) during a read access; this is for 8-bit devices where the byte lane enable is connected to the write enable pin, so it must be de-asserted during a read access (default at reset); the byte lane select pins are used as write enables in this configuration

8.2.10 Bank status register (SMBSR)

The bank status register reflects the status flags of each memory bank.

Table 37 shows the bit assignment of the SMBSR register.

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Table 37. SMBSR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 2	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
1	WRITEPROTERR	R/W		write protect error
			1	a write access to a write protected memory device was initiated; writing logic 1 to this register clears the write protect status flag
			0*	writing a logic 0 has no effect
0	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

8.3 General subsystem

8.3.1 Clock generation unit

8.3.1.1 Overview

The key features are:

- Power mode management
- Reset control
- Control oscillator
- Control PLL
- Fractional clock divider for ADC clock
- Watchdog bark register

8.3.1.2 Description

The clock generation unit configures all internal clocks. There are four options for the source for the system clock:

- Crystal/external oscillator
- PLL
- Ring oscillator (ringo)
- Real time clock

Furthermore, the control of the oscillators and PLL takes part here, generally also used for power mode management. The clock switching between the several sources is performed in a safe way (glitch free).

8.3.1.3 CGU pin description

The CGU module in the SJA2020 has the following pins. Table 38 shows the CGU pins.

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Table 38: CGU pins

Symbol	Direction	Description
RESET_N	IN	external reset input, active LOW; pulled-up internally
XOUT_OSC	OUT	oscillator crystal output
XIN_OSC	IN	oscillator crystal input or external clock input

8.3.1.4 Register mapping

The clock generation unit registers are shown in Table 39.

The clock generation unit registers have an offset to the base address CGU RegBase which can be found in the memory map (see Table 7).

Note: any clock frequency adjustment has direct impact on the timing of on-board peripherals such as UART, SPI, watchdog, timers, CAN controller, LIN master controller, ADC, flash memory interface.

Table 39: CGU register summary

Address	Type	Reset value	Name	Description	Reference
000h	R/W	1h	CSC	clock switch configuration register	see Table 40
004h	R/W	0h	CFS1	clock frequency select 1 register	see Table 41
008h	R/W	0h	CFS2	clock frequency select 2 register	see Table 41
00Ch	R	1h	CSS	clock switch status register	see Table 43
010h	R/W	1h	CPC0	AHB clock power control register	see Table 44
014h	R/W	1h	CPC1	flash clock power control register	see Table 44
018h	R/W	1h	CPC2	general and peripheral subsystem clock power control register	see Table 44
01Ch	R/W	1h	CPC3	in-vehicle networking subsystem clock power control register	see Table 44
020h	R/W	0h	CPC4	ADC clock power control register	see Table 44
024h	-	-	reserved	reserved register; do not modify	
028h	R	3h	CPS0	AHB clock power status register	see Table 46
02Ch	R	3h	CPS1	flash clock power status register	see Table 46
030h	R	3h	CPS2	general and peripheral subsystem clock power status register	see Table 46
034h	R	3h	CPS3	in-vehicle networking subsystem clock power status register	see Table 46
038h	R	2h	CPS4	ADC clock power status register	see Table 46
03Ch	-	-	reserved	reserved register; do not modify	
040h	-	-	reserved	reserved register; do not modify	
044h	-	-	reserved	reserved register; do not modify	
048h	-	-	reserved	reserved register; do not modify	
04Ch	-	-	reserved	reserved register; do not modify	
050h	R/W	0h	CFCE4	ADC fractional clock enable register	see Table 47
054h	-	-	reserved	reserved register; do not modify	
058h	R/W	7FFC 3FECh	CFD	fractional clock divider register	see Table 48

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Table 39: CGU register summary …continued

Address	Type	Reset value	Name	Description	Reference
C00h	R/W	1h	CPM	power mode register	see Table 49
C04h	R	0h	CWDB	watchdog bark register	see Table 51
C08h	R/W	1h	CRTCOPM	real time clock oscillator power mode register	see Table 52
C0Ch	-	-	reserved	reserved register; do not modify	
C10h	R/W	1h	COPM	oscillator power mode register	see Table 53
C14h	-	-	reserved	reserved register; do not modify	
C18h	R	1h	COLS	oscillator lock status register	see Table 54
C1Ch	-	-	reserved	reserved register; do not modify	
C20h	-	-	reserved	reserved register; do not modify	
C24h	-	-	reserved	reserved register; do not modify	
C28h	-	-	reserved	reserved register; do not modify	
C2Ch	-	-	reserved	reserved register; do not modify	
C30h	-	-	reserved	reserved register; do not modify	
C34h	-	-	reserved	reserved register; do not modify	
C38h	-	-	reserved	reserved register; do not modify	
C3Ch	-	-	reserved	reserved register; do not modify	
C40h	R/W	0h	CPCSS	PLL clock source select register	see Table 55
C44h	R/W	1h	CPPDM	PLL Power-down mode register	see Table 56
C48h	-	-	reserved	reserved register; do not modify	
C4Ch	R	0h	CPLS	PLL lock status register	see Table 57
C50h	-	-	reserved	reserved register; do not modify	
C54h	R/W	0h	CPMR	PLL multiplication ratio register	see Table 58
C58h	R/W	0h	CPPD	PLL post divider register	see Table 60
C5Ch	R/W	0h	CRPM	ring oscillator power mode register	see Table 62
C60h	R/W	18h	CRPD	ring oscillator post divider register	see Table 63
C64h	R/W	5h	CRFS	ring oscillator frequency select register	see Table 65

8.3.1.5 Clock switch configuration register (CSC)

The clock switch configuration register configures the side of the clock switch to be used as the system clock. There are two clock switch sides to avoid clock glitches when switching between the four clock source inputs: the oscillator frequency, the PLL frequency, the ringo and the real time clock.

Table 40 shows the bit assignment of the CSC register.

Table 40. CSC register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 2	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

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Table 40. CSC register bit description *...continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
1 to 0	ENF	R/W		switch select
			3h	reserved, do not use
			2h	the clock switch uses side 2 as source clock
			1h*	the clock switch uses side 1 as source clock
			0h	reserved, do not use

8.3.1.6 Clock frequency select registers (CFS1 and CFS2)

The clock frequency select registers determines the input clock source of side 1 and side 2 respectively of the frequency switch.

Table 41 shows the bit assignment of the CFS1 and CFS2 registers.

Table 41. CFS1 and CFS2 register bit assignment
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 2	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
1 to 0	FS1 for CFS1 FS2 for CFS2	R/W	0h*	input frequency select; see Table 42

Table 42: Input clock frequency sources

FS[1:0]	Function
00	oscillator frequency
01	PLL frequency
10	ring oscillator frequency (ringo)
11	RTC frequency

8.3.1.7 Clock switch status register (CSS)

The clock switch status control register represents the selected input clock source and clock switch status.

Table 43 shows the bit assignment of the CSS register.

Table 43. CSS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 4	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
3 to 2	FSS	R	0h*	frequency select status; see Table 42
1 to 0	FS_SELECT	R		switch select
			3h	reserved
			2h	the clock switch uses side 2 as source clock
			1h*	the clock switch uses side 1 as source clock
			0h	reserved

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8.3.1.8 Clock power control registers (CPC0, CPC1, CPC2, CPC3 and CPC4)

The AHB clock power control register (CPC0) configures the clock operation for the ARM processor, SRAM and static memory controller.

The flash clock power control register (CPC1) configures the clock operation for the flash.

The general and peripheral subsystem clock power control register (CPC2) configures the clock operation for the general subsystem, the peripheral subsystem and the modulation and sampling control subsystem.

The in-vehicle networking subsystem clock power control register (CPC3) configures the clock operation for the in-vehicle networking subsystem VPB cluster.

The ADC clock power control register (CPC4) configures the clock operation for the ADC.

Table 44 shows the bit assignment of the CPC registers.

Table 44. CPC register bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 3	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
2 to 1	WAKE	R/W	0h*	wake mode; see Table 45
0 in CPC0	reserved	-	1*	reserved; do not modify, read as logic 1, write as logic 1
0 in CPC1	RUN	R/W		run enable
			1*	the clock is enabled
			0	the clock is disabled
0 in CPC2	reserved	-	1*	reserved; do not modify, read as logic 1, write as logic 1
0 in CPC3	RUN	R/W		run enable
			1*	the clock is enabled
			0	the clock is disabled
0 in CPC4	RUN	R/W		run enable
			1	the clock is enabled
			0*	the clock is disabled

Table 45: Wake mode configuration bits

PM[1:0]	Function
00	wake up disabled, the clock is not switched off when entering a low power mode and not switched on an a wake up event
01	unsupported, results in unpredicted behavior
10	unsupported, results in unpredicted behavior
11	wake up enabled, the clock is switched off when entering a low power mode and switched on an a wake up event

8.3.1.9 Clock power status registers (CPS0, CPS1, CPS2, CPS3 and CPS4)

The AHB clock power status register (CPS0) reflects the operational status of the clock for the ARM processor, SRAM and static memory controller.

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The flash clock power status register (CPS1) reflects the operational status of the clock for the flash.

The general and peripheral subsystem clock power status register (CPS2) reflects the operational status of the clock for the general and peripheral subsystem VPB clusters.

The in-vehicle networking subsystem clock power status register (CPS3) reflects the operational status of the clock for the in-vehicle networking subsystem VPB cluster.

The ADC clock power status register (CPS4) reflects the operational status of the clock for the ADC.

Table 46 shows the bit assignment of the CPS0 register.

Table 46. CPS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 2	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
1	WAKEUP	R		wake up
			1*	the wake up condition is activated
			0	the wake up condition is not activated
0	ACTIVE	R	1* for CPS0, CPS1, CPS2 and CPS3; 0* for CPS4	active
			1	the clock is functional
			0	the clock is not functional

8.3.1.10 Fractional clock enable register (CFCE4)

The fractional clock enable register configures the fractional clock as clock source instead of the clock from the selected switch side. The fractional clock is only targeted for the ADC.

Table 47 shows the bit assignment of the CFCE4 register.

Table 47. CFCE4 register bits
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	FCE	R/W		fractional clock enable
			1	the fractional clock is the clock source
			0*	the clock from the selected switch side is the clock source

8.3.1.11 Fractional clock divider register (CFD)

The fractional clock divider register determines the clock input frequency for the ADC which may be maximum 4.5 MHz for correct operation.

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The ADC clock frequency is determined by the following formula: $f_{i(ADC)} = f_{clk(sys)} \times \frac{n}{m}$

To minimize the power consumption the values for n and m should be selected as large as possible. Note that the system clock frequency is at least twice ADC clock frequency:

$$f_{i(ADC)} \leq f_{clk(sys)} \times \frac{1}{2}$$

Table 48 shows the bit assignment of the CFD register.

Table 48. CFD register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
30 to 17	MSUB[13:0]	R/W	3FFEh*	fractional clock divider parameter MSUB; signed value defined by (– n)
16 to 3	MADD[13:0]	R/W	07FDh*	fractional clock divider parameter MADD; unsigned value defined by (m – n)
2	STRETCH	R/W		clock stretching
			1*	must be set to logic 1 to feed the required approximately 50 % duty cycle clock to the ADC
			0	
1	RESET	R/W		fractional divider reset
			1	the fractional clock divider is reset asynchronously; the reset must be active while changing the ADC clock frequency
			0*	
0	EN	R/W		enable
			1	the fractional clock divider is running to serve as the ADC clock if the ADC fractional clock is enabled in the fractional clock enable register
			0*	

8.3.1.12 Power mode register (CPM)

The power mode register configures the operation mode and wake up mechanism.

Table 49 shows the bit assignment of the CPM register.

Table 49. CPM register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 2	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
1 to 0	PM[1:0]	R/W	1h*	power mode; see Table 50

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Table 50: Power mode configuration bits

PM[1:0]	Function
00	unsupported
01	normal operation mode, this mode is automatically set after wake-up
10	unsupported, results in unpredicted behavior
11	Idle mode, wake-up event results in resume

8.3.1.13 Watchdog bark register (CWDB)

The watchdog bark register indicates whether a system reset was caused by the watchdog or not. This register is cleared only by an external or power-on reset.

Table 51 shows the bit assignment of the CWDB register.

Table 51. CWDB register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	WDB	R		watchdog bark
			1	a watchdog reset occurred
			0*	an external or power-on reset occurred

8.3.1.14 Real time clock oscillator power mode register (CRTCOPM)

The real time clock oscillator power mode register can switch off the 32 kHz oscillator. This is recommended in case the real time clock is not used. It is not allowed to switch on the real time clock oscillator again once switched off.

Table 52 shows the bit assignment of the CRTCOPM register.

Table 52. CRTCOPM register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	RTCOPM	R/W		real time clock oscillator power mode
			1*	the 32 kHz oscillator is active
			0	the 32 kHz oscillator is inactive and in Power-down mode

8.3.1.15 Oscillator power mode register (COPM)

The oscillator power mode register is used to switch on and off the system oscillator.

Table 53 shows the bit assignment of the COPM register.

Table 53. COPM register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

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Table 53. COPM register bit description …continued
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
0	OPM	R/W		oscillator power mode
			1*	the oscillator is active
			0	the system oscillator is inactive and in Power-down mode

8.3.1.16 Oscillator lock status register (COLS)

The oscillator lock status register represents the status of the oscillator clock frequency stability. The lock detector goes high after a delay based on a gray code counter.

Table 57 shows the bit assignment of the COLS register.

Table 54. COLS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	OLS	R		oscillator lock status
			1*	the oscillator is locked
			0	the oscillator is not in lock or in Power-down mode

8.3.1.17 PLL clock source select register (CPCSS)

The PLL clock source select register determines the input frequency for the PLL.

Table 55 shows the bit assignment of the CPCSS register.

Table 55. CPCSS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	PCSS	R/W		PLL clock source select
			1	the oscillator frequency is the input frequency for the PLL
			0*	no clock is fed to the PLL

8.3.1.18 PLL Power-down mode register (CPPDM)

The PLL Power-down mode register is used to switch on and off the PLL. The PLL must be in Power-down mode during configuration change.

Table 56 shows the bit assignment of the CPPDM register.

Table 56. CPPDM register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	PPDM	R/W		PLL Power-down mode
			1*	the PLL is inactive and in Power-down mode
			0	the PLL is active

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8.3.1.19 PLL lock status register (CPLS)

The PLL lock status register represents the status of the PLL clock frequency stability. The lock detector measures the phase difference between the rising edges of the input and feedback clocks.

Only when this difference is smaller than the so called 'lock criterion' for more than eight consecutive input clock periods, the lock output switches from LOW to HIGH. A single too large phase difference immediately resets the counter and causes the lock signal to drop (if it was HIGH). Requiring eight phase measurements in a row to be below a certain figure ensures that the lock detector will not indicate lock until both the phase and frequency of the input and feedback clocks are very well aligned. This effectively prevents false lock indications, and thus ensures a glitch free lock signal.

Table 57 shows the bit assignment of the CPLS register.

Table 57. CPLS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	PLS	R		PLL lock status
			1	the PLL is locked
			0*	the PLL is not in lock or in Power-down mode

8.3.1.20 PLL multiplication ratio register (CPMR)

The PLL multiplication ratio register defines the ratio between the PLL output clock and the input clock.

The multiplication ratio can be calculated from the following formula: $PMR = \frac{f_{clk(sys)}}{f_{i(osc)}}$

Table 58 shows the bit assignment of the CPMR register.

Table 58. CPMR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 3	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
2 to 0	PMR[2:0]	R/W	00h*	PLL multiplication ratio; see Table 59

Table 59: Multiplication ratio configuration bits

PMR[2:0]	Function
000	input frequency multiplication by 1
001	input frequency multiplication by 2
010	input frequency multiplication by 3
011	input frequency multiplication by 4
100	input frequency multiplication by 5
101	input frequency multiplication by 6
110	unsupported, results in unpredicted behavior
111	unsupported, results in unpredicted behavior

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8.3.1.21 PLL post divider register (CPPD)

The PLL post divider register defines division ratio between the PLL CCO frequency and PLL output clock frequency. The post division guarantees an output clock with a 50 % duty cycle. The CCO frequency must fulfil the specified limits.

The post division ratio can be calculated from the following formula: $PPD = \frac{f_{CCO}}{f_{clk(sys)}}$

Table 60 shows the bit assignment of the CPPD register.

Table 60. CPPD register bits
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 2	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
1 to 0	PPD[1:0]	R/W	0h*	PLL post divider; see Table 61

Table 61: PLL post divider configuration bits

PPD[1:0]	Function
00	post division by 2
01	post division by 4
10	post division by 8
11	post division by 16

8.3.1.22 Ring oscillator power mode register (CRPM)

The ring oscillator power mode register is used to switch on and off the ring oscillator.

Figure 9 shows the structure of the ring oscillator.

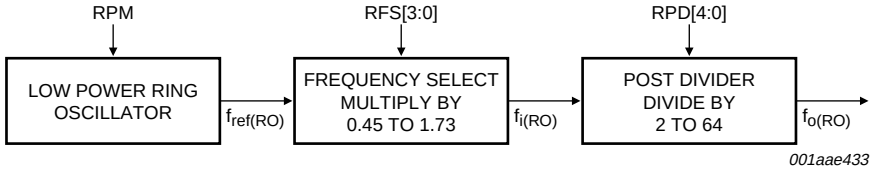

Fig 9. Ring oscillator block diagram

Table 62 shows the bit assignment of the CRPM register.

Table 62. CRPM register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	RPM	R/W		oscillator power mode
			1	the ring oscillator is active
			0*	the ring oscillator is inactive and in Power-down mode

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8.3.1.23 Ring oscillator post divider register (CRPD)

The ring oscillator post divider register defines division ratio between the calibrated internal ring oscillator frequency (see Section 8.3.1.24) and ring oscillator output clock frequency. The post division guarantees an output clock with a 50 % duty cycle.

The post division ratio can be calculated from the following formula:

$$f_{o(RO)} = \frac{f_{i(RO)}}{2 \times (RPD + 1)}$$

Table 63 shows the bit assignment of the CRPD register.

Table 63. CRPD register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 5	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
4 to 0	RPD[4:0]	R/W	18h*	ring oscillator post divider; see Table 64

Table 64: Ring oscillator post divider configuration bits

RPD[4:0]	Function
00000	post division by 2
00001	post division by 4
00010	post division by 6
00011	post division by 8
...	...
11110	post division by 62
11111	post division by 64

8.3.1.24 Ring oscillator frequency select register (CRFS)

The ring oscillator frequency select ratio register is used to calibrate the internal ring oscillator frequency $f_{i(RO)}$ to compensate for frequency variation in the internal ring oscillator reference frequency $f_{ref(RO)}$. See Section 12 for the specified range of $f_{ref(RO)}$.

Table 65 shows the bit assignment of the CRFS register.

Table 65. CRFS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 4	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
3 to 0	RFS[3:0]	R/W	5h*	ring oscillator frequency select; see Table 66

Table 66. Ring oscillator frequency select configuration bits

RFS[3:0]	Function
0000	$f_{i(RO)} = 0$ Hz
0001	$f_{i(RO)} = f_{ref(RO)} \times 0.45$
0010	$f_{i(RO)} = f_{ref(RO)} \times 0.63$
0011	$f_{i(RO)} = f_{ref(RO)} \times 0.77$
0100	$f_{i(RO)} = f_{ref(RO)} \times 0.89$

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Table 66. Ring oscillator frequency select configuration bits *...continued*

RFS[3:0]	Function
0101	$f_{i(RO)} = f_{ref(RO)} \times 1.00$
0110	$f_{i(RO)} = f_{ref(RO)} \times 1.10$
0111	$f_{i(RO)} = f_{ref(RO)} \times 1.18$
1000	$f_{i(RO)} = f_{ref(RO)} \times 1.26$
1001	$f_{i(RO)} = f_{ref(RO)} \times 1.34$
1010	$f_{i(RO)} = f_{ref(RO)} \times 1.41$
1011	$f_{i(RO)} = f_{ref(RO)} \times 1.48$
1100	$f_{i(RO)} = f_{ref(RO)} \times 1.55$
1101	$f_{i(RO)} = f_{ref(RO)} \times 1.61$
1110	$f_{i(RO)} = f_{ref(RO)} \times 1.67$
1111	$f_{i(RO)} = f_{ref(RO)} \times 1.73$

8.3.2 System control unit

8.3.2.1 Overview

The system control unit takes care of system related functions.

The key features are:

- Shadow memory remapping
- Configuration of I/O port pins multiplexer

Firstly, the mapping of a (partially) region into the shadow memory area. After reset, the flash region is shadowed. To increase the overall system performance, (a part of) the internal SRAM region is advised to shadow for interrupt handling.

Secondly, the function of each I/O pin. The I/O pin configuration should be consistent with the peripheral function usage.

8.3.2.2 SCU pin description

The SCU has no external pins.

8.3.2.3 Register mapping

The system control unit registers are shown in Table 67.

The system control unit registers have an offset to the base address SCU RegBase which can be found in the memory map (see Table 7).

Table 67: SCU register summary

Address	Type	Reset value	Name	Description	Reference
00h	R/W	2000 0000h	SSMM	shadow memory mapping register	see Table 68
04h	R/W	0000 0000h	SFSAP0	function select A port 0 register	see Table 70
08h	R/W	0000 0000h	SFSBP0	function select B port 0 register	see Table 71
0Ch	R/W	0000 0000h	SFSAP1	function select A port 1 register	see Table 70
10h	R/W	0000 0000h	SFSBP1	function select B port 1 register	see Table 71
14h	R/W	0000 0000h	SFSAP2	function select A port 2 register	see Table 70

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Table 67: SCU register summary …continued

Address	Type	Reset value	Name	Description	Reference
18h	R/W	0000 0000h	SFSBP2	function select B port 2 register	see Table 71
1Ch	R/W	0000 0000h	SPUCP0	pull-up control port 0 register	see Table 75
20h	R/W	0000 0000h	SPUCP1	pull-up control port 1 register	see Table 75
24h	R/W	0000 0000h	SPUCP2	pull-up control port 2 register	see Table 75

8.3.2.4 Shadow memory mapping register (SSMM)

The shadow memory mapping register defines which part of the memory region is present in the shadow memory area. The shadow memory mapping start address is the pointer within a region indicating the for shadowing in the shadow area starting at location 0000 0000h. In this way a whole region or only a part of the flash, SRAM or external memory bank can be remapped to the shadow area.

Table 68 shows the bit assignment of the SSMM register.

Table 68. SSMM register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 10	SMMSA[21:0]	R/W	2000 0000h*	shadow memory map start address; memory start address for mapping (a part of) a region to the shadow area; the start address is aligned on 1 kB boundaries and therefore the lowest 10 bits must be always logic 0
9 to 0	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

8.3.2.5 Port function select registers (SFSAP0 to SFSAP2 and SFSBP0 to SFSBP2)

The port function select register configures the pin functions individually on the corresponding I/O port. The function select A registers define the lower 16 port pins and the function select B registers define the upper 16 port pins. For port 2, the two most upper port pins are reserved.

See Table 72 to Table 74 for the pin function multiplex content.

The pin function selection is done with 2 bits in the port function select registers (see Table 69).

Table 69: Pin function select configuration bits

Value bits [1:0]	Function
00	select pin function 0 from corresponding I/O port configuration
01	select pin function 1 from corresponding I/O port configuration
10	select pin function 2 from corresponding I/O port configuration
11	select pin function 3 from corresponding I/O port configuration

Table 70 shows the bit assignment of the SFSAP0, SFSAP1 and SFSAP2 registers and Table 71 shows the bit assignment of the SFSBP0, SFSBP1 and SFSBP2 registers. at

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Table 70. SFSAP0, SFSAP1 and SFSAP2 register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 30	PFSP15[1:0]	R/W	0h*	port pin 15 function select
29 to 28	PFSP14[1:0]	R/W	0h*	port pin 14 function select
27 to 26	PFSP13[1:0]	R/W	0h*	port pin 13 function select
25 to 24	PFSP12[1:0]	R/W	0h*	port pin 12 function select
23 to 22	PFSP11[1:0]	R/W	0h*	port pin 11 function select
21 to 20	PFSP10[1:0]	R/W	0h*	port pin 10 function select
19 to 18	PFSP9[1:0]	R/W	0h*	port pin 9 function select
17 to 16	PFSP8[1:0]	R/W	0h*	port pin 8 function select
15 to 14	PFSP7[1:0]	R/W	0h*	port pin 7 function select
13 to 12	PFSP6[1:0]	R/W	0h*	port pin 6 function select
11 to 10	PFSP5[1:0]	R/W	0h*	port pin 5 function select
9 to 8	PFSP41:0]	R/W	0h*	port pin 4 function select
7 to 6	PFSP3[1:0]	R/W	0h*	port pin 3 function select
5 to 4	PFSP2[1:0]	R/W	0h*	port pin 2 function select
3 to 2	PFSP1[1:0]	R/W	0h*	port pin 1 function select
1 to 0	PFSP0[1:0]	R/W	0h*	port pin 0 function select

Table 71. SFSBP0, SFSBP1 and SFSBP2 register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 30	PFSP31[1:0]	R/W	0h*	port pin 31 function select; reserved for port 2
29 to 28	PFSP30[1:0]	R/W	0h*	port pin 30 function select; reserved for port 2
27 to 26	PFSP29[1:0]	R/W	0h*	port pin 29 function select
25 to 24	PFSP28[1:0]	R/W	0h*	port pin 28 function select
23 to 22	PFSP27[1:0]	R/W	0h*	port pin 27 function select
21 to 20	PFSP26[1:0]	R/W	0h*	port pin 26 function select
19 to 18	PFSP25[1:0]	R/W	0h*	port pin 25 function select
17 to 16	PFSP24[1:0]	R/W	0h*	port pin 24 function select
15 to 14	PFSP23[1:0]	R/W	0h*	port pin 23 function select
13 to 12	PFSP22[1:0]	R/W	0h*	port pin 22 function select
11 to 10	PFSP21[1:0]	R/W	0h*	port pin 21 function select
9 to 8	PFSP20[1:0]	R/W	0h*	port pin 20 function select
7 to 6	PFSP19[1:0]	R/W	0h*	port pin 19 function select
5 to 4	PFSP18[1:0]	R/W	0h*	port pin 18 function select
3 to 2	PFSP17[1:0]	R/W	0h*	port pin 17 function select
1 to 0	PFSP16[1:0]	R/W	0h*	port pin 16 function select

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Table 72: Port 0 function assignment

Symbol	Description			
	Default function	Function 1	Function 2	Function 3
P0.0	GPIO 0; pin 0	GPIO 0; pin 0	EXT BUS A0	EXT BUS A0
P0.1	GPIO 0; pin 1	GPIO 0; pin 1	EXT BUS A1	EXT BUS A1
P0.2	GPIO 0; pin 2	GPIO 0; pin 2	EXT BUS A2	EXT BUS A2
P0.3	GPIO 0; pin 3	GPIO 0; pin 3	EXT BUS A3	EXT BUS A3
P0.4	GPIO 0; pin 4	GPIO 0; pin 4	EXT BUS A4	EXT BUS A4
P0.5	GPIO 0; pin 5	GPIO 0; pin 5	EXT BUS A5	EXT BUS A5
P0.6	GPIO 0; pin 6	GPIO 0; pin 6	EXT BUS A6	EXT BUS A6
P0.7	GPIO 0; pin 7	GPIO 0; pin 7	EXT BUS A7	EXT BUS A7
P0.8	GPIO 0; pin 8	GPIO 0; pin 8	EXT BUS A8	EXT BUS A8
P0.9	GPIO 0; pin 9	GPIO 0; pin 9	EXT BUS A9	EXT BUS A9
P0.10	GPIO 0; pin 10	GPIO 0; pin 10	EXT BUS A10	EXT BUS A10
P0.11	GPIO 0; pin 11	GPIO 0; pin 11	EXT BUS A11	EXT BUS A11
P0.12	GPIO 0; pin 12	GPIO 0; pin 12	EXT BUS A12	EXT BUS A12
P0.13	GPIO 0; pin 13	GPIO 0; pin 13	EXT BUS A13	EXT BUS A13
P0.14	GPIO 0; pin 14	GPIO 0; pin 14	EXT BUS A14	EXT BUS A14
P0.15	GPIO 0; pin 15	GPIO 0; pin 15	EXT BUS A15	EXT BUS A15
P0.16	GPIO 0; pin 16	GPIO 0; pin 16	EXT BUS A16	EXT BUS A16
P0.17	GPIO 0; pin 17	GPIO 0; pin 17	EXT BUS A17	EXT BUS A17
P0.18	GPIO 0; pin 18	GPIO 0; pin 18	EXT BUS A18	EXT BUS A18
P0.19	GPIO 0; pin 19	GPIO 0; pin 19	EXT BUS A19	EXT BUS A19
P0.20	GPIO 0; pin 20	SPI2 SCS	EXT BUS A20	EXT BUS A20
P0.21	GPIO 0; pin 21	SPI2 SCK	EXT BUS A21	EXT BUS A21
P0.22	GPIO 0; pin 22	SPI2 SDI	EXT BUS A22	EXT BUS A22
P0.23	GPIO 0; pin 23	SPI2 SDO	EXT BUS A23	EXT BUS A23
P0.24	GPIO 0; pin 24	GPIO 0; pin 24	SPI1 SCS	SPI1 SCS
P0.25	GPIO 0; pin 25	GPIO 0; pin 25	SPI1 SCK	SPI1 SCK
P0.26	GPIO 0; pin 26	GPIO 0; pin 26	SPI1 SDI	SPI1 SDI
P0.27	GPIO 0; pin 27	GPIO 0; pin 27	SPI1 SDO	SPI1 SDO
P0.28	GPIO 0; pin 28	GPIO 0; pin 28	SPI0 SCS	SPI0 SCS
P0.29	GPIO 0; pin 29	GPIO 0; pin 29	SPI0 SCK	SPI0 SCK
P0.30	GPIO 0; pin 30	GPIO 0; pin 30	SPI0 SDI	SPI0 SDI
P0.31	GPIO 0; pin 31	GPIO 0; pin 31	SPI0 SDO	SPI0 SDO

Table 73: Port 1 function assignment

Symbol	Description			
	Default function	Function 1	Function 2	Function 3
P1.0	GPIO 1; pin 0	GPIO 1; pin 0	EXT BUS D0	EXT BUS D0
P1.1	GPIO 1; pin 1	GPIO 1; pin 1	EXT BUS D1	EXT BUS D1
P1.2	GPIO 1; pin 2	GPIO 1; pin 2	EXT BUS D2	EXT BUS D2
P1.3	GPIO 1; pin 3	GPIO 1; pin 3	EXT BUS D3	EXT BUS D3

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Table 73: Port 1 function assignment *...continued*

Symbol	Description			
	Default function	Function 1	Function 2	Function 3
P1.4	GPIO 1; pin 4	GPIO 1; pin 4	EXT BUS D4	EXT BUS D4
P1.5	GPIO 1; pin 5	GPIO 1; pin 5	EXT BUS D5	EXT BUS D5
P1.6	GPIO 1; pin 6	GPIO 1; pin 6	EXT BUS D6	EXT BUS D6
P1.7	GPIO 1; pin 7	GPIO 1; pin 7	EXT BUS D7	EXT BUS D7
P1.8	GPIO 1; pin 8	GPIO 1; pin 8	EXT BUS D8	EXT BUS D8
P1.9	GPIO 1; pin 9	GPIO 1; pin 9	EXT BUS D9	EXT BUS D9
P1.10	GPIO 1; pin 10	GPIO 1; pin 10	EXT BUS D10	EXT BUS D10
P1.11	GPIO 1; pin 11	GPIO 1; pin 11	EXT BUS D11	EXT BUS D11
P1.12	GPIO 1; pin 12	GPIO 1; pin 12	EXT BUS D12	EXT BUS D12
P1.13	GPIO 1; pin 13	GPIO 1; pin 13	EXT BUS D13	EXT BUS D13
P1.14	GPIO 1; pin 14	GPIO 1; pin 14	EXT BUS D14	EXT BUS D14
P1.15	GPIO 1; pin 15	GPIO 1; pin 15	EXT BUS D15	EXT BUS D15
P1.16	GPIO 1; pin 16	TIMER3 CAP3	EXT BUS D16	TIMER3 MAT3
P1.17	GPIO 1; pin 17	TIMER3 CAP2	EXT BUS D17	TIMER3 MAT2
P1.18	GPIO 1; pin 18	TIMER3 CAP1	EXT BUS D18	TIMER3 MAT1
P1.19	GPIO 1; pin 19	TIMER3 CAP0	EXT BUS D19	TIMER3 MAT0
P1.20	GPIO 1; pin 20	TIMER2 CAP3	EXT BUS D20	TIMER2 MAT3
P1.21	GPIO 1; pin 21	TIMER2 CAP2	EXT BUS D21	TIMER2 MAT2
P1.22	GPIO 1; pin 22	TIMER2 CAP1	EXT BUS D22	TIMER2 MAT1
P1.23	GPIO 1; pin 23	TIMER1 CAP3	EXT BUS D23	TIMER1 MAT3
P1.24	GPIO 1; pin 24	TIMER1 CAP2	EXT BUS D24	TIMER1 MAT2
P1.25	GPIO 1; pin 25	TIMER1 CAP1	EXT BUS D25	TIMER1 MAT1
P1.26	GPIO 1; pin 26	TIMER0 CAP3	EXT BUS D26	TIMER0 MAT3
P1.27	GPIO 1; pin 27	TIMER0 CAP2	EXT BUS D27	TIMER0 MAT2
P1.28	GPIO 1; pin 28	TIMER0 CAP1	EXT BUS D28	TIMER0 MAT1
P1.29	GPIO 1; pin 29	TIMER0 CAP0	EXT BUS D29	TIMER0 MAT0
P1.30	GPIO 1; pin 30	RTCK	EXT BUS D30	EXT BUS D30
P1.31	GPIO 1; pin 31	GPIO 1; pin 31	EXT BUS D31	EXT BUS D31

Table 74: Port 2 function assignment

Symbol	Description			
	Default function	Function 1	Function 2	Function 3
P2.0	GPIO 2; pin 0	GPIO 2; pin 0	EXT BUS OEN	EXT BUS OEN
P2.1	GPIO 2; pin 1	GPIO 2; pin 1	EXT BUS WEN	EXT BUS WEN
P2.2	GPIO 2; pin 2	GPIO 2; pin 2	EXT BUS BLS0	EXT BUS BLS0
P2.3	GPIO 2; pin 3	GPIO 2; pin 3	EXT BUS BLS1	EXT BUS BLS1
P2.4	GPIO 2; pin 4	GPIO 2; pin 4	EXT BUS BLS2	EXT BUS BLS2
P2.5	GPIO 2; pin 5	GPIO 2; pin 5	EXT BUS BLS3	EXT BUS BLS3
P2.6	GPIO 2; pin 6	GPIO 2; pin 6	CAN0 TXDC	CAN0 TXDC
P2.7	GPIO 2; pin 7	GPIO 2; pin 7	CAN0 RXDC	CAN0 RXDC

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Table 74: Port 2 function assignment *...continued*

Symbol	Description			
	Default function	Function 1	Function 2	Function 3
P2.8	GPIO 2; pin 8	GPIO 2; pin 8	CAN1 TXDC	CAN1 TXDC
P2.9	GPIO 2; pin 9	GPIO 2; pin 9	CAN1 RXDC	CAN1 RXDC
P2.10	GPIO 2; pin 10	GPIO 2; pin 10	CAN2 TXDC	CAN2 TXDC
P2.11	GPIO 2; pin 11	GPIO 2; pin 11	CAN2 RXDC	CAN2 RXDC
P2.12	GPIO 2; pin 12	GPIO 2; pin 12	CAN3 TXDC	CAN3 TXDC
P2.13	GPIO 2; pin 13	GPIO 2; pin 13	CAN3 RXDC	CAN3 RXDC
P2.14	GPIO 2; pin 14	LIN3 TXDL	CAN4 TXDC	CAN4 TXDC
P2.15	GPIO 2; pin 15	LIN3 RXDL	CAN4 RXDC	CAN4 RXDC
P2.16	GPIO 2; pin 16	LIN2 TXDL	CAN5 TXDC	CAN5 TXDC
P2.17	GPIO 2; pin 17	LIN2 RXDL	CAN5 RXDC	CAN5 RXDC
P2.18	GPIO 2; pin 18	UART TXD	LIN1 TXDL	LIN1 TXDL
P2.19	GPIO 2; pin 19	UART RXD	LIN1 RXDL	LIN1 RXDL
P2.20	GPIO 2; pin 20	GPIO 2; pin 20	LIN0 TXDL	LIN0 TXDL
P2.21	GPIO 2; pin 21	GPIO 2; pin 21	LIN0 RXDL	LIN0 RXDL
P2.22	GPIO 2; pin 22	GPIO 2; pin 22	TIMER2 CAP0	TIMER2 MAT0
P2.23	GPIO 2; pin 23	GPIO 2; pin 23	TIMER1 CAP0	TIMER1 MAT0
P2.24	GPIO 2; pin 24	GPIO 2; pin 24	EXTINT0	EXTINT0
P2.25	GPIO 2; pin 25	GPIO 2; pin 25	EXTINT1	EXTINT1
P2.26	GPIO 2; pin 26	EXTINT2	EXT BUS CS3	EXT BUS CS3
P2.27	GPIO 2; pin 27	EXTINT3	EXT BUS CS2	EXT BUS CS2
P2.28	GPIO 2; pin 28	GPIO 2; pin 28	EXT BUS CS1	EXT BUS CS1
P2.29	GPIO 2; pin 29	GPIO 2; pin 29	EXT BUS CS0	EXT BUS CS0

8.3.2.6 Pull-up control registers (SPUCP0, SPUCP1 and SPUCP2)

The pull-up control register configures the pull-up per pin on the corresponding I/O port. For port 2, the two most upper port pins are reserved. Note that the pull-up must be switched off before a 5 V signal is applied to the respective port pin.

Table 70 shows the bit assignment of the SPUCP0, SPUCP1 and SPUCP2 registers.

Table 75. SPUCP0, SPUCP1 and SPUCP2 register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	PUC[31:0] [1]	R/W	0000 0000h*	port pin pull-up control
			1	corresponding port pin is floating when 3-state
			0	corresponding port pin is pulled-up

[1] PUC[31:30] are reserved for port 2.

8.3.3 SPI

8.3.3.1 Overview

Three SPIs are included to enable synchronous serial communication with slave or master peripherals.

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The key features are:

- Master or slave operation
- Programmable clock bit rate and prescale
- Separate transmit and receive first-in, first-out memory buffers, 16-bit wide, 8 locations deep
- Programmable choice of interface operation: Motorola SPI, National Semiconductors Microwire or Texas Instruments (synchronous serial)
- Programmable data frame size from 4 bits to 16 bits
- Independent masking of transmit FIFO, receive FIFO, and receive overrun interrupts
- Internal loopback test mode

Note that in case the receive FIFO is not empty and the serial port remains idle for a fixed 32-bit period of the system clock, the receive time-out is asserted to ensure proper servicing of the received data.

More information about SPI can also be found in ARM PrimeCell documentation (see Ref. 4).

8.3.3.2 SPI pin description

The three SPI modules in the SJA2020 have the following pins. The pins are combined with other functions on the port pins of the SJA2020, see Section 8.3.2. Table 76 shows the SPI pins, x runs from 0 to 2.

Table 76: SPI pins

Symbol	Direction	Description
SPIx SCS	IN/OUT[1]	SPI x chip select
SPIx SCK	IN/OUT[1]	SPI x clock
SPIx SDI	IN	SPI x data input
SPIx SDO	OUT	SPI x data output

[1] Direction depends on master or slave mode.

8.3.3.3 Register mapping

The SPI registers are shown in Table 77. The SPI registers have an offset to the base address SPI RegBase which can be found in the memory map (see Table 7).

Table 77: SPI register summary

Address	Type	Reset value	Name	Description	Reference
00h	R/W	0000h	SSPCR0	control register 0	see Table 78
04h	R/W	0h	SSPCR1	control register 1	see Table 81
08h	R/W	-	SSPDR	FIFO data register	see Table 82
0Ch	R	03h	SSPSR	status register	see Table 83
10h	R/W	00h	SSPCPSR	clock prescale register	see Table 84
14h	R/W	0h	SSPIMSC	interrupt enable register	see Table 85

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Table 77: SPI register summary …continued

Address	Type	Reset value	Name	Description	Reference
18h	R	8h	SSPRIS	raw interrupt status register	see Table 86
1Ch	R	0h	SSPMIS	masked interrupt status register	see Table 87
20h	W	0h	SSPICR	interrupt clear register	see Table 88

8.3.3.4 SPI control register 0 (SSPCR0)

The SPI control register 0 configures the SPI operation mode.

In all modes, the SPI clock is only active during transmission and reception of data. The SPI clock idle state is utilized to provide time-out indication that occurs when the receive FIFO still contains data after a time-out period.

Table 78 shows the bit assignment of the SSPCR0 register.

Table 78. SSPCR0 register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 16	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
15 to 8	SCR[7:0]	R/W	00h*	serial clock rate [1]
7	SPH	R/W		clock phase which is applicable to Motorola frame format only; the clock phase bit selects the clock edge that captures data after the chip select SCSn becomes active LOW
			1	data is captured on the second clock edge
			0*	data is captured on the first clock edge
6	SPO	R/W		clock polarity which is applicable to Motorola frame format only; the clock polarity bit selects the SPI clock steady state level
			1	the SPI clock output is HIGH when no data is being transferred
			0*	the SPI clock output is LOW when no data is being transferred
5 to 4	FRF[1:0]	R/W	0h*	frame format; see Table 79
3 to 0	DSS[2:0]	R/W	0h*	data size select; see Table 80

[1] The transmit and receive bit rate is determined by following formula: $bit\ rate = \frac{f_{clk(sys)}}{SPSDVSR \times (1 + SCR)}$

Where: $f_{clk(sys)}$ = system clock frequency; SPSDVSR = clock prescale divisor, see Table 84; SCR = serial clock rate, see Table 78.

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Table 79: SPI frame format configuration

FRF[1:0]	Function
00	**Motorola SPI frame format.** Full-duplex, 4-wire synchronous transfers; the transmit data line SDOn is arbitrarily forced logic 0 if inactive; the chip select line SCSn is active logic 0 and is asserted during the entire frame transmission; continuous transfers are separated by a one SPI clock period idle (HIGH) state of the chip select line SCSn; the clock phase and polarity are programmable
01	**Texas instruments synchronous serial frame format.** Full-duplex, 4-wire synchronous transfer; transmit data line SDOn is 3-stateable when not transmitting; the chip select line SCSn is always pulsed high for one serial clock starting at its rising edge, prior to the transmission of each frame; for this frame format the output data is driven on the rising edge of the SPI clock and latches the data on the falling edge
10	**National Semiconductors Microwire frame format.** Half-duplex transfer using 8-bit control message; the transmit data line SDOn is arbitrarily forced logic 0 if inactive; the chip select line SCSn is active logic 0 and is asserted during the entire frame transmission; continuous transfers keep the chip select line logic 0; the frame starts with transmitting an 8-bit control message to the slave device; after this message has been sent, the slave device decodes it and, after waiting one serial clock after the 8-bit control message has been sent, responds with the requested data; the returned data can be 4 bits to 16 bits in length, making a total frame length anywhere from 13 bits to 25 bits
11	reserved; undefined operation

Table 80: SPI data size select configuration

DSS[3:0]	Function
0000	reserved; undefined operation
0001	reserved; undefined operation
0010	reserved; undefined operation
0011	4-bit data
0100	5-bit data
0101	6-bit data
0110	7-bit data
0111	8-bit data
1000	9-bit data
1001	10-bit data
1010	11-bit data
1011	12-bit data
1100	13-bit data
1101	14-bit data
1110	15-bit data
1111	16-bit data

8.3.3.5 SPI control register 1 (SSPCR1)

The SPI control register 1 controls several SPI configuration functions.

Table 81 shows the bit assignment of the SSPCR1 register.

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Table 81. SSPCR1 register bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 4	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
3	SOD	R/W		slave mode output disable; this bit is relevant only in the slave mode (bit MS = 1); in multiple slave systems, it is possible for a master to broadcast a message to all slaves in the system while ensuring that only one slave drives data onto its serial output line; to operate in such systems, the slave output mode bit can be set if the slave is not supposed to drive the data output line
			1	the slave must not drive the data output line SDOn
			0*	the slave can drive to data output line SDOn
2	MS	R/W		master or slave mode select; this bit can be modified only when the serial port is disabled (bit SSE = 0)
			1	the device is configured as slave
			0*	the device is configured as master
1	SSE	R/W		synchronous serial port enable
			1	the serial port is enabled
			0*	the serial port is disabled
0	LBM	R/W		loop back mode; when logic 1 the output of the transmit serial shifter is connected to the input of the receive serial shifter internally; when logic 0, normal serial port operation is enabled
			1	the output of the transmit serial shifter is connected to the input of the receive serial shifter internally
			0*	normal serial port operation is enabled

8.3.3.6 SPI FIFO data register (SSPDR)

The SPI FIFO data register written is 16 bits wide. When read, the data entry in the receive FIFO is accessed. When written, the data is written to the entry in the transmit FIFO. When a data size of less than 16 bits is selected, the user must right-justify data written to the transmit FIFO. The transmit logic ignores unused bits. Received data less than 16 bits is automatically right-justified in the receive buffer; unused bits are undefined and should be discarded.

When programmed for National Semiconductors Microwire frame format, the default size for transmit data is eight bits. The receive data size is programmable.

The transmit FIFO and the receive FIFO are not cleared even when the serial port enable bit is set to logic 0. This allows the software to fill the transmit FIFO before enabling the serial port.

Table 82 shows the bit assignment of the SSPDR register.

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Table 82. SSPDR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 16	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
15 to 0	DATA[15:0]	R/W	-	transmit or receive FIFO data; when read, data from the receive FIFO is accessed; when written, data is written into the transmit FIFO

8.3.3.7 SPI status register (SSPSR)

The SPI status register reflects the FIFO status and the serial port busy status.

The SPS register is read only. Table 83 shows the bit assignment of the SPS register.

Table 83. SPSR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 5	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
4	BSY	R		busy flag
			1	the serial port is transmitting and/or receiving a frame or the transmit FIFO is not empty
			0*	the serial port is idle
3	RFF	R		receive FIFO full
			1	the receive FIFO is full
			0*	the receive FIFO is not full
2	RNE	R		receive FIFO not empty
			1	the receive FIFO is not empty
			0*	the receive FIFO is empty
1	TNF	R		transmit FIFO not full
			1*	the transmit FIFO is not full
			0	the transmit FIFO is full
0	TFE	R		transmit FIFO empty
			1*	the transmit FIFO is empty
			0	the transmit FIFO is not empty

8.3.3.8 SPI clock prescale register (SSPCPSR)

The SPI clock prescale register specifies the system clock frequency prescale division factor.

Table 84 shows the bit assignment of the SSPCPSR register.

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Table 84. SSPCPSR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
7 to 0	SPSDVSR	R/W	00h*	clock prescale divisor; the system clock frequency is divided by the clock prescale value which must be an even number from 2 to 254; the least significant bit always returns logic 0 on reads

8.3.3.9 SPI interrupt enable register (SSPIMSC)

The SPI interrupt enable register is used to enable the four types of interrupts referred to in the interrupt status register.

Table 85 shows the bit assignment of the SSPIMSC register.

Table 85. SSPIMSC register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 4	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
3	TXIM	R/W		transmit FIFO interrupt enable
			1	the transmit FIFO half empty or less condition interrupt is not masked
			0*	the transmit FIFO half empty or less condition interrupt is masked
2	RXIM	R/W		receive FIFO interrupt enable
			1	the receive FIFO half full or less condition interrupt is not masked
			0*	the receive FIFO half full or less condition interrupt is masked
1	RTIM	R/W		receive time-out interrupt enable
			1	the receive FIFO not empty and no read prior to time-out period interrupt is not masked
			0*	the receive FIFO not empty and no read prior to time-out period interrupt is masked
0	RORIM	R/W		receive overrun interrupt enable
			1	the receive FIFO written to while full condition interrupt is not masked
			0*	the receive FIFO written to while full condition interrupt is masked

8.3.3.10 SPI raw interrupt status register (SSPRIS)

The SPI raw interrupt status register reflects the raw interrupt status prior to interrupt masking.

The SSPRIS register is read only. Table 86 shows the bit assignment of the SSPRIS register.

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Table 86. SSPRIS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 4	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
3	TXRIS	R		transmit FIFO raw interrupt status
			1*	the transmit FIFO half empty or less condition interrupt prior to masking has occurred
			0	
2	RXRIS	R		receive FIFO raw interrupt status
			1	the receive FIFO half full or less condition interrupt prior to masking has occurred
			0*	
1	RTRIS	R		receive time-out raw interrupt status
			1	the receive FIFO not empty and no read prior to time-out period interrupt prior to masking has occurred
			0*	
0	RORRIS	R		receive overrun raw interrupt status
			1	the receive FIFO written to while full condition interrupt prior to masking has occurred
			0*	

8.3.3.11 SPI masked interrupt status register (SSPMIS)

The SPI masked interrupt status register reflects the masked interrupt status.

The SSPMIS register is read only. Table 87 shows the bit assignment of the SSPMIS register.

Table 87. SSPMIS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 4	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
3	TXMIS	R		transmit FIFO masked interrupt status
			1	the transmit FIFO interrupt enable was set and the transmit FIFO half empty or less condition interrupt has occurred
			0*	
2	RXMIS	R		receive FIFO masked interrupt status
			1	the receive FIFO interrupt enable was set and the receive FIFO half full or less condition interrupt has occurred
			0*	
1	RTMIS	R		receive time-out masked interrupt status
			1	the receive time-out interrupt enable was set and the receive FIFO not empty and no read prior to time-out period interrupt has occurred
			0*	

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Table 87. SSPMIS register bit description *...continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
0	RORMIS	R		receive overrun masked interrupt status
			1	the receive FIFO overrun interrupt enable was set and the receive FIFO written to while full condition interrupt has occurred
			0*	

8.3.3.12 SPI interrupt clear register (SSPICR)

The SPI interrupt clear register clears the set raw and masked interrupt status.

The SSPICR register is write only. Table 88 shows the bit assignment of the SSPMICR register.

Table 88. SSPICR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 2	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
1	RTIC	W		receive time-out clear interrupt
			1	the raw and masked receive time-out interrupt are cleared
			0	writing logic 0 has no effect
0	RORIC	W		receive overrun masked interrupt status
			1	the raw and masked receive FIFO overrun interrupt are cleared
			0	writing logic 0 has no effect

8.3.4 Watchdog

8.3.4.1 Overview

The purpose of the watchdog is to reset the ARM7 processor within a reasonable amount of time if it enters an erroneous state. The watchdog will generate a system reset if the user program fails to trigger the watchdog correctly within a predetermined amount of time.

The key features are:

- Internally chip reset if not periodically triggered
- Debug mode with interrupt instead of reset
- Watchdog time period change protected with access sequence
- Programmable 32-bit watchdog timer period

The watchdog consists of a 32-bit counter. The clock is directly fed to the timer. The timer increments when clocked.

The watchdog should be used in the following manner:

- For debugging purposes the watchdog debug mode in the watchdog mode register should be set before the watchdog has been locked. The debug mode is locked by programming a new watchdog reload value

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- Enable access to the watchdog reload value register by writing AAAA AAAAh followed by 5555 5555h
- Program the watchdog timer reload value in watchdog reload value register
- Trigger the watchdog by writing the watchdog trigger register periodically before the watchdog counter overflows

To generate watchdog interrupts in the watchdog debug mode, the interrupt has to be enabled via the watchdog interrupt status enable register. A watchdog overflow interrupt can be cleared by writing the watchdog interrupt clear status register. In case a watchdog overflow occurred in the watchdog debug mode, clearing the watchdog overflow interrupt is the only way to trigger the watchdog again resulting in restart of counting the programmed watchdog period. If the watchdog interrupt is not enabled in watchdog debug mode, the watchdog can be triggered again by writing the watchdog trigger register.

The watchdog is stalled when the AHB clock or the general and peripheral subsystem clock is stopped for entering power saving modes. In this case the watchdog counter value is maintained. Therefore, it is recommended to trigger the watchdog before switching off the AHB clock or the general and peripheral subsystem clock to avoid unexpected watchdog reset after leaving power savings modes.

A watchdog reset is equal to an external reset: the program counter will start from 0000 0000h and registers are cleared. The clock generation unit contains a watchdog bark register to distinguish between both events.

8.3.4.2 Watchdog pin description

The watchdog has no external pins.

8.3.4.3 Register mapping

The watchdog registers are shown in Table 89. The watchdog registers have an offset to the base address WD RegBase which can be found in the memory map (see Table 7).

Table 89: Watchdog register summary

Address	Type	Reset value	Name	Description	Reference
00h	R/W	0h	WDMOD	watchdog mode register	see Table 90
04h	R/W	00FF FFFFh	WDRV	watchdog timer reload value	see Table 91
08	R/W	0000 0000h	WDCV	watchdog timer counter value	see Table 92
0Ch	W	-	WDTRIG	watchdog trigger	see Table 93
10h	W	-	WDISS	watchdog interrupt set status	see Table 94
14h	W	-	WDICS	watchdog interrupt clear status	see Table 95
18h	R	0h	WDIE	watchdog interrupt enable	see Table 96
1Ch	R	0h	WDIS	watchdog interrupt status	see Table 97
20h	W	-	WDISE	watchdog interrupt set enable	see Table 98
24h	W	-	WDICE	watchdog interrupt clear enable	see Table 99

8.3.4.4 Watchdog mode register (WDMOD)

The watchdog debug bit can be set after reset only before the watchdog reload value has been programmed. After setting this bit, it can always be cleared to enable normal watchdog operation.

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Table 90 shows the bit assignment of the WDMOD register.

Table 90. WDMOD register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 4	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
3	WDTOF	R		time out flag
			1	a watchdog time out has occurred in debug mode
			0*	
2	WDCEF	R		counter enable flag
			1	the watchdog timer is active
			0*	the watchdog timer is inactive
1	WDDBLCK	R		debug lock
			1	the watchdog debug mode has been locked and can not be entered again; the lock is activated after writing a new value in watchdog reload value register
			0*	
0	WDDB	R/W		debug mode
			1	a watchdog overflow results in an interrupt
			0*	a watchdog overflow results in a reset; this bit can be reset any time but only be set when the debug lock is not active

8.3.4.5 Watchdog reload value register (WDRV)

The watchdog reload value register contains the watchdog value which is reloaded into the watchdog timer on a trigger. The actual watchdog time period depends on the clock frequency. The watchdog reload value register is protected against erroneously changing. Programming a new watchdog value is only accepted after the write sequence AAAA AAAAh followed by 5555 5555h to this register.

Table 91 shows the bit assignment of the WDRV register.

Table 91. WDRV register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	WDRV[31:0]	R/W	00FF FFFFh*	watchdog reload value; reading this register shows programmed watchdog value

8.3.4.6 Watchdog counter value register (WDCV)

The watchdog counter value register contains the actual watchdog timer counter value.

Table 92 shows the bit assignment of the WDCV register.

Table 92. WDCV register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	WDCV[31:0]	R	00FF FFFFh*	watchdog counter value; reading this register shows the current value of the watchdog timer counter

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8.3.4.7 Watchdog trigger register (WDTRIG)

The watchdog trigger register is used to (re)start the watchdog time-out period as programmed in the watchdog reload value register.

Table 93 shows the bit assignment of the WDTRIG register.

Table 93. WDTRIG register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	KICKDOG	W		watchdog trigger
			1	triggers the watchdog resulting in (re)start of counting the programmed watchdog period
			0	writing logic 0 has no effect

8.3.4.8 Watchdog interrupt set status (WDISS)

The watchdog interrupt set status register sets the bits in the watchdog interrupt status register.

The WDISS register is write only. Table 94 shows the bit assignment of the WDISS register.

Table 94. WDISS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as write
0	INT_SET_STATUS[0]	W		
			1	the corresponding bit in the watchdog interrupt status register is set
			0	the corresponding bit in the watchdog interrupt status register is unchanged

8.3.4.9 Watchdog interrupt clear status (WDICS)

The watchdog interrupt clear status register clears the bits in the watchdog interrupt status register.

The WDICS register is write only. Table 95 shows the bit assignment of the WDICS register.

Table 95. WDICS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as write
0	INT_CLR_STATUS[0]	W		
			1	the corresponding bit in the watchdog interrupt status register is cleared
			0	the corresponding bit in the watchdog interrupt status register is unchanged

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8.3.4.10 Watchdog interrupt enable (WDIE)

The watchdog interrupt enable register determines when the watchdog gives an interrupt request if the corresponding interrupt enable has been set.

The WDIE register is read only. Table 96 shows the bit assignment of the WDIE register.

Table 96. WDIE register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0
0	OVERFLOW	R		watchdog overflow interrupt enable
			1	bit INT_SET_ENABLE[0] is set to enable the watchdog overflow interrupt
			0*	bit INT_CLR_ENABLE[0] is reset to disable the interrupt

8.3.4.11 Watchdog interrupt status register (WDIS)

The watchdog interrupt status register determines when the watchdog gives an interrupt request if the corresponding interrupt enable has been set.

The WDIS is read only. Table 97 shows the bit assignment of the WDIS register.

Table 97. WDIS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0
0	OVERFLOW	R		watchdog overflow interrupt
			1	a watchdog overflow occurred in watchdog debug mode or logic 1 is written to bit INT_SET_STATUS[0]
			0*	no interrupt is pending or logic 1 is written to bit INT_CLR_STATUS[0]

8.3.4.12 Watchdog interrupt set enable (WDISE)

The watchdog interrupt set enable register sets the bits in the watchdog interrupt enable register.

The WDISE register is write only. Table 98 shows the bit assignment of the WDISE register.

Table 98. WDISE register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as write
0	SET_ENABLE[0]	W	-	
			1	the corresponding bit in the watchdog interrupt enable register is set
			0	the corresponding bit in the watchdog interrupt enable register is unchanged

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8.3.4.13 Watchdog interrupt clear enable (WDICE)

The watchdog interrupt clear enable register clears the bits in the watchdog interrupt status enable register.

The WDICE register is write only. Table 99 shows the bit assignment of the WDICE register.

Table 99. WDICE register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as write
0	CLR_ENABLE[0]	W	-	
			1	the corresponding bit in the watchdog interrupt enable register is cleared
			0	the corresponding bit in the watchdog interrupt enable register is unchanged

8.3.5 Analog-to-digital converter

8.3.5.1 Overview

The SJA2020 includes a 10-bit successive approximation analog-to-digital converter.

The basic characteristics of the ADC interface module are:

- Four dedicated analog inputs for eight channels, selected by an analog multiplexer
- Measurement range up to 3.6 V
- 400 ksample/s at 10-bit resolution up to 1500 ksample/s at 2-bit resolution
- Programmable resolution from 2 bits to 10 bits
- Single analog-to-digital conversion scan mode and continuous analog-to-digital conversion scan mode
- Optional conversion on transition on GPIO pin, external input or timer capture/match signal
- Converted digital values are stored in a register per channel
- Power-down mode

The ADC clock must be less than half the system clock frequency, but is limited to 4.5 MHz as maximum frequency. The clock generation unit provides a programmable fractional system clock divider dedicated for the ADC clock to fulfil this constraint or to select the desired lower sampling frequency. The conversion rate is determined by the ADC clock frequency divided by the number of resolution bits plus one. Accessing ADC registers requires an enabled ADC clock which is controllable via the clock generation unit. The analog inputs 0 … 3 are connected to channel 0 … 3 and 4 … 7 respectively.

8.3.5.2 ADC pin description

The ADC has the following pins. Some pins are combined with other functions on the port pins of the SJA2020, see Section 8.3.2. Table 100 shows the ADC pins.

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Table 100: Analog-to-digital converter pins

Symbol	Direction	Description
VREFN	IN	ADC low reference level
AI0	IN	analog input for channel 0 and channel 4
AI1	IN	analog input for channel 1 and channel 5
AI2	IN	analog input for channel 2 and channel 6
AI3	IN	analog input for channel 3 and channel 7
TR0	IN	ADC start trigger 0 input
TR1	IN	ADC start trigger 1 input

8.3.5.3 Register mapping

The ADC registers are shown in Table 101. The ADC registers have an offset to the base address ADC RegBase which can be found in the memory map (see Table 7).

Table 101: AD converter register summary

Address	Type	Reset value	Name	Description	Reference
00h	R	000h	ACD0	ADC channel 0 conversion data register	see Table 102
04h	R	000h	ACD1	ADC channel 1 conversion data register	see Table 102
08h	R	000h	ACD2	ADC channel 2 conversion data register	see Table 102
0Ch	R	000h	ACD3	ADC channel 3 conversion data register	see Table 102
10h	R	000h	ACD4	ADC channel 4 conversion data register	see Table 102
14h	R	000h	ACD5	ADC channel 5 conversion data register	see Table 102
18h	R	000h	ACD6	ADC channel 6 conversion data register	see Table 102
1Ch	R	000h	ACD7	ADC channel 7 conversion data register	see Table 102
20h	R/W	00h	ACON	ADC control register	see Table 103
24h	R/W	0000h	ACC	ADC channel configuration register	see Table 105
28h	R/W	0h	AIE	ADC interrupt enable register	see Table 107
2Ch	R	0h	AIS	ADC interrupt status register	see Table 108
30h	W	-	AIC	ADC interrupt clear register	see Table 109

8.3.5.4 ADC channel conversion data registers (ACD0 to ACD7)

The SJA2020 contains a conversion data register for each of the eight ADC channel inputs. These eight registers store the result of an analog-to-digital conversion scan through all active channels. The selected bit resolution in the ADCn (n from 0 to 7) channel configuration register simultaneously defines the number of valid most significant conversion data bits in the ADC channel conversion data registers. The remaining conversion data bits become logic 0 accordingly.

The ACD registers are read only. Table 102 shows the bit assignment of the ACD registers.

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Table 102. ACD register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 10	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
9 to 0	ACD[9:0]	R	000h*	conversion data; the value represents the voltage on the corresponding channel input pin, divided by the voltage on the $V_{DD(ADC)}$ pin

8.3.5.5 ADC control register (ACON)

The ADC control register provides the configuration of ADC operation mode and reflects the analog-to-digital conversion status.

Table 103 shows the bit assignment of the ACON register.

Table 103. ACON register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 7	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
6	AS	R		ADC status
			1	the analog-to-digital conversion scan is in progress
			0*	the ADC is idle
5 to 3	ASC[2:0]	R/W	0h*	ADC scan configuration; see Table 104
2	ASM	R/W		ADC scan mode
			1	a repetitive conversion scan is performed after the start trigger as configured in the ADC scan configuration bits (ASC); the ADC conversion data registers are updated continuously; a continuous scan process is terminated by clearing the ADC scan mode bit
			0*	a single conversion scan is performed after the start trigger as configured in the ADC scan configuration; the results are stored in the ADC conversion data registers
1	AEN	R/W		ADC enable
			1	the ADC is enabled for conversion scans
			0*	the ADC will be switched into low power mode; starting a new conversion scan is not possible; an ongoing conversion scan is completed before disabling
0	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

Table 104: Conversion scan configuration bits

ASC[2:0]	Function
000	ADC in inactive operational mode
001	ADC in inactive operational mode
010	start conversion scan through all active channels[1]
011	start conversion scan through all active channels[1]
100	start conversion scan through all active channels after rising edge on pin 64 (P2[23]/CAP1[0]/MAT1[0])

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Table 104: Conversion scan configuration bits *…continued*

ASC[2:0]	Function
101	start conversion scan through all active channels after falling edge on pin 64 (P2[23]/CAP1[0]/MAT1[0])
110	start conversion scan through all active channels after rising edge on pin 65 (P2[22]/CAP2[0]/MAT2[0])
111	start conversion scan through all active channels after falling edge on pin 65 (P2[22]/CAP2[0]/MAT2[0])

[1] In single scan conversion mode (ASM = 0), the ASC value should be set to 'inactive' as soon as the ADC conversion is started. This is because in single scan mode, a new conversion will be started according the trigger condition defined by the ASC bits when the AEN bit is set after the conversion has completed.

8.3.5.6 ADC channel configuration register (ACC)

The ADC channel configuration register defines which analog input channels are included during an analog-to-digital conversion scan. Furthermore, the resolution per channel can be defined from 2 bits to 10 bits.

Table 105 shows the bit assignment of the ACC register.

Table 105. ACC register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 28	ACC7[3:0]	R/W	0h*	channel 7 configuration; see Table 106
27 to 24	ACC6[3:0]	R/W	0h*	channel 6 configuration; see Table 106
23 to 20	ACC5[3:0]	R/W	0h*	channel 5 configuration; see Table 106
19 to 16	ACC4[3:0]	R/W	0h*	channel 4 configuration; see Table 106
15 to 12	ACC3[3:0]	R/W	0h*	channel 3 configuration; see Table 106
11 to 8	ACC2[3:0]	R/W	0h*	channel 2 configuration; see Table 106
7 to 4	ACC1[3:0]	R/W	0h*	channel 1 configuration; see Table 106
3 to 0	ACC0[3:0]	R/W	0h*	channel 0 configuration; see Table 106

Table 106: Channel selection and resolution value bits

ACCn[3:0]	Function
0000	channel not selected
0001	reserved
0010	2-bit resolution
0011	3-bit resolution
0100	4-bit resolution
0101	5-bit resolution
0110	6-bit resolution
0111	7-bit resolution
1000	8-bit resolution
1001	9-bit resolution
1010	10-bit resolution
1011	reserved
1100	reserved

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Table 106: Channel selection and resolution value bits *...continued*

ACCn[3:0]	Function
1101	reserved
1110	reserved
1111	reserved

8.3.5.7 ADC interrupt enable register (AIE)

The ADC interrupt enable register contains the enable for the scan interrupt.

Table 107 shows the bit assignment of the AIE register.

Table 107. AIE register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	ASIE	R/W		ADC scan interrupt enable
			1	an interrupt is generated if a single conversion scan has finished
			0*	

8.3.5.8 ADC interrupt status register (AIS)

The ADC interrupt status register indicates the presence of the scan interrupt.

The AIS register is read only. Table 108 shows the bit assignment of the AIS register.

Table 108. AIS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; read as logic 0
0	ASI	R		ADC scan interrupt
			1	an interrupt is pending due to a completed conversion scan
			0*	

8.3.5.9 ADC interrupt clear register (AIC)

The ADC interrupt clear register provides the mechanism to clear scan interrupt.

The AIC register is write only. Table 109 shows the bit assignment of the AIC register.

Table 109. AIC register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, write as logic 0
0	ASIC	W	-	analog-to-digital conversion scan interrupt clear
			1	the scan interrupt flag is cleared
			0	

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8.3.6 Event router

8.3.6.1 Overview

The event router provides bus controlled routing of input events to the vectored interrupt controller for use as interrupt or wake up signals.

The key features are:

- Input events can be used either directly or latched (edge detected) as interrupt source
- Direct events will disappear when the event becomes inactive
- Latched events will remain active until they are explicitly cleared
- Programmable input level and edge polarity
- Event detection maskable
- Event detection is fully asynchronous, thus no clock is required

The event router allows the event source to be defined, its polarity to be selected, its activation type to be selected and the interrupt to be masked or enabled. The event router can be used to start a clock on an external event.

The real-time clock tick interrupt event needs to be captured on the rising edge.

The vectored interrupt controller interrupt inputs are active HIGH.

8.3.6.2 Event router pin description and mapping to register bit positions

The event router module in the SJA2020 is connected to the following pins. The pins are combined with other functions on the port pins of the SJA2020, see Section 8.3.2. Table 110 shows the pins connected to the event router. It also shows the corresponding bit position in the event router registers and the default polarity, see Table 118.

Table 110: Event router pin connections

Symbol	Direction	Bit position	Description	Default polarity, see Table 118
EXTINT0	IN	0	external interrupt input 0	1
EXTINT1	IN	1	external interrupt input 1	1
EXTINT2	IN	2	external interrupt input 2	1
EXTINT3	IN	3	external interrupt input 3	1
CAN0 RXDC	IN	4	CAN0 receive data input and wake-up	0
CAN1 RXDC	IN	5	CAN1 receive data input and wake-up	0
CAN2 RXDC	IN	6	CAN2 receive data input and wake-up	0
CAN3 RXDC	IN	7	CAN3 receive data input and wake-up	0
CAN4 RXDC	IN	8	CAN4 receive data input and wake-up	0
CAN5 RXDC	IN	9	CAN5 receive data input and wake-up	0
LIN0 RXDC	IN	10	LIN0 receive data input and wake-up	0

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Table 110: Event router pin connections …continued

Symbol	Direction	Bit position	Description	Default polarity, see Table 118
LIN1 RXDC	IN	11	LIN1 receive data input and wake-up	0
LIN2 RXDC	IN	12	LIN2 receive data input and wake-up	0
LIN3 RXDC	IN	13	LIN3 receive data input and wake-up	0
-	IN	14	RTC tick event	1
-	n.a.	15	CAN interrupt (internal), combined general interrupt of all CAN controllers and the CAN look-up table, see Section 8.5.1.33	1
-	n.a.	16	VIC IRQ (internal)	1
-	n.a.	17	VIC FIQ (internal)	1

8.3.6.3 Register mapping

The event router registers are shown in Table 111. The event router registers have an offset to the base address ER RegBase which can be found in the memory map (see Table 7).

Table 111: Event router register summary

Address	Type	Reset value	Name	Description	Reference
C00h	R	0 0000h	PEND	event status register	see Table 112
C20h	W	-	INT_CLR	event status clear register	see Table 113
C40h	W	-	INT_SET	event status set register	see Table 114
C60h	R	3 FFFFh	MASK	event enable register	see Table 115
C80h	W	-	MASK_CLR	event enable clear register	see Table 116
CA0h	W	-	MASK_SET	event enable set register	see Table 117
CC0h	R/W	3 C00Fh	APR	activation polarity register	see Table 118
CE0h	R/W	3 FFFFh	ATR	activation type register	see Table 119
D00h	-	-	reserved	reserved; do not modify	
D20h	R/W	0 0000h	RSR	raw status register	see Table 120

8.3.6.4 Event status register (PEND)

The event status register determines when the event router forwards an interrupt request to the vectored interrupt controller if the corresponding event enable has been set.

Table 112 shows the bit assignment of the PEND register.

Table 112. PEND register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 18	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

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Table 112. PEND register bit description *...continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
17 to 0	PEND[17:0]	R		
			1	an event on corresponding pin x has occurred or logic 1 is written to the corresponding bit in the INT_SET register
			0*	no event is pending or logic 1 has been written to the corresponding bit in the INT_CLR register

8.3.6.5 Event status clear register (INT_CLR)

The event status clear register clears the bits in the event status register.

Table 113 shows the bit assignment of the INT_CLR register.

Table 113. INT_CLR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 18	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
17 to 0	INT_CLR[17:0]	W	-	
			1	the corresponding bit in the event status register is cleared
			0	the corresponding bit in the event status register is unchanged

8.3.6.6 Event status set register (INT_SET)

The event status set register sets the bits in the event status register.

Table 114 shows the bit assignment of the INT_SET register.

Table 114. INT_SET register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 18	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
17 to 0	INT_SET[17:0]	W	-	
			1	the corresponding bit in the event status register is set
			0	the corresponding bit in the event status register is unchanged

8.3.6.7 Event enable register (MASK)

The event enable register determines when the event router sets the event status and forwards this to the vectored interrupt controller if the corresponding event enable has been set.

Table 115 shows the bit assignment of the MASK register.

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Table 115. MASK register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 18	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
17 to 0	MASK[17:0]	R	3 FFFFh*	event enable; this bit is set by writing a logic 1 to the corresponding bit in the MASK_SET register; this bit is cleared by writing a logic 1 to the corresponding bit in the MASK_CLR register
			1	the event router sets the event status and forwards the corresponding event to the vectored interrupt controller
			0	the event router masks the event status and does not forward the corresponding event to the vectored interrupt controller

8.3.6.8 Event enable clear register (MASK_CLR)

The event enable clear register clears the bits in the event enable register.

Table 116 shows the bit assignment of the MASK_CLR register.

Table 116. MASK_CLR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 18	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
17 to 0	MASK_CLR[17:0]	W		
			1	the corresponding bit in the event enable register is cleared
			0	the corresponding bit in the event enable register is unchanged

8.3.6.9 Event enable set register (MASK_SET)

The event enable set register sets the bits in the event enable register.

Table 117 shows the bit assignment of the MASK_SET register.

Table 117. MASK_SET register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 18	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
17 to 0	MASK_SET[17:0]	W	-	
			1	the corresponding bit in the event enable register is set
			0	the corresponding bit in the event enable register is unchanged

8.3.6.10 Activation polarity register (APR)

The activation polarity register is used to configure which level is the active state for the event source.

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Table 118 shows the bit assignment of the APR register.

Table 118. APR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 18	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
17 to 0	APR[17:0]	R/W	3 C00Fh*	
			1	the corresponding event is high sensitive (HIGH level or rising edge)
			0	the corresponding event is low sensitive (LOW level or falling edge)

8.3.6.11 Activation type register (ATR)

The activation type register is used to configure whether an event is used directly or if it is latched. If it is latched, the interrupt will persist after its event source has become inactive until it is cleared by an interrupt clear write action. The event router includes an edge detection circuit which prevents reassertion of an event interrupt if the input remains at the active level after the latch is cleared. Level sensitive events are expected to be held and removed by the event source.

Table 119 shows the bit assignment of the ATR register.

Table 119. ATR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 18	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
17 to 0	ATR[17:0]	R/W	3 FFFFh*	
			1	the corresponding event is latched (edge sensitive)
			0	the corresponding event is directly forwarded (level sensitive)

8.3.6.12 Raw status register (RSR)

The raw status shows unmasked events including latched events. Level sensitive events are removed by the event source. Edge sensitive events need to be cleared via the event clear register.

Table 120 shows the bit assignment of the RSR register.

Table 120. RSR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 18	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
17 to 0	RSR[17:0]	R	0 0000h*	
			1	the corresponding event has occurred
			0	the corresponding event has not occurred

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8.3.7 Real-time clock

8.3.7.1 Overview

The real time clock is driven by a dedicated low power, low frequency crystal oscillator. Battery backed solutions are enabled by separated voltage domains on-chip.

The key features are:

- Real time and date
- Separate voltage domain to enable separate battery solutions
- Optimized for accurate 32.678 kHz crystal oscillator frequency
- Minute tick for interrupt handling

The real time clock is capable to represent the real time and date via standard C library functions. Every minute, a tick is generated for interrupt handling purposes.

The real time clock is initialized via an on-chip power-on reset within its own voltage domain only. Accessing the real-time clock registers requires a running 32 kHz oscillator and a system clock frequency of at least twice the real time clock frequency. In case of no RTC supply, the registers content is undefined.

8.3.7.2 RTC pin description

The RTC in the SJA2020 has the following pins, see Table 121.

Table 121: Real time clock pins

Symbol	Direction	Description
XIN_RTC	IN	real time clock crystal input or external clock input
XOUT_RTC	OUT	real time clock crystal output

8.3.7.3 Register mapping

The real-time clock registers are shown in Table 122.

The real-time clock registers have an offset to the base address RTC RegBase which can be found in the memory map (see Table 7).

Table 122. Real-time clock register summary

Address	Type	Reset value	Name	Description	Reference
000h	R	0000 0000h	RTC_TIME_SECONDS	elapsed time seconds register	see Table 123
010h	R	0000h	RTC_TIME_FRACTION	seconds fraction register	see Table 124
020h	R/W	0000 0000h	RTC_PORTIME	real-time offset register	see Table 125
FC0h	R/W	1h	RTC_CONTROL	real-time control register	see Table 126

8.3.7.4 RTC elapsed time seconds register (RTC_TIME_SECONDS)

The RTC elapsed time seconds register reflects the time in seconds since power-up.

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The RTC_TIME_SECONDS register is read only. Table 123 shows the bit assignment of the RTC_TIME_SECONDS register.

Table 123. RTC_TIME_SECONDS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	RTC_TIME_ SECONDS[31:0]	R	0000 0000h*	elapsed time in seconds; provides the number of seconds passed after power-on event occurred

8.3.7.5 RTC seconds fraction register (RTC_TIME_FRACTION)

The RTC seconds fraction register reflects the passed number of clock cycles from the current second. Note that the RTC seconds fraction register is only updated when reading the RTC elapsed time seconds register.

The RTC_TIME_FRACTION register is read only. Table 124 shows the bit assignment of the RTC_TIME_FRACTION register.

Table 124. RTC_TIME_FRACTION register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 15	reserved	-	-	reserved; read as logic 0
14 to 0	RTC_TIME_ FRACTION[14:0]	R	0000h*	seconds fraction register; provides the fractional part of a second in clock ticks

8.3.7.6 RTC real time offset register (RTC_PORTIME)

The RTC real time offset register holds the offset to the real time and date. Providing the offset of power-up time in elapsed seconds since 1 January 1970, standard C libraries can be used in order to easily access the current time and date.

Table 125 shows the bit assignment of the RTC_PORTIME register.

Table 125. RTC_PORTIME register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	RTC_PORTIME[31:0]	R/W	0000 0000h*	real time offset value; contains the real time offset value in seconds at power-on event

8.3.7.7 RTC real time control register (RTC_CONTROL)

The RTC real time control register provides the minute tick enable for real time clock applications.

Table 126 shows the bit assignment of the RTC_CONTROL register.

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Table 126. RTC_CONTROL register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31	RTC_TICK_ENABLE	R/W		real time clock tick enable
			1*	the minute tick is inactive
			0	the real time clock sends every minute a tick interrupt request to the event router
30 to 0	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

8.4 Peripheral subsystem

8.4.1 Timer

8.4.1.1 Overview

Four identical timers are present which are designed to count cycles of the clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. They also include capture inputs to trap the timer value when a transition occurs in an input signal, optionally generating an interrupt

The key features are:

- 32-bit timer/counter with programmable 32-bit prescaler
- Up to four 32-bit capture channels per timer, that take a snapshot of the timer value when a transition occurs in an input signal; a capture event may also optionally generate an interrupt
- Four 32-bit match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match
  - Stop timer on match with optional interrupt generation
  - Reset timer on match with optional interrupt generation
- Up to four external outputs per timer corresponding to match registers, with the following capabilities:
  - Set LOW on match
  - Set HIGH on match
  - Toggle on match
  - Do nothing on match

8.4.1.2 Timer pin description

The four timers in the SJA2020 have the following pins. The timer pins are combined with other functions on the port pins of the SJA2020, see Section 8.3.2. Table 127 shows the timer pins, x runs from 0 to 3.

Table 127: Timer pins

Symbol	Direction	Description
TIMERx CAP[0]	IN	TIMER x capture input 0
TIMERx CAP[1]	IN	TIMER x capture input 1
TIMERx CAP[2]	IN	TIMER x capture input 2

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Table 127: Timer pins …continued

Symbol	Direction	Description
TIMERx CAP[3]	IN	TIMER x capture input 3
TIMERx MAT[0]	OUT	TIMER x match output 0
TIMERx MAT[1]	OUT	TIMER x match output 1
TIMERx MAT[2]	OUT	TIMER x match output 2
TIMERx MAT[3]	OUT	TIMER x match output 3

8.4.1.3 Register mapping

The timer registers are shown in Table 128. The timer registers have an offset to the base address TMR RegBase which can be found in the memory map (see Table 7).

Table 128: Timer register summary

Address	Type	Reset value	Name	Description	Reference
00h	R/W	00h	IR	timer interrupt register	see Table 129
04h	R/W	0h	TCR	timer control register	see Table 130
08h	R/W	0000 0000h	TC	timer counter value	see Table 131
0Ch	R/W	0000 0000h	PR	prescale register	see Table 132
10h	R/W	0000 0000h	PC	prescale counter value	see Table 133
14h	R/W	000h	MCR	match control register	see Table 134
18h	R/W	0000 0000h	MR0	match register 0	see Table 135
1Ch	R/W	0000 0000h	MR1	match register 1	see Table 135
20h	R/W	0000 0000h	MR2	match register 2	see Table 135
24h	R/W	0000 0000h	MR3	match register 3	see Table 135
28h	R/W	000h	CCR	capture control register	see Table 136
2Ch	R	0000 0000h	CR0	capture register 0	see Table 137
30h	R	0000 0000h	CR1	capture register 1	see Table 137
34h	R	0000 0000h	CR2	capture register 2	see Table 137
38h	R	0000 0000h	CR3	capture register 3	see Table 137
3Ch	R/W	000h	EMR	external match register	see Table 138

8.4.1.4 Timer interrupt register (IR)

The timer interrupt register consists of 4 bits for the interrupts on the match register matches and 4 bits for the interrupts on capture events. If an interrupt is being generated, then the corresponding bit in the timer interrupt register will be logic 1. Otherwise, the bit will be logic 0. Writing a logic 1 to the corresponding timer interrupt register bit will reset the interrupt. Writing logic 0 has no effect. Writing a logic 1 instead of logic 0 allows to write the contents of the interrupt register to itself thus providing a quick method of clearing.

An interrupt is generated if one of the match registers matches the contents of the timer counter and the interrupt is enabled through the match control register or the concerned capture input satisfies one of the conditions in the capture control register and the interrupts are enabled via the capture control register.

Table 129 shows the bit assignment of the IR register.

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Table 129. IR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
7	INTR_C3	R/W	0*	interrupt bit for a CR3 load on capture 3 event; writing logic 1 clears the interrupt flag
6	INTR_C2	R/W	0*	interrupt bit for a CR2 load on capture 2 event; writing logic 1 clears the interrupt flag
5	INTR_C1	R/W	0*	interrupt bit for a CR1 load on capture 1 event; writing logic 1 clears the interrupt flag
4	INTR_C0	R/W	0*	interrupt bit for a CR0 load on capture 0 event; writing logic 1 clears the interrupt flag
3	INTR_M3	R/W	0*	interrupt bit for a MR3 and TC match; writing logic 1 clears the interrupt flag
2	INTR_M2	R/W	0*	interrupt bit for a MR2 and TC match; writing logic 1 clears the interrupt flag
1	INTR_M1	R/W	0*	interrupt bit for a MR1 and TC match; writing logic 1 clears the interrupt flag
0	INTR_M0	R/W	0*	interrupt bit for a MR0 and TC match; writing logic 1 clears the interrupt flag

8.4.1.5 Timer control register (TCR)

The timer control register maintains 2 bits which are used to control the operation of the timer counter. Bit COUNTER_ENABLE switches on and off the timer and prescale counter. Bit COUNTER_RESET clears the timer and prescale counter.

Table 130 shows the bit assignment of the TCR register.

Table 130. TCR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 2	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
1	COUNTER_ RESET	R/W	0*	reset timer and prescale counter; if this bit is set, the counters remain reset until this bit is cleared again
0	COUNTER_ ENABLE	R/W	0*	enable timer and prescale counter; if this bit is set, the counters are running

8.4.1.6 Timer counter (TC)

The timer counter represents the timer count value which is incremented every prescale cycle.

Table 131 shows the bit assignment of the TC register.

Table 131. TC register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	TC[31:0]	R/W	0000 0000h*	timer counter; it is advised not to access this register

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8.4.1.7 Prescale register (PR)

The prescale register determines the number of clock cycles as prescale value for the timer counter clock.

Table 132 shows the bit assignment of the PR register.

Table 132. PR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	PR[31:0]	R/W	0000 0000h*	prescale register; this register specifies the maximum value for the prescale counter

8.4.1.8 Prescale counter (PC)

The prescale counter represents the prescale count value which is incremented every clock cycle.

Table 133 shows the bit assignment of the PC register.

Table 133. PC register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	PC[31:0]	R	0000 0000h*	prescale counter; this register reflects the prescale counter value

8.4.1.9 Match control register (MCR)

Each match register can be configured through the match control register to stop both the timer counter and prescale counter thus maintaining their value at the time of the match, to restart the timer counter at logic 0, to allow the counters to continue counting and/or generate an interrupt when its contents match those of the timer counter. A stop on match has higher priority than reset on match.

An interrupt is generated if one of the match registers matches the contents of the timer counter and the interrupt is enabled through the match control register.

The match control register is used to control what operations are performed when one of the match registers matches the timer counter.

Table 134 shows the bit assignment of the MCR register.

Table 134. MCR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 12	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
11	STOP_3	R/W		stop on match MR3 and TC
			1	the timer and prescale counter stop counting and bit COUNTER_ENABLE will be cleared if MR3 matches TC
			0*	

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Table 134. MCR register bit description *…continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
10	RESET_3	R/W		reset on match MR3 and TC
			1	the timer counter is reset if MR3 matches TC
			0*	
9	INTR_3	R/W		interrupt on match MR3 and TC
			1	an interrupt is generated if MR3 matches TC
			0*	
8	STOP_2	R/W		stop on match MR2 and TC
			1	the timer and prescale counter stop counting and bit COUNTER_ENABLE will be cleared if MR2 matches TC
			0*	
7	RESET_2	R/W		reset on match MR2 and TC
			1	the timer counter is reset if MR2 matches TC
			0*	
6	INTR_2	R/W		interrupt on match MR2 and TC
			1	an interrupt is generated if MR2 matches TC
			0*	
5	STOP_1	R/W		stop on match MR1 and TC
			1	the timer and prescale counter stop counting and bit COUNTER_ENABLE will be cleared if MR1 matches TC
			0*	
4	RESET_1	R/W		reset on match MR1 and TC
			1	the timer counter is reset if MR1 matches TC
			0*	
3	INTR_1	R/W		interrupt on match MR1 and TC
			1	an interrupt is generated if MR1 matches TC
			0*	
2	STOP_0	R/W		stop on match MR0 and TC
			1	the timer and prescale counter stop counting and bit COUNTER_ENABLE will be cleared if MR0 matches TC
			0*	
1	RESET_0	R/W		reset on match MR0 and TC
			1	the timer counter is reset if MR0 matches TC
			0*	
0	INTR_0	R/W		interrupt on match MR0 and TC
			1	an interrupt is generated if MR0 matches TC
			0*	

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8.4.1.10 Match registers (MR0 to MR3)

The match registers determine the timer counter match value. Four match registers are available per timer.

Table 135 shows the bit assignment of the MRn registers, n from 0 to 3.

Table 135. MR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	MR[31:0]	R/W	0000 0000h*	match register; this register specifies the match value for the timer counter

8.4.1.11 Capture control register (CCR)

The capture control register is used to control when one of the possible four capture registers is loaded with the value in the timer counter and if an interrupt is generated, when the capture occurs.

A rising edge is detected if the sequence of logic 0 followed by logic 1 is found. A falling edge is detected if the sequence of logic 1 followed by logic 0 is found. The capture control register maintains 2 bits for each of the counter registers to allow the sequence detection to be enabled for each of the capture registers. If the enabled sequence is detected, the timer counter value is loaded in the capture register. If enabled through the capture control register, then an interrupt is generated. Setting both the rising and falling bits at the same time is a valid configuration.

A reset clears the CCR register.

Table 136 shows the bit assignment of the CCR register.

Table 136. CCR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 12	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
11	EVENT_3	R/W		interrupt on capture event by input 3
			1	a CR3 load due to a capture event on input 3 will generate an interrupt
			0*	
10	FALL_3	R/W		capture on capture input 3 falling
			1	a sequence of logic 1 followed by logic 0 from capture input 3 will cause CR3 to be loaded with the contents of TC
			0*	
9	RISE_3	R/W		capture on capture input 3 rising
			1	a sequence of logic 0 followed by logic 1 from capture input 3 will cause CR3 to be loaded with the contents of TC
			0*	

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Table 136. CCR register bit description *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
8	EVENT_2	R/W		interrupt on capture event by input 2
			1	a CR2 load due to a capture event on input 2 will generate an interrupt
			0*	
7	FALL_2	R/W		capture on capture input 2 falling
			1	a sequence of logic 1 followed by logic 0 from capture input 2 will cause CR2 to be loaded with the contents of TC
			0*	
6	RISE_2	R/W		capture on capture input 2 rising
			1	a sequence of logic 0 followed by logic 1 from capture input 2 will cause CR2 to be loaded with the contents of TC
			0*	
5	EVENT_1	R/W		interrupt on capture event by input 1
			1	a CR1 load due to a capture event on input 1 will generate an interrupt
			0*	
4	FALL_1	R/W		capture on capture input 1 falling
			1	a sequence of logic 1 followed by logic 0 from capture input 1 will cause CR1 to be loaded with the contents of TC
			0*	
3	RISE_1	R/W		capture on capture input 1 rising
			1	a sequence of logic 0 followed by logic 1 from capture input 1 will cause CR1 to be loaded with the contents of TC
			0*	
2	EVENT_0	R/W		interrupt on capture event by input 0
			1	a CR0 load due to a capture event on input 0 will generate an interrupt
			0*	
1	FALL_0	R/W		capture on capture input 0 falling
			1	a sequence of logic 1 followed by logic 0 from capture input 0 will cause CR0 to be loaded with the contents of TC
			0*	
0	RISE_0	R/W		capture on capture input 0 rising
			1	a sequence of logic 0 followed by logic 1 from capture input 0 will cause CR0 to be loaded with the contents of TC
			0*	

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8.4.1.12 Capture registers (CR0 to CR3)

The capture registers are loaded with the timer counter value when there is an event on the concerned capture input. Four capture registers are available per timer.

Table 137 shows the bit assignment of the CRn registers, n from 0 to 3.

Table 137. CR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	CR[31:0]	R	0000 0000h*	capture register; this register reflects after a capture event the timer counter captured value

8.4.1.13 External match register (EMR)

The external match register provides both control and status of the external match pins. The external match flags and the match outputs can either toggle, go logic 0, go logic 1 or maintain state when the contents of match register is equal to the contents of timer counter. Writing directly to external match bits is allowed to change the level of the flags and outputs.

Table 138 shows the bit assignment of the EMR register.

Table 138. EMR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 12	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
11 to 10	CTRL_3[1:0]	R/W	0h*	external match control 3; see Table 139
9 to 8	CTRL_2[1:0]	R/W	0h*	external match control 2; see Table 139
7 to 6	CTRL_1[1:0]	R/W	0h*	external match control 1; see Table 139
5 to 4	CTRL_0[1:0]	R/W	0h*	external match control 0; see Table 139
3	EMR_3	R/W	0*	external match 3; when MR3 matches TC, the external match flag 3 can either toggle, go logic 0, go logic 1, or do nothing; bit CTRL_3 controls the functionality of this output; this bit can also be driven onto the match output 3 in a positive-logic manner (logic 0 = LOW, logic 1 = HIGH)

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Table 138. EMR register bit description *...continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
2	EMR_2	R/W	0*	external match 2; when MR2 matches TC, the external match flag 2 can either toggle, go logic 0, go logic 1, or do nothing; bit CTRL_2 controls the functionality of this output; this bit can also be driven onto the match output 2 in a positive-logic manner (logic 0 = LOW, logic 1 = HIGH)
1	EMR_1	R/W	0*	external match 1; when MR1 matches TC, the external match flag 1 can either toggle, go logic 0, go logic 1, or do nothing; bit CTRL_1 controls the functionality of this output; this bit can also be driven onto the match output 1 in a positive-logic manner (logic 0 = LOW, logic 1 = HIGH)
0	EMR_0	R/W	0*	external match 0; when MR0 matches TC, the external match flag 0 can either toggle, go logic 0, go logic 1, or do nothing; bit CTRL_0 controls the functionality of this output; this bit can also be driven onto the match output 0 in a positive-logic manner (logic 0 = LOW, logic 1 = HIGH)

Table 139: External match control bit description

CTRL_n[1:0]	Function
00	do nothing
01	set logic 0
10	set logic 1
11	toggle

8.4.2 UART

8.4.2.1 Overview

The UART is commonly used to implement a serial interface such as an RS232. The SJA2020 contains an industry standard 550 UART with 16-byte transmit and receive FIFOs, but can also be put into 450 mode without FIFOs.

The key features are:

- 16-byte receive and transmit FIFOs
- Register locations conform to 550 industry standard
- Receiver FIFO trigger points at 1 byte, 4 bytes, 8 bytes and 14 bytes
- Built-in baud rate generator

Note that each LIN controller has also a standard 450 UART without FIFOs.

8.4.2.2 UART pin description

The UART in the SJA2020 have the following pins. The UART pins are combined with other functions on the port pins of the SJA2020, see Section 8.3.2. Table 140 shows the UART pins.

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Table 140: UART pins

Symbol	Direction	Description
UARTx TXD	OUT	UART channel x transmit data output
UARTx RXD	IN	UART channel x receive data input

8.4.2.3 Register mapping

The UART registers are shown in Table 142.

The UART registers have an offset to the base address UART RegBase which can be found in the memory map (see Table 7).

Some UART registers are dependent on the setting of bit DLAB, see Table 149.

Table 141: UART register summary

Address	Bit	Type	Reset value	Name	Description	Reference
00h	DLAB = 0	R	-	RBR	receiver buffer register	see Table 142
		W	-	THR	transmit holding register	see Table 143
	DLAB = 1	R/W	01h	DLL	divisor latch LSB register	see Table 154
04h	DLAB = 0	R/W	0h	IER	interrupt enable register	see Table 144
	DLAB = 1	R/W	00h	DLM	divisor latch MSB register	see Table 155
08h		R	01h	IIR	interrupt ID register	see Table 145
		W	00h	FCR	FIFO control register	see Table 147
0Ch		R/W	00h	LCR	line control register	see Table 149
10h		-	-	-	[1]	
14h		R	60h	LSR	line status register	see Table 152
18h		-	-	-	[1]	
1Ch		R/W	00h	SCR	scratch register	see Table 153

[1] Reserved for future expansion; write all logic 0 only.

8.4.2.4 Receive buffer register (RBR)

The receive buffer register is the top byte of the receive FIFO. The top byte of the receive FIFO contains the oldest character received and can be read via the bus interface. In 450 mode, received data is passed from the receive shift register to the top byte of the receive buffer register, essentially producing an 1-byte Rx FIFO. The least significant bit represents the oldest received data bit. If the character received is less than 8 bits, the unused most significant bits are padded with logic 0.

The RBR register is read only and the divisor latch access bit DLAB must be logic 0 for access.

Table 142 shows the bit assignment of the RBR register.

Table 142. RBR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; read as logic 0
7 to 0	RBR[7:0]	R	-	receive buffer register; contains the oldest received byte in the receive FIFO

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8.4.2.5 Transmit holding register (THR)

The transmit holding register is the top byte of the transmit FIFO. The top byte is the newest character in the transmit FIFO and can be written via the bus interface. In 450 mode, data is passed from the THR to the transmit shift register, essentially producing a 1-byte transmit FIFO. The least significant bit represents the first bit to transmit.

The THR register is write only and the divisor latch access bit DLAB must be logic 0 for access. Table 143 shows the bit assignment of the THR register.

Table 143. THR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, write as logic 0
7 to 0	THR[7:0]	W	-	transmit holding register; writing to the transmit holding register causes the data to be stored in the transmit FIFO; the byte will be sent when it reaches the bottom of the FIFO and the transmitter is available

8.4.2.6 Interrupt enable register (IER)

The interrupt enable register is used to enable the four types of interrupts referred to in the interrupt identification register. The divisor latch access bit DLAB must be logic 0 in order to access the IER register.

Table 144 shows the bit assignment of the IER register.

Table 144. IER register bits
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 3	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
2	LSIE	R/W		receiver line status interrupt enable
			1	the receive line status interrupt is enabled
			0*	
1	TBEIE	R/W		transmit holding register empty interrupt enable
			1	the transmit holding register empty interrupt is enabled
			0*	
0	RBIE	R/W		receive buffer register interrupt register enable
			1	the receive data available interrupt is enabled
			0*	

8.4.2.7 Interrupt ID register (IIR)

The interrupt ID register provides a status code that denotes the priority and source of a pending interrupt. When an interrupt is generated, the interrupt ID register indicates that an interrupt is pending and encodes the type in its three least significant bits. The interrupts are frozen during an access to the interrupt ID register. If an interrupt occurs during an access, the interrupt is recorded for the next interrupt ID register access.

The IIR register is read only.

Table 145 shows the bit assignment of the IIR register.

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Table 145. IIR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; read as logic 0
7	FIFO_ EN	R	0*	FIFOs enabled; represents FIFO enable bit of the FIFO control register; in 450 mode this bit is always logic 0
6	FIFO_ EN	R	0*	FIFOs enabled; represents FIFO enable bit of the FIFO control register; in 450 mode this bit is always logic 0
5 to 4	reserved	-	-	reserved; read as logic 0
3 to 0	INT_ID[3:0]	R	1h*	interrupt identification; see Table 146

Table 146: Interrupt identification configuration bits

INT_ID[3:0]	Priority level	Interrupt		
		Type	Source	Reset method
0001	none	none	none	none
0110	1	receiver line status	overrun error, parity error, framing error, or break interrupt	read line status register
0100	2	received data available	receiver data available in 450 mode or trigger level reached in 550 mode	read receive buffer register
1100	2	character time-out indication	no characters have been removed from or input to receiver FIFO during the last four character times, and there is at least one character in it during this time	read receive buffer register
0010	3	transmitter holding register empty	transmit holding register empty	read interrupt ID register (if source of interrupt) or writing into transmitter holding register

8.4.2.8 FIFO control register (FCR)

The FIFO control register enables and clears the FIFOs, sets the receiver FIFO level, and selects the type of DMA signalling.

The FCR register is write only.

Table 147 shows the bit assignment of the FCR register.

Table 147. FCR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, write as logic 0
7 to 6	REV_TRIG[1:0]	W	0h*	trigger level for receiver FIFO interrupt; see Table 148
5 to 4	reserved	-	-	reserved; write as logic 0

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Table 147. FCR register bit description *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
3	DMA_M	W		DMA mode
			1	when logic 1 and in FIFO mode, multiple character transfers are performed until the transmitter FIFO is filled or the receiver FIFO is empty; the receiver direct memory access becomes active when the receive FIFO trigger level is reached or a character time-out occurred
			0*	only single character transfers are done as default in 450 mode
2	TX_FIFO_R	W		transmitter FIFO reset
			1	when logic 1 and in FIFO mode, all bytes in the transmitter FIFO and the transmitter FIFO pointer are cleared; the shift register is not cleared; the transmitter FIFO reset bit is self clearing
			0*	
1	RX_FIFO_R	W		receiver FIFO reset
			1	when logic 1 and in FIFO mode, all bytes in the receiver FIFO and the receiver FIFO pointer are cleared; the shift register is not cleared; the receiver FIFO reset bit is self clearing
			0*	
0	FIFO_EN	W		
			1	the transmitter and receiver FIFOs are enabled and the UART operates in FIFO mode; the FIFO enable bit must be set when other FIFO control register bits are written to or they are not programmed; changing this bit clears the FIFOs
			0*	the UART operates in 450 mode

Table 148: Receiver trigger level configuration bits

REV_TRIG [1:0]	Function
00	receiver FIFO contains 1 byte
01	receiver FIFO contains 4 bytes
10	receiver FIFO contains 8 bytes
11	receiver FIFO contains 14 bytes

8.4.2.9 Line control register (LCR)

The line control register controls the format of the asynchronous data communication exchange.

Table 149 shows the bit assignment of the LCR register.

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Table 149. LCR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
7	DLAB	R/W		divisor latch access bit
			1	the divisor latch registers of the baud rate generator can be accessed
			0*	the receiver buffer register, the transmit holding register, and the interrupt enable register can be accessed
6	BC	R/W		break control
			1	a break transmission condition is forced which puts the TXD output to LOW
			0*	the break transmission condition is disabled; the break condition has no affect on the transmitter logic; it only affects the TXD line
5 to 4	PS[1:0]	R/W	0h*	parity select; see Table 150
3	PEN	R/W		parity enable
			1	a parity bit is generated in transmitted data between the last data word bit and the first stop bit; in received data the parity is checked
			0*	
2	STB	R/W		number of stop bits
			1	the number of generated stop bits are 2; except the word length is 5 bits, then 1.5 stop bits are generated
			0*	only 1 stop bit is generated
1 to 0	WLS[1:0]	R/W	0h*	word length select; see Table 151

Table 150: Parity select configuration bits

PS [1:0]	Function
00	odd parity: an odd number of logic 1 in the data and parity bits
01	even parity: an even number of logic 1 in the data and parity bits
10	forced logic 1 stick parity
11	forced logic 0 stick parity

Table 151: Word length configuration bits

WLS [1:0]	Function
00	5-bit character length
01	6-bit character length
10	7-bit character length
11	8-bit character length

8.4.2.10 Line status register (LSR)

The line status register provides the information concerning the data transfers.

The LSR register is read only.

Table 152 shows the bit assignment of the LSR register.

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Table 152. LSR register bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; read as logic 0
7	RXFE	R		error in receiver FIFO
			1	the receiver FIFO contains at least one parity, framing, or break error; in 450 mode the error in receiver FIFO bit is always cleared
			0*	
6	TEMT	R		transmitter empty
			1*	the transmitter holding register, transmitter FIFO and the transmitter shift register are both empty; the transmitter empty bit is cleared when either the transmitter holding register or the transmitter shift register contains a data character
			0	
5	THRE	R		transmitter holding register empty
			1*	the transmitter holding register or transmitter FIFO is empty; if the transmitter holding register empty interrupt enable is set, an interrupt is generated; the transmitter holding register empty bit is set when the contents of the transmitter holding register is transferred to the transmitter shift register; the transmitter holding register empty bit is cleared concurrently with loading the transmitter holding register or transmitter FIFO
			0	
4	BI	R		break interrupt
			1	the received data input was held low for longer than a full-word transmission time; a full-word transmission time is defined as the total time to transmit the start, data, parity, and stop bits; the break interrupt bit is cleared upon reading; in FIFO mode, this error is associated with the particular character in the receiver FIFO to which it applies; this error is revealed when its associated character is at the top of the receiver FIFO; when a break occurs, only one logic 0 is loaded into the receiver FIFO; the UART tries to resynchronize after a framing error; to accomplish this, it is assumed that the framing error is due to the next start bit; the UART samples this start bit twice and then accepts the input data
			0*	

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Table 152. LSR register bit description *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
3	FE	R		framing error
			1	the received character did not have a valid (set) stop bit; the framing error is cleared upon Ring; in FIFO mode, this error is associated with the particular character in the receiver FIFO to which it applies; this error is revealed when its associated character is at the top of the receiver FIFO; when a break occurs, only one logic 0 is loaded into the receiver FIFO; the next character transfer is enabled after the RXD input line goes to the marking state (all logic 1) for at least two sample times and then receives the next valid start bit
			0*	
2	PE	R		parity error
			1	the parity of the received data character does not match the parity selected in the line control register; the parity error is cleared upon reading; in FIFO mode, this error is associated with the particular character in the receiver FIFO to which it applies; this error is revealed when its associated character is at the top of the receiver FIFO
			0*	
1	OE	R		overrun error
			1	the character in the receiver buffer register was overwritten by the next character transferred into this register before it was read; the overrun error is cleared upon reading; if the FIFO mode data continues to fill the receiver FIFO beyond the trigger level, an overrun error occurs only after the receiver FIFO is full and the next character has been completely received in the shift register; an overrun error is signalled as soon it happens; the character in the shift register is overwritten, but not transferred to the receiver FIFO
			0*	
0	DR	R		data ready
			1	a complete incoming character has been received and transferred to the receiver buffer register or the receiver FIFO; the data ready bit is cleared by reading all of the data in the receiver buffer register or the receiver FIFO
			0*	

8.4.2.11 Scratch register (SCR)

The scratch register is intended for the programmer's use as scratch pad in the sense that it temporarily holds the programmer's data without affecting any other UART operation.

Table 153 shows the bit assignment of the SCR register.

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Table 153. SCR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, write as logic 0, read as logic 0
7 to 0	SCR[7:0]	R/W	00h*	scratch register; this register can be written and/or read at user's discretion

8.4.2.12 Divisor latch LSB and divisor latch MSB registers (DLL and DLM)

The two divisor latch registers store the divisor in 16-bit binary format for the programmable baud generator. The output frequency of the baud generator is 16 times the baud rate. The input frequency of the baud generator is the system clock frequency divided by the divisor value. A written value of 0000h into the divisor will be treated like value 0001h.

The divisor latch access bit DLAB must be set in order to access the DLL and DLM register.

Table 154 and Table 155 show the bit assignment of respective the DLL and DLM register.

Table 154. DLL register bits
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, write as logic 0, read as logic 0
7 to 0	DLL	R/W	01h*	divisor latch LSB register; the divisor latch LSB register contains the lower byte of the 16-bit divisor

Table 155. DLM register bits
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, write as logic 0, read as logic 0
7 to 0	DLM	R/W	00h*	divisor latch MSB register; the divisor latch MSB register contains the higher byte of the 16-bit divisor

8.4.3 General purpose I/O

8.4.3.1 Overview

Three general purpose I/O ports provide individual control over each bidirectional port pin. There are two registers to control the I/O direction and output level. The inputs are synchronized to achieve stable read levels. The I/O pad behavior depends on the configuration programmed in the I/O pad multiplex register.

The key features are:

- General purpose parallel inputs and outputs
- Direction control of individual bits
- Synchronized input sampling for stable input data values
- All I/O defaults to input at reset to avoid any possible bus conflicts

To generate an open-drain output, set the bit in the output register to the desired value.

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Use the direction register to control the signal. When set to output, the output driver will actively drive the value on the output; when set to input, the signal is floating and can be pulled externally.

8.4.3.2 GPIO pin description

The three GPIO ports in the SJA2020 have the following pins. The GPIO pins are combined with other functions on the port pins of the SJA2020, see Section 8.3.2. Table 157 shows the GPIO pins.

Table 156: GPIO pins

Symbol	Direction	Description
GPIO0 pin[31:0]	IN/OUT	GPIO port 0, pins 31 to 0
GPIO1 pin[31:0]	IN/OUT	GPIO port 1, pins 31 to 0
GPIO2 pin[29:0]	IN/OUT	GPIO port 2, pins 29 to 0

8.4.3.3 Register mapping

The general purpose I/O registers have an offset to the base address GPIO RegBase which can be found in the memory map (see Table 7).

The general purpose I/O registers are shown in Table 157.

Table 157: General purpose I/O register summary

Address	Type	Reset value	Name	Description	Reference
0h	R	-	PINS	port input register	see Table 158
4h	R/W	0000 0000h	OR	port output register	see Table 159
8h	R/W	0000 0000h	DR	port direction register	see Table 160

8.4.3.4 Port input register (PINS)

The port input register is used to reflect the synchronized input level on each I/O pin individually. In case of writing to the port input register, the contents is written into the port output register.

Table 158 shows the bit assignment of the PINS register.

Table 158. PINS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	PINS[31:0]	R/W	-	port input value; bit 0 corresponds to pin Pn[0], etc.; if a input pin is HIGH, then the respective bit is logic 1 and if a input pin is LOW, then the respective bit is logic 0

8.4.3.5 Port output register (OR)

The port output register is used to define the output level on each I/O pin individually in case this pin is configured as output by the port direction register. If the port input register is written, the port output register is written.

Table 159 shows the bit assignment of the OR register.

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Table 159. OR register bits
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	OR[31:0]	R/W	0000 0000h*	port output value; bit 0 corresponds to pin Pn[0], etc.; if configured as output, then a logic 1 drives the respective port to HIGH

8.4.3.6 Port direction register (DR)

The port direction register is used to control each I/O pin output driver enable individually.

Table 160 shows the bit assignment of the DR register.

Table 160. DR register bit
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	DR[31:0]	R/W	0000 0000h*	port direction control; bit 0 corresponds to pin Pn[0], etc.; if the bit is logic 1, then the respective port pin is configured as output

8.5 In-vehicle networking subsystem

8.5.1 CAN

8.5.1.1 Overview

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The six CAN controllers in the SJA2020 provide a full implementation of the CAN protocol according to the CAN specification version 2.0B. The gateway concept is fully scalable with the number of CAN controllers and always operates together with a separated powerful and flexible hardware acceptance filter.

The key features are:

- Supports 11-bit identifier as well as 29-bit identifier
- Double receive buffer and triple transmit buffer
- Programmable error warning limit and error counters with read/write access
- Arbitration lost capture and error code capture with detailed bit position
- Single shot transmission (no re-transmission)
- Listen only mode (no acknowledge, no active error flags)
- Reception of ‘own’ messages (self reception request)

8.5.1.2 CAN pin description

The six CAN controllers in the SJA2020 have the following pins. The CAN pins are combined with other functions on the port pins of the SJA2020, see Section 8.3.2. Table 161 shows the CAN pins, x runs from 0 to 5.

Table 161: CAN pins

Symbol	Direction	Description
CANx TXDC	OUT	CAN channel x transmit data output
CANx RXDC	IN	CAN channel x receive data input

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8.5.1.3 Register mapping

The CAN registers are shown in Table 162.

The CAN registers have an offset to the CAN base addresses which can be found in the memory map (see Table 7).

Table 162: CAN register summary

Address	Type	Reset value	Name	Description	Reference
CAN controller; CANC RegBase offset					
00h	R/W	01h	CCMODE	CAN controller mode register	see Table 163
04h	W	00h	CCCMD	CAN controller command register	see Table 164
08h	R/W	0000 003Ch	CCGS	CAN controller global status register	see Table 165
0Ch	R	0000 0000h	CCIC	CAN controller interrupt and capture register	see Table 166
10h	R/W	000h	CCIE	CAN controller interrupt enable register	see Table 169
14h	R/W	1C 0000h	CCBT	CAN controller bus timing register	see Table 170
18h	R/W	60h	CCEWL	CAN controller error warning limit register	see Table 171
1Ch	R	3C 3C3Ch	CCSTAT	CAN controller status register	see Table 172
20h	R/W	0000 0000h	CCRXBMI	CAN controller receive buffer message info register	see Table 173
24h	R/W	0000 0000h	CCRXBID	CAN controller receive buffer identifier register	see Table 174
28h	R/W	0000 0000h	CCRXBDA	CAN controller receive buffer data A register	see Table 175
2Ch	R/W	0000 0000h	CCRXBDB	CAN controller receive buffer data B register	see Table 176
30h	R/W	0000 0000h	CCTXB1MI	CAN controller transmit buffer 1 message info register	see Table 177
34h	R/W	0000 0000h	CCTXB1ID	CAN controller transmit buffer 1 identifier register	see Table 178
38h	R/W	0000 0000h	CCTXB1DA	CAN controller transmit buffer 1 data A register	see Table 179
3Ch	R/W	0000 0000h	CCTXB1DB	CAN controller transmit buffer 1 data B register	see Table 180
40h	R/W	0000 0000h	CCTXB2MI	CAN controller transmit buffer 2 message info register	see Table 177
44h	R/W	0000 0000h	CCTXB2ID	CAN controller transmit buffer 2 identifier register	see Table 178
48h	R/W	0000 0000h	CCTXB2DA	CAN controller transmit buffer 2 data A register	see Table 179
4Ch	R/W	0000 0000h	CCTXB2DB	CAN controller transmit buffer 2 data B register	see Table 180
50h	R/W	0000 0000h	CCTXB3MI	CAN controller transmit buffer 3 message info register	see Table 177

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Table 162: CAN register summary …continued

Address	Type	Reset value	Name	Description	Reference
54h	R/W	0000 0000h	CCTXB3ID	CAN controller transmit buffer 3 identifier register	see Table 178
58h	R/W	0000 0000h	CCTXB3DA	CAN controller transmit buffer 3 data A register	see Table 179
5Ch	R/W	0000 0000h	CCTXB3DB	CAN controller transmit buffer 3 data B register	see Table 180
CAN ID-look-up table memory; CANAFM RegBase offset					
000h to 7FCh	R/W	-	CAFMEM	CAN ID-look-up table memory	see Table 181
CAN acceptance filter; CANAFR RegBase offset					
00h	R/W	1h	CAMODE	CAN acceptance filter mode register	see Table 188
04h	R/W	000h	CASFESA	CAN acceptance filter standard frame explicit start address register	see Table 189
08h	R/W	000h	CASFGSA	CAN acceptance filter standard frame group start address register	see Table 190
0Ch	R/W	000h	CAEFESA	CAN acceptance filter extended frame explicit start address register	see Table 191
10h	R/W	000h	CAEFGSA	CAN acceptance filter extended frame group start address register	see Table 192
14h	R/W	000h	CAEOTA	CAN acceptance filter end of table address register	see Table 193
18h	R	000h	CALUTEA	CAN acceptance filter look-up table error address register	see Table 194
1Ch	R	0h	CALUTE	CAN acceptance filter look-up table error register	see Table 195
CAN central status; CANCS RegBase offset					
0h	R	3F 3F3Fh	CCCTS	CAN controllers central transmit status register	see Table 196
4h	R	00 003Fh	CCCRS	CAN controllers central receive status register	see Table 197
8h	R	0000h	CCCMS	CAN controllers central miscellaneous status register	see Table 198

The following CAN controller register tables have a soft reset mode value besides the reset value:

- A hardware reset overrules the soft reset mode
- If no soft reset value is specified the content is unchanged by the soft reset mode
- Bit fields with ‘X’ means that the content is unchanged upon setting the soft reset mode

The reset value shows the result of hardware reset, while the soft reset mode value indicates the result when the RM bit is set either by software or due to a bus-off condition.

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8.5.1.4 CAN controller mode register (CCMODE)

The CAN controller mode register is used to change the behavior of the CAN controller.

Table 163 shows the bit assignment of the CCMODE register.

Table 163: CCMODE register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 6	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
5	RPM [1]	R/W		X	reverse polarity mode
			1		RXDC and TXDC pins are HIGH for a dominant bit
			0*		RXDC and TXDC pins are LOW for a dominant bit
4	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
3	TPM [1][2]	R/W		X	transmit priority mode
			1		the priority depends on the contents of the transmit priority register within the transmit buffer
			0*		the transmit priority depends on the CAN identifier
2	STM [1]	R/W		X	self test mode; this bit is only writable in soft reset mode
			1		the controller will consider a transmitted message successful if there is no acknowledgment; use this state in conjunction with the self reception request bit in the CAN controller command register
			0*		a transmitted message must be acknowledged to be considered successful
1	LOM [1][3]	R/W		X	listen only mode; this bit is only writable in soft reset mode
			1		the controller gives no acknowledgment on CAN, even if a message is successfully received; messages cannot be sent, and the controller operates in error passive mode
			0*		the CAN controller acknowledges a successfully-received message

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Table 163: CCMODE register bit description *…continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
0	RM [4][5]	R/W		1	soft reset mode
			1*		soft reset mode active; CAN operation is disabled, and writable registers can be written. Bits having a soft reset mode value are being reset.
			0		soft reset mode inactive; the CAN controller in normal operation and certain registers can not be written

[1] A write access to the RPM, TPM, STM and LOM registers is possible only if the soft reset mode is entered previously.

[2] In cases where the same transmit priority or the same ID is chosen for more than one buffer, then the transmit buffer with the lowest buffer number is sent first.

[3] This mode of operation forces the CAN controller to be error passive. Message transmission is not possible.

[4] During a hardware reset or when the bus status bit is set 1 (bus-off), the soft reset mode bit is set 1 (present). After the soft reset mode bit is set 0 the CAN controller will wait for:

a) One occurrence of bus-free signal (11 recessive bits), if the preceding reset has been caused by a Hardware reset or a CPU-initiated reset.

b) 128 occurrences of bus-free, if the preceding reset has been caused by a CAN controller initiated bus-off, before re-entering the bus-on mode.

[5] When entering soft reset mode, it is not possible to access any other register within the same instruction.

8.5.1.5 CAN controller command register (CCCMD)

The CAN controller command register initiates an action within the transfer layer of the CAN controller.

The CCCMD register is write only. Table 164 shows the bit assignment of the CCCMD register.

Table 164: CCCMD register bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 8	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
7	STB3	W	-	-	select transmit buffer 3; when logic 1, transmit buffer 3 is selected for transmission
6	STB2	W	-	-	select transmit buffer 2; when logic 1, transmit buffer 2 is selected for transmission
5	STB1	W	-	-	select transmit buffer 1; when logic 1, transmit buffer 1 is selected for transmission

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Table 164: CCCMD register bit description *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
4	SRR [1][2][3]	W	-	-	self reception request; when logic 1, a message shall be transmitted from the selected transmit buffer and received simultaneously; transmission and self reception request has to be set simultaneously with STB3, STB2 or STB1
3	CDO	W	-	-	clear data overrun; when logic 1, the data overrun bit in the CAN controller status register is cleared; this command bit is used to clear the Data Overrun condition signalled by the Data Overrun Status bit; as long as the Data Overrun Status bit is set no further Data Overrun Interrupt is generated
2	RRB [4]	W	-	-	release receive buffer; when logic 1, the receive buffer, representing the message memory space in the double receive buffer is released
1	AT [5][3]	W	-	-	abort transmission; when logic 1, if not already in progress, a pending transmission request is cancelled; if the abort transmission and transmit request bits are set in the same write operation, frame transmission is attempted once and no retransmission is attempted if an error is flagged nor if arbitration is lost
0	TR [2][6][3]	W	-	-	transmission request; when logic 1, a message from the selected transmit buffer is queued for transmission

[1] Upon self reception request a message is transmitted and simultaneously received if the acceptance filter is set to the corresponding identifier. A receive and a transmit interrupt will indicate correct self reception (see also self test mode in mode register).

[2] It is possible to select more than one message buffer for transmission. If more than one buffer is selected for transmission (TR = 1 or SRR = 1) the internal transmit message queue is organized such as that depending on the Transmit Priority Mode (TPM) the transmit buffer with the lowest CAN identifier (ID) or the lowest 'local priority' (TXPRIO) wins the prioritization and is sent first.

[3] Setting the command bits TR and AT simultaneously results in transmitting a message once. No re-transmission will be performed in case of an error or arbitration lost (single shot transmission). Setting the command bits SRR and AT simultaneously results in sending the transmit message once using the self-reception feature. No re-transmission will be performed in case of an error or arbitration lost. Setting the command bits TR, AT and SRR simultaneously results in transmitting a message once as described for TR and AT. The moment the transmit status bit is set within the status register, the internal transmission request bit is cleared automatically. Setting TR and SRR simultaneously will ignore the set SRR bit.

[4] After reading the contents of the receive buffer, the CPU can release this memory space by setting the release receive buffer bit to 1. This may result in another message becoming immediately available. If there is no other message available, the receive interrupt bit is reset. If the RRB command is given, it will take at least 2 internal clock cycles before a new interrupt is generated.

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[5] The abort transmission bit is used when the CPU requires the suspension of the previously requested transmission, e.g. to transmit a more urgent message before. A transmission already in progress is not stopped. In order to see if the original message has been either transmitted successfully or aborted, the transmission complete status bit should be checked. This should be done after the Transmit Buffer Status bit has been set 1 or a transmit interrupt has been generated.

[6] If the transmission request or the self-reception request bit was set 1 in a previous command, it cannot be cancelled by resetting the bits. The requested transmission may only be cancelled by setting the abort transmission bit.

8.5.1.6 CAN controller global status register (CCGS)

The CAN controller global status register reflects the global status of the CAN controller including the transmit and receive error counter values.

Table 165 shows the bit assignment of the CCGS register.

Table 165: CCGS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 24	TXERR[7:0]	R/W	00h*	X	transmit error counter; this register reflects the current value of the transmit error counter; this register is only writable in soft reset mode; if a bus off event occurs, the transmit error counter is initialized to 127 to count the minimum protocol-defined time (128 occurrences of the bus free signal); reading the transmit error counter during this time gives information about the status of the bus off recovery; if bus off is active, a write access to transmit error counter in the range of 0 to 254 clears the bus off flag and the controller will wait for one occurrence of 11 consecutive recessive bits (bus free) after clearing of soft reset mode bit
23 to 16	RXERR[7:0]	R/W	00h*	X	receive error counter; this register reflects the current value of the receive error counter; this register is only writable in soft reset mode; if a bus off event occurs, the receive error counter is initialized to 00h; as long as the bus off condition is valid, writing to this register has no effect
15 to 8	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
7	BS [1]	R		0	bus status
			1		the CAN controller is currently prohibited from bus activity because the transmit error counter reached its limiting value of FFh
			0*		

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Table 165: CCGS register bit description *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
6	ES [2]	R		0	error status
			1		one or both of the transmit and receive error counters has reached the limit set in the error warning limit register
			0*		
5	TS [3]	R		1	transmit status
			1*		the CAN controller is transmitting a message
			0		
4	RS [3]	R		1	receive status
			1*		the CAN controller is receiving a message
			0		
3	TCS [4]	R		X	transmission complete status
			1*		all requested message transmissions have been successfully completed
			0		at least one of the previously requested transmission is not yet completed
2	TBS	R		1	transmit buffer status
			1*		all transmit buffers are available for the CPU
			0		at least one of the transmit buffers contains a previously queued message that has not yet been sent
1	DOS [5]	R		0	data overrun status
			1		a message was lost because the preceding message to this CAN controller was not read and released quickly enough
			0*		no data overrun has occurred
0	RBS [6]	R		0	receive buffer status
			1		at least one complete message is available in the double receive buffer; this bit is cleared by the release receive buffer command in the CAN controller command register if no subsequent received message is available
			0*		no message is available in the double receive buffer

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[1] When the transmit error counter exceeds the limit of 255, the bus status bit is set 1 (bus-off), the CAN controller will set the soft reset mode bit to 1 (present) and an error warning interrupt is generated, if enabled. Afterwards the transmit error counter is set to '127' and the receive error counter is cleared. It will stay in this mode until the CPU clears the soft reset mode bit. Once this is completed the CAN controller will wait the minimum protocol-defined time (128 occurrences of the bus-free signal) counting down the transmit error counter. After that the bus status bit is cleared (bus-on), the error status bit is set 0 (ok), the error counters are reset and an error warning interrupt is generated, if enabled. Reading the TX error counter during this time gives information about the status of the bus-off recovery.

[2] Errors detected during reception or transmission will affect the error counters according to the CAN specification. The error status bit is set when at least one of the error counters has reached or exceeded the error warning Limit. An error warning interrupt is generated, if enabled. The default value of the error warning limit after hardware reset is 96 decimal, see also CCEWL register bits.

[3] If both the receive status and the transmit status bits are 0 (idle) the CAN-bus is idle. If both bits are set the controller is waiting to become idle again. After hardware reset 11 consecutive recessive bits have to be detected until idle status is reached. After bus-off this will take 128 times of 11 consecutive recessive bits.

[4] The transmission complete status bit is set 0 (incomplete) whenever the transmission request bit or the self reception request bit is set 1 at least for one of the three transmit buffers. The transmission complete status bit will remain 0 until all messages are transmitted successfully.

[5] If there is not enough space to store the message within the receive buffer, that message is dropped and the data overrun condition is signalled to the CPU in the moment this message becomes valid. If this message is not completed successfully (e.g. because of an error), no overrun condition is signalled.

[6] After reading all messages and releasing their memory space with the command 'release receive buffer' this bit is cleared.

8.5.1.7 CAN controller interrupt and capture register (CCIC)

The CAN controller interrupt and capture register allows the identification of an interrupt source. Reading the interrupt register clears all interrupt bits except the receive interrupt bit which requires release receive buffer command. If there is another message available within the receive buffer after the release receive buffer command, the receive interrupt is set again. Otherwise the receive interrupt keeps cleared.

Bus errors are captured in a detailed error report. When a transmitted message loses arbitration, the bit where the arbitration has lost is captured. Once either of these registers is captured, its value will remain the same until it is read, at which time it is released to capture a new value.

The CCIC register is read only. Table 166 shows the bit assignment of the CCIC register.

Table 166: CCIC register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 29	reserved	-	-	-	reserved; do not modify, read as logic 0

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Table 166: CCIC register bit description *...continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
28 to 24	ALCBIT[4:0]	R	00h*	X	arbitration lost bit; in case the arbitration is lost while transmitting a message, the bit number within the frame is captured into this register)
			00h*		arbitration lost in the first, most significant bit of the identifier
			:		:
			0Bh		11: arbitration lost in SRTR bit (RTR bit for standard frame messages)
			0Ch		12: arbitration lost in IDE bit 13: arbitration lost in 12th bit of identifier (extended frame only)
			:		:
			1Eh		30: arbitration lost in last bit of identifier (extended frame only)
			0Fh		31: arbitration lost in RTR bit (extended frames only)
23 to 22	ERRT[1:0]	R	0h*	X	error type; the bus error type is captured in this register; see Table 167
21	ERRDIR	R		X	error direction
			1		he bus error is captured during receiving
			0*		the bus error is captured during transmitting
20 to 16	ERRCC[4:0]	R	00h*	X	error code capture; the location of the error within the frame is captured in this register; see Table 168
15 to 11	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
10	TI3	R		0	transmit interrupt 3
			1		the transmit buffer status 3 is released (transition from logic 0 to logic 1) and the transmit interrupt enable 3 is set
			0*		
9	TI2	R		0	transmit interrupt 2
			1		the transmit buffer status 2 is released (transition from logic 0 to logic 1) and the transmit interrupt enable 2 is set
			0*		
8	IDI	R		0	ID ready interrupt
			1		a CAN identifier has been received and the ID ready interrupt enable is set
			0*		

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Table 166: CCIC register bit description *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
7	BEI	R		X	bus error interrupt
			1		a CAN controller has detected a bus error and the bus error interrupt enable is set
			0*		
6	ALI	R		0	arbitration lost interrupt
			1		the CAN controller has lost arbitration while attempting to transmit and the arbitration lost interrupt enable is set
			0*		
5	EPI	R		0	error passive interrupt
			1		the CAN controller has reached the error passive status (at least one error counter exceeds the CAN protocol defined level of 127) or if the CAN controller is in error passive status and enters the error active status again and the error passive interrupt enable is set
			0*		
4	reserved	-	-	-	reserved; read as logic 0
3	DOI	R		0	data overrun interrupt
			1		the data overrun occurred and the data overrun interrupt enable is set
			0*		
2	EWI	R		X	error warning interrupt
			1		a change of either the error status or bus status occurred and the error warning interrupt enable is set
			0*		
1	TI1	R		0	transmit interrupt 1
			1		the transmit buffer status 1 is released (transition from logic 0 to logic 1) and the transmit interrupt enable 1 is set
			0*		
0	RI [1]	R		0	receive interrupt
			1		the receive buffer status is logic 1 and the receive interrupt enable is set
			0*		

[1] The receive interrupt bit is not cleared upon a read access to the interrupt register. Giving the command 'release receive buffer' will clear RI temporarily. If there is another message available within the receive buffer after the release command, RI is set again. Otherwise RI keeps cleared.

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Table 167: Bus error type values

ERRT[1:0]	Function
00	bit error
01	form error
10	stuff error
11	other error

Table 168: Bus error capture code values

ERRCC [4:0]	Function
0 0000	reserved
0 0001	reserved
0 0010	identifier bits 21 to 28
0 0011	start of frame
0 0100	standard frame RTR bit
0 0101	IDE bit
0 0110	reserved
0 0111	identifier bits 13 to 17
0 1000	CRC sequence
0 1001	reserved bit 0
0 1010	data field
0 1011	data length code
0 1100	extended frame RTR bit
0 1101	reserved bit 1
0 1110	identifier bits 0 to 4
0 1111	identifier bits 5 to 12
1 0000	reserved
1 0001	active error flag
1 0010	intermission
1 0011	tolerate dominant bits
1 0100	reserved
1 0101	reserved
1 0110	passive error flag
1 0111	error delimiter
1 1000	CRC delimiter
1 1001	acknowledge slot
1 1010	end of frame
1 1011	acknowledge delimiter
1 1100	overload flag
1 1101	reserved
1 1110	reserved
1 1111	reserved

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8.5.1.8 CAN controller interrupt enable register (CCIE)

The CAN controller interrupt enable register allows enabling the different types of CAN controller interrupts.

Table 169 shows the bit assignment of the CCIE register.

Table 169: CCIE register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 11	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
10	TI3E	R/W		X	transmit interrupt enable 3
			1		an interrupt is generated if the transmit buffer status 3 is released (transition from logic 0 to logic 1)
			0*		
9	TI2E	R/W		X	transmit interrupt enable 2
			1		an interrupt is generated if the transmit buffer status 2 is released (transition from logic 0 to logic 1)
			0*		
8	IDIE	R/W		X	ID ready interrupt enable
			1		an interrupt is generated if a CAN identifier has been received
			0*		
7	BEIE	R/W		X	bus error interrupt enable
			1		an interrupt is generated if a CAN controller has detected a bus error
			0*		
6	ALIE	R/W		X	arbitration lost interrupt enable
			1		an interrupt is generated if the CAN controller has lost arbitration while attempting to transmit
			0*		
5	EPIE	R/W		X	error passive interrupt enable
			1		an interrupt is generated if the CAN controller has reached the error passive status (at least one error counter exceeds the CAN protocol defined level of 127) or if the CAN controller is in error passive status and enters the error active status again
			0*		
4	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0

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Table 169: CCIE register bit description *...continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
3	DOIE	R/W		X	data overrun interrupt enable
			1		an interrupt is generated if the data overrun occurred
			0*		
2	EWIE	R/W		X	error warning interrupt enable
			1		an interrupt is generated if a change of either the error status or bus status occurred
			0*		
1	TIE1	R/W		X	transmit interrupt enable 1
			1		an interrupt is generated if the transmit buffer status 1 is released (transition from logic 0 to logic 1)
			0*		
0	RIE	R/W		X	receive interrupt enable
			1		an interrupt is generated if the receive buffer is not empty
			0*		

8.5.1.9 CAN controller bus timing register (CCBT)

The CAN controller bus timing register defines the timing characteristics of the CAN bus. The bus timing register is only writable in soft reset mode.

Table 170 shows the bit assignment of the CCBT register.

Table 170: CCBT register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 24	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
23	SAM	R/W		X	
			1		the bus is sampled three times; recommended for low/medium speed buses, where filtering spikes on the bus-line is beneficial
			0*		the bus is sampled once; recommended for high speed buses
22 to 20	TSEG2[2:0]	R/W	1h*	X	timing segment 2; time segment after the sample point which is determined by the formula of [1]
19 to 16	TSEG1[3:0]	R/W	Ch*	X	timing segment 1; time segment before the sample point which is determined by the formula of [2]

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Table 170: CCBT register bit description *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
15 to 14	SJW[1:0]	R/W	0h*	X	synchronization jump width; the synchronization jump length is determined by the formula of [3]
13 to 10	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
9 to 0	BRP[9:0]	R/W	000h*	X	baud rate prescaler; the baud rate prescaler derives the CAN clock t_{scl} from the system clock $f_{clk(sys)}$; the CAN controller clock period is calculated by the formula of [4]

[1] $t_{seg2} = t_{scl} \times (TSEG2 + 1)$

[2] $t_{seg1} = t_{scl} \times (TSEG1 + 1)$

[3] $t_{SJW} = t_{scl} \times (SJW + 1)$

[4] $t_{scl} = \frac{BRP + 1}{f_{clk(sys)}}$

8.5.1.10 CAN controller error warning limit register (CCEWL)

The CAN controller error warning limit register sets the limit on the transmit or receive errors at which an interrupt can occur. This register is only writable in soft reset mode.

Table 171 shows the bit assignment of the CCEWL register.

Table 171: CCEWL register bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 8	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
7 to 0	EWL[7:0]	R/W	60h*	X	error warning limit; during CAN operation, this value is compared to both the transmit and receive error counters; if either of these counters matches this value, the error status bit is set

8.5.1.11 CAN controller status register (CCSTAT)

The CAN controller status register reflects the transmit status of all three transmit buffers including the global status of the CAN controller.

The CCSTAT register is read only. Table 172 shows the bit assignment of the CCSTAT register.

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Table 172: CCSTAT register bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 24	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
23	BS	R		0	bus status
			1		the CAN controller is currently prohibited from bus activity because the transmit error counter reached its limiting value of FFh
			0*		
22	ES	R		0	error status
			1		one or both of the transmit and receive error counters has reached the limit set in the error warning limit register
			0*		
21	TS3	R		1	transmit status 3
			1*		the CAN controller is transmitting a message from transmit buffer 3
			0		
20	RS	R		1	receive status
			1*		the CAN controller is receiving a message
			0		
19	TCS3 [1]	R		X	transmission complete status 3
			1*		the last requested message transmissions from transmit buffer 3 has been successfully completed
			0		the previously requested transmission is not yet completed
18	TBS3 [2]	R		1	transmit buffer status 3
			1*		transmit buffer 3 is available for the CPU
			0		transmit buffer 3 contains a previously queued message that has not yet been sent
17	DOS	R		0	data overrun status
			1		a message was lost because the preceding message to this CAN controller was not read and released quickly enough
			0*		no data overrun has occurred

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Table 172: CCSTAT register bit description *…continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
16	RBS	R		0	receive buffer status
			1		at least one complete message is available in the double receive buffer; this bit is cleared by the release receive buffer command in the CAN controller command register if no subsequent received message is available
			0*		no message is available in the double receive buffer
15	BS	R		0	bus status
			1		the CAN controller is currently prohibited from bus activity because the transmit error counter reached its limiting value of FFh
			0*		
14	ES	R		0	error status
			1		one or both of the transmit and receive error counters has reached the limit set in the error warning limit register
			0*		
13	TS2	R		1	transmit status 2
			1*		the CAN controller is transmitting a message from transmit buffer 2
			0		
12	RS	R		1	receive status
			1*		the CAN controller is receiving a message
			0		
11	TCS2 [1]	R		X	transmission complete status 2
			1*		the requested message transmission from transmit buffer 2 has been successfully completed
			0		the previously requested transmission from transmit buffer 2 is not yet completed
10	TBS2 [2]	R		1	transmit buffer status 2
			1*		transmit buffer 2 is available for the CPU
			0		transmit buffer 2 contains a previously queued message that has not yet been sent

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Table 172: CCSTAT register bit description *…continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
9	DOS	R		0	data overrun status; when logic 1, a message was lost because the preceding message to this CAN controller was not read and released quickly enough; when logic 0, no data overrun has occurred
			1		a message was lost because the preceding message to this CAN controller was not read and released quickly enough
			0*		no data overrun has occurred
8	RBS	R		0	receive buffer status
			1		at least one complete message is available in the double receive buffer; this bit is cleared by the release receive buffer command in the CAN controller command register if no subsequent received message is available
			0*		no message is available in the double receive buffer
7	BS	R		0	bus status
			1		the CAN controller is currently prohibited from bus activity because the transmit error counter reached its limiting value of FFh
			0*		
6	ES	R		0	error status
			1		one or both of the transmit and receive error counters has reached the limit set in the error warning limit register
			0*		
5	TS1	R		1	transmit status 1
			1*		the CAN controller is transmitting a message from transmit buffer 1
			0		
4	RS	R		1	receive status
			1*		the CAN controller is receiving a message
			0		
3	TCS1 [1]	R		X	transmission complete status 1
			1*		the requested message transmission from transmit buffer 1 has been successfully completed
			0		the previously requested transmission from transmit buffer 1 is not yet completed

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Table 172: CCSTAT register bit description *...continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
2	TBS1 [2]	R		1	transmit buffer status
			1*		transmit buffer 1 is available for the CPU
			0		transmit buffer 1 contains a previously queued message that has not yet been sent
1	DOS	R		0	data overrun status
			1		a message was lost because the preceding message to this CAN controller was not read and released quickly enough
			0*		no data overrun has occurred
0	RBS	R		0	receive buffer status
			1		at least one complete message is available in the double receive buffer; this bit is cleared by the release receive buffer command in the CAN controller command register if no subsequent received message is available
			0*		no message is available in the double receive buffer

[1] The transmission complete status bit is set 0 (incomplete) whenever the transmission request bit or the self reception request bit is set 1 for this TX buffer. The transmission complete status bit will remain 0 until a message is transmitted successfully.

[2] If the CPU tries to write to this transmit buffer when the transmit buffer status bit is 0 (locked), the written byte will not be accepted and will be lost without this being signalled.

8.5.1.12 CAN controller receive buffer message info register (CCRXBMI)

The CAN controller receive buffer message info register reflects the characteristics of the received message. This register is read only.

Table 173 shows the bit assignment of the CCRXBMI register.

Table 173: CCRXBMI register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31	FF	R		X	frame format
			1		an extended frame format message has been received
			0*		a standard frame format message has been received
30	RTR	R		X	remote frame request
			1		a remote frame has been received
			0*		a data frame has been received
29 to 20	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0

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Table 173: CCRXBMI register bit description *...continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
19 to 16	DLC[3:0]	R	0h*	X	data length code; this register contains the number of data bytes received in case bit RTR is logic 0 or the requested number of data bytes in case bit RTR is logic 1; values larger than eight are handled as eight data bytes
15 to 11	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
10	BP	R		X	bypass mode
			1		the message was received in the acceptance filter bypass mode which makes the identifier index field meaningless
			0*		
9 to 0	IDI[9:0]	R	000h*	X	identifier index; in case bit BP is not set, this register contains the zero-based number of the look-up table entry at which the acceptance filter matched the received identifier; disabled entries in the standard tables are included in this numbering, but will not be considered for filtering

8.5.1.13 CAN controller receive buffer identifier register (CCRXBID)

The CAN controller receive buffer identifier register contains the identifier field of the received message. This register is read only.

Table 174 shows the bit assignment of the CCRXBID register.

Table 174: CCRXBID register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 29	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
28 to 0	ID[28:0]	R	0000 0000h*	X	identifier; this register contains the identifier of received CAN message; in case a standard frame format has been received, the least significant 11 bits represent the 11-bit identifier

8.5.1.14 CAN controller receive buffer data A register (CCRXBDA)

The CAN controller receive buffer data A register contains the first four data bytes of the received message. This register is read only.

Table 175 shows the bit assignment of the CCRXBDA register.

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Table 175: CCRXBDA register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 24	DB4[7:0]	R	00h*	X	data byte 4; if the data length code value is four or more, this register contains the fourth data byte of the received message
23 to 16	DB3[7:0]	R	00h*	X	data byte 3; if the data length code value is three or more, this register contains the third data byte of the received message
15 to 8	DB2[7:0]	R	00h*	X	data byte 2; if the data length code value is two or more, this register contains the second data byte of the received message
7 to 0	DB1[7:0]	R	00h*	X	data byte 1; if the data length code value is one or more, this register contains the first data byte of the received message

8.5.1.15 CAN controller receive buffer data B register (CCRXBDB)

The CAN controller receive buffer data B register contains the second four data bytes of the received message. This register is read only.

Table 176 shows the bit assignment of the CCRXBDB register.

Table 176: CCRXBDB register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 24	DB8[7:0]	R	00h*	X	data byte 8; if the data length code value is eight or more, this register contains the eighth data byte of the received message
23 to 16	DB7[7:0]	R	00h*	X	data byte 7; if the data length code value is seven or more, this register contains the seventh data byte of the received message
15 to 8	DB6[7:0]	R	00h*	X	data byte 6; if the data length code value is six or more, this register contains the sixth data byte of the received message
7 to 0	DB5[7:0]	R	00h*	X	data byte 5; if the data length code value is five or more, this register contains the fifth data byte of the received message

8.5.1.16 CAN controller transmit buffer message info register (CCTXB1MI, CCTXB2MI and CCTXB3MI)

The CAN controller transmit buffer message info register reflects the characteristics of the transmit message. This register is only writable when the transmit buffer is released (corresponding transmit buffer status bit is logic 1).

Table 177 shows the bit assignment of the CCTXB1MI, CCTXB2MI and CCTXB3MI registers.

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Table 177: CCTXB1MI, CCTXB2MI and CCTXB3MI register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31	FF	R/W		X	frame format
			1		an extended frame format message is transmitted
			0*		a standard frame format message is transmitted
30	RTR	R/W		X	remote frame request
			1		a remote frame format message is transmitted
			0*		a data frame format message is transmitted
29 to 20	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
19 to 16	DLC[3:0]	R/W	0h*	X	data length code; this register contains the number of data bytes to be transmitted in case bit RTR is logic 0 or the requested number of data bytes in case bit RTR is logic 1; values larger than eight are handled as eight data bytes
15 to 8	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
7 to 0	TXPRIO[7:0]	R/W	00h*	X	transmit priority; if the transmit priority mode bit in the CAN controller mode register is set, the transmit buffer with the lowest transmit priority value wins the prioritization and is sent first; in cases where the same transmit priority or the same ID is chosen for more than one transmit buffer, then the transmit buffer with the lowest buffer number is send first

8.5.1.17 CAN controller transmit buffer identifier register (CCTXB1ID, CCTXB2ID and CCTXB3ID)

The CAN controller transmit buffer identifier register contains the identifier field of the transmit message. This register is only writable when the transmit buffer is released (corresponding transmit buffer status bit is logic 1).

Table 178 shows the bit assignment of the CCTXB1ID, CCTXB2ID and CCTXB3ID registers.

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Table 178: CCTXB1ID, CCTXB2ID and CCTXB3ID register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 29	reserved	-	-	-	reserved; do not modify, read as logic 0, write as logic 0
28 to 0	ID[28:0]	R/W	0000 0000h*	X	identifier; this register contains the identifier of transmit CAN message; in case a standard frame format is transmitted, the least significant 11 bits must represent the 11-bit identifier

8.5.1.18 CAN controller transmit buffer data A register (CCTXB1DA, CCTXB2DA and CCTXB3DA)

The CAN controller transmit buffer data A register contains the first four data bytes of the transmit message. This register is only writable when the transmit buffer is released (corresponding transmit buffer status bit is logic 1).

Table 179 shows the bit assignment of the CCTXB1DA, CCTXB2DA and CCTXB3DA registers.

Table 179: CCTXB1DA, CCTXB2DA and CCTXB3DA register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 24	DB4[7:0]	R/W	00h*	X	data byte 4; if the data length code value is four or more, this register contains the fourth data byte of the received message
23 to 16	DB3[7:0]	R/W	00h*	X	data byte 3; if the data length code value is three or more, this register contains the third data byte of the received message
15 to 8	DB2[7:0]	R/W	00h*	X	data byte 2; if the data length code value is two or more, this register contains the second data byte of the received message
7 to 0	DB1[7:0]	R/W	00h*	X	data byte 1; if the data length code value is one or more, this register contains the first data byte of the received message

8.5.1.19 CAN controller transmit buffer data B register (CCTXB1DB, CCTXB2DB and CCTXB3DB)

The CAN controller transmit buffer data B register contains the second four data bytes of the transmit message. This register is only writable when the transmit buffer is released (corresponding transmit buffer status bit is logic 1).

Table 180 shows the bit assignment of the CCTXB1DB, CCTXB2DB and CCTXB3DB registers.

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Table 180: CCTXB1DB, CCTXB2DB and CCTXB3DB register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Soft reset mode value	Description
31 to 24	DB8[7:0]	R/W	00h*	X	data byte 8; if the data length code value is eight or more, this register contains the eighth data byte of the received message
23 to 16	DB7[7:0]	R/W	00h*	X	data byte 7; if the data length code value is seven or more, this register contains the seventh data byte of the received message
15 to 8	DB6[7:0]	R/W	00h*	X	data byte 6; if the data length code value is six or more, this register contains the sixth data byte of the received message
7 to 0	DB5[7:0]	R/W	00h*	X	data byte 5; if the data length code value is five or more, this register contains the fifth data byte of the received message

8.5.1.20 Global acceptance filter

The Global acceptance filter provides look-up for received identifiers, called acceptance filtering in CAN terminology, for all the CAN controllers. It includes a CAN ID look-up table memory, in which software maintains one to five sections of identifiers. The CAN ID look-up table memory is 2 kB large (512 words each 32 bits). It can contain up to 1024 standard frame identifiers (SFF) or 512 extended frame identifiers (EFF) or a mixture of both types.

Note that the whole CAN ID look-up table memory is only word accessible.

The CAN ID look-up table memory is structured into up to five sections. In each section the identifiers of a certain CAN message type are listed, see Table 181.

Table 181. Overview of sections in CAN ID look-up table memory

Name of section	Reception method	CAN message frame format	Explicit IDs or Group of IDs
Standard Frame Format FullCAN identifier section	stored directly in memory	Standard Frame Format (SFF)	explicit
Standard Frame Format explicit identifier section	buffered	Standard Frame Format (SFF)	explicit
Standard Frame Format group identifier section	buffered	Standard Frame Format (SFF)	group
Extended Frame Format explicit identifier section	buffered	Extended Frame Format (EFF)	explicit
Extended frame format group identifier section	buffered	Extended Frame Format (EFF)	group

To indicate the boundaries of the different sections within the ID look-up table memory, five start address registers exist. In those start address registers the offset regarding the base address CANAFM (see Table 7) is stored. The Standard Frame Format FullCAN identifier section always starts at the offset 00h, the following sections start as defined in the start address registers. The look-up table ends with the FullCAN message object section, starting at the offset CAEOTA. A non-existing section is indicated by equal values in consecutive start-address registers.

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See Figure 10 for the structure of the CAN ID look-up table memory.

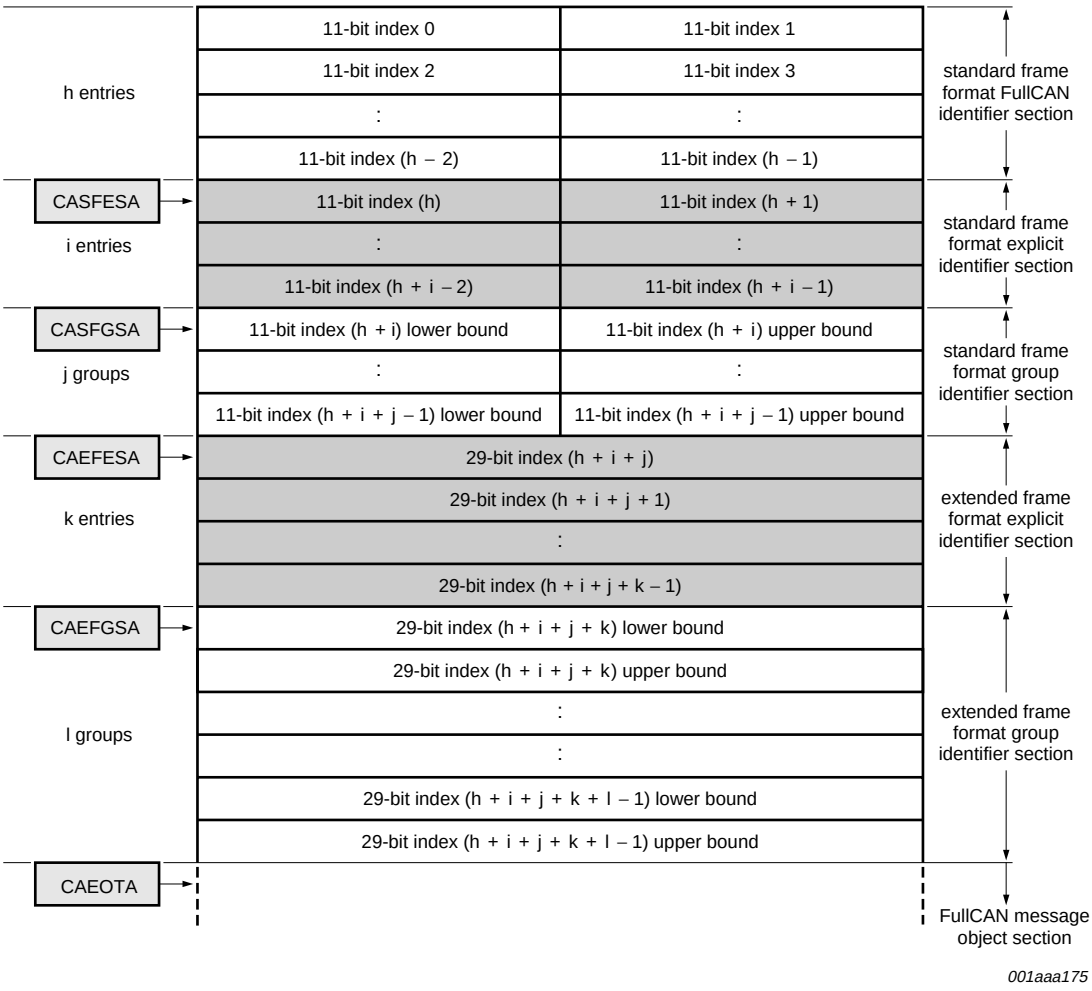

Fig 10. ID look-up table memory

8.5.1.21 Standard frame format FullCAN identifier section

If the CAN acceptance filter is set into FullCAN mode (EFCAN = 1) the FullCAN identifier section in the look-up table is enabled. Otherwise the acceptance filter ignores this section. The entries of the FullCAN identifier section must be arranged in ascending numerical order, one per half word, two per word (see Figure 10).

Since each CAN controller has its own address map, each table entry also contains the number of the CAN controller to which it applies. This section starts at the offset 00h and contains identifiers index 0 to (h - 1). The bit allocation is given in Table 182.

Table 182. SFF FullCAN identifier section bit description

Bit	Symbol	Description
31 to 29	SCC	even index: CAN controller number
28	MDB	even index: message disable bit; logic 0 is message enabled and logic 1 is message disabled
27	-	not used

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Table 182. SFF FullCAN identifier section bit description *...continued*

Bit	Symbol	Description
26 to 16	ID[28:18]	even index: 11-bit CAN 2.0 B identifier
15 to 13	SCC	odd index: CAN controller number
12	MDB	odd index: message disable bit; logic 0 is message enabled and logic 1 is message disabled
11	-	not used
10 to 0	ID[28:18]	odd index: 11-bit CAN 2.0 B identifier

If an incoming message is detected, the acceptance filter tries to find the ID in the FullCAN section first and continues searching in the following sections. In case of an identifier match during the acceptance filter process, the received FullCAN message object data is moved from the receive buffer of the appropriate CAN controller into the FullCAN message object section.

Table 183 shows the detailed layout structure of one FullCAN message stored in the FullCAN message object section of the look-up table.

The base address of a specific message object data can be calculated by the contents of the CAEOTA and the index i of the ID in the section (see Figure 10). Message object data address = CAEOTA + (12 × i).

Table 183. FullCAN message object layout

Bit	Symbol	Description
Msg_ObjAddr + 0		
31	FF	CAN frame format
30	RTR	remote frame request
29 to 26	-	not used
25 to 24	SEM[1:0]	semaphore bits
23 to 23	-	not used
22 to 16	RXDLC[6:0]	data length code
15 to 11	-	not used
10 to 0	ID[28:18]	identifier bits 28 to 18
Msg_ObjAddr + 4		
31 to 24	RXDATA4[7:0]	receive data 4
23 to 16	RXDATA3[7:0]	receive data 3
15 to 8	RXDATA2[7:0]	receive data 2
7 to 0	RXDATA1[7:0]	receive data 1
Msg_ObjAddr + 8		
31 to 24	RXDATA8[7:0]	receive data 8
23 to 16	RXDATA7[7:0]	receive data 7
15 to 8	RXDATA6[7:0]	receive data 6
7 to 0	RXDATA5[7:0]	receive data 5

Since the FullCAN message object section of the look-up table RAM can be accessed both by the acceptance filter internal state machine and the CPU, there is a method for insuring that no CPU reads from a FullCAN message object occurs while the internal state machine is writing to that object.

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For this purpose the acceptance filter uses a 3-state semaphore, encoded with the two semaphore bits SEM[1:0] for each message object. This mechanism provides the CPU with information about the current state of the acceptance filter internal state machine activity in the FullCAN message object section.

The semaphore operates in the following manner:

- SEM[1:0] = 01: Acceptance filter is in the process of updating the buffer
- SEM[1:0] = 11: Acceptance filter has finished updating the buffer
- SEM[1:0] = 00: CPU is in the process of reading from the buffer / no update since last reading from the buffer

Before writing the first data byte into a message object SEM[1:0] is set to 01. After having written the last data byte into the message object, the acceptance filter internal state will update the semaphore bits by setting SEM[1:0] = 11.

Before reading from a message object, the CPU should read SEM[1:0] to determine the current state of the message object. If SEM[1:0] = 01, the internal state machine is currently active in this message object. If SEM[1:0] = 11, the message object is available to be read.

Before the CPU begins reading from the message object, it should clear SEM[1:0] = 00. When the CPU has finished reading, it should check SEM[1:0] again. In case of SEM[1:0] unequal to 00, the message object has been changed during reading. Therefore the contents of the message object should be read out once again. If, on the other hand, SEM[1:0] = 00 as expected, the valid data has been successfully read by the CPU.

Conditions to activate the FullCAN mode:

- The EFCAN bit in the CAMODE register has to be set
- The start address offset of the Standard Frame Format explicit identifier section CASFESA has to be larger than logic 0
- The available space for the FullCAN message object section must be large enough to store one FullCAN object for any FullCAN identifier

8.5.1.22 Standard frame format explicit identifier section

The entries of the SFF explicit identifier section must be arranged in ascending numerical order, one per half word, two per word (see Figure 10). Since each CAN controller has its own address map, each entry also contains the number of the CAN controller to which it applies.

This section starts with the CASFESA start address register and contains the identifiers index h to index (h + i – 1). The bit allocation of the first word is given in Table 184.

Table 184. SFF explicit identifier section bit description

Bit	Symbol	Description
31 to 29	SCC	even index: CAN controller number
28	MDB	even index: message disable bit; logic 0 is message enabled and logic 1 is message disabled
27	-	not used
26 to 16	ID[28:18]	even index: 11-bit CAN 2.0 B identifier

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Table 184. SFF explicit identifier section bit description *...continued*

Bit	Symbol	Description
15 to 13	SCC	odd index: CAN controller number
12	MDB	odd index: message disable bit; logic 0 is message enabled and logic 1 is message disabled
11	-	not used
10 to 0	ID[28:18]	odd index: 11-bit CAN 2.0 B identifier

By means of the message disable bits particular CAN identifiers can be turned on and off dynamically from acceptance filtering. When the acceptance filter function is enabled, only the message disable bits in the acceptance filter look-up table memory can be changed by software. Disabled entries must maintain the ascending sequence of identifiers.

8.5.1.23 Standard frame format group identifier section

The table of SFF group identifier section contains paired upper and lower bounds, one pair per word. These pairs must be arranged in ascending numerical order (see Figure 10).

This section starts with the CASFGSA start address register and contains the identifiers index (h + i) lower bound to index (h + i + j – 1) upper bound. The bit allocation of the first word is given in Table 185.

Table 185. SFF group identifier section bit description

Bit	Symbol	Description
31 to 29	SCC	lower bound: CAN controller number
28	MDB	lower bound: message disable bit; logic 0 is message enabled and logic 1 is message disabled
27	-	not used
26 to 16	ID[28:18]	lower bound: 11-bit CAN 2.0 B identifier
15 to 13	SCC	upper bound: CAN controller number
12	MDB	upper bound: message disable bit; logic 0 is message enabled and logic 1 is message disabled
11	-	not used
10 to 0	ID[28:18]	upper bound: 11-bit CAN 2.0 B identifier

By means of the message disable bits particular CAN identifier groups can be turned on and off dynamically from acceptance filtering. When the acceptance filter function is enabled, only the message disable bits in the acceptance filter look-up table memory can be changed by software. Note that in this section the lower bound and upper bound message disable bit must always have the same value. Disabled entries must maintain the ascending sequence of identifiers.

8.5.1.24 Extended frame format explicit identifier section

If extended identifiers (29-bit) are used in the application, at least one of the other two tables in acceptance filter look-up table must not be empty, one for explicit extended identifiers and one for ranges of extended identifiers. The table of explicit extended identifiers must be arranged in ascending numerical order (see Figure 10).

This section with start address EFF contains the identifiers ID (i + j + 1) to ID (i + j + k). The bit allocation of the first word is given in Table 186.

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Table 186. EFF explicit identifier section bit description

Bit	Symbol	Description
31 to 29	SCC	CAN controller number
28 to 0	ID[28:0]	29-bit CAN 2.0 B identifier

8.5.1.25 Extended frame format group identifier section

The Extended Frame Format (EFF) group identifier section must contain an even number of entries, of the same form as in the EFF explicit identifier section (see Figure 10). Like the EFF explicit identifier section, the EFF group identifier section must be arranged in ascending numerical order. The upper and lower bounds in the section are implicitly paired as an inclusive group of extended addresses, such that any received address that falls in the inclusive group is accepted and received. Software must maintain the section to consist of such word pairs.

This section starts with CAEFGSA start address register and contains the identifiers index (h + i + j + k) lower bound to index (h + i + j + k + l – 1) upper bound. The bit allocation is given in Table 187.

Table 187. EFF group identifier section bit description

Bit	Symbol	Description
CAEFGSA start address		
31 to 29	SCC	lower bound: CAN controller number
28 to 0	ID[28:0]	lower bound: 29-bit CAN 2.0 B identifier
CAEFGSA start address + 4		
31 to 29	SCC	upper bound: CAN controller number
28 to 0	ID[28:0]	upper bound: 29-bit CAN 2.0 B identifier

8.5.1.26 CAN acceptance filter mode register (CAMODE)

The CAN acceptance filter mode register is used to change the behavior of the acceptance filter.

Table 188 shows the bit assignment of the CAMODE register.

Table 188. CAMODE register bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 3	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
2	EFCAN	R/W		FullCAN extension mode
			1	the FullCAN functionality is enabled
			0*	the FullCAN functionality is disabled

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Table 188. CAMODE register bit description *…continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
1	ACCBP	R/W		acceptance filter bypass
			1	all Rx messages are accepted on enabled CAN controllers; software must set this bit before modifying the contents of any of the acceptance filter registers, and before modifying the contents of look-up table RAM in any way other than setting or clearing disable bits in standard identifier entries
			0*	when both this bit and bit ACCOFF are logic 0, the acceptance filter operates to screen received CAN identifiers
0	ACCOFF	R/W		acceptance filter off
			1*	if bit ACCBP = 0, the acceptance filter is not operational; all received CAN messages are ignored
			0	the acceptance filter is operational

8.5.1.27 CAN acceptance filter standard frame explicit start address register (CASFESA)

The CAN acceptance filter standard frame explicit start address register.

Table 189 shows the bit assignment of the CASFESA register.

Table 189. CASFESA register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 12	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
11 to 2	SFESA[9:0]	R/W	00h*	standard frame explicit start address; this register defines the start address of the section of explicit standard identifiers in acceptance filter look-up table; if the section is empty, write the same value in this register and the SFGSA register; if bit EFCAN = 1, this value also indicates the size of the section of standard identifiers which the acceptance filter will search and (if found) automatically store received messages in acceptance filter section; write access is only possible during the acceptance filter bypass or acceptance filter off mode; read access is possible in acceptance filter on and off mode; the standard frame explicit start address is aligned on word boundaries and therefore the lowest 2 bits must be always logic 0
1 to 0	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

8.5.1.28 CAN acceptance filter standard frame group start address register (CASFGSA)

The CAN acceptance filter standard frame group start address register.

Table 190 shows the bit assignment of the CASFGSA register.

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Table 190. CASFGSA register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 12	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
11 to 2	SFGSA[9:0]	R/W	00h*	standard frame group start address; this register defines the start address of the section of grouped standard identifiers in acceptance filter look-up table; if the section is empty, write the same value in this register and the EFESA register; the largest value that should be written to this register is 7FCh, when only the standard explicit section is used, and the last word (address 7F8h) in acceptance filter look-up table is used; write access is only possible during the acceptance filter bypass or acceptance filter off mode; read access is possible in acceptance filter on and off mode; the standard frame group start address is aligned on word boundaries and therefore the lowest 2 bits must be always logic 0
1 to 0	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

8.5.1.29 CAN acceptance filter extended frame explicit start address register (CAEFESA)

The CAN acceptance filter extended frame explicit start address register.

Table 191 shows the bit assignment of the CAEFESA register.

Table 191. CAEFESA register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 12	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
11 to 2	EFESA[9:0]	R/W	00h*	extended frame explicit start address; this register defines the start address of the section of explicit extended identifiers in acceptance filter look-up table; if the section is empty, write the same value in this register and the EFGSA register; the largest value that should be written to this register is 7FCh, when both extended sections are empty and the last word (address 7F8h) in acceptance filter look-up table is used; write access is only possible during the acceptance filter bypass or acceptance filter off mode; read access is possible in acceptance filter on and off mode; the extended frame explicit start address is aligned on word boundaries and therefore the lowest 2 bits must be always logic 0
1 to 0	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

8.5.1.30 CAN acceptance filter extended frame group start address register (CAEFGSA)

The CAN acceptance filter extended frame group start address register.

Table 192 shows the bit assignment of the CAEFGSA register.

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Table 192. CAEFGSA register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 12	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
11 to 2	EFGSA[9:0]	R/W	00h*	extended frame group start address; this register defines the start address of the section of grouped extended identifiers in acceptance filter look-up table; if the section is empty, write the same value in this register and the EOTA register; the largest value that should be written to this register is 7FCh, when this section is empty and the last word (address 7F8h) in acceptance filter look-up table is used; write access is only possible during the acceptance filter bypass or acceptance filter off mode; read access is possible in acceptance filter on and off mode; the extended frame group start address is aligned on word boundaries and therefore the lowest 2 bits must be always logic 0
1 to 0	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

8.5.1.31 CAN acceptance filter end of look up table address register (CAEOTA)

The CAN acceptance filter end of look up table address register.

Table 193 shows the bit assignment of the CAEOTA register.

Table 193. CAEOTA register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 12	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
11 to 2	EOTA[9:0]	R/W	00h*	End of look-up table address. The largest value of the register CAEOTA should never exceed 7FC. If bit EFCAN = 0, the register should contain the next address above the last active acceptance filter identifier section. If bit EFCAN = 1, the register contains the start address of the FullCAN message object section. In case of an identifier match in the standard frame format FullCAN identifier section during the acceptance filter process, the received FullCAN message object data is moved from the receive buffer of the appropriate CAN controller into the FullCAN message object section. Each defined FullCAN message needs three address lines for the message data in the FullCAN message object data section. Write access is only possible during the acceptance filter bypass or acceptance filter off mode; read access is possible in acceptance filter on and off mode.
1 to 0	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

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8.5.1.32 CAN acceptance filter look-up table error address register (CALUTEA)

The CAN acceptance filter look-up table error address register represents the address in the look-up table at which a problem has been detected when the look-up table error bit is set.

The CALUTEA register is read only. Table 194 shows the bit assignment of the CALUTEA register.

Table 194. CALUTEA register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 11	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
10 to 2	LUTEA[8:0]	R	00h*	look-up table error address; this register contains the address in the look-up table at which the acceptance filter encountered an error in the content of the tables; this address is valid when the look-up table error bit is set; reading this register clears the LUTE look-up table error bit
1 to 0	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0

8.5.1.33 CAN acceptance filter look-up table error register (CALUTE)

The CAN acceptance filter look-up table error register provides the configuration status of the look-up table contents. In case of an error an interrupt is generated via the general CAN interrupt input source of the vectored interrupt controller.

The CALUTE register is read-only. Table 195 shows the bit assignment of the CALUTE register.

Table 195. CALUTE register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	LUTE	R		look-up table error
			1	the acceptance filter has encountered an error in the content of the look-up table; reading the LUTEA register clears this bit; this error condition is part of the general CAN interrupt input source
			0*	

8.5.1.34 CAN controllers central transmit status register (CCCTS)

The CAN controllers central transmit status register provides bundled access to transmission status of all the CAN controllers. The status flags are the same as present in the status register of the corresponding CAN controller.

The CCCTS register is read only. Table 196 shows the bit assignment of the CCCTS register.

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Table 196. CCCTS register bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 22	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
21	TCS5	R		CAN controller 5 transmission completed status
			1*	the transmission was completed successfully
			0	
20	TCS4	R		CAN controller 4 transmission completed status
			1*	the transmission was completed successfully
			0	
19	TCS3	R		CAN controller 3 transmission completed status
			1*	the transmission was completed successfully
			0	
18	TCS2	R		CAN controller 2 transmission completed status
			1*	the transmission was completed successfully
			0	
17	TCS1	R		CAN controller 1 transmission completed status
			1*	the transmission was completed successfully
			0	
16	TCS0	R		CAN controller 0 transmission completed status
			1*	the transmission was completed successfully
			0	
15 to 14	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
13	TBS5	R		CAN controller 5 transmit buffer status
			1*	the transmit buffers are empty
			0	
12	TBS4	R		CAN controller 4 transmit buffer status
			1*	the transmit buffers are empty
			0	
11	TBS3	R		CAN controller 3 transmit buffer status
			1*	the transmit buffers are empty
			0	
10	TBS2	R		CAN controller 2 transmit buffer status
			1*	the transmit buffers are empty
			0	
9	TBS1	R		CAN controller 1 transmit buffer status
			1*	the transmit buffers are empty
			0	
8	TBS0	R		CAN controller 0 transmit buffer status
			1*	the transmit buffers are empty
			0	

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Table 196. CCCTS register bit description *…continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 6	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
5	TS5	R		CAN controller 5 transmit status
			1*	a message is being transmitted
			0	
4	TS4	R		CAN controller 4 transmit status
			1*	a message is being transmitted
			0	
3	TS3	R		CAN controller 3 transmit status
			1*	a message is being transmitted
			0	
2	TS2	R		CAN controller 2 transmit status
			1*	a message is being transmitted
			0	
1	TS1	R		CAN controller 1 transmit status
			1*	a message is being transmitted
			0	
0	TS0	R		CAN controller 0 transmit status
			1*	a message is being transmitted
			0	

8.5.1.35 CAN controllers central receive status register (CCCRS)

The CAN controllers central receive status register provides bundled access to reception status of all the CAN controllers. The status flags are the same as present in the status register of the corresponding CAN controller.

The CCCRS register is read only. Table 197 shows the bit assignment of the CCCRS register.

Table 197. CCCRS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 22	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
21	DOS5 [1]	R		CAN controller 5 data overrun status
			1	the received message was lost due to not fast enough read out of preceding message
			0*	
20	DOS4 [1]	R		CAN controller 4 data overrun status
			1	the received message was lost due to not fast enough read out of preceding message
			0*	

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Table 197. CCCRS register bit description *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
19	DOS3 [1]	R		CAN controller 3 data overrun status
			1	the received message was lost due to not fast enough read out of preceding message
			0*	
18	DOS2 [1]	R		CAN controller 2 data overrun status
			1	the received message was lost due to not fast enough read out of preceding message
			0*	
17	DOS1 [1]	R		CAN controller 1 data overrun status
			1	the received message was lost due to not fast enough read out of preceding message
			0*	
16	DOS0 [1]	R		CAN controller 0 data overrun status
			1	the received message was lost due to not fast enough read out of preceding message
			0*	
15 to 14	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
13	RBS5 [1]	R		CAN controller 5 receive buffer status
			1	the receive buffers contains a received message
			0*	
12	RBS4 [1]	R		CAN controller 4 receive buffer status
			1	the receive buffers contains a received message
			0*	
11	RBS3 [1]	R		CAN controller 3 receive buffer status
			1	the receive buffers contains a received message
			0*	
10	RBS2 [1]	R		CAN controller 2 receive buffer status
			1	the receive buffers contains a received message
			0*	
9	RBS1 [1]	R		CAN controller 1 receive buffer status
			1	the receive buffers contains a received message
			0*	
8	RBS0 [1]	R		CAN controller 0 receive buffer status
			1	the receive buffers contains a received message
			0*	
7 to 6	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
5	RS5	R		CAN controller 5 receive status
			1*	a message is being received
			0	

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Table 197. CCCRS register bit description *...continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
4	RS4	R		CAN controller 4 receive status
			1*	a message is being received
			0	
3	RS3	R		CAN controller 3 receive status
			1*	a message is being received
			0	
2	RS2	R		CAN controller 2 receive status
			1*	a message is being received
			0	
1	RS1	R		CAN controller 1 receive status
			1*	a message is being received
			0	
0	RS0	R		CAN controller 0 receive status
			1*	a message is being received
			0	

[1] This bit is unchanged in case a FullCAN message is received.

8.5.1.36 CAN controllers central miscellaneous status register (CCCMS)

The CAN controllers central miscellaneous status register provides bundled access to the bus and error status of all the CAN controllers. The status flags are the same as present in the status register of the corresponding CAN controller.

The CCCMS register is read only. Table 198 shows the bit assignment of the CCCMS register.

Table 198. CCCMS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 14	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
13	BS5	R		CAN controller 5 bus status
			1	the CAN controller is currently prohibited from bus activity because the transmit error counter reached its limiting value of FFh
			0*	
12	BS4	R		CAN controller 4 bus status
			1	the CAN controller is currently prohibited from bus activity because the transmit error counter reached its limiting value of FFh
			0*	

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Table 198. CCCMS register bit description *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
11	BS3	R		CAN controller 3 bus status
			1	the CAN controller is currently prohibited from bus activity because the transmit error counter reached its limiting value of FFh
			0*	
10	BS2	R		CAN controller 2 bus status
			1	the CAN controller is currently prohibited from bus activity because the transmit error counter reached its limiting value of FFh
			0*	
9	BS1	R		CAN controller 1 bus status
			1	the CAN controller is currently prohibited from bus activity because the transmit error counter reached its limiting value of FFh
			0*	
8	BS0	R		CAN controller 0 bus status
			1	the CAN controller is currently prohibited from bus activity because the transmit error counter reached its limiting value of FFh
			0*	
7 to 6	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
5	ES5	R		CAN controller 5 error status
			1	error warning limit has been exceeded
			0*	
4	ES4	R		CAN controller 4 error status; when logic 1, error warning limit has been exceeded
			1	error warning limit has been exceeded
			0*	
3	ES3	R		CAN controller 3 error status
			1	error warning limit has been exceeded
			0*	
2	ES2	R		CAN controller 2 error status
			1	error warning limit has been exceeded
			0*	
1	ES1	R		CAN controller 1 error status
			1	error warning limit has been exceeded
			0*	
0	ES0	R		CAN controller 0 error status
			1	error warning limit has been exceeded
			0*	

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8.5.2 LIN

8.5.2.1 Overview

The SJA2020 contains four LIN master controllers which can be used as dedicated LIN master controller or as standard 450 UART with additional support for the sync break generation.

The key features are:

- Complete LIN message handling and transfer
- One interrupt per LIN message
- Slave response time out detection
- Programmable sync break length
- Automatic sync field generation
- Programmable inter byte space
- Hardware of software parity generation
- Automatic checksum generation
- Fault confinement
- Fractional baud rate generator
- Configurable as standard UART

8.5.2.2 LIN pin description

The four LIN controllers in the SJA2020 have the following pins. The LIN pins are combined with other functions on the port pins of the SJA2020, see Section 8.3.2. Table 199 shows the LIN pins, x runs from 0 to 3.

Table 199: LIN controller pins

Symbol	Direction	Description
LINx TXDL	OUT	LIN channel x transmit data output
LINx RXDL	IN	LIN channel x receive data input

8.5.2.3 Register mapping

The LIN master controller registers are shown in Table 200.

The LIN master controller registers have an offset to the base address LIN RegBase which can be found in the memory map (see Table 7). The function of a register is dependent on the LIN master controller mode (bit LM).

Table 200. LIN register summary

Address	Type	Reset value	Name	Description	Reference
LIN master controller common registers					
00h	R/W	01h	LMODE	LIN master controller mode register	see Table 201
04h	R/W	00h	LCFG	LIN master controller configuration register	see Table 202
08h	R/W	00h	LCMD	LIN master controller command register	see Table 205

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Table 200. LIN register summary …continued

Address	Type	Reset value	Name	Description	Reference
0Ch	R/W	0 0001h	LFBRG	LIN master controller fractional baud rate generator register	see Table 206
LIN master controller registers (bit LM = 0)					
10h	R	342h	LSTAT	LIN master controller status register	see Table 207
14h	R	000h	LIC	LIN master controller interrupt and capture register	see Table 208
18h	R/W	10h	LIE	LIN master controller interrupt enable register	see Table 210
1Ch	-	-	reserved	reserved for future expansion	
20h	R/W	00h	LCS	LIN master controller check sum register	see Table 211
24h	R/W	00h	LTO	LIN master controller time-out register	see Table 212
28h	R/W	000 0000h	LID	LIN master controller message buffer identifier register	see Table 213
2Ch	R/W	0000 0000h	LDATA	LIN master controller message buffer data A register	see Table 214
30h	R/W	0000 0000h	LDATB	LIN master controller message buffer data B register	see Table 215
34h	R/W	0000 0000h	LDATC	LIN master controller message buffer data C register	see Table 216
38h	R/W	0000 0000h	LDATD	LIN master controller message buffer data D register	see Table 217
LIN UART registers (bit LM = 1)					
10h	R	-	RBR	receiver buffer register	see Table 218
	W	-	THR	transmit holding register	see Table 219
14h	R/W	0h	IER	interrupt enable register	see Table 220
18h	R	1h	IIR	interrupt ID register	see Table 221
1Ch	R/W	00h	LCR	line control register	see Table 223
20h	-	-	reserved	reserved for future expansion	
24h	R	60h	LSR	line status register	see Table 226
28h	-	-	reserved	reserved for future expansion	
2Ch	R/W	00h	SCR	scratch register	see Table 227

8.5.2.4 LIN master controller mode register (LMODE)

The LIN master controller mode register provides the selection between the LIN master controller and UART configuration.

Table 201 shows the bit assignment of the LMODE register.

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Table 201. LMODE register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
7	LM	R/W		LIN master controller mode. Changing from LIN master controller mode to UART mode is only possible if the LIN reset mode was set before and should be done with bit LM = 1 and bit LRM = 1; changing from UART mode to LIN master controller mode should be done with bit LM = 0 and bit LRM = 1
			1	the LIN master controller operates in UART mode
			0*	the LIN master controller operates as LIN master controller
6 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	LRM	R/W		LIN reset mode; only writable in LIN master controller mode
			1*	the LIN master controller is in reset mode and the current message transmission or reception is aborted; the registers LCMD, LSTAT, LIC, LCS, LID, LDATA, LDATB, LDATC and LDATD get their reset value
			0	the LIN master controller is in normal operation mode

8.5.2.5 LIN master controller configuration register (LCFG)

The LIN master controller configuration register is used to change the length for the sync break field, the inter byte space and contains software enable bits for the identifier parity and checksum calculation. In LIN master controller mode, the register is only writable if the LIN master controller is in reset mode.

Table 202 shows the bit assignment of the LCFG register.

Table 202. LCFG register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
7	SWPA	R/W		software ID parity
			1	the software generated ID parity from the message buffer is used to send onto the LIN bus
			0*	only the hardware generated parity is used to send onto the LIN bus
6	SWCS	R/W		software checksum
			1	the checksum is generated by software
			0*	the checksum is generated by hardware
5	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
4 to 3	IBS[1:0]	R/W	0h*	inter byte space length; the inter byte space length is inserted during transmission; see Table 203
2 to 0	SBL[2:0]	R/W	0h*	sync break logic 0 length; writing a value of 7h will always read as 6h; see Table 204

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Table 203: Inter byte space length configuration bits

IBS[1:0]	Function
00	0 bits inter byte space length
01	1 bits inter byte space length
10	2 bits inter byte space length
11	3 bits inter byte space length

Table 204: Sync break length configuration bits

SBL[2:0]	Function
000	10 bits sync break length
001	11 bits sync break length
010	12 bits sync break length
011	13 bits sync break length
100	14 bits sync break length
101	15 bits sync break length
110	16 bits sync break length
111	16 bits sync break length

8.5.2.6 LIN master controller command register (LCMD)

The LIN master controller command register is used to initiate a LIN message transmission. In LIN master controller mode, the register is only writable if the LIN master controller is in reset mode.

A dedicated sync break generator is added to the standard UART functionality to ease the sync break generation for LIN messages with a standard UART. A break interrupt is generated after the sync break delimiter has been transmitted if enabled.

Table 205 shows the bit assignment of the LCMD register.

Table 205: LCMD register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
7	SSB	R/W		send sync break; only writable in LIN UART mode
			1	a sync break is send onto the LIN bus; this bit is automatically cleared
			0*	
6 to 1	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
0	TR	R/W		transmit request; only writable in LIN master controller mode
			1	a transmission of a complete LIN message will be initiated; this bit is automatically cleared
			0*	

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8.5.2.7 LIN master controller fractional baud rate generator register (LFBRG)

The LIN master controller fractional baud rate generator register stores the divisor in 16-bit binary format and the fraction in 4-bit binary format for the programmable baud generator. The output frequency of the baud generator is 16 times the baud rate. The input frequency of the baud generator is the system clock frequency $f_{clk(sys)}$ divided by the divisor plus fraction value. In LIN master controller mode this register is only writeable in reset mode.

The baud rate can be calculated from the following formula:

$$baudrate = \frac{f_{clk(sys)}}{16 \times INT + FRAC}$$

Table 206 shows the bit assignment of the LFBRG register.

Table 206. LFBRG register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 20	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
19 to 16	FRAC	R/W	0h*	fractional value; in LIN UART mode only writable if in reset mode; contains the 4-bit fraction of the baud division
15 to 0	INT	R/W	0001h*	integer value; in LIN UART mode only writable if in reset mode; contains the 16-bit baud rate divisor

8.5.2.8 LIN master controller status register (LSTAT)

The LIN master controller status register reflects the status of the LIN master controller.

Figure 11 shows the status flag handling in terms of transmitting and receiving header and response fields.

The LSTAT register is read only. Table 207 shows the bit assignment of the LSTAT register.

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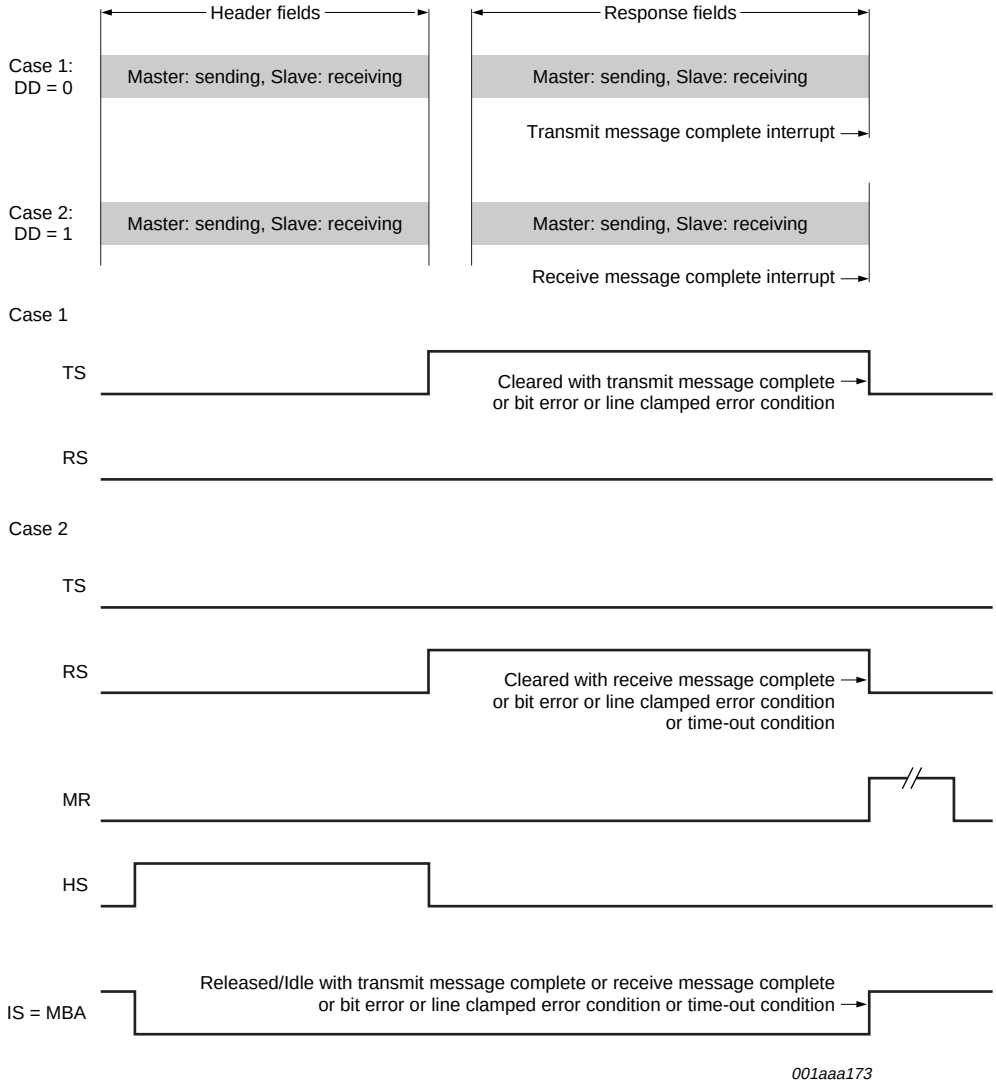

Fig 11. LIN master controller status flag handling

Table 207. LSTAT register bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 10	reserved	-	-	reserved; read as logic 0
9	TTL	R		TXD line level
			1*	the current TXD line level is dominant
			0	the current TXD line level is recessive
8	RLL	R		RXD line level
			1*	the current RXD line level is dominant
			0	the current RXD line level is recessive
7	reserved	-	-	reserved; read as logic 0

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Table 207. LSTAT register bit description *...continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
6	IS	R		idle status
			1*	the LIN bus is idle
			0	the LIN bus is active
5	ES	R		error status
			1	a bit-error of line clamped error condition was detected
			0*	no errors have been detected; the error status is cleared automatically when a new transmission is initiated
4	TS	R		transmit status
			1	the LIN master controller is transmitting LIN response fields
			0*	
3	RS	R		receive status
			1	the LIN master controller is receiving LIN response fields
			0*	
2	HS	R		header status
			1	the LIN master controller is transmitting the LIN header fields
			0*	
1	MBA	R		message buffer access
			1*	the message buffer is released and available for CPU access
			0	the message buffer is locked and the CPU cannot access the message buffer; a message is either waiting for transmission or is in transmitting process or receiving a message
0	MR	R		message received
			1	the message buffer contains a valid received message
			0*	the message buffer does not contain a valid message; the message received status is cleared automatically with a write access to the message buffer or by a new transmission request

8.5.2.9 LIN master controller interrupt and capture register (LIC)

The LIN master controller interrupt and capture register determines when the LIN master controller gives an interrupt request if the corresponding interrupt enable has been set. Reading the interrupt register clears the interrupt source. A detailed bus error capture is reported.

The LIC register is read only. Table 208 shows the bit assignment of the LIC register.

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Table 208. LIC register bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 12	reserved	-	-	reserved; read as logic 0
11 to 8	EC[3:0]	R	0h*	error capture; see Table 209
7	reserved	-	-	reserved; read as logic 0
6	WPI	R		wake-up and LIN protocol error interrupt
			1	a dominant bus level has been detected when the LIN bus was idle; a dominant bus level on the LIN bus can be caused by a wake-up message of a slave node as well as by arbitrary created or faulty generated messages of LIN slaves or by a stuck dominant level
			0*	
5	RTLCEI	R		line clamped error interrupt
			1	no valid message can be generated on the LIN bus due to clamped dominant or recessive RXD or TXD line
			0*	
4	NRI	R		slave not responding error interrupt
			1	the slave response is not completed within a certain time out period; the time out period is configurable via the time out register
			0*	
3	CSI	R		checksum error interrupt
			1	the received checksum field does not match with the calculated checksum
			0*	
2	BEI	R	0*	bit error interrupt; the error capture bits represent the detailed status in case of (when this bit is logic 1):
				a difference between transmit and receive bit stream is detected
				the configured inter byte space length is violated
				a stop bit of fields from received slave responses was not recessive
1	TI	R		transmit message complete interrupt
			1	a complete LIN message frame was transmitted or in cases where data length code is set to logic 0 (no response fields can be expected)
			0*	
0	RI	R		receive message complete interrupt
			1	the last byte, the checksum field of the incoming bit stream is moved from receive shift register into the message buffer
			0*	

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Table 209: Bus error capture interpretation bits

EC[3:0]	Function
0000	bit error in sync break field
0001	bit error in sync field
0010	bit error in identifier field
0011	bit error in data field
0100	bit error in checksum field
0101	bit error in inter byte space
0110	bit error in stop bit of received slave responses
0111	reserved
1000	recessive line clamped error; RXD / TXD line stuck recessive
1001	dominant line clamped error; RXD / TXD line stuck dominant
1010	reserved
:	:
1111	reserved

8.5.2.10 LIN master controller interrupt enable register (LIE)

The LIN master controller interrupt enable register determines when the LIN master controller gives an interrupt request if the corresponding interrupt enable has been set.

Table 210 shows the bit assignment of the LIE register.

Table 210. LIE register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 7	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
6	WPIE	R/W		wake up and LIN protocol error interrupt enable
			1	detection of a dominant bus level when the LIN bus was idle results in the respective interrupt
			0*	
5	RTLCEIE	R/W		line clamped error interrupt enable; when logic 1, whenever no valid message can be generated on the LIN bus results in the respective interrupt
			1	whenever no valid message can be generated on the LIN bus results in the respective interrupt
			0*	
4	NRIE	R/W		slave not responding error interrupt enable
			1*	whenever the slave response is not completed within the configured time out period results in the respective interrupt
			0	
3	CSIE	R/W		checksum error interrupt enable
			1	whenever the received checksum field does not match with the calculated checksum results in the respective interrupt
			0*	

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Table 210. LIE register bit description *...continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
2	BEIE	R/W		bit error interrupt enable
			1	detection of a bit error results in the respective interrupt
			0*	
1	TIE	R/W		transmit message complete interrupt enable
			1	whenever a complete LIN message frame was transmitted or in cases where data length code is set to logic 0 (no response fields can be expected) results in the respective interrupt
			0*	
0	RIE	R/W		receive message complete interrupt enable
			1	whenever the last byte, the checksum field of the incoming bit stream is moved from receive shift register into the message buffer results in the respective interrupt
			0*	

8.5.2.11 LIN master controller checksum register (LCS)

The LIN master controller LIN master controller checksum register contains the checksum value. In cases when the LIN master controller is transmitting the response fields, the checksum register contains the checksum value to be transmitted onto the LIN bus. In cases when the LIN master controller is receiving the response fields, the checksum register contains the received checksum from the slave. If the software checksum bit in the configuration register is set to logic 0, the checksum register appears to the CPU as a read only memory. By setting the software checksum bit the checksum register appears to the CPU as a read/write memory. In this case and before a transmission is initiated, the software has to provide the checksum to the checksum register.

Table 211 shows the bit assignment of the LCS register.

Table 211. LCS register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
7 to 0	CS	R/W	00h*	LIN message checksum; when the LIN master controller is transmitting, the checksum register contains the hardware or software calculated checksum value depending on the software checksum bit; when the LIN master controller is receiving, the checksum register contains the received checksum value from the slave node

8.5.2.12 LIN master controller time-out register (LTO)

The LIN master controller time-out register is used to define the maximum number of bit times (t_{bit}) within a response from all LIN slaves connected to one node should be completed. The time-out starts as soon as the LIN header was transmitted (the value of the time-out register is decremented with every bit time) and a slave response is expected. When enabled, the Slave not responding error interrupt (NRI) gets asserted as soon as the time-out limit is exceeded.

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The time-out (t_{to}) time to be programmed can be calculated from the following formulas:

$$t_{to} = \frac{t_{resp(max)}}{t_{bit}} = 1.4 \times \frac{t_{resp(nom)}}{t_{bit}}$$

with

$$t_{resp(nom)} = 10 \times \frac{N_{data} + 1}{t_{bit}}$$

Note: t_{bit} is the nominal time required to transmit a bit, as defined in LIN physical layer; N_{data} is the number of data fields sent with the slave response.

Table 212 shows the bit assignment of the LTO register.

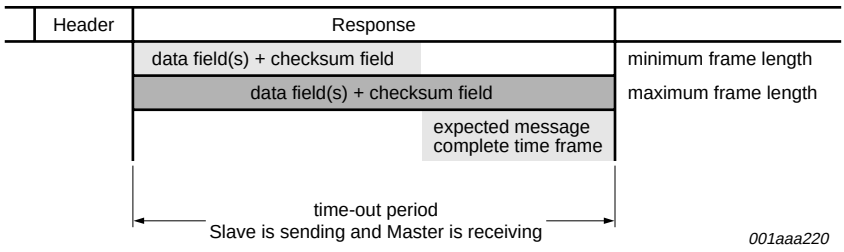

Fig 12. Time-out period for all LIN slave nodes

Table 212. LTO register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
7 to 0	TO	R/W	00h*	LIN message time-out; this register defines the maximum number of bit times when a response from all slave nodes should be completed

8.5.2.13 LIN master controller message buffer registers (LID, LDATA, LDATB, LDATC and LDATD)

The access to the message buffer is limited and controlled by the message buffer access bit of the status register. The access to the LIN master controller message buffer registers is only possible when the LIN master controller IP is in operating mode. Before accessing the message buffer the CPU should always read the message buffer access bit first to determine whether an access is possible or not. In cases where the message buffer is locked a write access is not successful whereas a read delivers logic 0 as result.

The first part of the message buffer is the LIN message identifier register (LID) containing the header information and control format of the LIN message.

Table 213 shows the bit assignment of the LID register.

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Table 213. LID register bits
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 26	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
25	CSID	R/W		checksum ID inclusion
			1	the identifier field is included in the checksum calculation
			0*	the identifier field is not included in the checksum calculation
24	DD	R/W		data direction
			1	the response field is expected to be send by a slave node
			0*	the response field is sent by the LIN master controller
23 to 21	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
20 to 16	DLC[4:0]	R/W	00h*	data length code; represents the binary number of data bytes in the LIN message response field; data length code values larger than 16 are handled as the maximum number of 16
15 to 8	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
7	P1	R/W	0*	LIN message parity bit 1
6	P0	R/W	0*	LIN message parity bit 0
5 to 0	ID	R/W	00h*	LIN message identifier

The rest of the message buffer contains the LIN message data registers (LDATA, LDATB, LDATC and LDATD).

Table 214, Table 215, Table 216 and Table 217 show the bit assignment of the LDATA, LDATB, LDATC and LDATD registers, respectively.

Table 214. LDATA register bits
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 24	DF4[7:0]	R/W	00h*	LIN message data field 4
23 to 16	DF3[7:0]	R/W	00h*	LIN message data field 3
15 to 8	DF2[7:0]	R/W	00h*	LIN message data field 2
7 to 0	DF1[7:0]	R/W	00h*	LIN message data field 1

Table 215. LDATB register bits
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 24	DF8[7:0]	R/W	00h*	LIN message data field 8
23 to 16	DF7[7:0]	R/W	00h*	LIN message data field 7
15 to 8	DF6[7:0]	R/W	00h*	LIN message data field 6
7 to 0	DF5[7:0]	R/W	00h*	LIN message data field 5

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Table 216. LDATC register bits
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 24	DF12[7:0]	R/W	00h*	LIN message data field 12
23 to 16	DF11[7:0]	R/W	00h*	LIN message data field 11
15 to 8	DF10[7:0]	R/W	00h*	LIN message data field 10
7 to 0	DF9[7:0]	R/W	00h*	LIN message data field 9

Table 217. LDATD register bits
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 24	DF16[7:0]	R/W	00h*	LIN message data field 16
23 to 16	DF15[7:0]	R/W	00h*	LIN message data field 15
15 to 8	DF14[7:0]	R/W	00h*	LIN message data field 14
7 to 0	DF13[7:0]	R/W	00h*	LIN message data field 13

8.5.2.14 Receive buffer register (RBR)

The receive buffer register is a 1-byte buffer and can be read via the bus interface. The received data is passed from the receive shift register to the receive buffer. The least significant bit represents the oldest received data bit. If the character received is less than 8 bits, the unused most significant bits are padded with logic 0.

The RBR register is read only. Table 218 shows the bit assignment of the RBR register.

Table 218. RBR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; read as logic 0
7 to 0	RBR[7:0]	R	-	receive buffer register; contains the received byte

8.5.2.15 Transmit holding register (THR)

The transmit holding register is a 1-byte transmit buffer and can be written via the bus interface. The data is passed from the transmit holding register to the transmit shift register when the last one is idle. The least significant bit represents the first bit to transmit.

The THR register is write only. Table 219 shows the bit assignment of the THR register.

Table 219. THR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, write as logic 0
7 to 0	THR[7:0]	W	-	transmit holding register; writing to the transmit holding register causes the data to be stored in the transmit buffer; the byte will be sent when the transmitter is available

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8.5.2.16 Interrupt enable register (IER)

The interrupt enable register is used to enable the three types of interrupts referred to in the interrupt identification register.

Table 220 shows the bit assignment of the IER register.

Table 220. IER register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 3	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
2	LSIE	R/W		receiver line status interrupt enable
			1	the receive line status interrupt is enabled
			0*	
1	TBEIE	R/W		transmit holding register empty interrupt enable
			1	the transmit holding register empty interrupt is enabled
			0*	
0	RBIE	R/W		receive buffer register interrupt register enable
			1	the receive data available interrupt is enabled
			0*	

8.5.2.17 Interrupt ID register (IIR)

The interrupt ID register provides a status code that denotes the priority and source of a pending interrupt. When an interrupt is generated, the interrupt ID register indicates that an interrupt is pending and encodes the type in its three bits. The interrupts are frozen during an access to the interrupt ID register. If an interrupt occurs during an access, the interrupt is recorded for the next interrupt ID register access.

The IIR register is read only. Table 221 shows the bit assignment of the IIR register.

Table 221. IIR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 3	reserved	-	-	reserved; read as logic 0
2 to 0	INT_ID[2:0]	R	1h*	interrupt identification; see Table 222

Table 222: Interrupt identification control functions details

INT_ID[2:0]	Priority level	Interrupt		
		Type	Source	Method
001	none	none	none	none

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Table 222: Interrupt identification control functions details *...continued*

INT_ID[2:0]	Priority level	Interrupt		
		Type	Source	Method
110	1	receiver line status	overrun error, parity error, framing error, or break interrupt	read the line status register LSR
100	2	received data available	receiver data available	read the receive buffer register RBR
010	3	transmitter holding register empty	transmit holding register empty	read the interrupt identification register (if source of interrupt) or writing into the transmitter holding register THR

8.5.2.18 Line control register (LCR)

The line control register controls the format of the asynchronous data communication exchange.

Table 223 shows the bit assignment of the LCR register.

Table 223. LCR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 7	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
6	BC	R/W		break control
			1	a break transmission condition is forced which puts the TXD output low
			0*	the break transmission condition is disabled; the break condition has no affect on the transmitter logic; it only affects the TXD line
5 to 4	PS[5:4]	R/W	0h*	parity select; see Table 224
3	PEN	R/W		parity enable
			1	a parity bit is generated in transmitted data between the last data word bit and the first stop bit; in received data the parity is checked
			0*	
2	STB	R/W		number of stop bits
			1	the number of generated stop bits are 2; except the word length is 5 bits, then 1.5 stop bits are generated
			0*	1 stop bit is generated
1 to 0	WLS[1:0]	R/W	0h*	word length select; see Table 225

Table 224: Parity select configuration bits

PS[5:4]	Function
00	odd parity (an odd number of logic 1s in the data and parity bits)
01	even parity (an even number of logic 1s in the data and parity bits)
10	forced logic 1 stick parity
11	forced logic 0 stick parity

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Table 225: Word length configuration

WLS[1:0]	Function
00	5-bit character length
01	6-bit character length
10	7-bit character length
11	8-bit character length

8.5.2.19 Line status register (LSR)

The line status register provides the information concerning the data transfers.

The LSR register is read only. Table 226 shows the bit assignment of the LSR register.

Table 226. LSR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 7	reserved	-	-	reserved; read as logic 0
6	TEMT	R		transmitter empty
			1*	the transmitter holding register and the transmitter shift register are both empty; the transmitter empty bit is cleared when either the transmitter holding register or the transmitter shift register contains a data character
			0	
5	THRE	R		transmitter holding register empty
			1*	the transmitter holding register is empty; if the transmitter holding register empty interrupt enable is set, an interrupt is generated; the transmitter holding register empty bit is set when the contents of the transmitter holding register is transferred to the transmitter shift register; the transmitter holding register empty bit is cleared concurrently with loading the transmitter holding register
			0	
4	BI	R		break interrupt
			1	the received data input was held low for longer than a full-word transmission time; a full-word transmission time is defined as the total time to transmit the start, data, parity, and stop bits; the break interrupt bit is cleared upon reading; the UART tries to resynchronize after a framing error; to accomplish this, it is assumed that the framing error is due to the next start bit; the UART samples this start bit twice and then accepts the input data
			0*	
3	FE	R		framing error
			1	the received character did not have a valid (set) stop bit; the framing error is cleared upon reading; the next character transfer is enabled after the RXD input line goes to the marking state (1s) for at least two sample times and then receives the next valid start bit
			0*	

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Table 226. LSR register bit description *...continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
2	PE	R		parity error
			1	the parity of the received data character does not match the parity selected in the line control register; the parity error is cleared upon reading
			0*	
1	OE	R		overrun error
			1	the character in the receiver buffer register was overwritten by the next character transferred into this register before it was read; the overrun error is cleared upon reading
			0*	
0	DR	R		data ready
			1	a complete incoming character has been received and transferred to the receiver buffer register; the data ready bit is cleared by reading the data in the receiver buffer register
			0*	

8.5.2.20 Scratch register (SCR)

The scratch register is intended for the programmer's use as scratch pad in the sense that it temporarily holds the programmer's data without affecting any other UART operation.

Table 227 shows the bit assignment of the SCR register.

Table 227. SCR register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 8	reserved	-	-	reserved; do not modify, write as logic 0, read as logic 0
7 to 0	SCR[7:0]	R/W	00h*	scratch register; this register can be written and/or read at the discretion of the user

8.6 Vectored interrupt controller

8.6.1 Overview

The SJA 2020 contains a very flexible and powerful Vectored Interrupt Controller (VIC) to interrupt the ARM processor on request.

The key features are:

- Level active interrupt request with programmable polarity
- 31 interrupt requests inputs
- Software interrupt request capability associated to each request input
- Observability of interrupt request state before masking
- Software programmable priority assignments to interrupt request up to 15 levels
- Software programmable routing of interrupt requests towards the ARM processor inputs IRQ and FIQ

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- Fast identification of interrupt request through vector
- Support for nesting of interrupt service routines

The vectored interrupt controller routes incoming interrupt requests to the ARM processor. The interrupt target is configured for each interrupt request input of the interrupt controller. The targets are defined as follows:

- Target 0 is ARM processor IRQ (standard interrupt service)
- Target 1 is ARM processor FIQ (fast interrupt service)

Interrupt request masking is performed individually per interrupt target by comparing the priority level assigned to a specific interrupt request with a target specific priority threshold. The priority levels are defined as follows:

- Priority level 0 corresponds to 'masked'; interrupt requests with priority 0 will never lead to an interrupt request
- Priority 1 corresponds to the lowest priority
- Priority 15 corresponds to the highest priority

Software interrupt support is provided and can be supplied for:

- Test the RTOS interrupt handling without using device specific interrupt service routines
- Software emulation of an interrupt requesting device, including interrupts

8.6.2 VIC pin description

The vectored interrupt controller module in the SJA2020 has no external pins.

8.6.3 Register mapping

The vectored interrupt controller registers are shown in Table 228. The vectored interrupt controller registers have an offset to the base address VIC RegBase which can be found in the memory map (see Table 7).

Table 228: Vectored interrupt controller register summary

Address	Access	Reset value	Name	Description	Reference
000h	R/W	-	INT_PRIORITY MASK_0	target 0 priority mask register	see Table 229
004h	R/W	-	INT_PRIORITY MASK_1	target 1 priority mask register	see Table 229
100h	R/W	-	INT_VECTOR_0	target 0 vector register	see Table 230
104h	R/W	-	INT_VECTOR_1	target 1 vector register	see Table 230
200h	R	-	INT_ PENDING_1_31	interrupt pending status register	see Table 231
300h	R	1 0F1Fh	INT_FEATURES	interrupt controller features register	see Table 232
404h	R/W	-	INT_REQUEST_1	interrupt request 1 control register	see Table 234

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Table 228: Vectored interrupt controller register summary …continued

Address	Access	Reset value	Name	Description	Reference
408h	R/W	-	INT_REQUEST_2	interrupt request 2 control register	see Table 234
40Ch	R/W	-	INT_REQUEST_3	interrupt request 3 control register	see Table 234
410h	R/W	-	INT_REQUEST_4	interrupt request 4 control register	see Table 234
414h	R/W	-	INT_REQUEST_5	interrupt request 5 control register	see Table 234
418h	R/W	-	INT_REQUEST_6	interrupt request 6 control register	see Table 234
41Ch	R/W	-	INT_REQUEST_7	interrupt request 7 control register	see Table 234
420h	R/W	-	INT_REQUEST_8	interrupt request 8 control register	see Table 234
424h	R/W	-	INT_REQUEST_9	interrupt request 9 control register	see Table 234
428h	R/W	-	INT_REQUEST_10	interrupt request 10 control register	see Table 234
42Ch	R/W	-	INT_REQUEST_11	interrupt request 11 control register	see Table 234
430h	R/W	-	INT_REQUEST_12	interrupt request 12 control register	see Table 234
434h	R/W	-	INT_REQUEST_13	interrupt request 13 control register	see Table 234
438h	R/W	-	INT_REQUEST_14	interrupt request 14 control register	see Table 234
43Ch	R/W	-	INT_REQUEST_15	interrupt request 15 control register	see Table 234
440h	R/W	-	INT_REQUEST_16	interrupt request 16 control register	see Table 234
444h	R/W	-	INT_REQUEST_17	interrupt request 17 control register	see Table 234
448h	R/W	-	INT_REQUEST_18	interrupt request 18 control register	see Table 234
44Ch	R/W	-	INT_REQUEST_19	interrupt request 19 control register	see Table 234
450h	R/W	-	INT_REQUEST_20	interrupt request 20 control register	see Table 234
454h	R/W	-	INT_REQUEST_21	interrupt request 21 control register	see Table 234
458h	R/W	-	INT_REQUEST_22	interrupt request 22 control register	see Table 234
45Ch	R/W	-	INT_REQUEST_23	interrupt request 23 control register	see Table 234
460h	R/W	-	INT_REQUEST_24	interrupt request 24 control register	see Table 234

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Table 228: Vectored interrupt controller register summary …continued

Address	Access	Reset value	Name	Description	Reference
464h	R/W	-	INT_REQUEST_25	interrupt request 25 control register	see Table 234
468h	R/W	-	INT_REQUEST_26	interrupt request 26 control register	see Table 234
46Ch	R/W	-	INT_REQUEST_27	interrupt request 27 control register	see Table 234
470h	R/W	-	INT_REQUEST_28	interrupt request 28 control register	see Table 234
474h	R/W	-	INT_REQUEST_29	interrupt request 29 control register	see Table 234
478h	R/W	-	INT_REQUEST_30	interrupt request 30 control register	see Table 234
47Ch	R/W	-	INT_REQUEST_31	interrupt request 31 control register	see Table 234

8.6.4 Interrupt priority mask register (INT_PRIORITYMASK)

The interrupt priority mask registers define the thresholds for priority level masking. Each interrupt target has its own priority limiter. The priority limiter can be used to define the minimum priority level for nesting interrupts; typically, the priority limiter is set to the priority level of the interrupt service routine that is currently being executed. By doing this, only interrupt requests at a higher priority level will lead to a nested interrupt service. Nesting can be disabled by setting the priority level to Fh in the interrupt request register.

Table 229 shows the bit assignment of the INT_PRIORITYMASK_n registers.

Table 229. INT_PRIORITYMASK register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 4	reserved	-	-	reserved; do not modify, read as logic 0, write as logic 0
3 to 0	PRIORITY_LIMITER[3:0]	R/W	-	priority limiter; this register determines a priority threshold that incoming interrupt requests must exceed to trigger interrupt requests towards the CPU and the event router

8.6.5 Interrupt vector register (INT_VECTOR)

The interrupt vector registers identify, individually for each interrupt target, the highest priority enabled pending interrupt request that is present at the time when the register is being read. The software interrupt service routine must always read the vector register that corresponds to the interrupt target. The interrupt vector content can be used as vector into a memory based table like shown in Figure 13. This table has 32 entries. To be able to use the register content as a full 32-bit address pointer, the table must be aligned to a 256 byte address boundary (or 2 048 to be future proof). If only the index variable is used as offset into the table, then this address alignment is not required. Each table entry has 64-bit width. It is recommended to pack per table entry:

- The start address of a peripheral specific interrupt service routine, plus

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- The associated priority limiter value (if nesting of interrupt service routine shall be performed)

A vector with index 0 indicates that no interrupt with priority above the priority threshold is pending. The vector table should implement for this entry a 'no interrupt' handler to treat this special case.

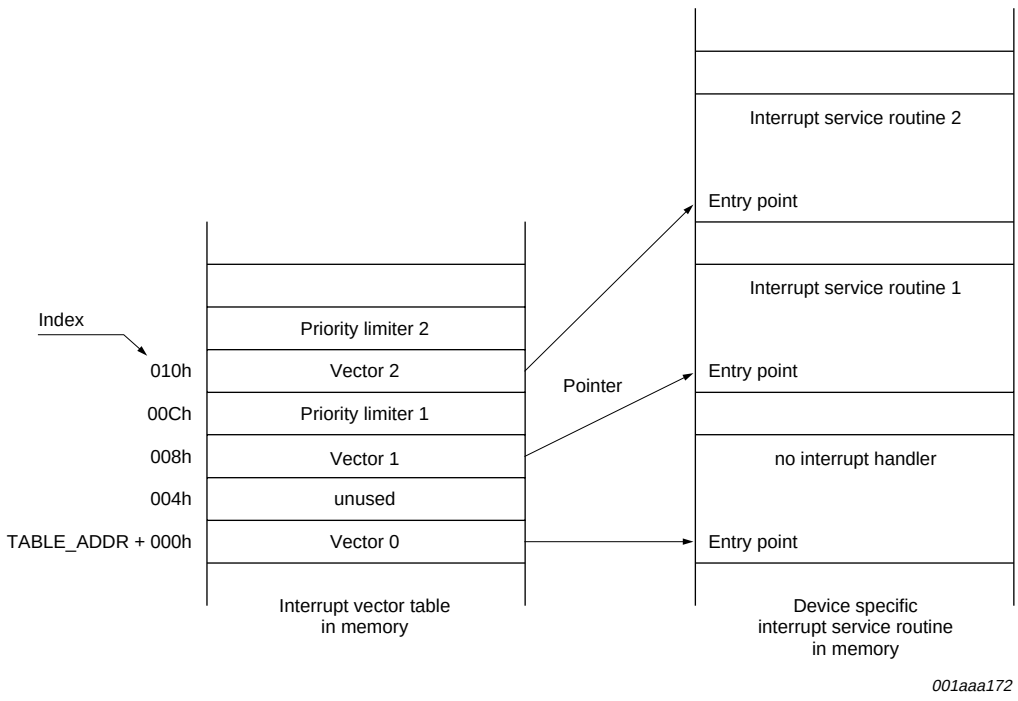

Fig 13. Memory based interrupt vector and priority table

Table 230 shows the bit assignment of the INT_VECTOR register.

Table 230. INT_VECTOR register bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 11	TABLE_ADDR[20:0]	R/W	-	table start address; indicates the lower address boundary of a 256 byte aligned vector table in memory; to be compatible with future extension an address boundary of 2048 byte is recommended
10 to 8	reserved	-	-	reserved; read as logic 0
7 to 3	INDEX[4:0]	R	-	index; indicates the interrupt request line of the interrupt request to be served by the controller:
				INDEX = 0 means no interrupt request to be served
				INDEX = 1 means serve interrupt request at input 1
				INDEX = n means serve interrupt request at input n
2 to 0	NULL[2:0]	R	-	always reflecting logic 0s

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8.6.6 Interrupt pending register (INT_PENDING_1_31)

The interrupt pending register gathers the pending bits of all interrupt request registers. Software can make use of the interrupt pending to gain a faster overview on pending interrupts than by reading the individual interrupt request registers.

The INT_PENDING_1_31 register is read only.

Table 231 shows the bit assignment of the INT_PENDING_1_31 register.

Table 231. INT_PENDING_1_31 register bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 1	PENDING	R	-	pending interrupt request; the bit position reflects the pending state of the corresponding interrupt request line
			1	an interrupt request is pending
			0	there is no interrupt request
0	reserved	-	-	reserved; read as logic 0

8.6.7 Interrupt controller features register (INT_FEATURES)

The interrupt controller features register indicates the vectored interrupt controller configuration of which an ISR can make use of for implementing interrupt controller configuration specific behavior.

The INT_FEATURES register is read only.

Table 232 shows the bit assignment of the INT_FEATURES register.

Table 232. INT_FEATURES register bits
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 16	reserved	-	-	reserved; read as don't care
21 to 16	T	R	01h*	number of targets (minus one)
15 to 8	P	R	0Fh*	number of priorities (minus one)
7 to 0	N	R	1Fh*	number of interrupt requests

8.6.8 Interrupt request register (INT_REQUEST)

The reference between the interrupt source and interrupt request line is reflected in Table 233.

Table 233: Interrupt source and request reference

Interrupt request	Interrupt source	Activation level	Description
1	timer 0	low	capture or match interrupt from timer 0
2	timer 1	low	capture or match interrupt from timer 1
3	timer 2	low	capture or match interrupt from timer 2
4	timer 3	low	capture or match interrupt from timer 3
5	UART	high	general interrupt from 16C550 UART
6	SPI 0	high	general interrupt from SPI 0
7	SPI 1	high	general interrupt from SPI 1

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Table 233: Interrupt source and request reference *...continued*

Interrupt request	Interrupt source	Activation level	Description
8	SPI 2	high	general interrupt from SPI 2
9	event router	high	event, wake-up or real time clock tick interrupt from event router
10	ADC	high	conversion scan completed interrupt from ADC
11	flash	high	signature, burn or erase finished interrupt from flash
12	watchdog	low	debug underflow interrupt from watchdog
13	embedded RT-ICE	high	communications RX for ARM debug mode
14	embedded RT-ICE	high	communications TX for ARM debug mode
15	LIN master controller 0	high	general interrupt from LIN master controller 0
16	LIN master controller 1	high	general interrupt from LIN master controller 1
17	LIN master controller 2	high	general interrupt from LIN master controller 2
18	LIN master controller 3	high	general interrupt from LIN master controller 3
19	all CAN controllers	high	combined general interrupt of all CAN controllers and the CAN Look-Up table [1]
20	CAN controller 0	high	message received interrupt from CAN controller 0 [2]
21	CAN controller 1	high	message received interrupt from CAN controller 1 [2]
22	CAN controller 2	high	message received interrupt from CAN controller 2 [2]
23	CAN controller 3	high	message received interrupt from CAN controller 3 [2]
24	CAN controller 4	high	message received interrupt from CAN controller 4 [2]
25	CAN controller 5	high	message received interrupt from CAN controller 5 [2]
26	CAN controller 0	high	message transmitted interrupt from CAN controller 0
27	CAN controller 1	high	message transmitted interrupt from CAN controller 1
28	CAN controller 2	high	message transmitted interrupt from CAN controller 2
29	CAN controller 3	high	message transmitted interrupt from CAN controller 3
30	CAN controller 4	high	message transmitted interrupt from CAN controller 4
31	CAN controller 5	high	message transmitted interrupt from CAN controller 5

[1] Combined general interrupt of all CAN controllers and the CAN look-up table; the following interrupts are combined here: error warning interrupt (EWI), data overrun interrupt (DOI), error passive interrupt (EPI), arbitration lost interrupt (ALI), bus error interrupt (BEI) and look-up table error interrupt (CALUTE); see Section 8.5.1.7 and Section 8.5.1.33 for details.

[2] Message received interrupt from CAN controller x; the Receive Interrupt (RI) and the ID ready interrupt (IDI) are combined here; see Section 8.5.1.7 for details.

The interrupt request registers hold the configuration information related to interrupt request inputs of the interrupt controller and allow to issue software interrupt requests. Each interrupt line has its own interrupt request register.

Table 234 shows the bit assignment of the INT_REQUEST register.

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Table 234. INT_REQUEST register bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31	PENDING	R/W		pending interrupt request; reflects the state of the interrupt source channel; the pending status is also visible in the interrupt pending register. Writing this bit has no effect.
			1	an interrupt request is pending
			0	there is no interrupt request
30	SET_SWINT	R/W		set software interrupt request
			1	writing logic 1 sets the local software interrupt request state
			0	writing a logic 0 has no effect on the local software interrupt request state; this bit is always read as logic 0
29	CLR_SWINT	R/W		clear software interrupt request
			1	writing logic 1 clears the local software interrupt request state
			0	writing a logic 0 has no effect on the local software interrupt request state; this bit is always read as logic 0
28	WE_PRIORITY_LEVEL	R/W		write enable priority level
			1	writing logic 1 enables the bit state change during the same register access
			0	writing logic 0 does not change the bit state; this bit is always read as logic 0
27	WE_TARGET	R/W		write enable target
			1	writing logic 1 enables the bit state change during the same register access; for changing the bit state, software must first disable the interrupt request (bit ENABLE = 0), then change this bit and finally re-enable the interrupt request (bit ENABLE = 1) again
			0	writing logic 0 does not change this bit state; this bit is always read as logic 0
26	WE_ENABLE	R/W		write enable
			1	writing logic 1 enables this bit state change during the same register access
			0	writing logic 0 does not change this bit state; this bit is always read as logic 0
25	WE_ACTIVE_LOW	R/W		write enable active LOW
			1	writing logic 1 enables the bit state change during the same register access
			0	writing logic 0 does not change the bit state; this bit is always read as logic 0
24 to 18	reserved	-		reserved; do not modify, write as logic 0, read as logic 0

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Table 234. INT_REQUEST register bit description *...continued*
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
17	ACTIVE_LOW	R/W		active LOW interrupt line; selects the polarity of the interrupt request line; state changing is only possible if the corresponding write enable bit has been set
			1	the interrupt request is active LOW
			0*	the interrupt request is active HIGH
16	ENABLE	R/W		enable interrupt request; controls the interrupt request processing by the interrupt controller; state changing is only possible if the corresponding write enable bit has been set
			1	the interrupt request may cause an ARM processor interrupt request if further conditions for this become true
			0*	the interrupt request is discarded and will not cause an ARM processor interrupt
15 to 9	reserved	-	-	reserved; do not modify, write as logic 0, read as logic 0
8	TARGET	R/W		interrupt target; defines the interrupt target of an interrupt request; state changing is only possible if the corresponding write enable bit has been set
			1	the target is the FIQ
			0*	the target is the IRQ
7 to 4	reserved	-	-	reserved; do not modify, write as logic 0, read as logic 0
3 to 0	PRIORITY_LEVEL[3:0]	R/W	-	interrupt priority level; determines the priority level of the interrupt request; state changing is only possible if the corresponding write enable bit has been set
			1	priority level 0 masks the interrupt request, thus it is ignored
			0	priority level 1 has the lowest priority level and 15 the highest

9. Limiting values

Table 235: Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Supply pins						
P_{tot}	total power dissipation		[1]	-	1	W
$V_{DD(CORE)}$	core supply voltage			–0.5	+2.0	V
$V_{DD(OSC\_PLL)}$	oscillator and PLL supply voltage			–0.5	+2.0	V
$V_{DD(RTC)}$	RTC supply voltage			–0.5	+2.0	V

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Table 235: Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(ADC)}$	ADC supply voltage			–0.5	+3.6	V
$V_{DD(IO)}$	I/O supply voltage			–0.5	+4.6	V
I_{DD}	supply current	average value per supply pin	[2]	-	98	mA
I_{SS}	ground current	average value per ground pin	[2]	-	98	mA
Input pins and I/O pins						
V_{XIN_OSC}	voltage on pin XIN_OSC			–0.5	+2.0	V
V_{XIN_RTC}	voltage on pin XIN_RTC			–0.5	+2.0	V
$V_{I(IO)}$	I/O input voltage					
	DC input voltage on 5 V tolerant port pins		[3][4] [5]	–0.5	$V_{DD(IO)}$ + 3.0	V
	DC input voltage on all other I/O and input pins			–0.5	$V_{DD(IO)}$ + 0.5	V
$V_{I(ADC)}$	ADC input voltage			–0.5	+3.6	V
V_{VREFN}	voltage on pin VREFN			–0.5	+3.6	V
$I_{I(ADC)}$	ADC input current	average value per input pin	[2]	-	35	mA
Output pins and I/O pins configured as output						
I_{OHS}	HIGH-state short-circuit output current	drive high, output shorted to $V_{SS(IO)}$	[6]	-	33	mA
I_{OLS}	LOW-state short-circuit output current	drive low, output shorted to $V_{DD(IO)}$	[6]	-	–38	mA
General						
T_{stg}	storage temperature			–40	+150	°C
T_{amb}	ambient temperature			–40	+105	°C
T_{vj}	virtual junction temperature		[7]	–40	+125	°C
Memory						
$n_{endu(fl)}$	endurance of flash memory			-	1000	cycle
$t_{ret(fl)}$	flash memory retention time			-	20	year
ESD						
V_{esd}	electrostatic discharge voltage	on all pins				
		HBM	[8]	–2000	+2000	V
		MM	[9]	–200	+200	V
		CDM	[10] [11]	–500	+500	V
		on corner pins				
		CDM	[10]	–750	+750	V

[1] Based on package heat transfer, not device power consumption.

[2] Peak current must be limited at 25 times average current.

[3] $V_{DD(IO)}$ must be present.

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[4] Not 5 V tolerant when pull-up is on.

[5] 6 V should not be exceeded.

[6] 112 mA per $V_{DD(IO)}$ or $V_{SS(IO)}$ should not be exceeded.

[7] In accordance with IEC 60747-1. An alternative definition of the virtual junction temperature is: $T_{vj} = T_{amb} + P_{tot} \times R_{th(j-a)}$ where $R_{th(j-a)}$ is a fixed value (see Section 10). The rating for T_{vj} limits the allowable combinations of power dissipation and ambient temperature.

[8] Human body model: according AEC-Q100 Rev-F, H2.

[9] Machine model: according AEC-Q100 Rev-F, M3.

[10] Charged device model: according AEC-Q100 Rev-F, C3B.

[11] Except for the $V_{DD(OSC\_PLL)}$ pin, which is guaranteed up to 375 V.

10. Thermal characteristics

Table 236: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	62	K/W

11. Static characteristics

Table 237: Static characteristics

$V_{DD(CORE)} = V_{DD(OSC\_PLL)} = V_{DD(RTC)} = 1.8\ V \pm 5\ \%$; $V_{DD(IO)} = 2.7\ V$ to $3.6\ V$; $V_{DD(ADC)} = 3.0\ V$ to $3.6\ V$; $T_{vj} = -40\ °C$ to $+125\ °C$; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified [1].

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
Core supply							
$V_{DD(CORE)}$	core supply voltage			1.71	1.80	1.89	V
$I_{DD(CORE)}$	core supply current	ARM7 and all peripherals active		-	1.1	2.0	mA/MHz
		all clocks off	[2]	-	10	300	µA
I/O supply							
$V_{DD(IO)}$	I/O supply voltage			2.7	-	3.6	V
Oscillator							
$V_{DD(OSC\_PLL)}$	oscillator and PLL supply voltage			1.71	1.80	1.89	V
$I_{DD(OSC\_PLL)}$	oscillator and PLL supply current	start-up		1.5	-	3	mA
		normal		-	-	1	mA
		power-down		-	-	1	µA
Real time clock							
$V_{DD(RTC)}$	RTC supply voltage			1.71	1.80	1.89	V
$I_{DD(RTC)}$	RTC supply current	normal		-	-	6	µA
		power-down		-	-	1	µA
Analog-to-digital converter							
$V_{DD(ADC)}$	ADC supply voltage			3.0	3.3	3.6	V

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Table 237: Static characteristics *...continued*

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$ = $V_{DD(RTC)}$ = 1.8 V ± 5 %; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DD(ADC)}$ = 3.0 V to 3.6 V; T_{vj} = −40 °C to +125 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified [1].

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DD(ADC)}$	ADC supply current	normal		-	-	400	µA
		power-down		-	-	1	µA
Input pins and I/O pins configured as input							
V_I	input voltage	all port pins and $V_{DD(IO)}$ applied	[3]	−0.5	-	+5.5	V
		all port pins and $V_{DD(IO)}$ not applied		−0.5	-	+3.6	V
		all other I/O pins, RESET_N, TRST_N, TDI, JTAGSEL, TMS, TCK		−0.5	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-state input voltage	all port pins, RESET_N, TRST_N, TDI, JTAGSEL, TMS, TCK		2.0	-	-	V
V_{IL}	LOW-state input voltage	all port pins, RESET_N, TRST_N, TDI, JTAGSEL, TMS, TCK		-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
I_{LIH}	HIGH-state input leakage current			-	-	1	µA
I_{LIL}	LOW-state input leakage current			-	-	1	µA
$I_{I(pd)}$	pull-down input current	all port pins, V_I = 3.3 V; V_I = 5.5 V		25	50	100	µA
$I_{I(pu)}$	pull-up input current	all port pins, RESET_N, TRST_N, TDI, JTAGSEL, TMS: V_I = 0 V; V_I > 3.6 V is not allowed		−25	−50	−100	µA
C_i	input capacitance			-	-	8	pF
Output pins and I/O pins configured as output							
V_O	output voltage			0	-	$V_{DD(IO)}$	V
V_{OH}	HIGH-state output voltage	TDO: I_{OH} = −8 mA; all other pins: I_{OH} = −4 mA		$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-state output voltage	TDO: I_{OL} = 8 mA; all other pins: I_{OL} = 4 mA		-	-	0.4	V
Analog-to-digital converter							
V_{VREFN}	voltage on pin VREFN			0	-	$V_{DD(ADC)}$ − 2	V
V_I	input voltage	at pins AI0, AI1, AI2, AI3		V_{VREFN}	-	$V_{DD(ADC)}$	V
Z_i	input impedance	between V_{VREFN} and $V_{DD(ADC)}$		-	30	-	kΩ
C_i	input capacitance	at pins AI0, AI1, AI2, AI3		-	-	1	pF
FSR	full scale range			2	-	10	bit
INL	integral non-linearity		[4]	−1	-	+1	LSB

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Table 237: Static characteristics *...continued*

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$ = $V_{DD(RTC)}$ = 1.8 V ± 5 %; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DD(ADC)}$ = 3.0 V to 3.6 V; T_{vj} = −40 °C to +125 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified [1].

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	differential non-linearity		[4]	−1	-	+1	LSB
$V_{err(offset)}$	offset error voltage			−20	-	+20	mV
$V_{err(FS)}$	full-scale error voltage			−20	-	+20	mV
Oscillator							
$R_{s(xtal)}$	crystal series resistance	f_{osc} = 10 MHz to 15 MHz	[5]				
		C_{xtal} = 10 pF; $C_{L(ext)}$ = 18 pF		-	-	160	Ω
		C_{xtal} = 20 pF; $C_{L(ext)}$ = 39 pF		-	-	60	Ω
		f_{osc} = 15 MHz to 20 MHz	[5]				
		C_{xtal} = 10 pF; $C_{L(ext)}$ = 18 pF		-	-	80	Ω
Real time clock							
$R_{s(xtal)}$	crystal series resistance	C_{xtal} = 11 pF; $C_{L(ext)}$ = 18 pF	[5]	-	-	100	Ω
		C_{xtal} = 13 pF; $C_{L(ext)}$ = 22 pF	[5]	-	-	100	Ω
		C_{xtal} = 15 pF; $C_{L(ext)}$ = 27 pF	[5]	-	-	100	Ω
Power-up reset							
$V_{trip(high)}$	high trip level voltage	on $V_{DD(CORE)}$	[6]	1.2	1.4	1.6	V
$V_{trip(low)}$	low trip level voltage	on $V_{DD(CORE)}$	[6]	1.1	1.3	1.5	V
$V_{trip(dif)}$	difference between high and low trip level voltage		[6]	50	120	180	mV

[1] All parameters are guaranteed over the virtual junction temperature range by design. Production testing is performed at T_{amb} = 125 °C on wafer level. Cased products are tested at T_{amb} = 25 °C. Production testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Leakage current is exponential to temperature; worst case value is at T_{vj} = 125 °C.

[3] Not 5 V tolerant when pull-up is on.

[4] INL and DNL are indirectly measured during production test by measuring the Dynamic Noise Reduction (DNR) and Effective Numbers of Bits (ENB).

[5] C_{xtal} is crystal load capacitance and $C_{L(ext)}$ are the two external load capacitors.

[6] The power-up reset has a time filter: $V_{DD(CORE)}$ must be above $V_{trip(high)}$ for 2 µs before the internal reset is de-asserted; $V_{DD(CORE)}$ must be below $V_{trip(low)}$ for 11 µs before internal reset is asserted.

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12. Dynamic characteristics

Table 238: Dynamic characteristics

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$ = $V_{DD(RTC)}$ = 1.8 V ± 5 %; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DD(ADC)}$ = 3.0 V to 3.6 V; T_{vj} = −40 °C to +125 °C; all voltages are defined with respect to ground; positive currents flow into the IC; unless otherwise specified [1].

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I/O pins							
t_{THL}	HIGH-to-LOW transition time	30 pF load capacitance		4	-	13.8	ns
t_{TLH}	LOW-to-HIGH transition time	30 pF load capacitance		4	-	13.8	ns
Internal clock							
$f_{clk(sys)}$	system clock frequency			10	-	60	MHz
$T_{clk(sys)}$	system clock period			16	-	100	ns
Ring oscillator							
$f_{ref(RO)}$	RO reference frequency	before ringo calibration (CRFS) and post (CRPD) dividers		1.0	-	1.80	MHz
$t_{startup}$	start-up time	at maximum frequency	[2]	-	6	100	µs
$t_{jit(cc)(p-p)}$	cycle-to-cycle jitter (peak-to-peak value)		[2]	-	-	1	ns
Oscillator							
$f_{i(osc)}$	oscillator input frequency			10	-	20	MHz
$t_{startup}$	start-up time		[3]	-	500	-	µs
$t_{jit(cc)(p-p)}$	cycle-to-cycle jitter (peak-to-peak value)		[2]	-	-	240	ps
PLL							
$f_{o(PLL)}$	PLL output frequency			10	-	60	MHz
f_{CCO}	CCO frequency			156	-	320	MHz
$t_{startup}$	start-up time		[2]	-	-	100	µs
$t_{jit(cc)(p-p)}$	cycle-to-cycle jitter (peak-to-peak value)		[2]	-	-	300	ps
Real time clock							
$f_{i(RTC)}$	RTC input frequency			-	32.768	-	kHz
$t_{startup}$	start-up time		[2]	-	-	1	s
$t_{jit(cc)(p-p)}$	cycle-to-cycle jitter (peak-to-peak value)		[2]	-	-	20	ns
Analog-to-digital converter							
$f_{i(ADC)}$	ADC input frequency			-	-	4.5	MHz

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Table 238: Dynamic characteristics *...continued*

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$ = $V_{DD(RTC)}$ = 1.8 V ± 5 %; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DD(ADC)}$ = 3.0 V to 3.6 V; T_{vj} = −40 °C to +125 °C; all voltages are defined with respect to ground; positive currents flow into the IC; unless otherwise specified [1].

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_s	sampling frequency	$f_{i(ADC)}$ = 4.5 MHz; $f_s = f_{i(ADC)} / (n+1)$ with n = resolution					
		in kilo samples per second		400	-	1500	ksample/s
		in bits		10	-	2	bit
t_{conv}	conversion time	in number of ADC clock cycles		3	-	11	cycle
		in number of bits		2	-	10	bit
Flash							
t_{init}	initialization time			-	-	150	µs
$t_{a(clk)}$	clock access time			-	-	67.5	ns
$t_{a(A)}$	address access time			-	-	49	ns
$t_{wr(pg)}$	page write time		[4]	-	1	-	ms
$t_{er(sect)}$	sector erase time		[4]	-	100	-	ms
$t_{fl(BIST)}$	flash word BIST time		[2]	-	42	70	ns
Static memory controller							
$t_{a(R)int}$	internal read access time		[2]	-	-	18	ns
$t_{a(W)int}$	internal write access time		[2]	-	-	19	ns
UART							
f_{UART}	UART frequency			$1/65024f_{clk(sys)}$	-	$1/2f_{clk(sys)}$	MHz
SPI							
f_{SPI}	SPI operating frequency	master operation		$1/65024f_{clk(sys)}$	-	$1/2f_{clk(sys)}$	MHz
		slave operation		$1/65024f_{clk(sys)}$	-	$1/12f_{clk(sys)}$	MHz

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 125 °C on wafer level. Cased products are tested at T_{amb} = 25 °C. Production testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] This parameter is not part of production test; worst case figure stated is based on simulations.

[3] Oscillator start-up time depends on the quality of the crystal. For most crystals it takes about 1000 clock pulses until the clock is fully stable.

[4] Maximum deviation should be within ±5 %.

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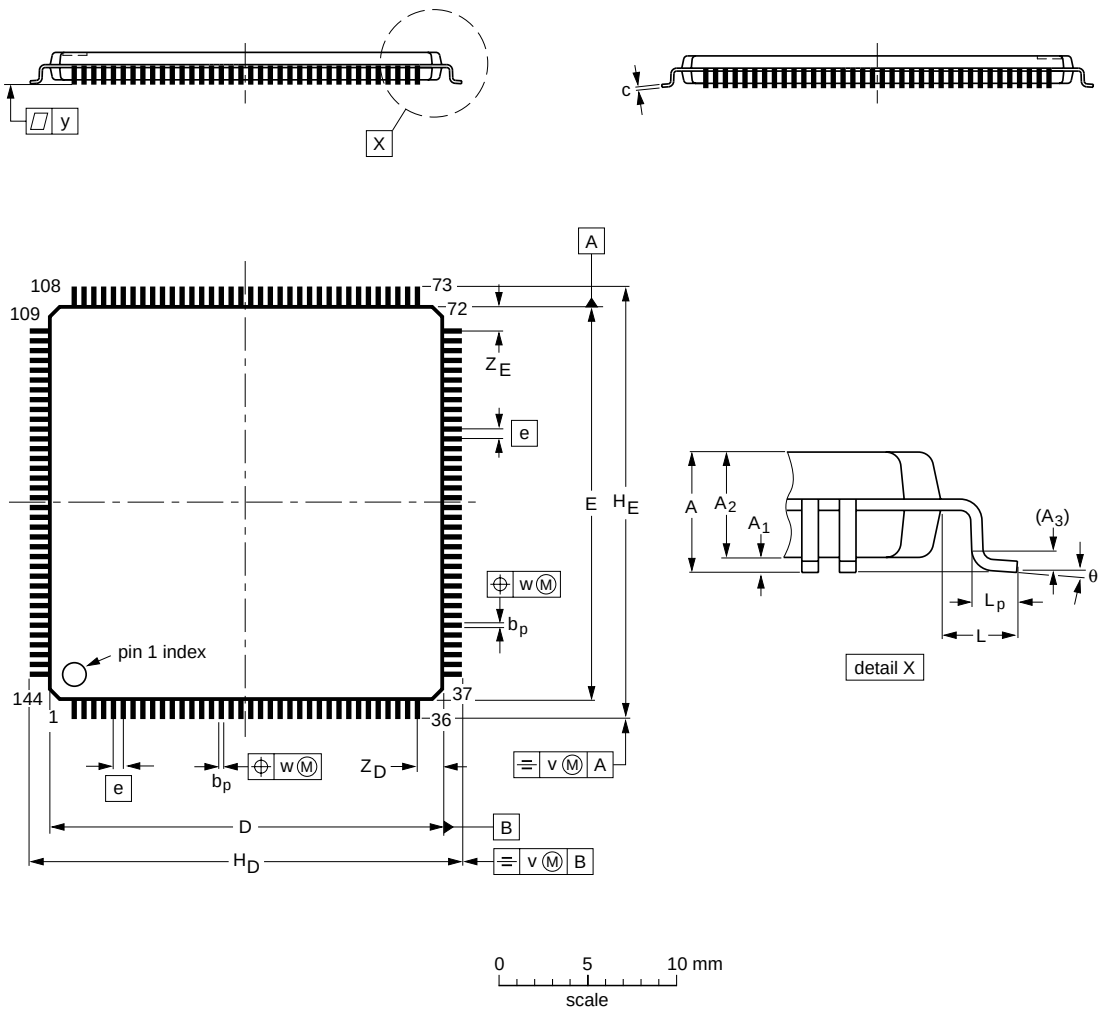
13. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 14. Package outline SOT486-1 (LQFP144)

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14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

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– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 239. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

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[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. References

[1] **UM —** SJA2020 User manual, UM10141_1

[2] **ANKI —** SJA2020 Application note ‘Known issues’, AN10383_1

[3] **ARM —** ARM web site

[4] **ARM-SSP —** ARM PrimeCell synchronous serial port (PL022) technical reference manual

[5] **CAN —** ISO 11898-1: 2002 road vehicles - Controller Area Network (CAN) - part 1: data link layer and physical signalling

[6] **LIN —** LIN specification package, revision 2.0

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16. Revision history

Table 240. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SJA2020_1 (9397 750 12148)	20060405	Objective data sheet	-	-

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17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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