6-OUTPUT LOW-POWER HCSL BUFFER FOR PCIE GEN1-2-3 AND QPI 9ZXL0651

General Description

The 9ZXL0651 is a low-power 6-output differential buffer that meets all the performance requirements of the Intel DB1200Z specification. It consumes 50% less power than standard HCSL devices and has internal terminations to allow direct connection to 85 ohm transmission lines. The 9ZXL0651 is backwards compatible to PCIe Gen1 and Gen2 and QPI 6.4GT/s specifications. A fixed, internal feedback path maintains low drift for critical QPI applications.

Recommended Application

6-Output Low-Power HCSL Buffer for PCIe Gen1-2-3 and QPI

Output Features

- 6 - 0.7V low-power HCSL (LP-HCSL) output pairs w/integrated terminations

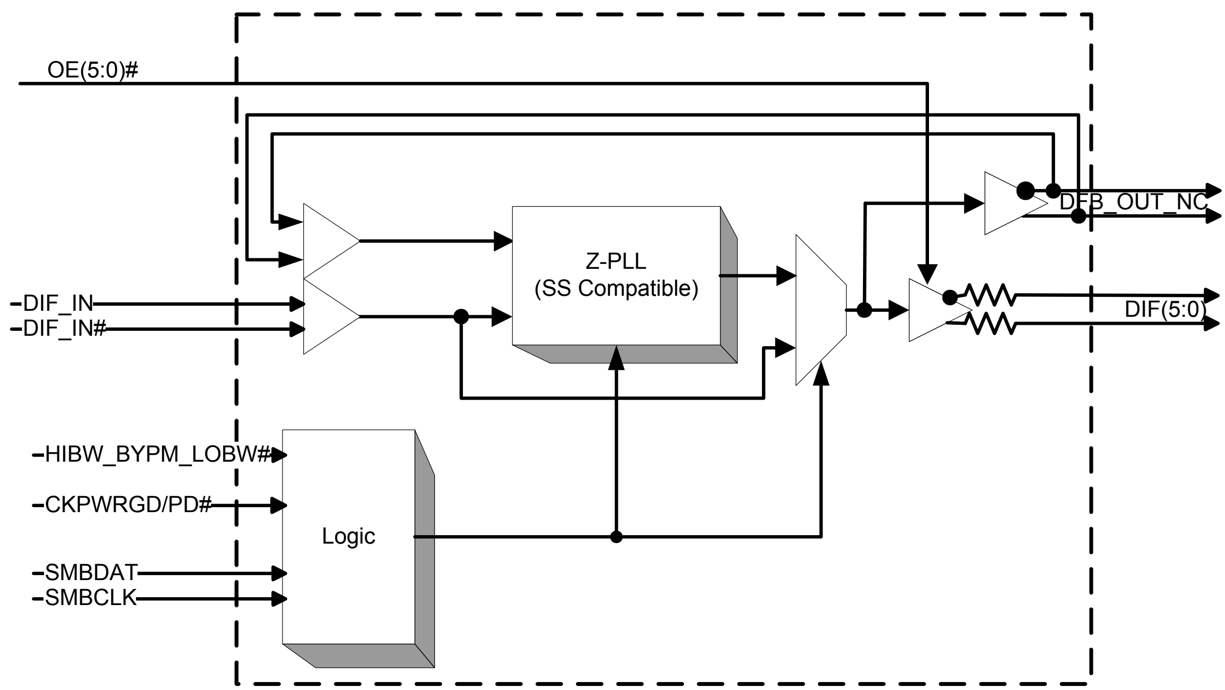
Features/Benefits

- Low-Power-HCSL outputs w/Zo = 85Ω; save power and board space - no termination resistors required. Ideal for blade servers.
- Space-saving 40-pin VFQFPN package
- Fixed feedback path for 0ps input-to-output delay
- 6 OE# pins; Hardware control of each output
- PLL or bypass mode; PLL can dejitter incoming clock
- Selectable PLL bandwidth; minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible; tracks spreading input clock for low EMI

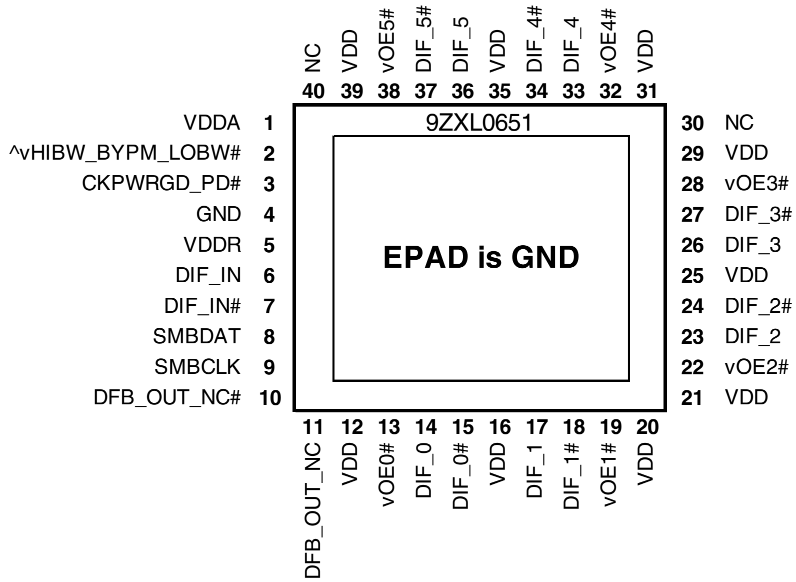
Key Specifications

- Cycle-to-cycle jitter <50ps
- Output-to-output skew <65 ps
- Input-to-output delay variation <50ps
- PCIe Gen3 phase jitter <1.0ps RMS
- QPI 9.6GT/s 12UI phase jitter <0.2ps RMS

Block Diagram



Pin Configuration



40-VFQFPN

^ prefix indicates internal Pull-Up Resistor
v prefix indicates Internal Pull-Down Resistor
^v prefix indicates Interal Pull-Up/Down Resistor (biased to VDD/2)

5mm x 5mm 0.4mm pin pitch

Power Management Table

CKPWRGD_PD#	DIF_IN/ DIF_IN#	SMBus EN bit	DIF(5:0)/ DIF(5:0)#	PLL STATE IF NOT IN BYPASS MODE
0	X	X	Low/Low	OFF
1	Running	0	Low/Low	ON
		1	Running	ON

PLL Operating Mode

HiBW_BypM_LoBW#	MODE
Low	PLL Lo BW
Mid	Bypass
High	PLL Hi BW

NOTE: PLL is OFF in Bypass Mode

PLL Operating Mode Readback Table

HiBW_BypM_LoBW#	Byte0, bit 7	Byte 0, bit 6
Low (Low BW)	0	0
Mid (Bypass)	0	1
High (High BW)	1	1

Tri-level Input Thresholds

Level	Voltage
Low	<0.8V
Mid	1.2<Vin<1.8V
High	Vin > 2.2V

Power Connections

Pin Number		Description
VDD	GND	
1	41	Analog PLL
5	4	Analog Input
12,16,20,24,27,31,32,36,40	41	DIF clocks

9ZXL0651 SMBus Address

1101100	+ Read/Write bit

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDA	PWR	3.3V power for the PLL core.
2	^vHIBW_BYPM_LOBW#	LATCHED IN	Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details.
3	CKPWRGD_PD#	Trays	3.3V Input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.
4	GND	GND	Ground pin.
5	VDDR	PWR	3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.
6	DIF_IN	IN	0.7 V Differential True input
7	DIF_IN#	IN	0.7 V Differential Complementary Input
8	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
9	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
10	DFB_OUT_NC#	OUT	Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization with input clock to eliminate phase error. This pin should NOT be connected on the circuit board, the feedback is internal to the package.
11	DFB_OUT_NC	OUT	True half of differential feedback output, provides feedback signal to the PLL for synchronization with the input clock to eliminate phase error. This pin should NOT be connected on the circuit board, the feedback is internal to the package.
12	VDD	PWR	Power supply, nominal 3.3V
13	vOE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
14	DIF_0	OUT	0.7V differential true clock output
15	DIF_0#	OUT	0.7V differential Complementary clock output
16	VDD	PWR	Power supply, nominal 3.3V
17	DIF_1	OUT	0.7V differential true clock output
18	DIF_1#	OUT	0.7V differential Complementary clock output
19	vOE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
20	VDD	PWR	Power supply, nominal 3.3V
21	VDD	PWR	Power supply, nominal 3.3V
22	vOE2#	IN	Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
23	DIF_2	OUT	0.7V differential true clock output
24	DIF_2#	OUT	0.7V differential Complementary clock output
25	VDD	PWR	Power supply, nominal 3.3V
26	DIF_3	OUT	0.7V differential true clock output
27	DIF_3#	OUT	0.7V differential Complementary clock output
28	vOE3#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
29	VDD	PWR	Power supply, nominal 3.3V
30	NC	N/A	No Connection.
31	VDD	PWR	Power supply, nominal 3.3V
32	vOE4#	IN	Active low input for enabling DIF pair 4. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
33	DIF_4	OUT	0.7V differential true clock output
34	DIF_4#	OUT	0.7V differential Complementary clock output
35	VDD	PWR	Power supply, nominal 3.3V
36	DIF_5	OUT	0.7V differential true clock output
37	DIF_5#	OUT	0.7V differential Complementary clock output
38	vOE5#	IN	Active low input for enabling DIF pair 5. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
39	VDD	PWR	Power supply, nominal 3.3V
40	NC	N/A	No Connection.
41	EPAD	GND	Ground Pad.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZXL0651. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDD, VDDA, VDDR	VDD for core logic and PLL			4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics–Clock Input Parameters

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	V_{IHDIF}	Differential inputs (single-ended measurement)	600	800	1150	mV	1
Input Low Voltage - DIF_IN	V_{ILDIF}	Differential inputs (single-ended measurement)	V_{SS} - 300	0	300	mV	1
Input Common Mode Voltage - DIF_IN	V_{COM}	Common Mode Input Voltage	300		1000	mV	1
Input Amplitude - DIF_IN	V_{SWING}	Peak to Peak value (single-ended measurement)	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.35			V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	1
Input Duty Cycle	d_{tin}	Measurement from differential wavefrom	45	50	55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–Input/Supply/Common Parameters

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T_{COM}	Commmercial range	0	35	70	°C	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	1
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	1
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	1
Input Frequency	F_{ibyp}	V_{DD} = 3.3 V, Bypass mode	1		150	MHz	2
	F_{ipll}	V_{DD} = 3.3 V, 100MHz PLL mode	90	100.00	110	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.53	1	ms	1,2
Input SS Modulation Frequency	f_{MODIN}	Allowable Frequency (Triangular Modulation)	30		33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	4	8	12	cycles	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of control inputs			10	ns	1,2
Trise	t_R	Rise time of control inputs			10	ns	1,2
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	1
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	1
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	1
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	1
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			100	kHz	1,5

[1]Guaranteed by design and characterization, not 100% tested in production.
[2]Control input must be monotonic from 20% to 80% of input swing.
[3]Time from deassertion until outputs are >200 mV
[4]DIF_IN input
[5]The differential input clock must be running for the SMBus to be active

Electrical Characteristics–DIF 0.7V Low Power HCSL Outputs

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on	1	2.9	4	V/ns	1, 2, 3
Slew rate matching	ΔTrf	Slew rate matching, Scope averaging on		7	20	%	1, 2, 4
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	754	850	mV	1
Voltage Low	VLow		-150	62	150		1
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		827	1150	mV	1
Min Voltage	Vmin		-300	10			1
Vswing	Vswing	Scope averaging off	300	1395		mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	300	453	550	mV	1, 5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		14	140	mV	1, 6

[1]Guaranteed by design and characterization, not 100% tested in production. C_L = 2pF, Zo = 85Ω differential trace impedance).

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

Electrical Characteristics–Current Consumption

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{DDVDDR}	100MHz, VDDR rail		4	6	mA	1
	$I_{DDVDDAPLL}$	100MHz, VDDA rail, PLL Mode		14	20	mA	1
	$I_{DDVDDABYP}$	100MHz, VDDA rail, Bypass Mode		3	5	mA	1
	I_{DDVDD}	100MHz, VDD rail		41	50	mA	1
Powerdown Current	$I_{DDVDDRPD}$	Power Down, VDDR Rail		3.5	5	mA	1
	$I_{DDVDDAPD}$	Power Down, VDDA Rail		1.6	3	mA	1
	$I_{DDVDDPD}$	Power Down, VDD Rail		0.3	2	mA	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] C_L = 2pF, Zo = 85Ω differential trace impedance

Electrical Characteristics–Skew and Differential Jitter Parameters

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
CLK_IN, DIF[x:0]	t_{SPO_PLL}	In-to-Out Skew in PLL mode @ 100MHz nominal value @35°C, 3.3V	-100	53	100	ps	1,2,4,5,8
CLK_IN, DIF[x:0]	t_{PD_BYP}	In-to-Out Skew in Bypass mode @ 100MHz nominal value @ 35°C, 3.3V	2.5	3.4	4.5	ns	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSPO_PLL}	In-to-Out Skew Varation in PLL mode across voltage and temperature	-50	0	50	ps	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSPO_BYP}	In-to-Out Skew Varation in Bypass mode across voltage and temperature	-250	0	250	ps	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DTE}	Random Differential Tracking error beween two 9ZX devices in Hi BW Mode		3	5	ps (rms)	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSSTE}	Random Differential Spread Spectrum Tracking error beween two 9ZX devices in Hi BW Mode		15	75	ps	1,2,3,5,8
DIF{x:0]	t_{SKEW_ALL}	Output-to-Output Skew across all outputs (Common to Bypass and PLL mode)		39	65	ps	1,2,3,8
PLL Jitter Peaking	$j_{peak-hibw}$	LOBW#_BYPASS_HIBW = 1			2.5	dB	7,8
PLL Jitter Peaking	$j_{peak-lobw}$	LOBW#_BYPASS_HIBW = 0			2	dB	7,8
PLL Bandwidth	pll_{HIBW}	LOBW#_BYPASS_HIBW = 1			4	MHz	8,9
PLL Bandwidth	pll_{LOBW}	LOBW#_BYPASS_HIBW = 0			1.4	MHz	8,9
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	50.1	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode @100MHz		-1.7	|2|	%	1,10
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode		14	50	ps	1,11
		Additive Jitter in Bypass Mode		0	25	ps	1,11

Notes for preceding table:

[1] C_L = 2pF, Zo = 85Ω differential trace impedance. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

[3] All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

[4] This parameter is deterministic for a given device

[5] Measured with scope averaging on to find mean value.

[6.] t is the period of the input clock

[7] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

[8.] Guaranteed by design and characterization, not 100% tested in production.

[9] Measured at 3 db down or half power point.

[10] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[11] Measured from differential waveform

Electrical Characteristics–Phase Jitter Parameters

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1}$	PCIe Gen 1		43	46	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		1.4	1.5	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2.4	2.7	3.1	ps (rms)	1,2
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz)		0.56	0.61	1	ps (rms)	1,2,4
	t_{jphQPI_SMI}	QPI & SMI (PLL BW of 17.04MHz 100/133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.27	0.51	1	ps (rms)	1,5
		QPI & SMI (PLL BW of 7.8MHz 100/133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.22	0.49	0.5	ps (rms)	1,5
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.16	0.28	0.3	ps (rms)	1,5
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.11	0.17	0.2	ps (rms)	1,5
Additive Phase Jitter, Bypass mode	$t_{jphPCIeG1}$	PCIe Gen 1		1	5	N/A	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.0	0.0	N/A	ps (rms)	1,2,6
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.0	0.0	N/A	ps (rms)	1,2,6
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz)		0.0	0.0	N/A	ps (rms)	1,2,4,6
	t_{jphQPI_SMI}	QPI & SMI (PLL BW of 17.04MHz 100/133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.25	0.3	N/A	ps (rms)	1,5,6
		QPI & SMI (PLL BW of 7.8MHz 100/133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.10	0.15	N/A	ps (rms)	1,5,6
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.0	0.0	N/A	ps (rms)	1,5,6
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.0	0.0	N/A	ps (rms)	1,5,6

[1] Applies to all outputs.

[2] See http://www.pcisig.com for complete specs

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] Subject to final ratification by PCI SIG.

[5] Calculated from Intel-supplied Clock Jitter Tool

[6] For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)^2 = (total jittter)^2 - (input jitter)^2

Clock Periods–Differential Outputs with Spread Spectrum Disabled

SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2,3

Clock Periods–Differential Outputs with Spread Spectrum Enabled

SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2,3

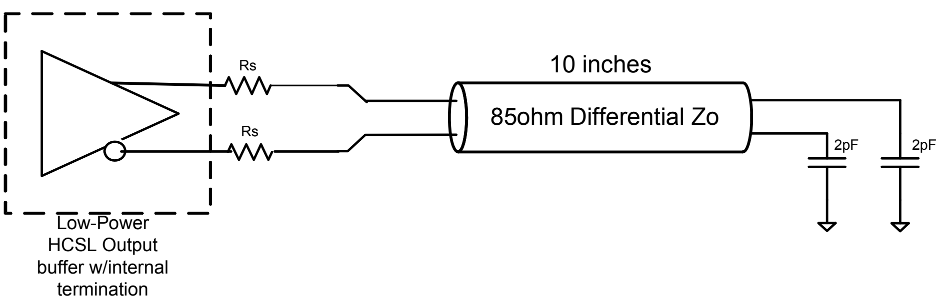
Notes:

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (+/-100ppm). The 9ZXL0651 itself does not contribute to ppm error.

[3] Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode

Test Loads



Differential Output Terminations

DIF Zo (Ω)	Rs (Ω)
100	7
85	0

Note: No resistors are required for connection to 85ohm transmission lines.

General SMBus Serial Interface Information for 9ZXL0651

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBusTable: PLL Mode, and Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	2	PLL Mode 1	PLL Operating Mode Rd back 1	R	See PLL Operating Mode Readback Table		Latch
Bit 6	2	PLL Mode 0	PLL Operating Mode Rd back 0	R			Latch
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		PLL_SW_EN	Enable S/W control of PLL BW	RW	HW Latch	SMBus Control	0
Bit 2		PLL Mode 1	PLL Operating Mode 1	RW	See PLL Operating Mode Readback Table		1
Bit 1		PLL Mode 0	PLL Operating Mode 1	RW			1
Bit 0		Reserved					1

Note: Setting bit 3 to '1' allows the user to overide the Latch value from pin 5 via use of bits 2 and 1. Use the values from the PLL Operating Mode Readback Table. Note that Bits 7 and 6 will keep the value originally latched on pin 5. A warm reset of the system will have to accomplished if the user changes these bits.

SMBusTable: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					1
Bit 6	26/27	DIF_3_En	Output Control - '0' overrides OE# pin	RW	Low/Low	Enable	1
Bit 5	23/24	DIF_2_En	Output Control - '0' overrides OE# pin	RW			1
Bit 4		Reserved					1
Bit 3		Reserved					1
Bit 2	17/18	DIF_1_En	Output Control - '0' overrides OE# pin	RW	Low/Low	Enable	1
Bit 1	14/15	DIF_0_En	Output Control - '0' overrides OE# pin	RW			1
Bit 0		Reserved					1

SMBusTable: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					1
Bit 2	36/37	DIF_5_En	Output Control - '0' overrides OE# pin	RW	Low/Low	Enable	1
Bit 1	33/34	DIF_4_En	Output Control - '0' overrides OE# pin	RW			1
Bit 0		Reserved					1

SMBusTable: Reserved Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

SMBusTable: Reserved Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

SMBusTable: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	A rev = 0000		X
Bit 6	-	RID2		R			X
Bit 5	-	RID1		R			X
Bit 4	-	RID0		R			X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBusTable: DEVICE ID

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Device ID 7 (MSB)		R	FB Hex		1
Bit 6	-	Device ID 6		R			1
Bit 5	-	Device ID 5		R			1
Bit 4	-	Device ID 4		R			1
Bit 3	-	Device ID 3		R			1
Bit 2	-	Device ID 2		R			0
Bit 1	-	Device ID 1		R			1
Bit 0	-	Device ID 0		R			1

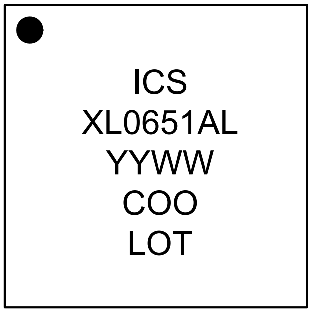
SMBusTable: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4	-	BC4	Writing to this register configures how many bytes will be read back.	RW	Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default.		0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			0

SMBusTable: Reserved Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

Marking Diagram

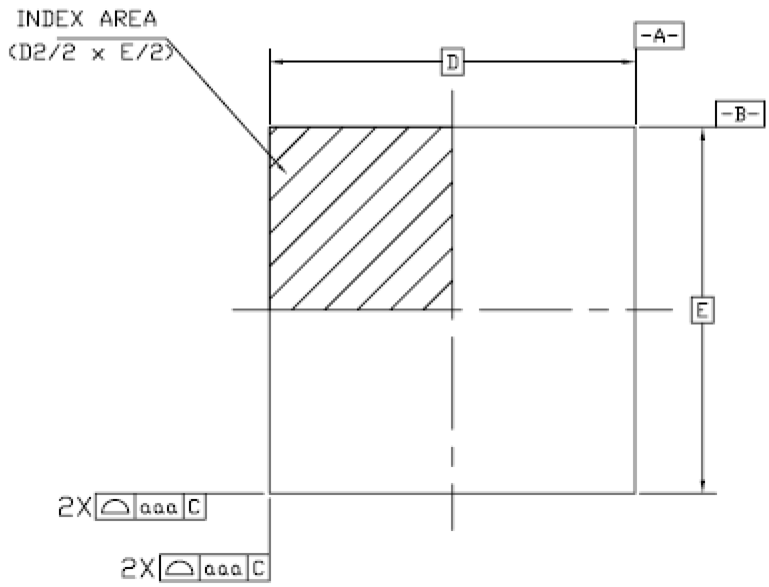


Notes:

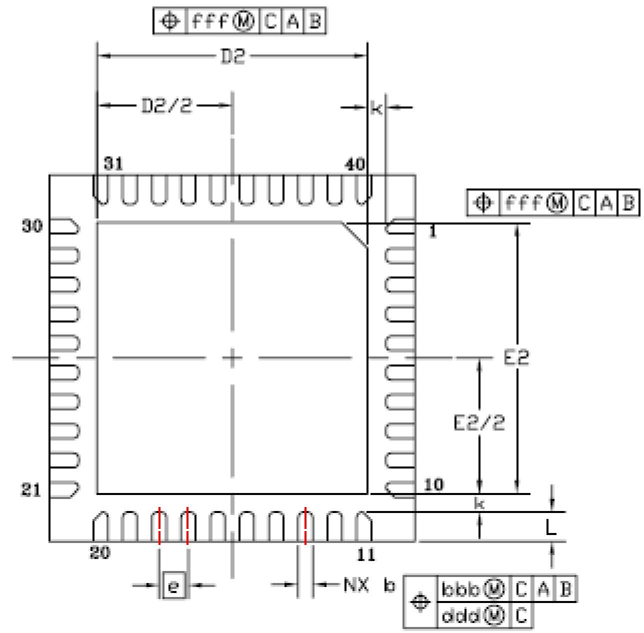
1. “L” denotes RoHS compliant package.
2. ‘LOT’ denotes the lot number.
3. “COO”: country of origin.
4. YYWW is the last two digits of the year and week that the part was assembled.

Package Outline and Package Dimensions (NDG40)

Package dimensions are kept current with JEDEC Publication No. 95

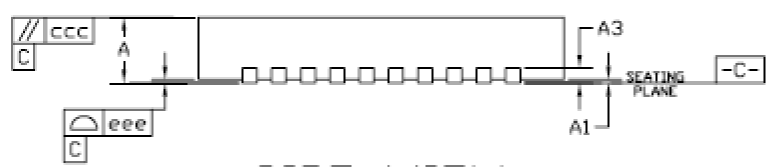


TOP VIEW



BOTTOM VIEW

SYMBOL	DIMENSION		
	MIN	NOM	MAX
b	0.15	0.20	0.25
D	5.00 BSC		
E	5.00 BSC		
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
L	0.30	0.40	0.50
e	0.40 BSC		
N	40		
ND	10 (note 3)		
NE	10 (note 3)		
A	0.80		1.00
A1	0.00	0.02	0.05
A3	0.2 REF		
k	0.35		
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		



SIDE VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

Ordering Information

Part / Order Number	Shipping Package	Package	Temperature
9ZXL0651AKLF	Trays	40-pin VFQFPN	0 to +70°C
9ZXL0651AKLFT	Tape and Reel	40-pin VFQFPN	0 to +70°C

"LF" suffix to the part number denotes Pb-Free configuration, RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

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Revision History

Rev.	Issue Date	Issuer	Description	Page #
A	10/31/2013	RDW	Updated Electrical Tables with characterization data and moved to final.	Various
B	11/25/2014	RDW	1. Updates to Byte 6, bits 7:4; default should be “1”. 2. Updated device ID in Byte 6 from “8B” to “FB”.	12
C	3/30/2015	RDW	1. Corrected Test Loads to remove references to IREF and Rp. These are not present on parts that have LP-HCSL outputs.	9

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