

Three-Terminal Low Current Positive Voltage Regulator

Features

- **Three-Terminal Regulators**
- **Maximum Input Voltage : 30V**
- **Output Voltages of 5V, 12V**
- **Output Current Up to 100mA**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short-Circuit Limiting**
- **Output Voltage Offered in 4% Tolerance**
- **SOP-8, SOT-89, and TO-92/TO-92A Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

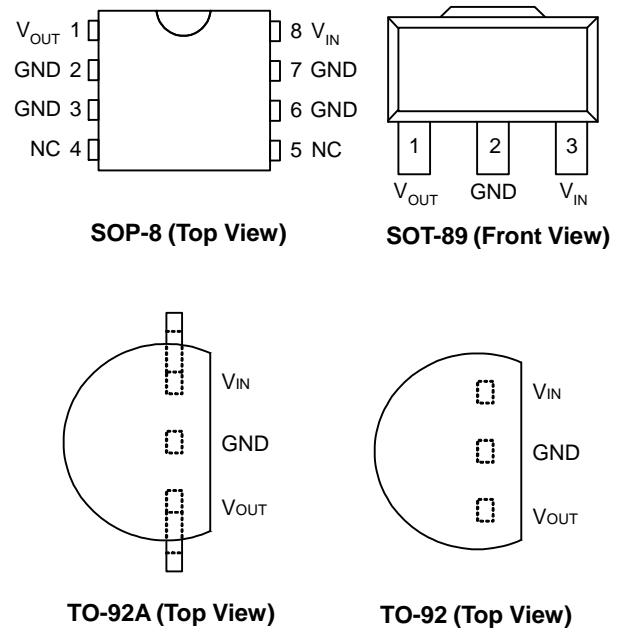
Applications

- **Battery-Powered Circuitry**
- **Post Regulator for Switching Power Supply**

General Description

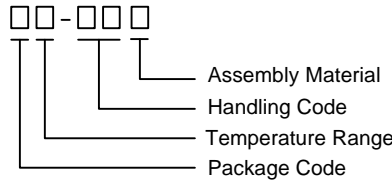
These series of fixed-voltage monolithic integrated-circuit voltage regulators are designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power-pass elements to make high-current voltage regulators. Each of these regulators can deliver up to 100mA of output current. The internal limiting and thermal shutdown features of these regulators make them essentially immune to overload. When used as a replacement for a Zener diode-resistor combination, an effective improvement in output impedance can be obtained together with lower-bias current.

Pin Configuration



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

<p>APL78L05/12</p>  <p> Assembly Material Handling Code Temperature Range Package Code </p>	<p> Package Code E : TO-92/TO-92A K : SOP-8 D : SOT-89 Operating Ambient Temperature Range C : 0 to 70 °C Handling Code TR : Tape & Reel TB : Tape & Box (only for TO-92A Bent Legs) PB : Plastic & Box Assembly Material G : Halogen and Lead Free Device </p>		
<p>APL78L05/12 E :</p>	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%; text-align: center;"> APL 78L05/12 XXXXX </td> <td style="width: 50%; text-align: center;">XXXXX - Date Code</td> </tr> </table>	APL 78L05/12 XXXXX	XXXXX - Date Code
APL 78L05/12 XXXXX	XXXXX - Date Code		
<p>APL78L05/12 D :</p>	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%; text-align: center;"> APL78L05/12 XXXXX </td> <td style="width: 50%; text-align: center;">XXXXX - Date Code</td> </tr> </table>	APL78L05/12 XXXXX	XXXXX - Date Code
APL78L05/12 XXXXX	XXXXX - Date Code		
<p>APL78L05/12 K :</p>	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%; text-align: center;"> APL78L05/12 ●XXXXX </td> <td style="width: 50%; text-align: center;">XXXXX - Date Code</td> </tr> </table>	APL78L05/12 ●XXXXX	XXXXX - Date Code
APL78L05/12 ●XXXXX	XXXXX - Date Code		

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V _{IN}	Input Voltage	30	V _{DC}
T _J	Operating Junction Temperature Range	Control Section Power Transistor	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ _{JA}	Thermal Resistance from Junction to Ambient in Free Air ^(Note 2)		
	SOP-8	160	°C/W
	SOT-89/TO-92/TO-92A	180	
θ _{JC}	Thermal Resistance from Junction to Case		
	SOP-8	30	°C/W
	SOT-89/TO-92/TO-92A	80	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Electrical Characteristics

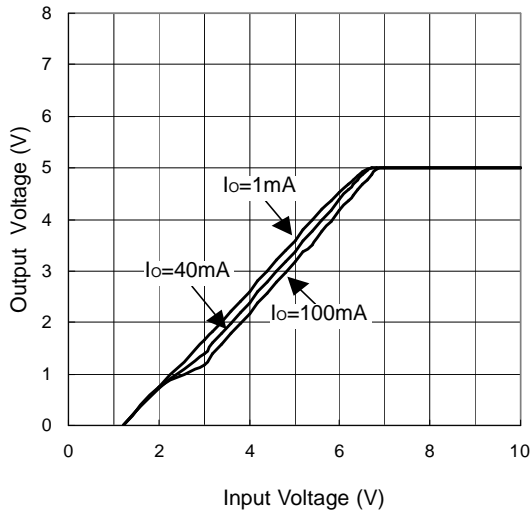
$V_{IN} = 10V$, $I_{OUT} = 40mA$, $T_A = 25^\circ C$, $C_{IN} = 0.33\mu F$, $C_{OUT} = 0.1\mu F$, unless otherwise specified.

Symbol	Parameter	Test Conditions	APL78L05			Unit
			Min.	Typ.	Max.	
V_O	Output Voltage		4.8	5.0	5.2	Vdc
	Output Voltage (0° to $+125^\circ C$)	$1.0mA \leq I_{OUT} \leq 40mA$	4.75	5	5.25	
		$7.0Vdc \leq V_{IN} \leq 20Vdc$ $V_{IN} = 10V, 1.0mA \leq I_{OUT} \leq 40mA$				
Reg_{line}	Line Regulation	$7.0Vdc \leq V_{IN} \leq 20Vdc$	-	29	150	mV
		$8.0Vdc \leq V_{IN} \leq 20Vdc$	-	26	100	
Reg_{load}	Load Regulation	$1.0mA \leq I_{OUT} \leq 100mA$	-	9	60	mV
		$1.0mA \leq I_{OUT} \leq 40mA$	-	5	30	
I_B	Quiescent Current		-	2.8	6.0	mA

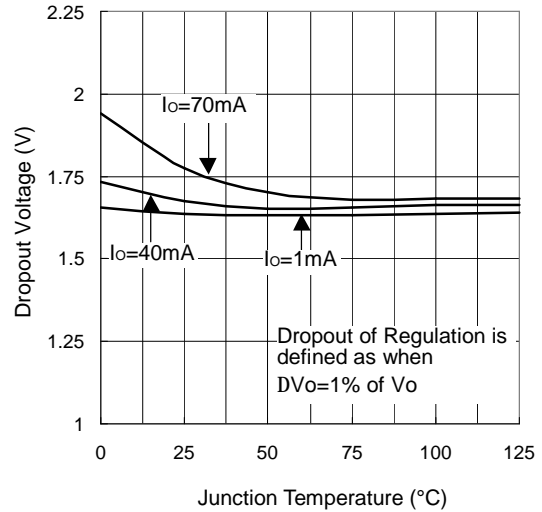
Symbol	Parameter	Test Conditions	APL78L12			Unit
			Min.	Typ.	Max.	
ΔI_B	Quiescent Current Change	$8.0Vdc \leq V_{IN} \leq 20Vdc$	-	0.15	1.5	mA
		$1.0mA \leq I_{OUT} \leq 40mA$	-	0.08	0.1	
$V_{IN}-V_O$	Dropout Voltage	$I_{OUT} = 100mA$	-	1.9	-	Vdc
V_O	Output Voltage		11.5	12	12.5	
V_O	Output Voltage (0° to $+125^\circ C$)	$1.0mA \leq I_{OUT} \leq 40mA$	11.4	12	12.6	
		$14Vdc \leq V_{IN} \leq 27Vdc$				
		$V_{IN} = 19V, 1.0mA \leq I_{OUT} \leq 40mA$				
Reg_{line}	Line Regulation	$14.5Vdc \leq V_{IN} \leq 27Vdc$	-	-	250	mV
Reg_{load}	Load Regulation	$1.0mA \leq I_{OUT} \leq 100mA$	-	-	100	
		$1.0mA \leq I_{OUT} \leq 40mA$	-	-	50	
I_B	Quiescent Current		-	-	6.5	mA
ΔI_B	Quiescent Current Change	$16Vdc \leq V_{IN} \leq 27Vdc$	-	-	1.5	
		$1.0mA \leq I_{OUT} \leq 40mA$	-	-	-	
$V_{IN}-V_O$	Dropout Voltage	$I_{OUT} = 100mA$	-	1.9	-	Vdc

Typical Operating Characteristics

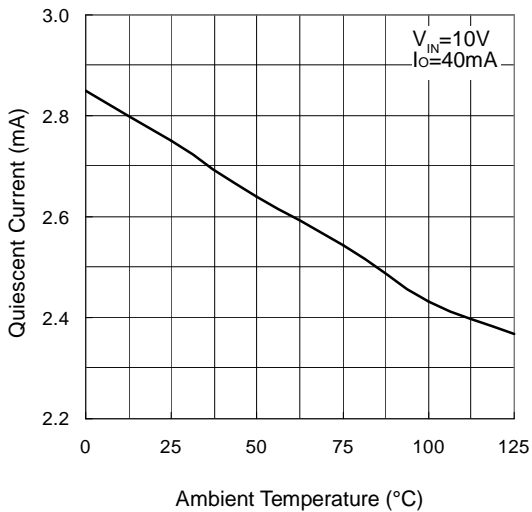
Output Voltage vs. Input Voltage



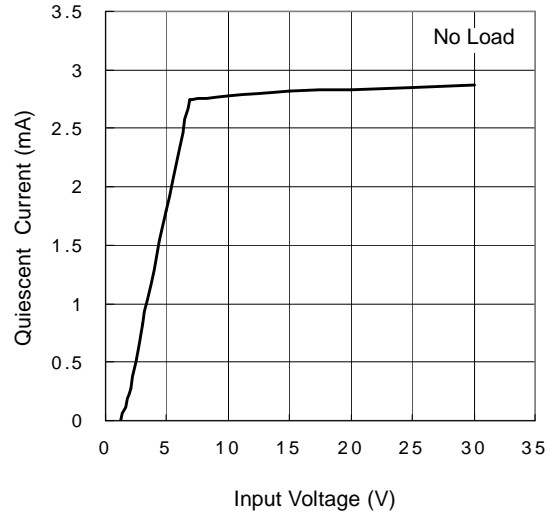
Dropout Voltage vs. Junction Temperature



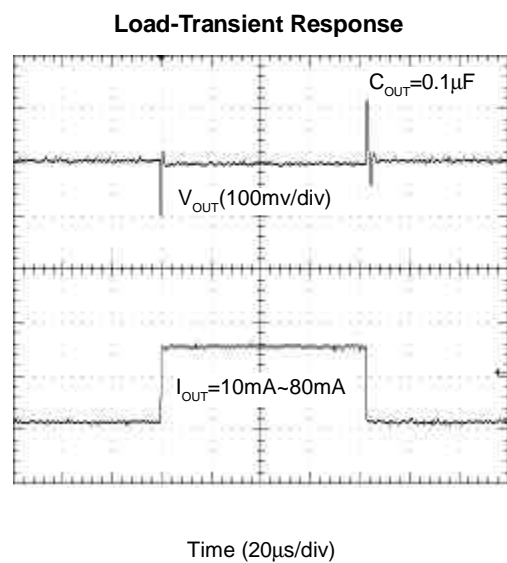
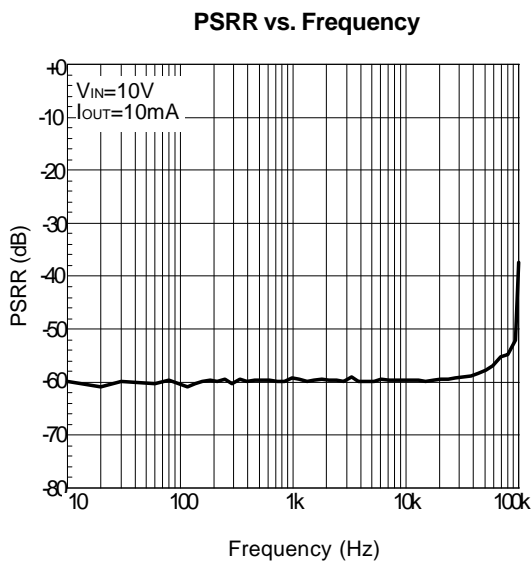
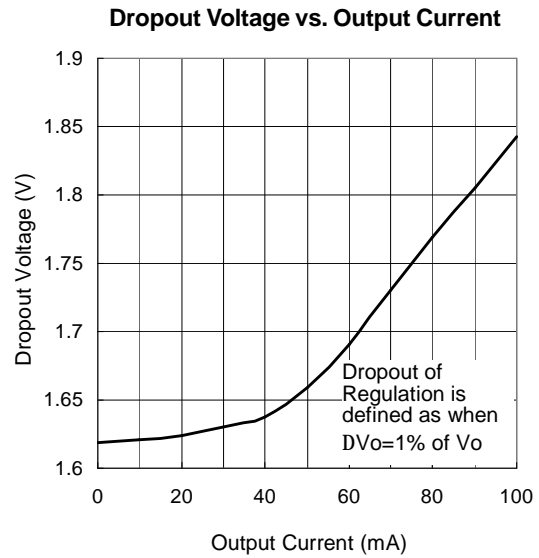
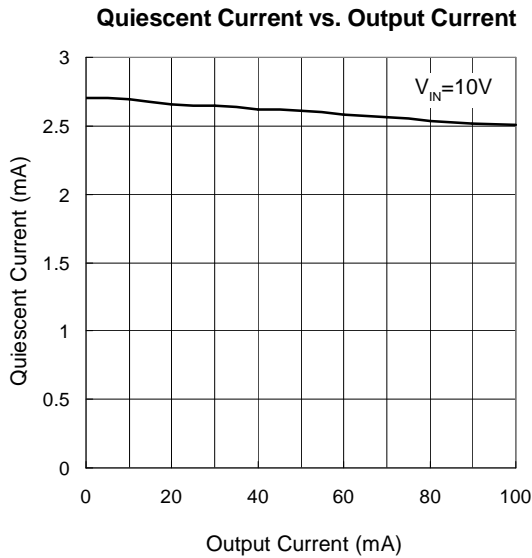
Quiescent Current vs. Ambient Temperature



Quiescent Current vs. Input Voltage

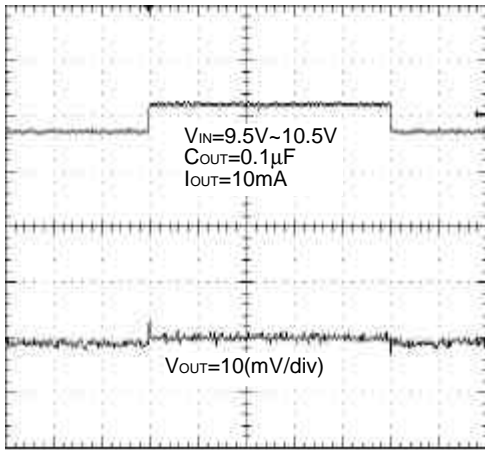


Typical Operating Characteristics (Cont.)



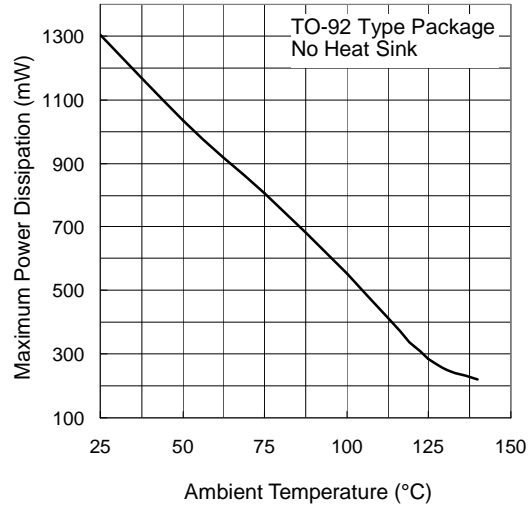
Typical Operating Characteristics (Cont.)

Line Transient Response

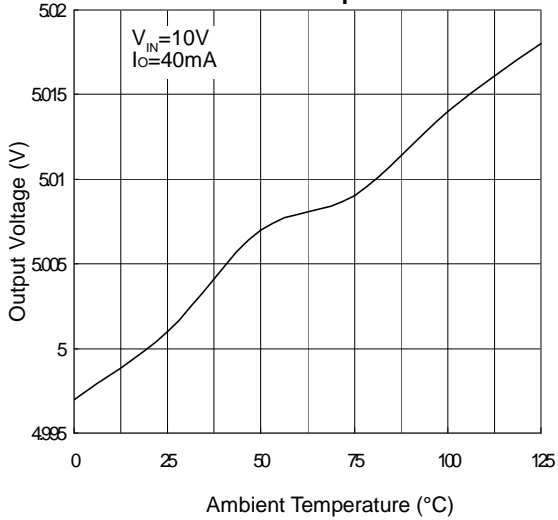


Time (100 $\mu s/div$)

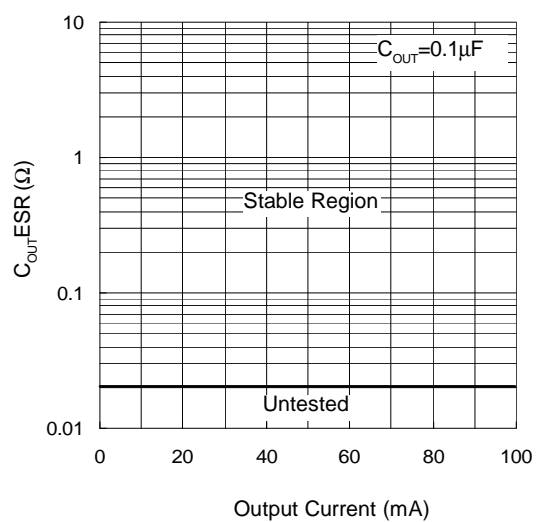
Maximum Power Dissipation vs. Ambient Temperature



Output Voltage vs. Ambient Temperature



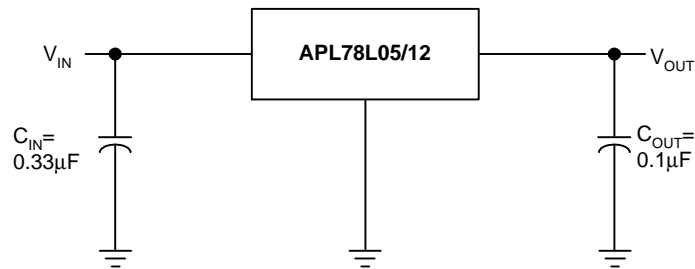
Region of Stable ESR vs. Output Current



Pin Description

PIN			NAME	FUNCTION
NO.				
SOP-8	TO-92	SOT-89		
1	1	1	V _{OUT}	Output Voltage Output Pin.
2,3,6,7	2	2	GND	Ground. A common ground is required between the input and the output voltage.
4,5	-	-	NC	No Internal Connection
8	3	3	V _{IN}	Power input pin of the device. The maximum Input Voltage can be 30V. It should be bypassed with a 0.33μF (minimum) capacitor to the GND.

Typical Application Circuit



Note

- a : A common ground is required between the input and the output voltage. The input voltage must remain typically 2V above the output voltage even during the low point on the input ripple voltage.
- b : C_{IN} is required if regulator is located an appreciable distance from power supply filter.
- c : C_{OUT} is not needed for stability; however, it improves transient response.

Application Information

The APL78L05/12, series of fixed voltage regulators, are designed with thermal overload protection that shuts down the circuit when subjected to an excessive power overload condition. In addition, the APL78L05/12 have the function of internal short circuit protection to limit the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input will be bypassed with a capacitor if the regulator connects to the power supply filter with long wire lengths, or if the output load capacitance is large. The input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. If the value of the capacitor is greater than 0.33μF, the capacitor with tantalum or mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

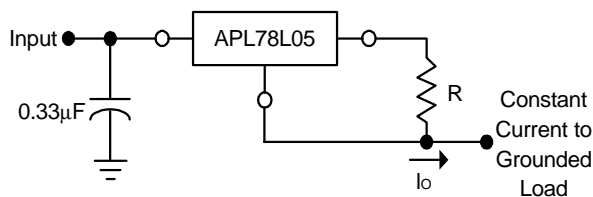


Figure 1. Current Regulator

The APL78L05 regulators can also be used as a current source when connected as above. In order to minimize dissipation, the APL78L05 is chosen in this application. Resistor R determines the current as below :

$$I_o = \frac{5.0V}{R} + I_b$$

$$I_b = 3.8mA \text{ over line and load changes}$$

For example, a 100mA current source would require R to be a 50Ω, 1/2W resistor and the output voltage compliance would be the input voltage less 7V.

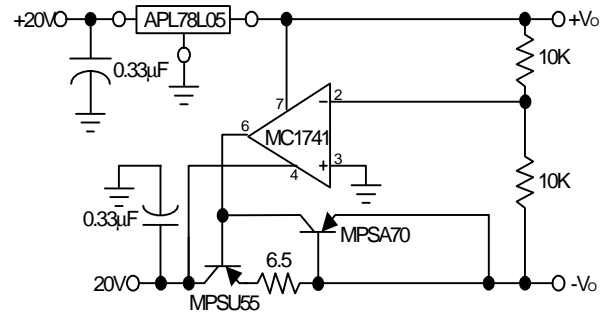


Figure 2. ±15V Tracking Voltage Regulator

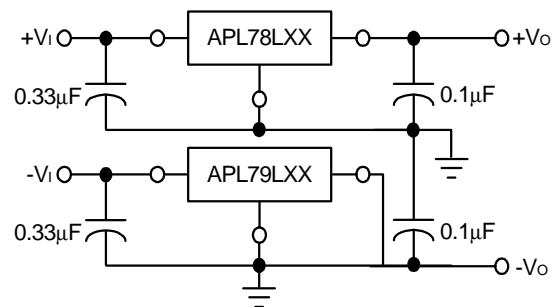
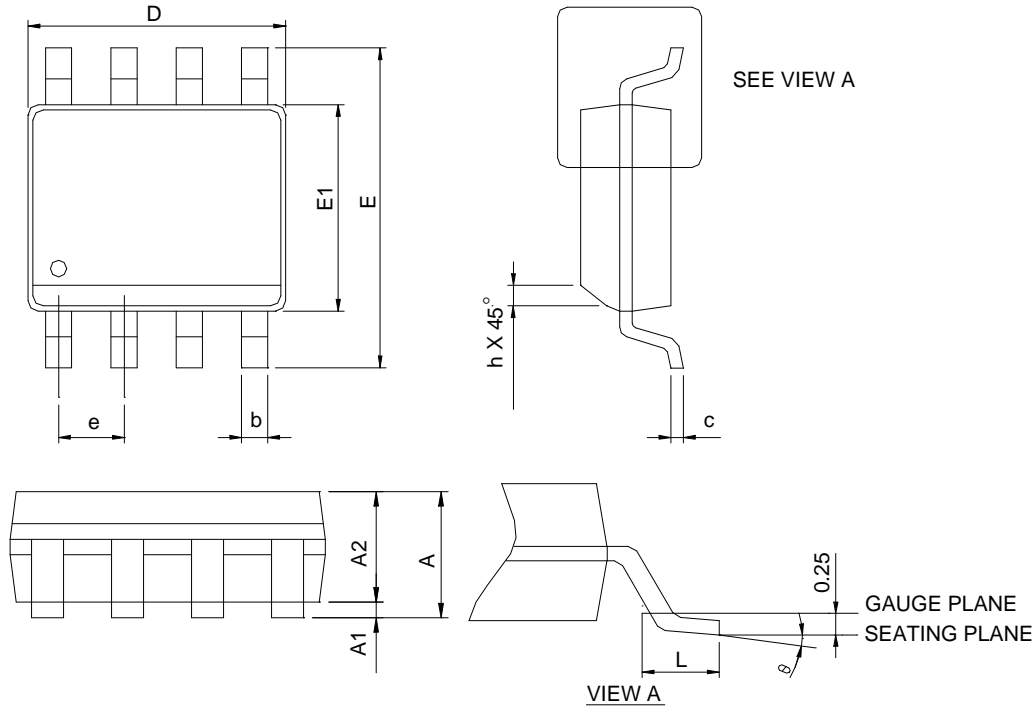


Figure 3. Positive and Negative Regulator

Package Information

SOP-8

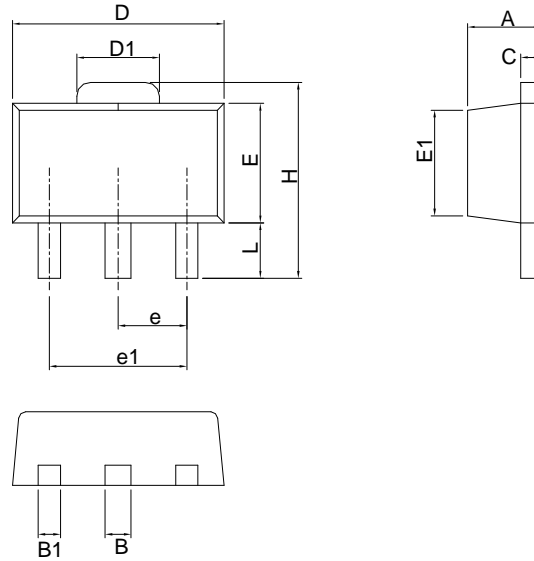


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

- Note: 1. Follow JEDEC MS-012 AA.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

SOT-89

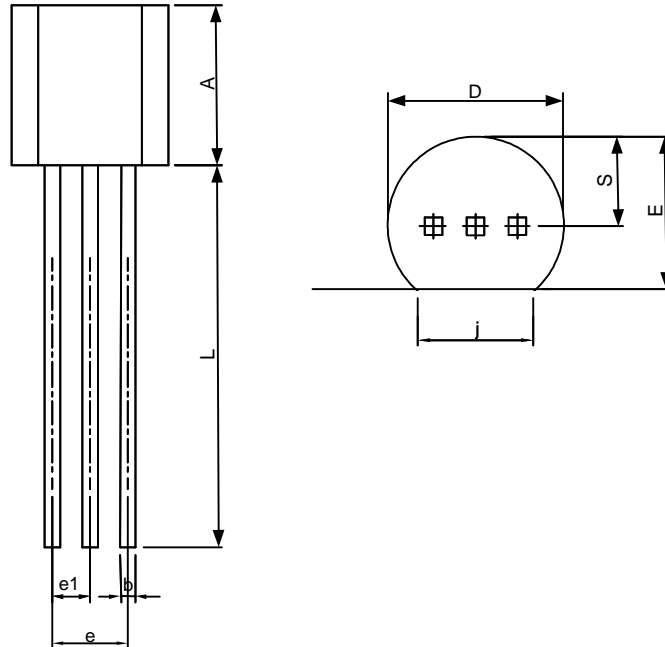


SYMBOL	SOT-89			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.40	1.60	0.055	0.063
B	0.44	0.56	0.017	0.022
B1	0.36	0.48	0.014	0.019
C	0.35	0.44	0.014	0.017
D	4.40	4.60	0.173	0.181
D1	1.62	1.83	0.064	0.072
E	2.29	2.60	0.090	0.102
E1	2.13	2.29	0.084	0.090
e	1.50 BSC		0.059 BSC	
e1	3.00 BSC		0.118 BSC	
H	3.94	4.25	0.155	0.167
L	0.89	1.20	0.035	0.047

Note : Follow JEDEC TO-243 AA.

Package Information

TO-92

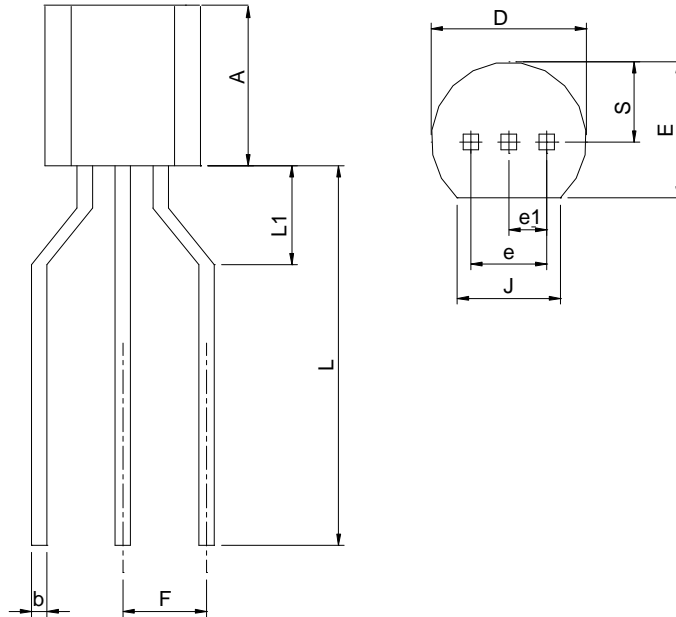


SYMBOL	TO-92			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.32	5.33	0.170	0.210
b	0.41	0.53	0.016	0.021
D	4.45	5.20	0.175	0.205
E	3.18	4.19	0.125	0.165
e	2.42	2.66	0.095	0.105
e1	1.15	1.39	0.045	0.055
j	3.43	4.00	0.135	0.157
L	12.70	15.00	0.500	0.591
S	2.03	2.66	0.080	0.105

Note : Follow JEDEC TO-92.

Package Information

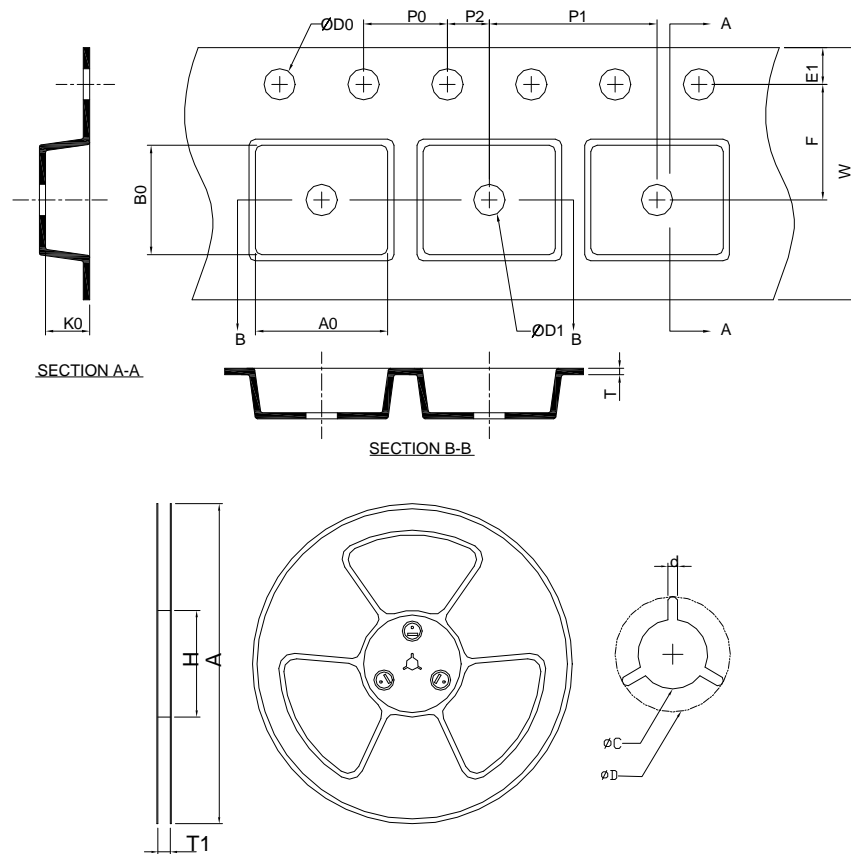
TO-92A



SYMBOL	TO-92A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.32	5.33	0.170	0.210
b	0.41	0.53	0.016	0.021
D	4.45	5.20	0.175	0.205
E	3.18	4.19	0.125	0.165
F	2.50	2.80	0.098	0.110
e	2.42	2.66	0.095	0.105
e1	1.15	1.39	0.045	0.055
J	3.34	4.00	0.135	0.157
L	12.70		0.500	
L1	1.70	3.30	0.067	0.130
S	2.03	2.66	0.080	0.105

Note : Follow JEDEC TO-92A

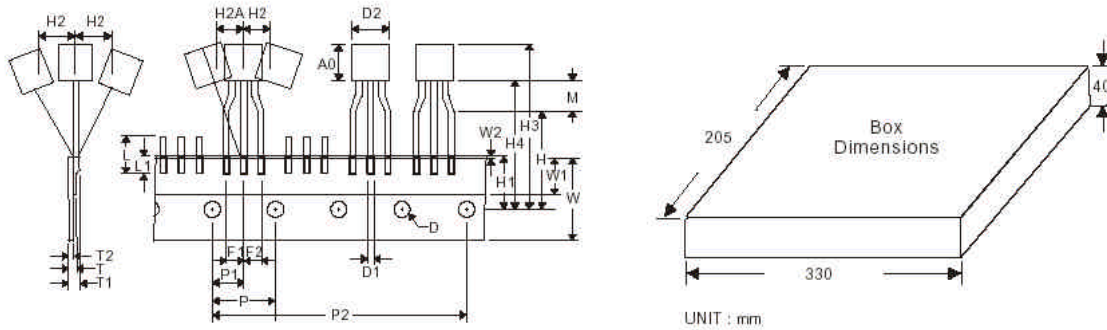
Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0 ±0.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40 ±0.20	5.20 ±0.20	2.10 ±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOT-89	178.0 ±0.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.50 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.80 ±0.20	4.50 ±0.20	1.80 ±0.20

(mm)

Carrier Tape & Box Dimensions



Application	A0	D	D1	D2	F1=F2	F1-F2	M	H	H1
TO-92A	4.32~5.33	4.0 ±0.2	0.36~0.53	4.45~5.20	2.5+0.2 -0.1	±0.3	1.7~3.3	16 ±0.5	9 ±0.5
	H2	H2A	H3	H4	H5=H0+M	L	L1	P	P1
	0.5 MAX	0.5 MAX	27.0 MAX	20.0 MAX	18.5 ±0.5	11.0 MAX	2.5 MIN	12.7 ±0.3	6.35 ±0.4
	P2	T	T1	T2	W	W1	W2	W	W1
	50.8 ±0.5	0.55 MAX	1.42 MAX	0.36~0.68	18.0 ±0.2	6.0 ±0.2	1	18.0 ±0.2	6.0 ±0.2

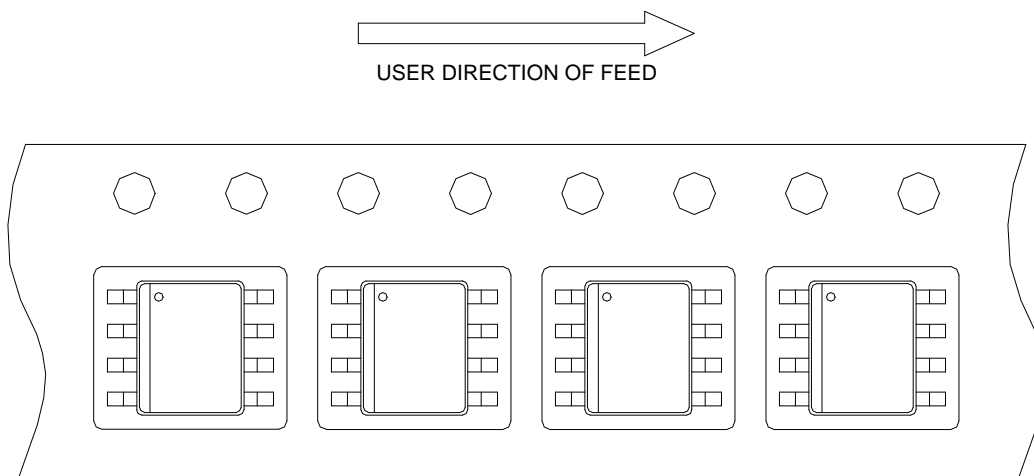
(mm)

Devices Per Unit

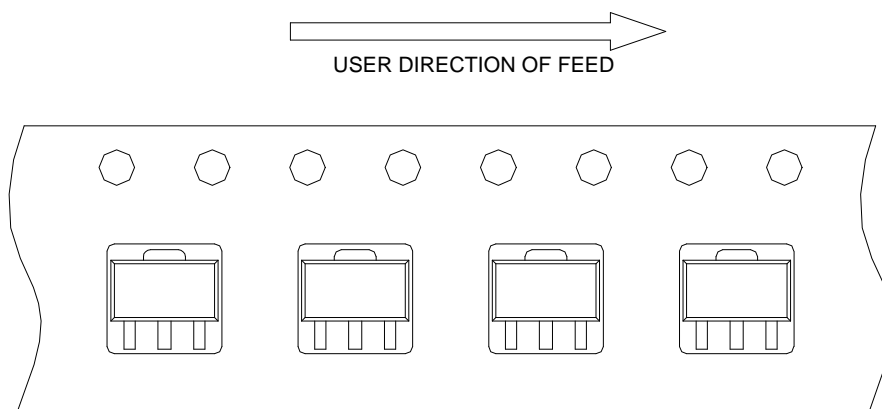
Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500
SOT-89	Tape & Reel	1000
TO-92A	Tape & Box	2000
TO-92	Plastic & Box	1000

Taping Direction Information

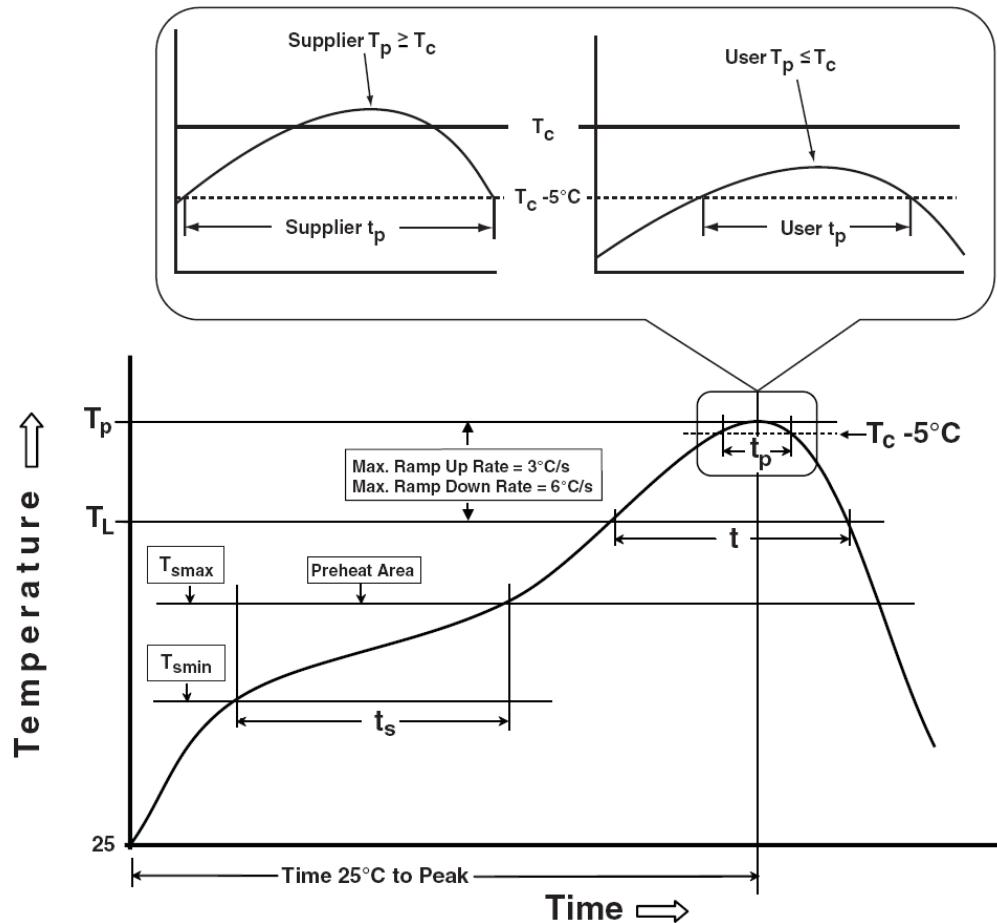
SOP-8



SOT-89



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T _j =125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM 2KV
MM	JESD-22, A115	VMM 200V
Latch-Up	JESD 78	10ms, 1 _{tr} 100mA

Customer Service

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