AN4106
Application note

EVLVIP26L-12WFN: 12 V/12 W, 60 kHz non-isolated flyback

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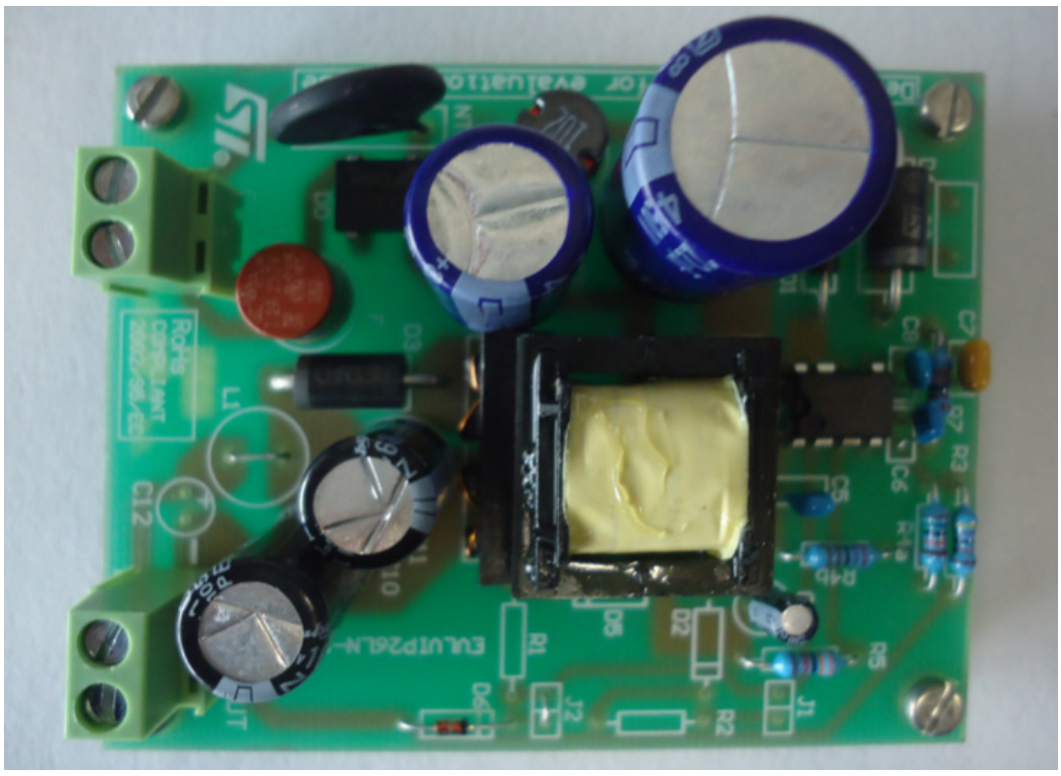
Introduction

This document describes a 12 V-1 A power supply set in non-isolated flyback topology with the VIPER26, a new offline high-voltage converter by STMicroelectronics.

The features of the device include an 800 V avalanche rugged power section, PWM operation at 60 kHz with frequency jittering for lower EMI, current limiting with adjustable set point, onboard soft-start, a safe auto-restart after a fault condition and low standby power.

The available protection includes thermal shutdown with hysteresis, delayed overload protection, and open loop failure protection. All protection is auto-restart mode.

Figure 1. EVLVIP26L-12WFN demonstration board



EVLVIP26L-12WFN

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1 Adapter features

The electrical specifications of the demonstration board are listed in *Table 1*.

Table 1. Electrical specifications

Symbol	Parameter	Value
V_{IN}	Input voltage range	90 V_{AC} - 265 V_{AC}
V_{OUT}	Output voltage	12 V
I_{OUT}	Max. output current	1 A
Δ_{VOUT_LF}	Precision of output regulation	± 5%
Δ_{VOUT_HF}	High frequency output voltage ripple	50 mV
T_{AMB}	Max. ambient operating temperature	60 ºC

2 Circuit description

The power supply is set in flyback topology. The complete schematic is given in *Figure 2*; a simplified schematic for V_{OUT} ≥12 V and the relevant BOM are given in *Figure 3* and in *Table 2* respectively. The input section includes a resistor R1 and an NTC for inrush current limiting, a diode bridge (D0) and a Pi filter for EMC suppression (C1, L2, C2). The transformer core is a standard E20. A Transil™ clamp network (D1, D4) is used for leakage inductance demagnetization. The output voltage value is set in a simple way through the R3-R4 voltage divider between the output terminal and the FB pin, according to the following formula:

Equation 1

$$V_{OUT} = 3.3V \cdot \left(1 + \frac{R3}{R4}\right)$$

In fact, the FB pin is the input of an error amplifier and is an accurate 3.3 V voltage reference. In the schematic the resistor R4 has been split into R4a and R4b in order to allow better tuning of the output voltage value. The compensation network is connected between the COMP pin (which is the output of the error amplifier) and the GND pin and is made up of C7, C8 and R7. The output rectifier D3 has been selected according to the calculated maximum reverse voltage, forward voltage drop and power dissipation and is a power Schottky type. A resistor has been connected between the LIM and GND pins in order to reduce the IDLIM to the value needed to supply the required output power, limiting the stress on the power components.

At power-up the DRAIN pin supplies the internal HV startup current generator which charges the VDD capacitor, C4, up to V_{DDon}. At this point the Power MOSFET starts switching, the generator is turned off and the IC is powered by the energy stored in C4. If the nominal value of V_{OUT} exceeds the V_{DDcson} threshold of the VIPER26 by a small signal diode forward voltage drop, the IC can be supplied directly from the output selecting jumper J2 in *Figure 2*. In this case jumper J1 is open because the auxiliary winding of the transformer is not needed and the schematic can be simplified, as in *Figure 3*. Since $V_{DDcsonmax}$ = 11.5 V, the minimum value of V_{OUT} allowing this connection is 12 V. If V_{OUT} < 12 V, the VIPER26 must be supplied through the auxiliary winding of the transformer (J1 selected, J2 open in *Figure 2*), delivering to the V_{DD} pin a voltage higher than V_{DDcson}. The voltage generated by the auxiliary winding increases with the load on the regulated output. An external clamp (D5, R1) can be added in this case, in order to avoid the V_{DD} operating range being exceeded.

The figures and measurements in this document refer to a case in which V_{DD} is supplied from the output, i.e. to the simplified schematic shown in *Figure 3*.

Figure 2. Application schematic - complete

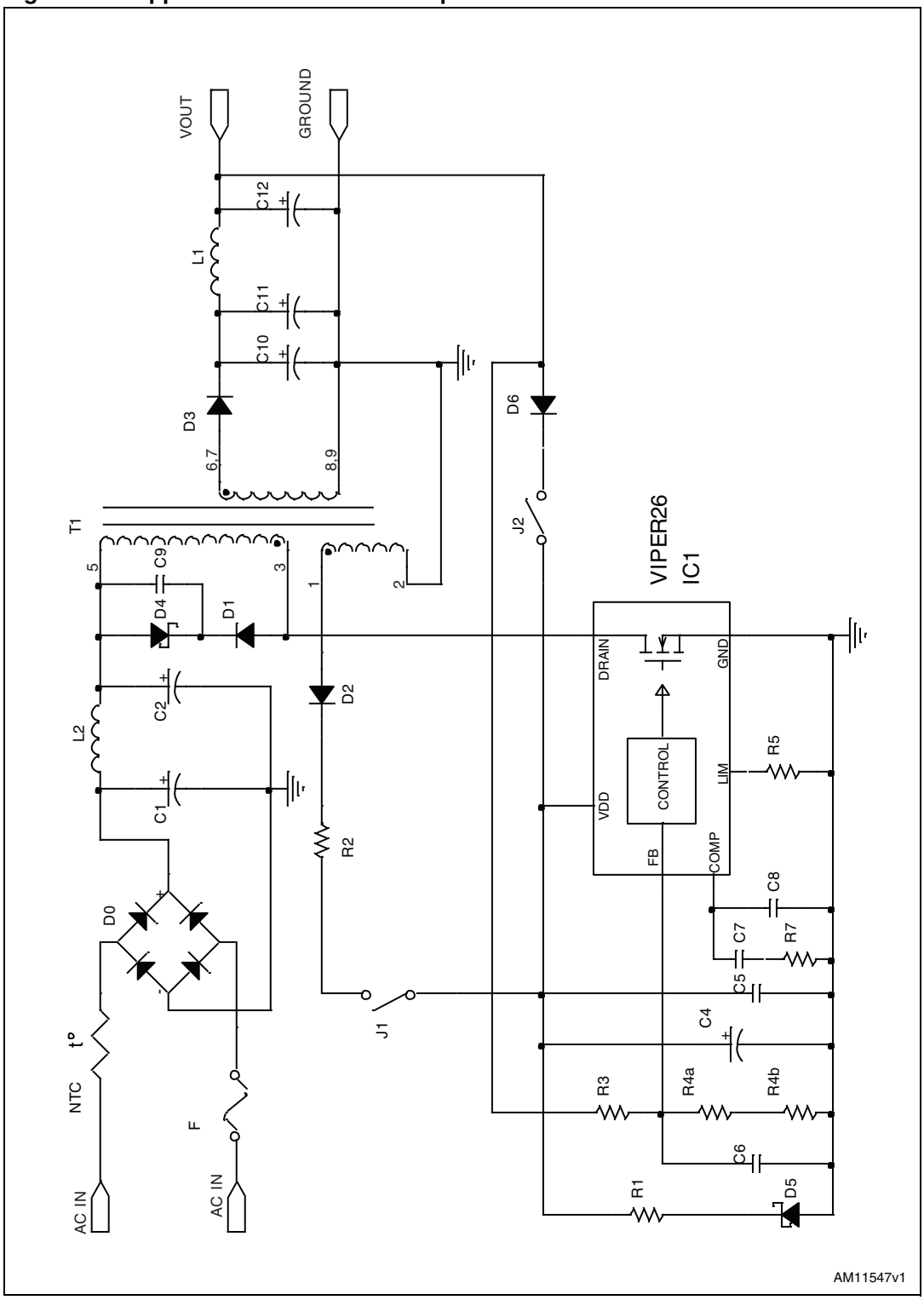
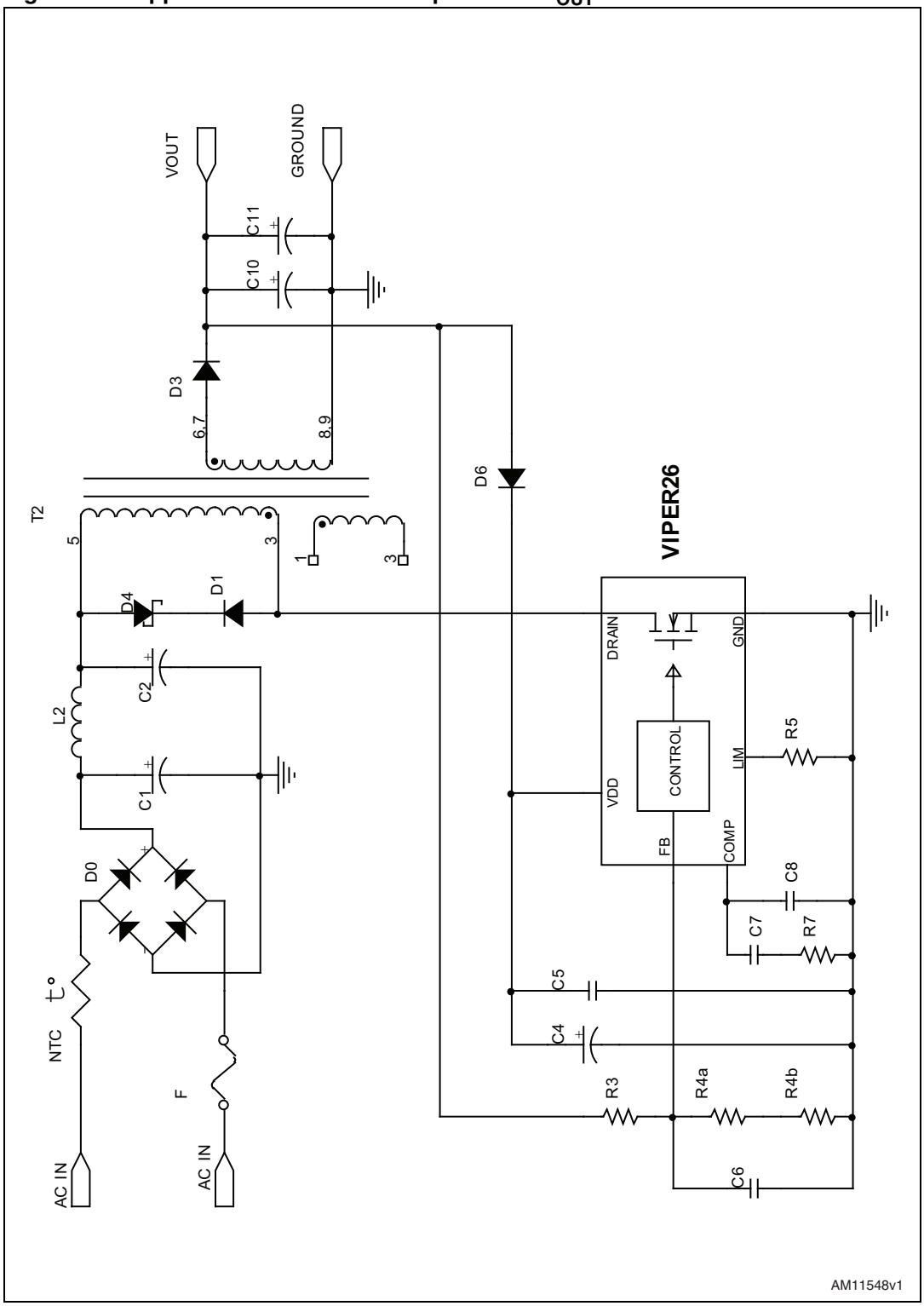


Figure 3. Application schematic - simplified for $V_{OUT} \geq 12$ V



3 Bill of material

Table 2. Bill of material (simplified schematic)

Reference	Part	Description	Manufacturer
NTC	2.2 Ω NTC	NTC thermistor	EPCOS
F	T2A 250V	2 A, 250 V_{AC} fuse, TR5 series	Wickmann
C1		10 µF, 400 V NHG series electrolytic capacitor	Panasonic
C2		22 µF, 35 V SMG series electrolytic capacitor	Panasonic
C4		2.2 µF, 63 V electrolytic capacitor	
C5		100 nF, 50 V ceramic capacitor	
C6		1 nF, 50 V ceramic capacitor	
C7		47 nF, 50 V ceramic capacitor	
C8		2.2 nF, 50 V ceramic capacitor	
C9	Not mounted		
C10		1000 µF, 16 V ultra low ESR electrolytic capacitor ZL series	Rubycon
C11		680 µF, 16 V ultra low ESR electrolytic capacitor ZL series	Rubycon
C12	Not mounted		
D0	DF06M	1 A - 600 V diode bridge	Vishay
D1	STTH1L06	1 A - 600 V ultrafast diode	ST
D2	Not mounted		
D3	STPS3150	3 A-150 V power Schottky (output diode)	ST
D4	1.5KE300A	Transil	ST
D5	Not mounted		
D6	1N4148	Small signal diode	Fairchild
R1	Not mounted		
R2	Not mounted		
R3		47k Ω 1% 1/4 W resistor	
R4a		15k Ω 1% 1/4 W resistor	
R4b		2.7k Ω 1% 1/4 W resistor	
R5		33k Ω 1/4 W resistor	
R7		3.3k Ω 1/4 W resistor	
L1	Short-circuit		

Table 2. Bill of material (simplified schematic) (continued)

Reference	Part	Description	Manufacturer
L2	RFB0807-102	Input filter inductor (L=1 mH, I_{SAT}=0.3 A; DCR_{max}=3.4 Ω)	Coilcraft
T1	1715.0049	60 kHz switch mode transformer	Magnetica
IC1	VIPER26LN	High-voltage 60 kHz PWM	ST
J1	Not mounted	Jumper	
J2	Short-circuit	Jumper	

4 Transformer

The characteristics of the transformer are listed in the table below:

Table 3. Transformer characteristics

Parameter	Value	Test conditions
Manufacturer	Magnetica	
Part number	1715.0049	
Primary inductance	1.6 mH ±15%	Measured at 1 kHz, T_{AMB} = 20 °C
Leakage inductance	0.74%	Measured at 10 kHz, T_{AMB} = 20 °C
Primary to secondary turn ratio (3 - 5)/(6,7- 8,9)	5.89 ± 5%	Measured at 10 kHz, T_{AMB} = 20 °C
Primary to auxiliary turn ratio (3 - 5)/(1 - 2)	5.89 ± 5%	Measured at 10 kHz, T_{AMB} = 20 °C

The figures below show electrical diagram, size and pin distances (in mm) of the transformer.

Figure 4. Transformer size and pin diagram, bottom view

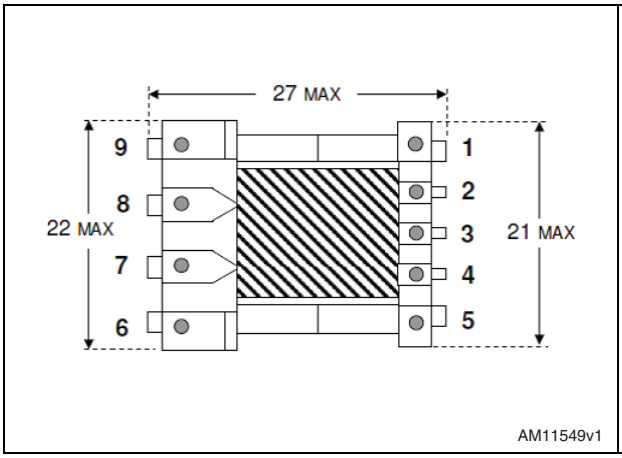


Figure 5. Transformer size, side view

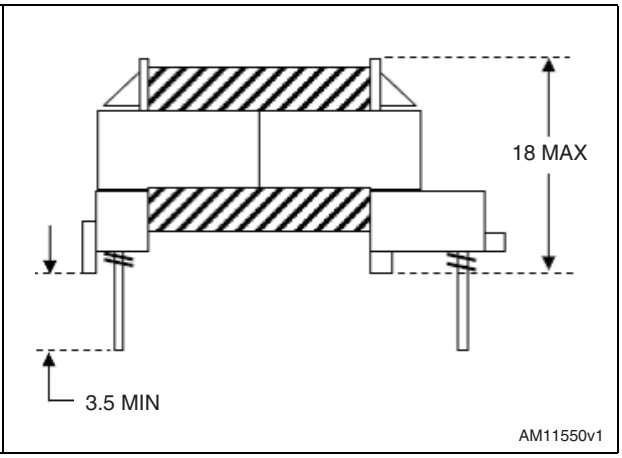


Figure 6. Transformer, pin distances

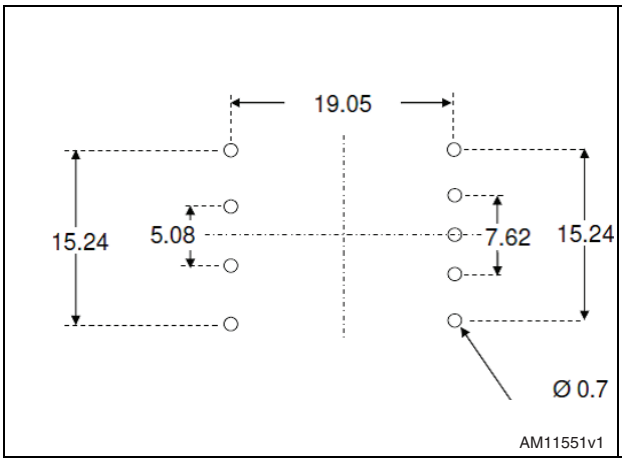
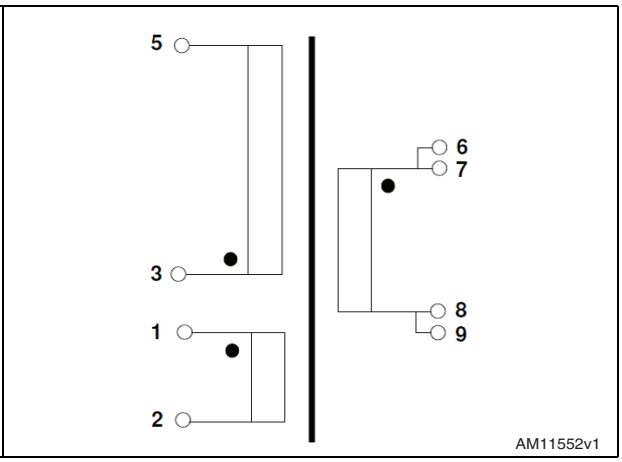


Figure 7. Transformer, electrical diagram



5 Testing the board

5.1 Typical waveforms

Drain voltage and current waveforms in full load condition are shown for the two nominal input voltages in *Figure 8* and *9*, and for minimum and maximum input voltage in *Figure 10* and *11* respectively.

Figure 8. Drain current and voltage at V_{IN} = 115 V_{AC}, full load

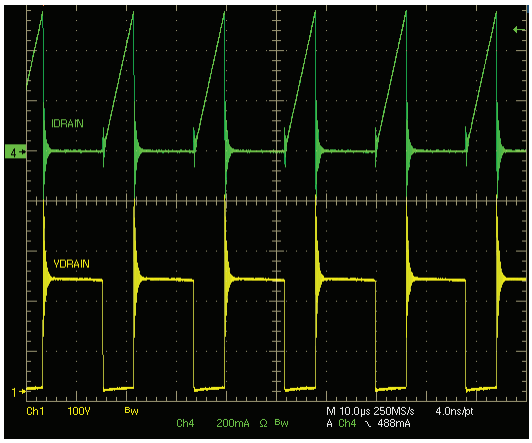


Figure 9. Drain current and voltage at V_{IN} = 230 V_{AC}, full load

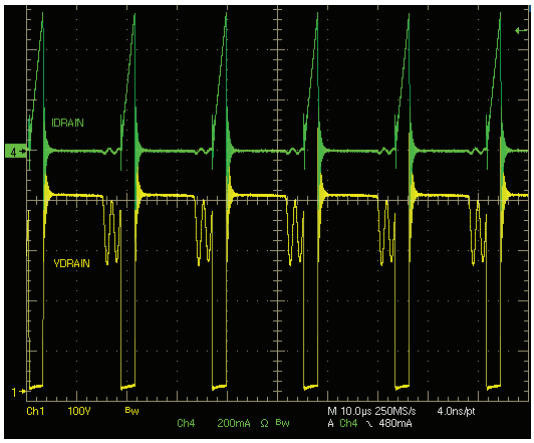


Figure 10. Drain current and voltage at V_{IN} = 90 V_{AC}, full load

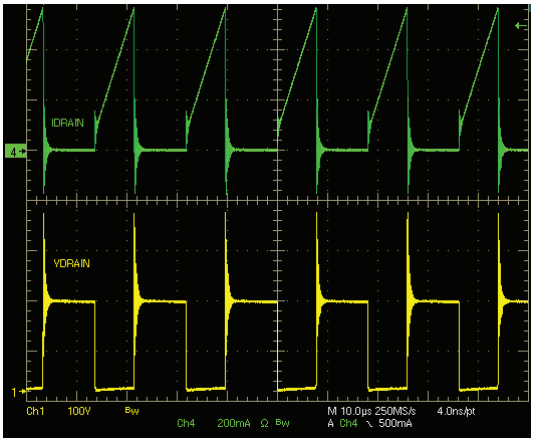
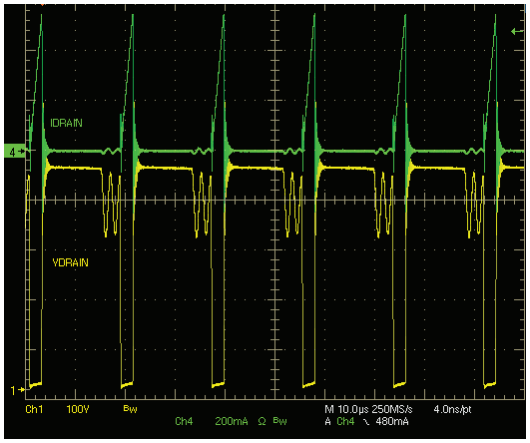


Figure 11. Drain current and voltage at V_{IN} = 265 V_{AC}, full load



6 Line/load regulation and output voltage ripple

The output voltage of the board has been measured in different line and load condition. The results are shown in *Table 4*. The output voltage is practically not affected by the line condition.

Table 4. Output voltage line-load regulation

V_{IN} [V_{AC}]	V_{OUT}			
	No load	50% load	75% load	100% load
90	12.18	12.16	12.17	12.19
115	12.18	12.17	12.17	12.19
150	12.18	12.17	12.18	12.18
180	12.18	12.17	12.18	12.18
230	12.18	12.18	12.18	12.17
265	12.18	12.18	12.18	12.18

Figure 12. Line regulation

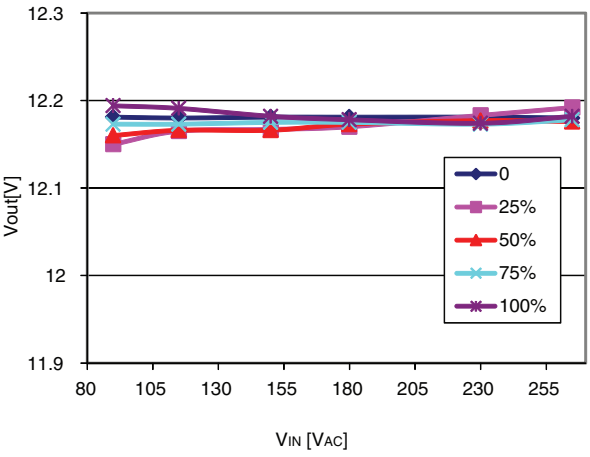
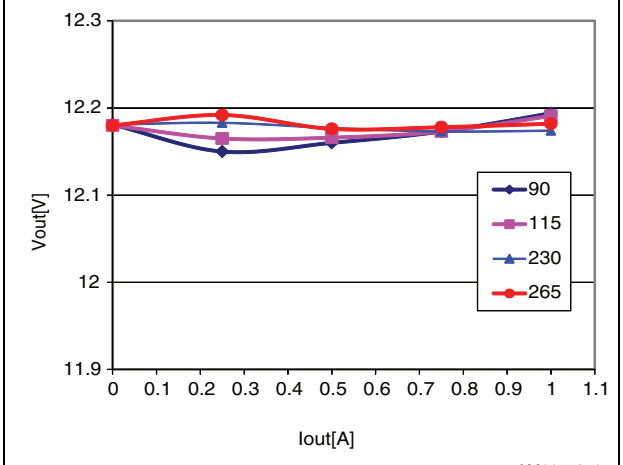


Figure 13. Load regulation



The ripple at the switching frequency superimposed at the output voltage has also been measured and the results are reported in *Table 5*.

Table 5. Output voltage ripple at half and full load

V_{IN} [V_{AC}]	V_{OUT} (mV)	
	Half load	Full load
90	17	23
115	16	21
230	18	25
265	17	24

Figure 14. Output voltage ripple at V_{IN} = 115 V_{AC}, full load

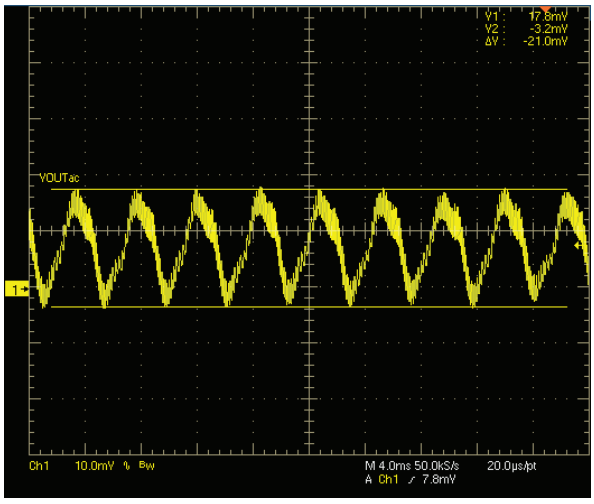
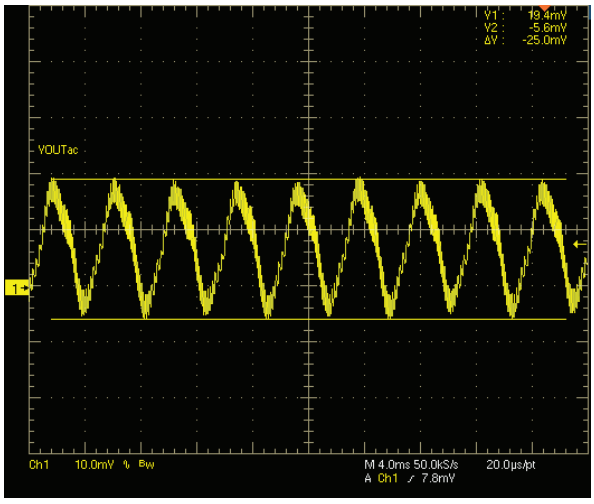


Figure 15. Output voltage ripple at V_{IN} = 230 V_{AC}, full load



7 Burst mode and output voltage ripple

When the converter is lightly loaded, the COMP pin voltage decreases. As it reaches the shutdown threshold, V_{COMPL} (1.1 V, typical), the switching is disabled and no more energy is transferred to the secondary side. So, the output voltage decreases and the regulation loop makes the COMP pin voltage increase again. As it rises 40 mV above the V_{COMPL} threshold, the normal switching operation is resumed. This results in a controlled on/off operation (referred to as “burst mode”) as long as the output power is so low that it requires a turn-on time lower than the minimum turn-on time of the VIPER26. This mode of operation keeps the frequency-related losses low when the load is very light or disconnected, making it easier to comply with energy-saving regulations. The figures below show the output voltage ripple when the converter is no/lightly loaded and supplied with 115 V_{AC} and with 230 V_{AC} respectively.

Figure 16. Output voltage ripple at V_{IN} = 115 V_{AC}, no load

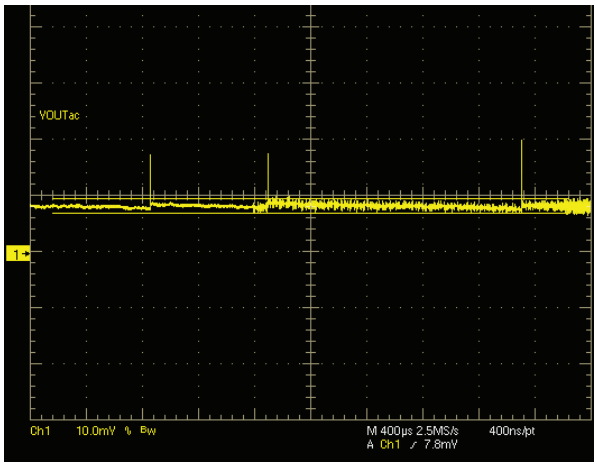


Figure 17. Output voltage ripple at V_{IN} = 230 V_{AC}, no load

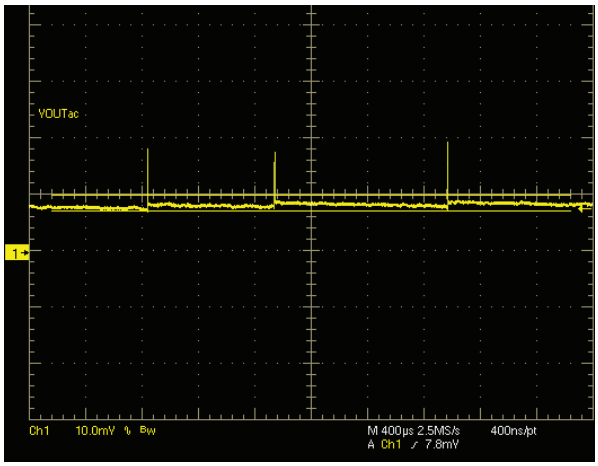


Figure 18. Output voltage ripple at V_{IN} = 115 V_{AC}, I_{OUT} = 25 mA

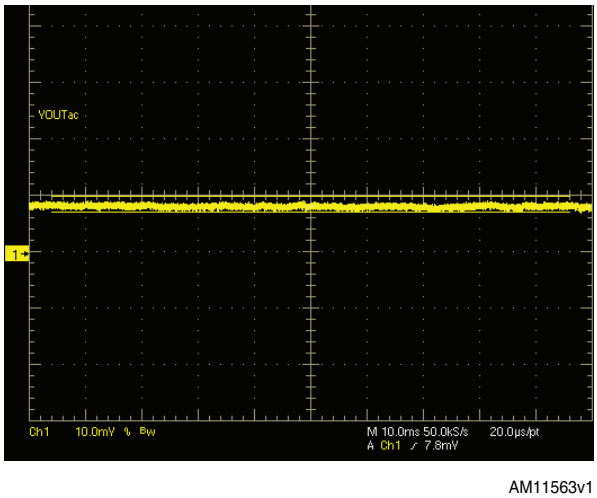


Figure 19. Output voltage ripple at V_{IN} = 230 V_{AC}, I_{OUT} = 25 mA

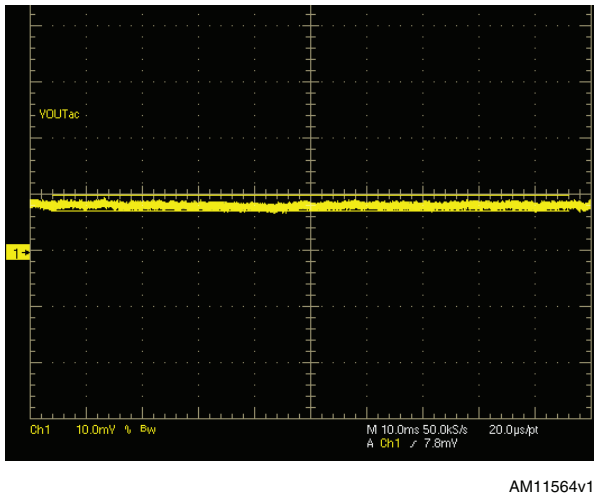


Table 6 shows the measured value of the burst mode frequency ripple measured in different operating conditions. The ripple in burst mode operation is very low.

Table 6. Output voltage ripple at no/light load

V_{IN} [V_{AC}]	V_{OUT} [mV]	
	No load	25 mA load
90	2	3
115	2	3
230	2	4
265	3	4

8 Efficiency

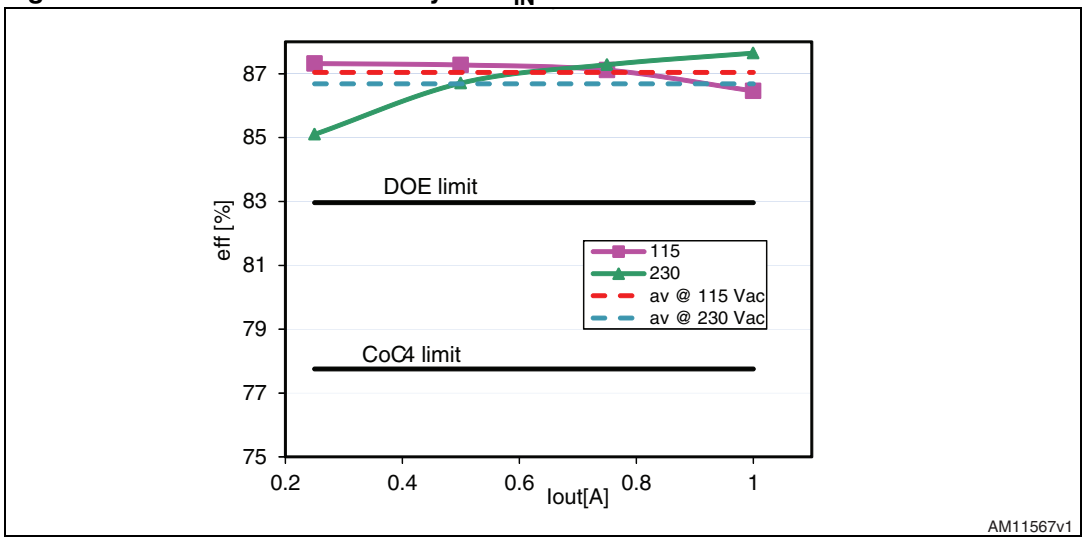
The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltage (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}).

External power supplies (the power supplies which are contained in a separate housing from the end-use devices they are powering) need to comply with the Code of Conduct, version 4 "Active mode efficiency" criterion, which states an active mode efficiency higher than 77.7% for a power throughput of 12 W.

Another standard to be applied to external power supplies in the coming years is the DOE (Department of energy) recommendation, whose active mode efficiency requirement for the same power throughput is 82.96%.

The presented demonstration board is compliant with both standards, as can be seen from Figure 20, where the average efficiencies of the board at 115 V_{AC} (87%) and at 230 V_{AC} (86.7%) are plotted with dotted lines, together with the above limits. In the same figure the efficiency at 25%, 50%, 75% and 100% of load for both input voltages is also shown.

Figure 20. Active mode efficiency vs. V_{IN}



9 Light load performance

The input power of the converter has been measured in no load condition for different input voltages and the results are reported in *Table 7*.

Table 7. No load input power

V_{IN} [V_{AC}]	P_{IN} [mW]
90	12.8
115	13.6
150	15.0
180	16.6
230	19.9
265	22.9

In version 2.0 of the Code of Conduct, version 4 program the power consumption of the power supply when it is not loaded is also considered. The criteria for compliance are given in the table below:

Table 8. Energy consumption criteria for no load

Nameplate output power (Pno)	Maximum power in no load for AC-DC EPS
0 W ≤P_{no} ≤50 W	< 0.3 W
50 W < P_{no} < 250 W	< 0.5 W

The power consumption of the presented board is about ten times lower than the Code of Conduct, version 4 limit. Even if this performance seems to be disproportionally better than the requirements, it is worth noting that often AC-DC adapter or battery charger manufacturers have very strict requirements about no load consumption and when the converter is used as an auxiliary power supply, the line filter is often the main line filter of the entire power supply which considerably increases standby consumption.

Even if the Code of Conduct, version 4 program does not have other requirements regarding light load performance, in order to give more information the input power and efficiency of the demonstration board also in two other light load cases is shown. *Table 9* and *Table 10* show the performances when the output load is 25 mW and 50 mW respectively.

Table 9. Light load performance at P_{OUT} = 25 mW

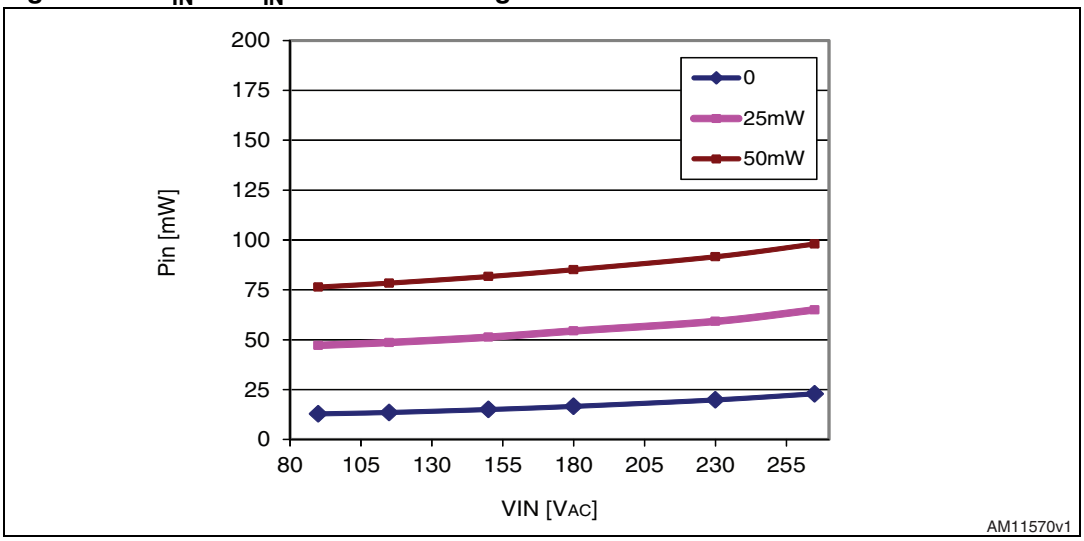
V_{IN} [V_{AC}]	P_{OUT} [mW]	P_{IN} [mW]	Efficiency (%)
90	25	47.2	53.0
115	25	48.7	51.4
150	25	51.2	48.7
180	25	54.4	45.9
230	25	59.2	42.2
265	25	65.0	38.5

Table 10. Light load performance at P_{OUT} = 50 mW

V_{IN} [V_{AC}]	P_{OUT} [mW]	P_{IN} [mW]	Efficiency (%)
90	50	76.4	65.4
115	50	78.4	63.8
150	50	81.7	61.2
180	50	85.1	58.7
230	50	91.6	54.6
265	50	98.0	51.0

The input power vs. input voltage for no load and light load condition (*Table 7*, *9* and *10*) are shown in the figure below.

Figure 21. P_{IN} vs. V_{IN} at no load and light load



Depending on the equipment supplied, it's possible to have several criteria to measure the standby or light load performance of a converter. One criterion is the measurement of the output power when the input power is equal to one watt. In *Table 11* the output power needed to have 1 W of input power in different line conditions is given. *Figure 22* shows the output power corresponding to P_{IN} = 1 W for different values of the input voltage.

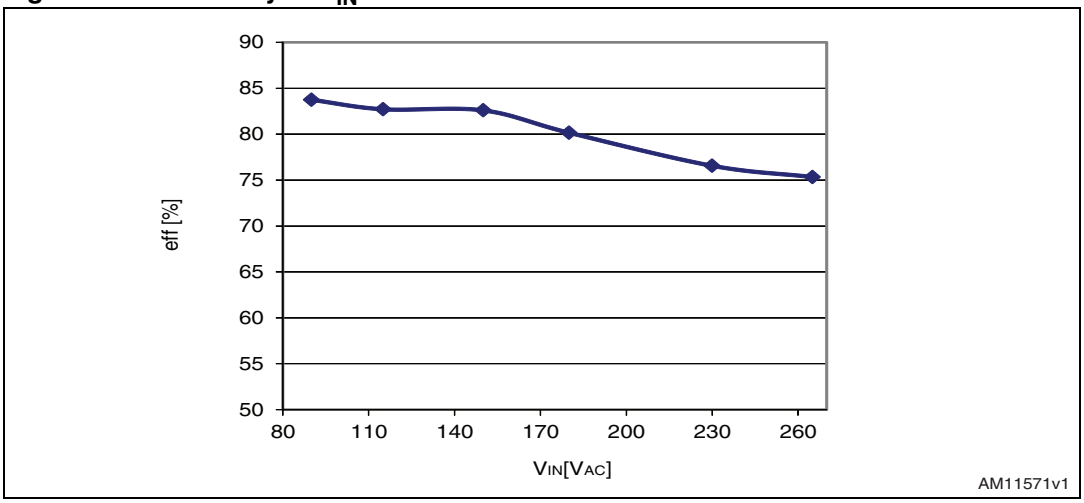
Table 11. P_{OUT} @ P_{IN} = 1 W

V_{IN} [V_{AC}]	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
90	1	0.837	83.7
115	1	0.827	82.7
150	1	0.826	82.6

Table 11. P_{OUT} @ P_{IN} = 1 W

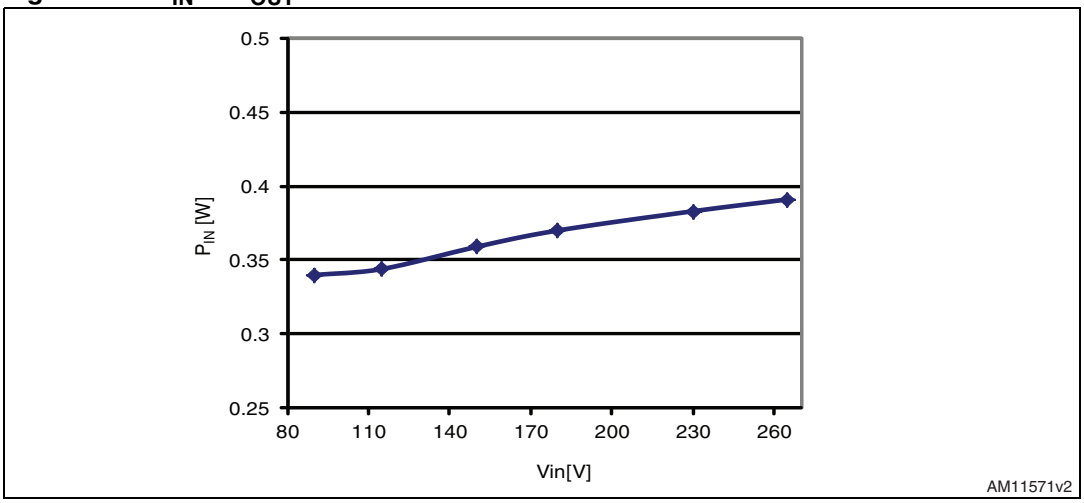
V_{IN} [V_{AC}]	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
180	1	0.801	80.1
230	1	0.766	76.6
265	1	0.753	75.3

Figure 22. Efficiency at P_{IN} = 1 W



Another requirement (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded with 250 mW. The converter can satisfy even this requirement, as shown in *Figure 23*.

Figure 23. P_{IN} at P_{OUT} = 0.25 W



10 Functional check

10.1 Soft-start

At startup the current limitation value reaches IDLIM after an internally set time, t_{SS}, whose typical value is 8.5 msec. This time is divided into 16 time intervals, each corresponding to a current limitation step progressively increasing. In this way the drain current is limited during the output voltage increase, therefore reducing the stress on the secondary diode. The soft-start phase is shown in *Figure 24* and *25*.

Figure 24. Soft-start at startup

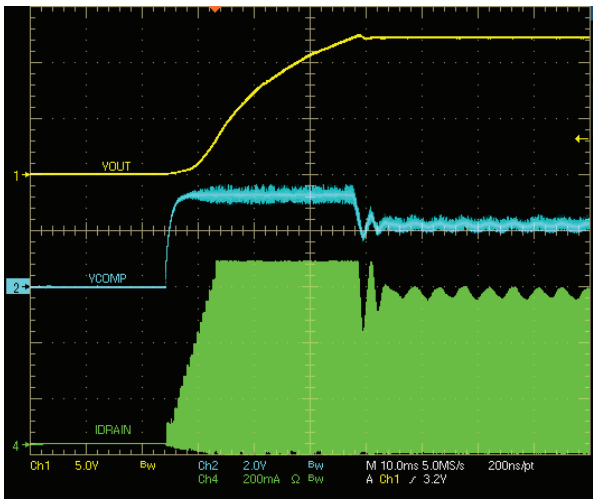
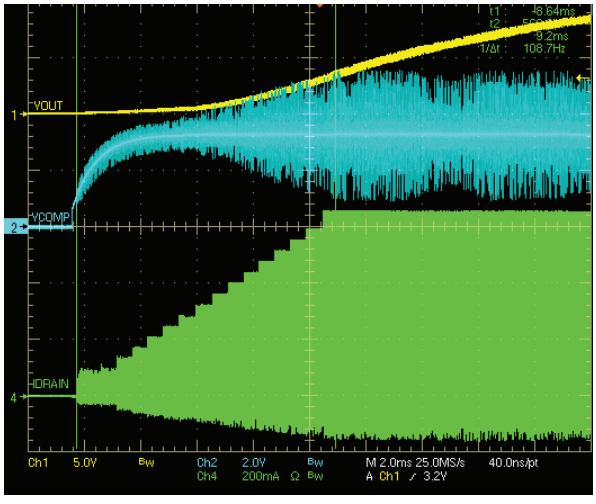


Figure 25. Soft-start at startup (zoom)



10.2 Overload protection

In case of overload or short-circuit (see *Figure 26*), the drain current reaches the IDLIM value (or the one set by the user through the RLIM resistor). Every cycle that this condition is met, a counter is incremented. If the fault is maintained continuously for the time t_{OVL} (50 msec typical, set internally), the overload protection is tripped, the power section is turned off and the converter is disabled for a $t_{RESTART}$ time (1 s typical). After this time has elapsed, the IC resumes switching and, if the short is still present, the protection occurs indefinitely in the same way (*Figure 27*). This ensures restart attempts of the converter with low repetition rate, so that it works safely with extremely low power throughput and avoids overheating of the IC in case of repeated overload events.

Moreover, every time the protection is tripped, the internal soft-start function (*Figure 25*) is invoked, in order to reduce the stress on the secondary diode.

After the short removal, the IC resumes working normally. If the short is removed during t_{SS} or t_{OVL}, i.e. before the protection tripping, the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short-circuit is removed during $t_{RESTART}$, the IC waits for the $t_{RESTART}$ period to elapse before resuming switching (*Figure 29*).

Figure 26. Output short-circuit applied: OLP tripping

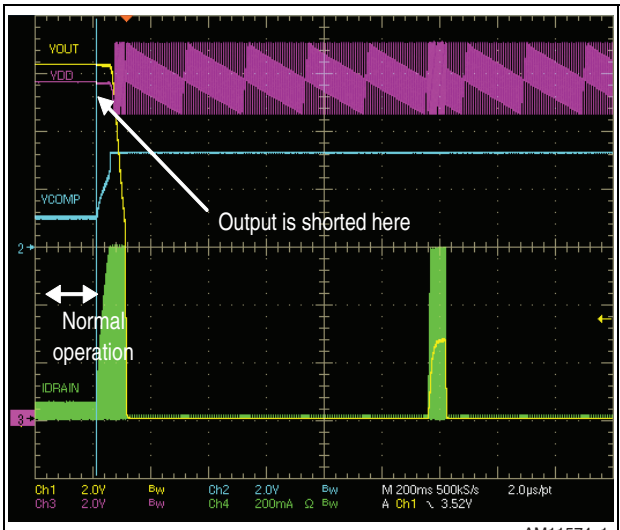


Figure 27. Output short-circuit maintained: OLP steady-state

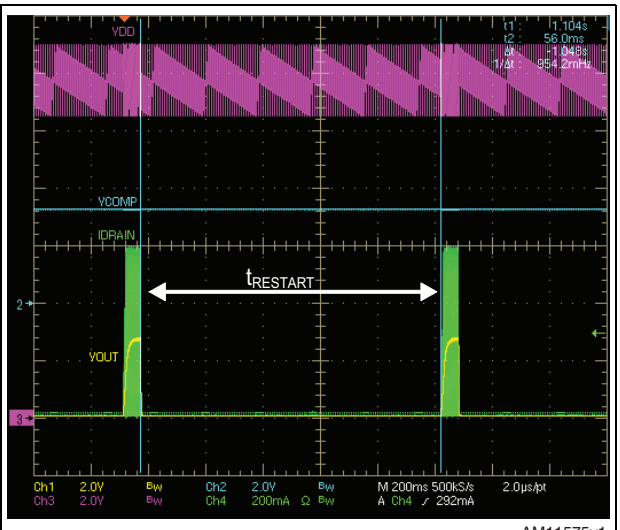


Figure 28. Output short-circuit maintained: OLP steady-state, zoom

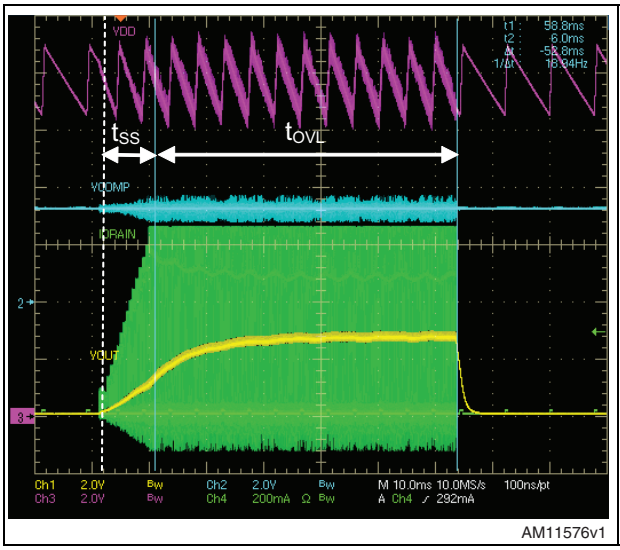
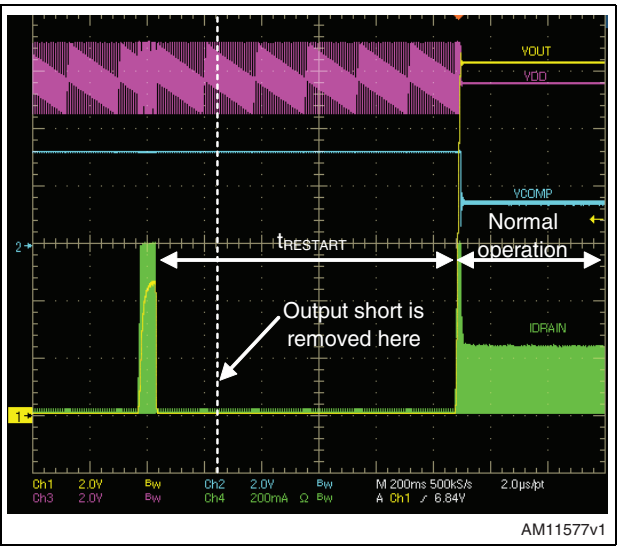


Figure 29. Output short-circuit removal and converter restart



10.3 Feedback loop failure protection

As the loop is broken (R4 = R4a+R4b shorted or R3 open), the output voltage V_{OUT} increases and the VIPER26 runs at its maximum current limitation. The V_{DD} pin voltage increases as well, because it is linked to the V_{OUT} voltage either directly or through the auxiliary winding, depending on the cases.

If the V_{DD} voltage reaches the $V_{DDclamp}$ threshold (23.5 V min.) in less than 50 msec, the IC is shut down by open loop failure protection (see *Figure 30* and *31*), otherwise by OLP, as described in the previous section. The breaking of the loop has been simulated by shorting the low-side resistor of the output voltage divider, R4 = R4a+R4b. The same behavior can be induced opening the high-side resistor, R3.

The protection acts in auto-restart mode with $t_{RESTART}$ = 1 s (*Figure 31*). As the fault is removed, normal operation is restored after the last $t_{RESTART}$ interval has been completed (*Figure 33*).

Figure 30. Feedback loop failure protection: tripping

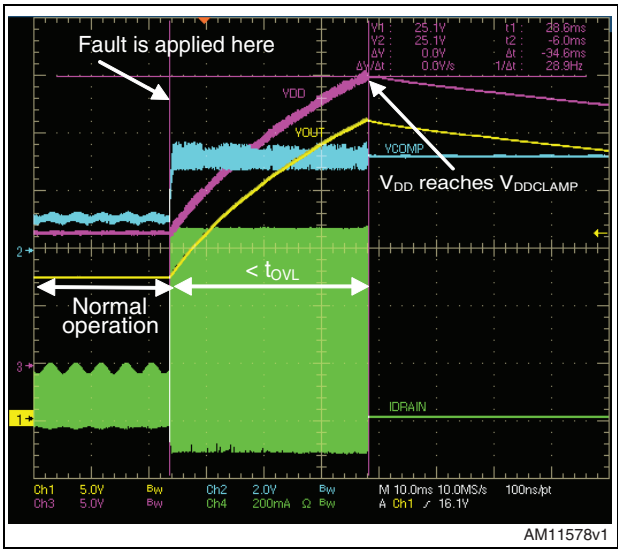


Figure 31. Feedback loop failure protection: steady-state

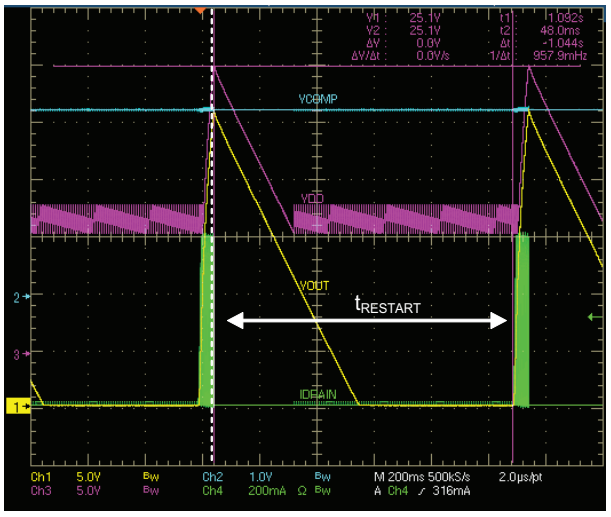


Figure 32. Feedback loop failure protection: steady-state, zoom

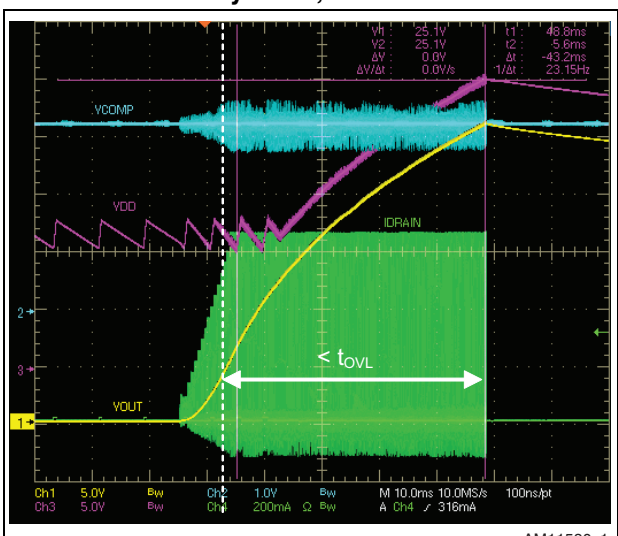
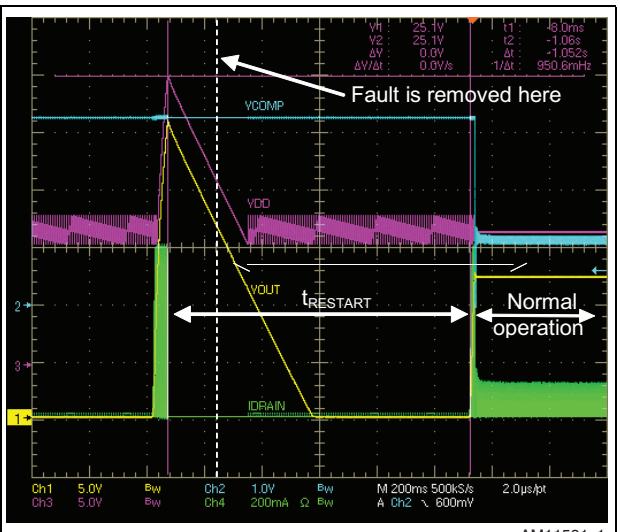


Figure 33. Feedback loop failure removal: converter restart

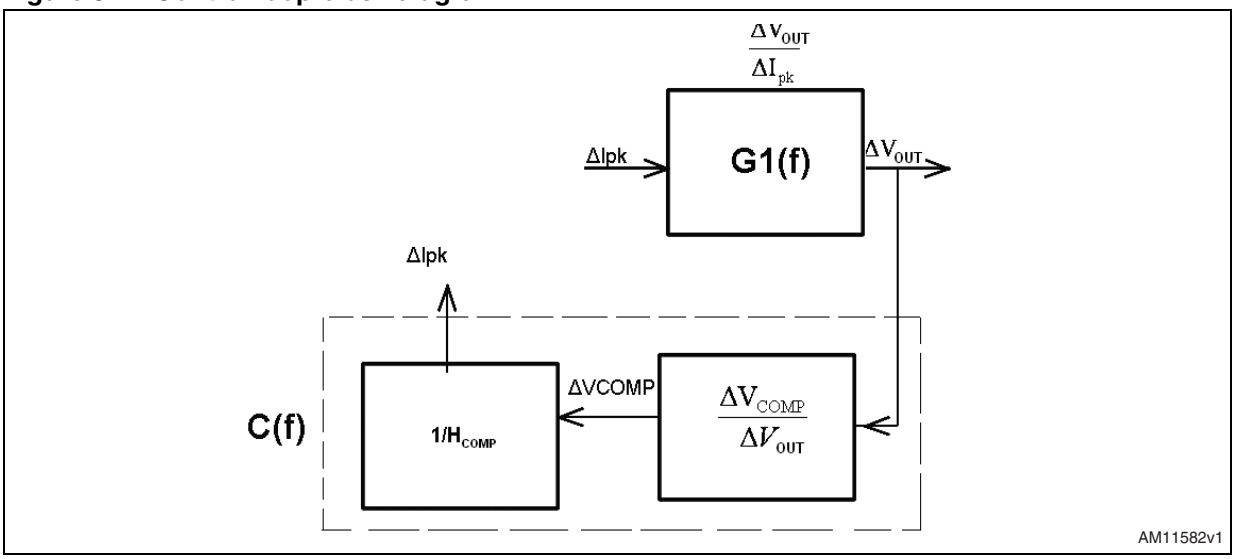


11 Feedback loop calculation guidelines

11.1 Transfer function

The set PWM modulator + power stage is indicated with G1(f), while C(f) is the “controller”, i.e. the network which is in charge to ensure the stability of the system.

Figure 34. Control loop block diagram



The mathematical expression of the power plant G1(f) is the following:

Equation 2

$$G_1(f) = \frac{\Delta V_{OUT}}{\Delta I_{pk}} = \frac{V_{OUT} \cdot (1 + \frac{j \cdot 2 \cdot \pi \cdot f}{z})}{Ipkp(fsw, Vdc) \cdot (1 + \frac{j \cdot 2 \cdot \pi \cdot f}{p})} = \frac{V_{OUT} \cdot (1 + \frac{j \cdot f}{fz})}{Ipkp(fsw, Vdc) \cdot (1 + \frac{j \cdot f}{fp})}$$

where V_{OUT} is the output voltage, Ipkp is the primary peak current, fp is the frequency of the pole due to the output load:

Equation 3

$$fp = \frac{1}{\pi \cdot C_{OUT} \cdot (R_{OUT} + 2ESR)}$$

and fz the frequency of the zero due to the ESR of the output capacitor:

Equation 4

$$fz = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot ESR}$$

The mathematical expression of the compensator C(f) is:

Equation 5

$$C(f) = \frac{\Delta I_{pk}}{\Delta V_{OUT}} = \frac{C_0}{H_{COMP}} \cdot \frac{1 + \frac{f \cdot j}{fZc}}{2 \cdot \pi \cdot f \cdot j \cdot \left(1 + \frac{f \cdot j}{fPc}\right)}$$

where (with reference to the schematic of *Figure 2*):

Equation 6

$$C_0 = -\frac{Gm}{C7 + C8} \cdot \frac{R4}{R3 + R4}$$

Equation 7

$$fZc = \frac{1}{2 \cdot \pi \cdot R7 \cdot C7}$$

Equation 8

$$fPc = \frac{C7 + C8}{2 \cdot \pi \cdot R7 \cdot C7 \cdot C8}$$

are to be chosen with the purpose to ensure the stability of the overall system. Gm = 2 mA/V (typical) is the VIPER26 transconductance.

11.2 Compensation procedure

The first step is to choose the pole and zero of the compensator and the crossover frequency, for instance:

- fZc = fp/2
- fPc = fz
- fcross = fcross_sel ≤fsw/10.

G1(fcross_sel) can be calculated from equation (2) and, being by definition | C(fcross_sel)*G1(fcross_sel)| = 1, C_0 can be calculated as follows:

Equation 9

$$C_0 = \frac{\left|2 \cdot \pi \cdot fcross_sel \cdot j\right| \cdot \left|1 + \frac{fcross_sel \cdot j}{fPc}\right|}{\left|1 + \frac{fcross_sel \cdot j}{fZc}\right|} \cdot \frac{H_{COMP}}{\left|G1(fcross_sel)\right|}$$

At this point the Bode diagram of G1(f)*C(f) can be plotted, in order to check the phase margin for the stability. If the margin is not high enough, another choice should be made for

fZc, fPc and fcross_sel, and the procedure repeated. When the stability is ensured, the next step is to find the values of the schematic components, which can be calculated, using the above formulas, as follows:

Equation 10

$$R5 = \frac{R6}{\frac{V_{OUT}}{3.3V} - 1}$$

Equation 11

$$C8 = \frac{fZc}{fPc} \cdot \frac{Gm}{|C_0|} \cdot \frac{R4}{R4 + R3}$$

Equation 12

$$C7 = C8 \cdot \left(\frac{fPc}{fZc} - 1 \right)$$

Equation 13

$$R7 = \frac{C7 + C8}{2 \cdot \pi \cdot fPc \cdot C7 \cdot C8}$$

12 Thermal measurements

A thermal analysis of the board at full load condition, @ T_{AMB} = 25 °C has been performed using an IR camera. The worst case is V_{IN} = 85 V_{AC}, but also the nominal input voltage cases (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}) have been considered. The results are shown in *Figure 35*, *36* and *37* and summarized in *Table 12*.

Figure 35. Thermal map at T_{AMB} = 25 °C, V_{IN} = 85 V_{AC}, full load

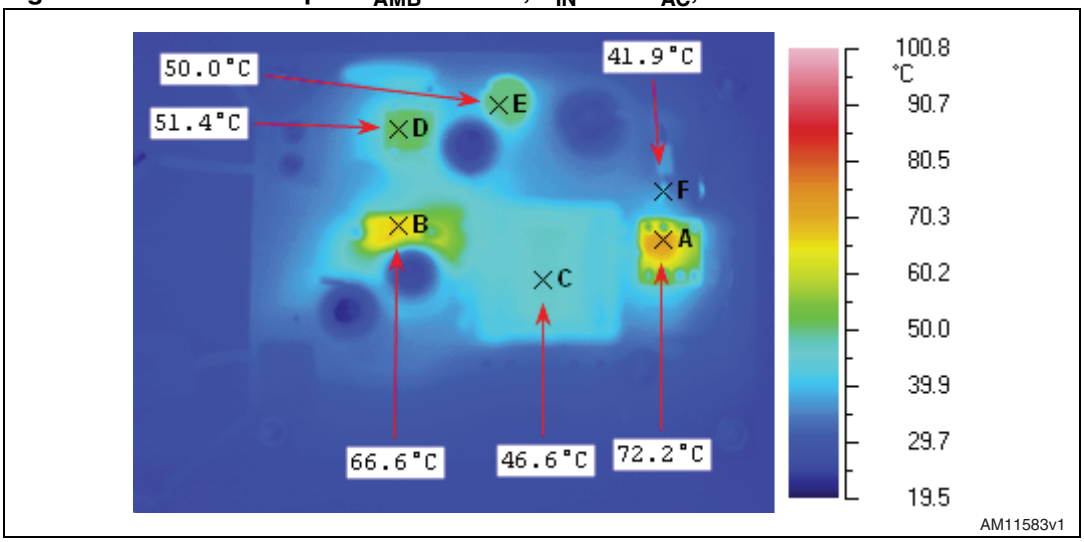


Figure 36. Thermal map at T_{AMB} = 25 °C, V_{IN} = 115 V_{AC}, full load

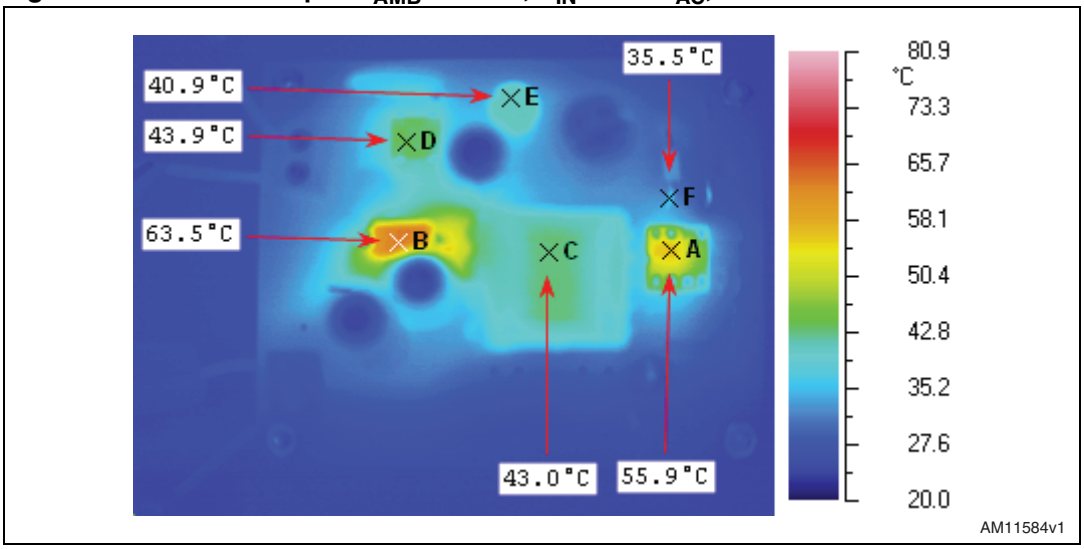


Figure 37. Thermal map at T_{AMB} = 25 °C, V_{IN} = 230 V_{AC}, full load

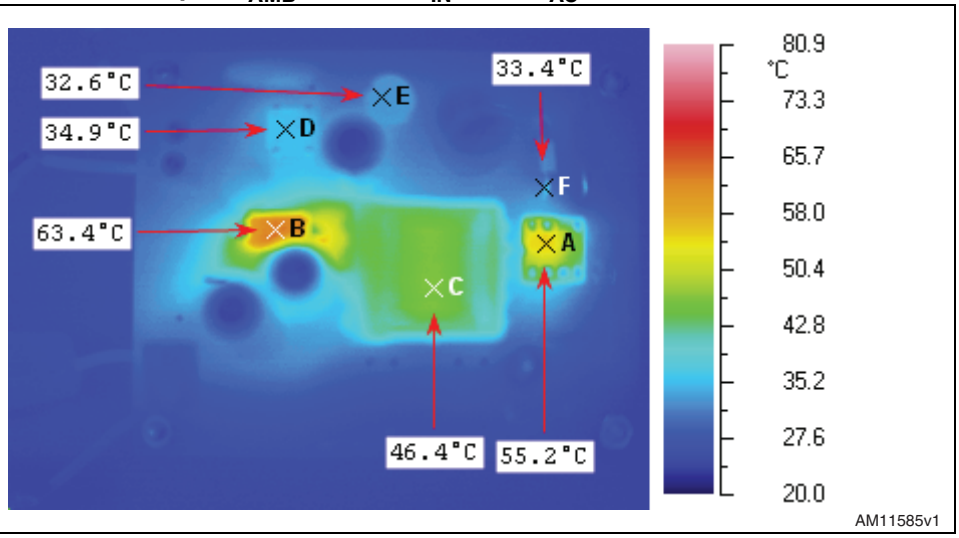


Table 12. Key components temperature @ V_{IN} = 85 V_{AC} /230 V_{AC}, full load (T_{AMB} = 25 °C)

Point	T [°C]		Reference
	V_{IN} = 85 V_{AC}	V_{IN} = 230 V_{AC}	
A	72.2	55.2	VIPER26
B	66.6	63.4	Output diode
C	46.6	46.4	Transformer
D	51.5	34.9	Diode bridge
E	50.0	32.6	Thermistor
F	41.9	33.4	Transil

13 EMI measurements

A pre-compliance test to EN55022 (Class B) European normative has been performed using an EMC analyzer and an LISN. First of all, a measurement of the background noise (board disconnected from the mains) was performed and is reported in *Figure 38*.

Then the average EMC measurements at 115 V_{AC}/full load and 230 V_{AC}/full load were performed and the results are shown in *Figure 39* and *40*.

Figure 38. Background noise measurement

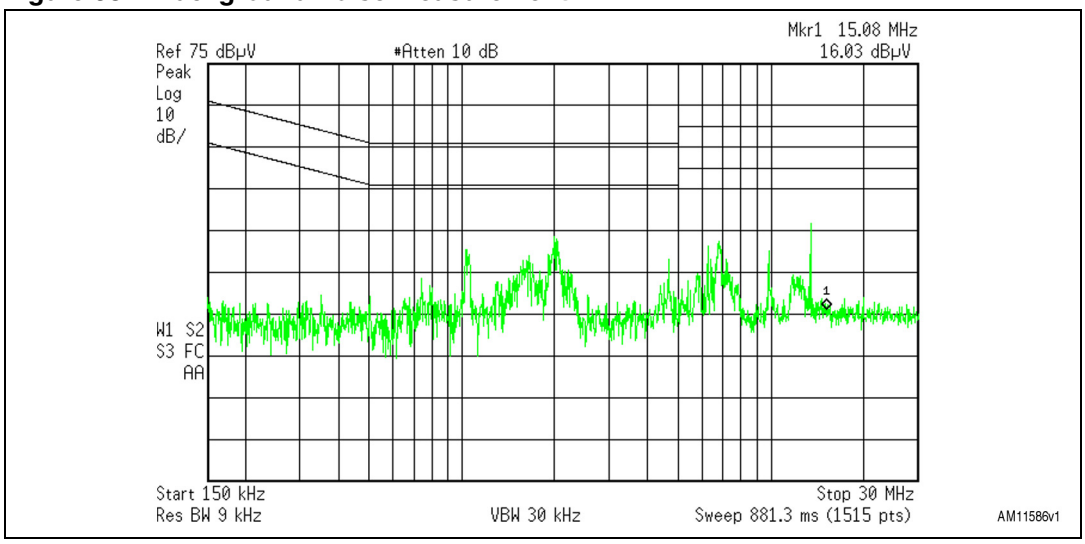


Figure 39. Average measurement at V_{IN} = 115 V_{AC}, full load

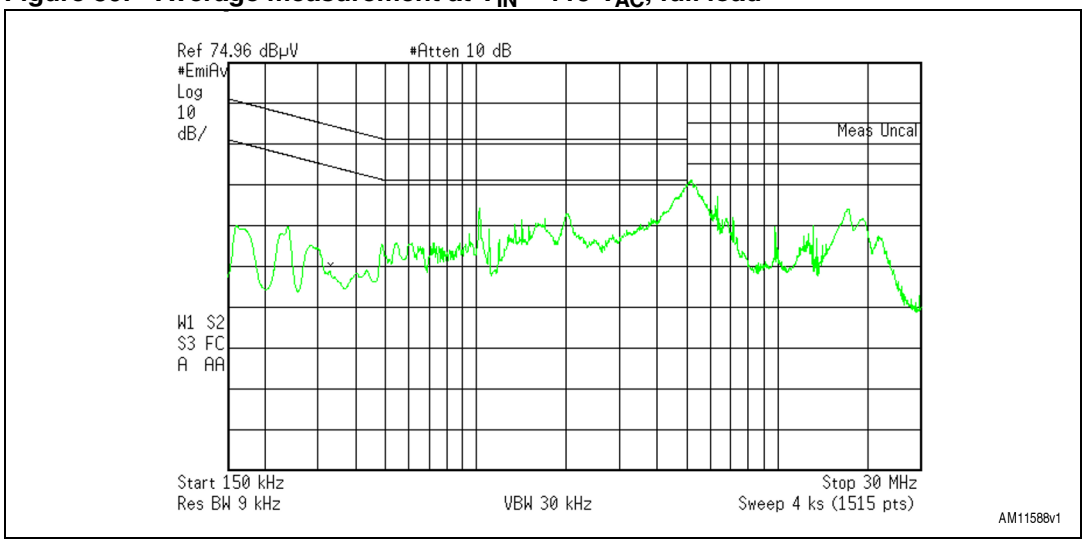
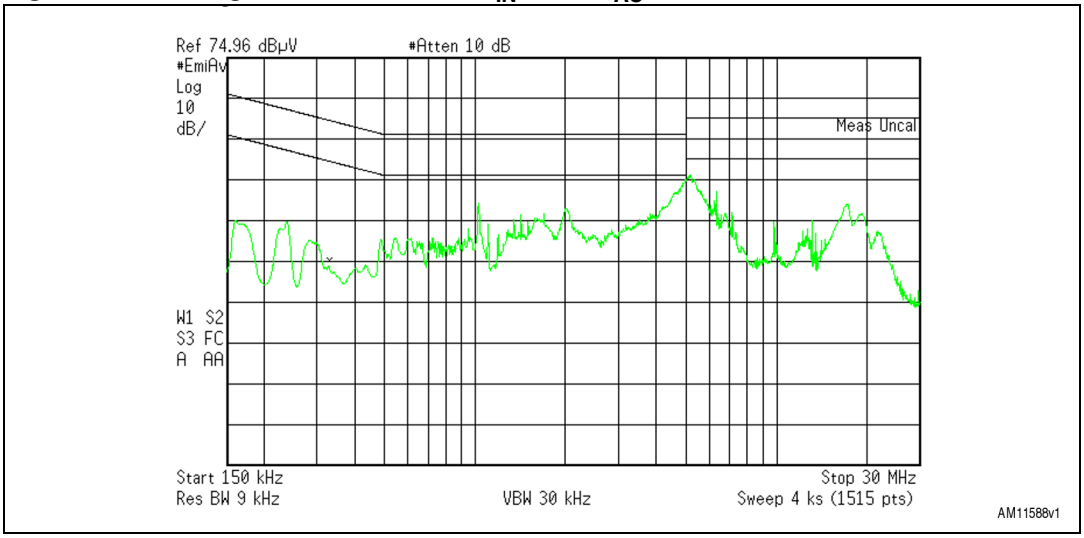


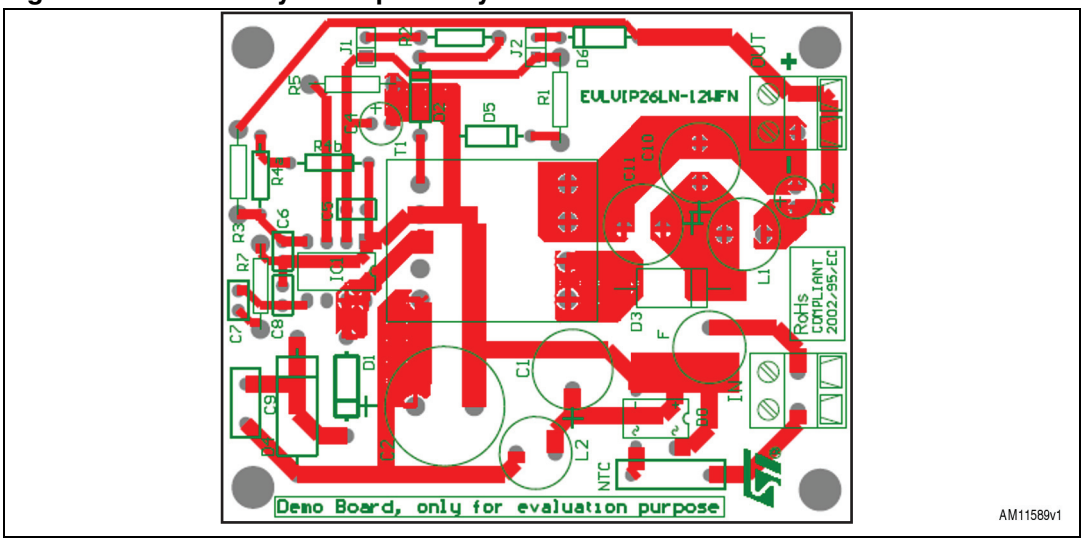
Figure 40. Average measurement at V_{IN} = 230 V_{AC}, full load



14 Board layout

Here below the board layout:

Figure 41. Bottom layer & top overlay



15 Conclusions

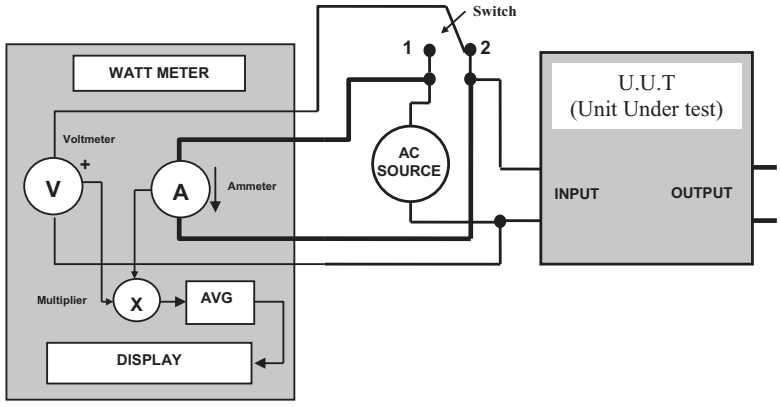
The VIPER26 allows a simple design of a non-isolated converter with few external components. In this document a non-isolated flyback has been described and characterized. Special attention has been given to light load performance, confirmed as very good by bench analysis. Efficiency has been compared to the requirements of the Code of Conduct, version 4 program (version 2.0) for an external AC-DC adapter with very good results in that the measured active mode efficiency is always higher with respect to the minimum required.

Appendix A Test equipment and measurement of efficiency and light load performance

The converter input power has been measured using a wattmeter. The wattmeter measures simultaneously the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument so it samples the current and voltage and converts them to digital forms. The digital samples are then multiplied giving the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher depending on the instrument used). The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 sec typ.).

Figure 42 shows how the wattmeter is connected to the UUT (unit under test) and to the AC source and the wattmeter internal block diagram.

Figure 42. Connections of the UUT to the wattmeter for power measurements



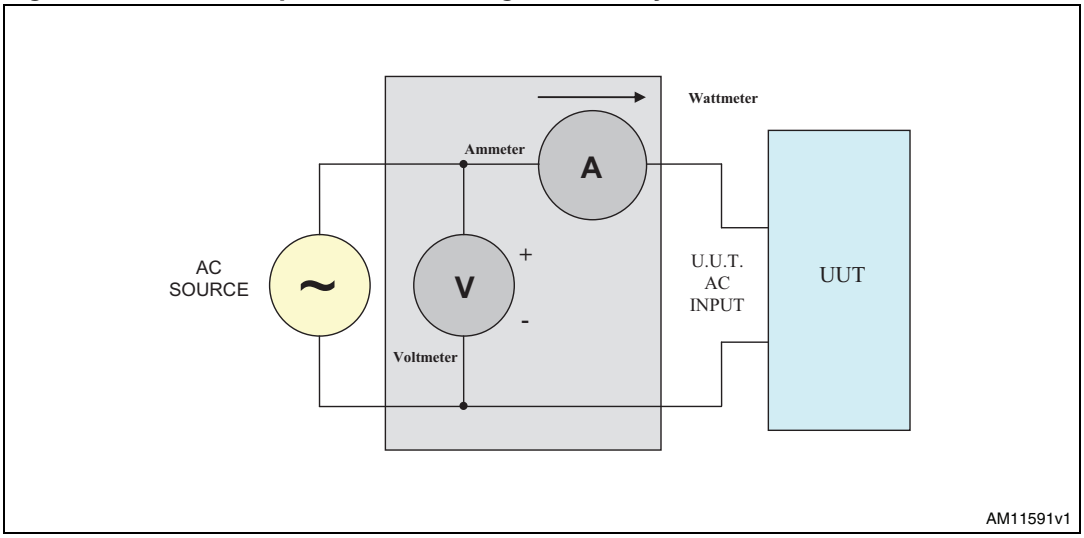
An electronic load has been connected to the output of the power converter (UUT), allowing the converter load current to be set and measured, while the output voltage has been measured by a voltmeter. The output power is the product between load current and output voltage. The ratio between the output power, calculated as previously stated, and the input power, measured by the wattmeter, is the converter's efficiency, which has been measured in different input/output conditions.

A.1 Measuring input power

With reference to *Figure 42*, the UUT input current causes a voltage drop across the ammeter's internal shunt resistance (the ammeter is not ideal as it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

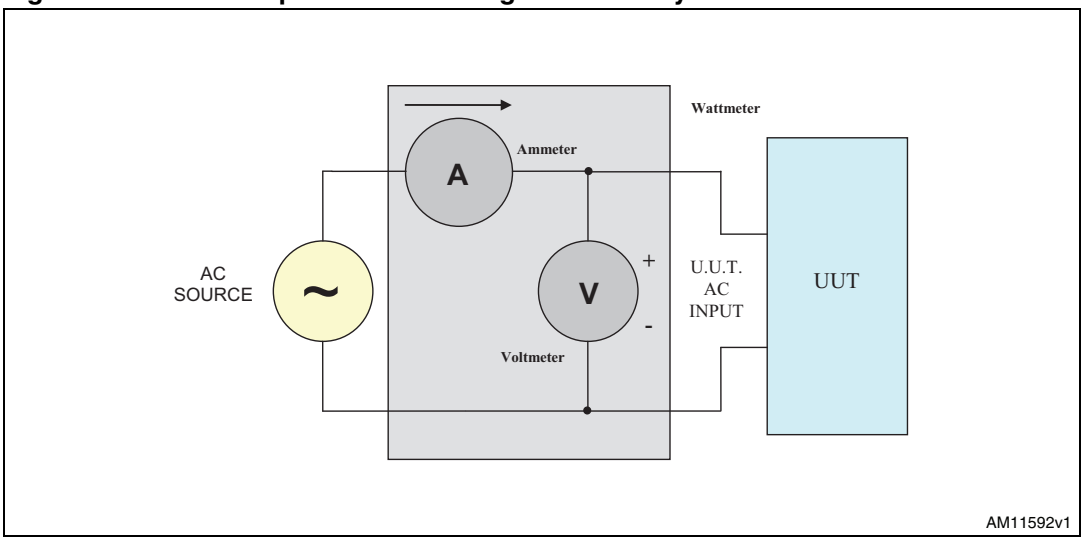
If the switch of *Figure 42* is in position 1 (see also the simplified scheme of *Figure 43*), this voltage drop causes an input measured voltage higher than the input voltage at the UUT input that, of course, affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example when we are measuring the input power of UUT in light load condition).

Figure 43. Switch in position 1 - setting for standby measurements



In the case of high UUT input current (i.e. for measurements in heavy load conditions), the voltage drop can be relevant compared to the UUT real input voltage. If this is the case, the switch in *Figure 42* can be changed to position 2 (see simplified scheme of *Figure 44*) where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

Figure 44. Switch in position 2 - setting for efficiency measurements



On the other hand, the position of *Figure 44* may introduce a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter itself (which is not an ideal instrument and doesn't have infinite input resistance) is not negligible. This is the reason why it is better to use the setting of *Figure 43* for light load measurements and *Figure 44* for heavy load measurements.

If it is not clear which measurement scheme has the lesser effect on the result, try with both and register the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT is operated at 100% of nameplate output current output for at least 30

minutes (warm-up period) immediately prior to conducting efficiency measurements. After this warm-up period, the AC input power is monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5-minute period. If AC input power is not stable over a 5-minute period, the average power or accumulated energy is measured over time for both AC input and DC output.

Some wattmeter models allow integration of the measured input power in a time range and then measure the energy absorbed by the UUT during the integration time. The average input power is calculated dividing by the integration time itself.

16 References

– Code of Conduct on Energy Efficiency of External Power Supplies, Version 4.
– VIPER26 datasheet.

17 Revision history

Table 13. Document revision history

Date	Revision	Changes
16-Oct-2012	1	Initial release.

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