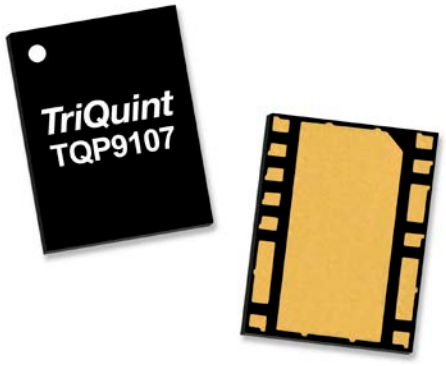
TQP9107

699-960 MHz 2-stage Power Amplifier

Applications

- Wireless Infrastructure
- Repeaters, Boosters, DAS
- High Power Amplifiers
- Small cell BTS

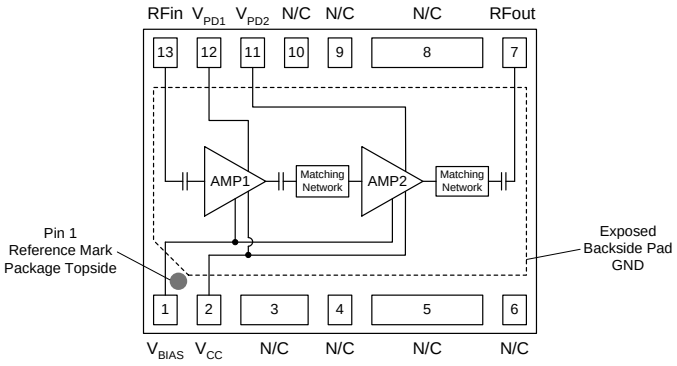


3.5 x 4.5 mm Leadless SMT Package

Product Features

- 699 – 960 MHz Frequency Range
- 35.5 dB gain
- +46 dBm Output IP3 at Pout = +24 dBm/tone
- 31% PAE at +27 dBm Pout
- Internally Matched
- Integrated Inter-Stage Matching
- Bias Adjustable
- Low idle current

Functional Block Diagram



Top View

General Description

The TQP9107 is a high-efficiency two-stage power amplifier in a low-cost surface-mount package. The amplifier is able to achieve 31% power added efficiency at +27 dBm output power while operating with a low 84 mA idle current. The amplifier is designed to ensure that all odd-order IMD products are below −17 dBm at all output power levels below +24 dBm/tone.

The TQP9107 integrates two high performance amplifier stages onto a module to allow for a compact system design and requires very few external components for operation. The amplifier is bias adjustable allowing the amplifier's power consumption to be optimized. The TQP9107 is available in a lead-free/RoHS-compliant 13-pin 3.5 x 4.5mm surface mount package and is pin-compatible to the higher frequency band version in the family with the TQP9108 (1.7-2.17 GHz).

Pin Configuration

Pin No.	Label
1	V_{BIAS}
2	V_{CC}
3, 4, 5, 6, 8, 9, 10	GND or N/C
7	RFout
11	V_{PD1}
12	V_{PD2}
13	RFin
Backside Pad	GND

Ordering Information

Part No.	Description
TQP9107	699-960 MHz Power Amplifier
TQP9107-PCB	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to +150 °C
Supply Voltage (V_{CC})	+6 V
RF Input Power, CW, 50Ω, T=25 °C	+7 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{CC}, V_{BIAS}		+4.3	+5	V
V_{PD1}, V_{PD2}		+4.0	+5	V
T_{CASE}	-40		+85	°C
Tj for >10^6 hours MTTF			+190	°C

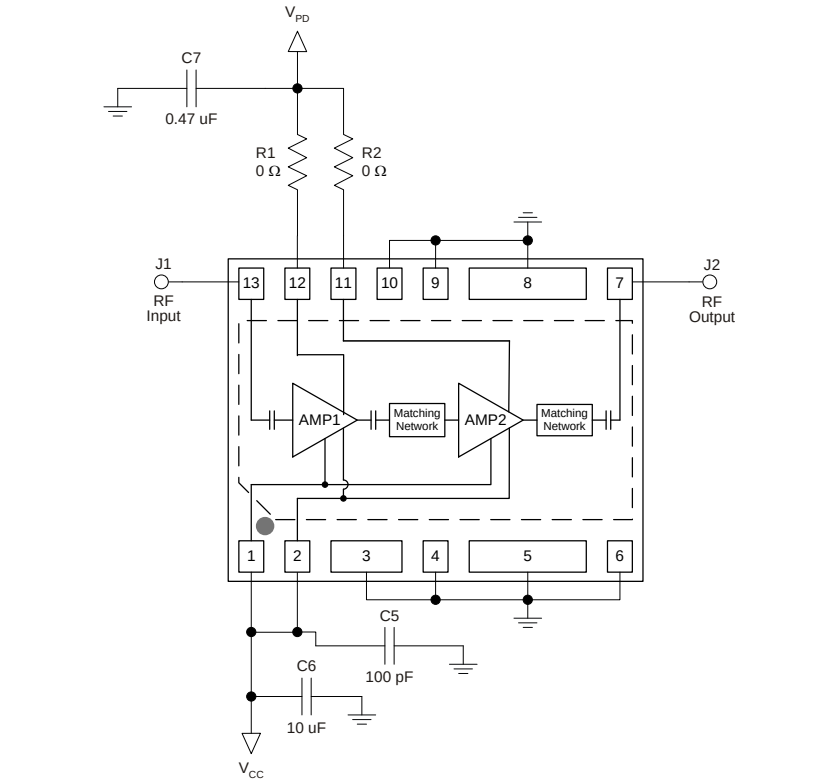
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

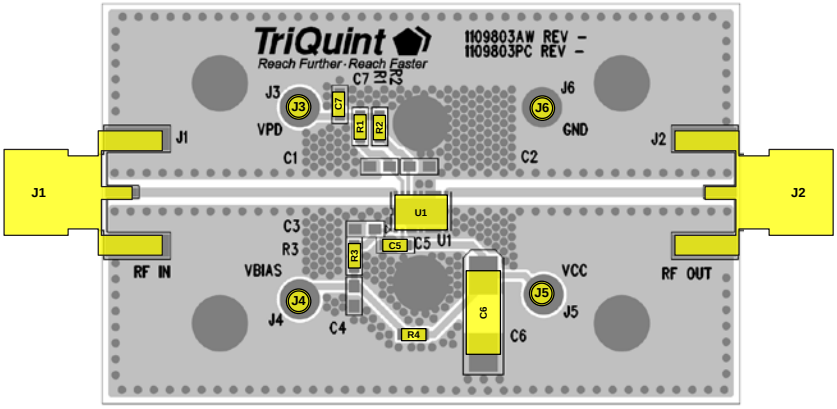
Electrical Specifications

Test conditions unless otherwise noted: V_{CC} = V_{BIAS} = +4.3 V, V_{PD1} = V_{PD2} =+4.0 V, Temp=+25 °C, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		699		960	MHz
Test Frequency			849		MHz
Gain		28.8	35.5		dB
Noise Figure			5		dB
Output P1dB			31.4		dBm
Output IP3	Pout = +23 dBm/tone, Δf = 600 kHz	+43	+46		dBm
IMD3, IMD5, IMD7	All power levels ≤ 23 dBm / tone			−17	dBm
Current, I_{CC}	Pout = +27 dBm		370		mA
Power Added Efficiency	Pout = +27 dBm		31		%
Idle Current	No RF Input Power		84		mA
Thermal Resistance, θ_{jc}	Junction to case		30.1		°C/W

Application Circuit Schematic Diagram





Bill of Material

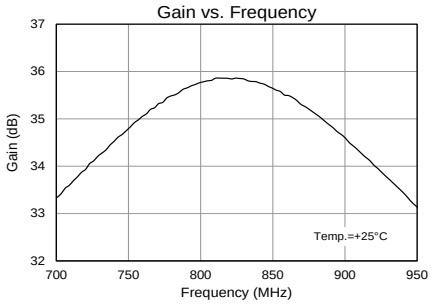
Reference Des.	Value	Description	Manuf.	Part Number
		Nelco FR4, PCB APP BOARD	TriQuint	1109803PC
U1		2-Stage Power Amplifier	TriQuint	TQP9107
C5	100 pF	CAP, 0603, 5%, 50V, NPO	various	
C6	10 uF	CAP, 6032, 20%, 50V, Tantalum	various	
C7	0.47 uF	CAP, 0603, 50V, X7R, 5%		
R1, R2, R3, R4	0 Ω	RES, 0603, 5%, 1/16W, Chip	various	

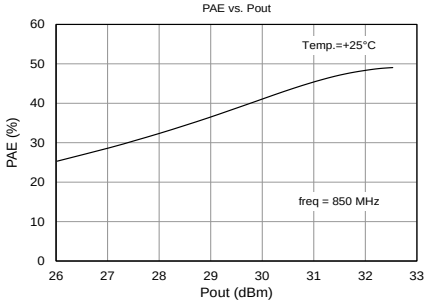
Typical Performance

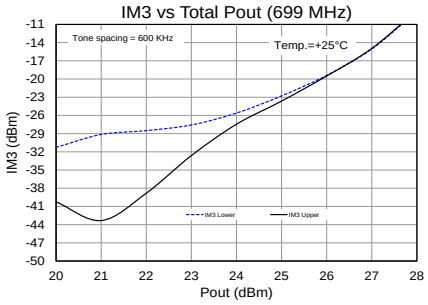
Test Conditions: V_{CC}=+4.3 V, Temp.=+25°C, 50Ω System

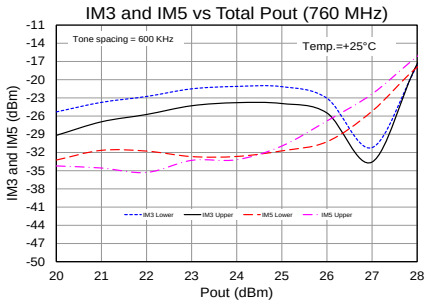
Parameter	Conditions	Typical Value				Units
Frequency		760	820	850	920	MHz
Gain		35.0	35.8	35.7	34.1	dB
IM3	Pout= +27 dBm, Δf= 600 KHz	-30	-27	-24	-17	dBm
IM5	Pout= +27 dBm, Δf= 600 KHz	-22	-21	-20	-21	dBm
Quiescent Collector Current, I_{CQ}	V_{PD} = 4V	84				mA

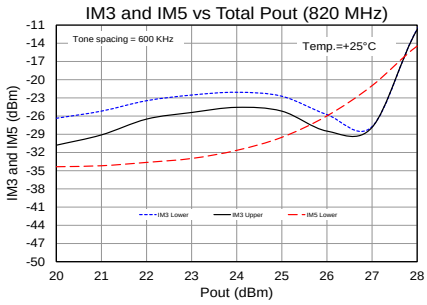
Performance Plots

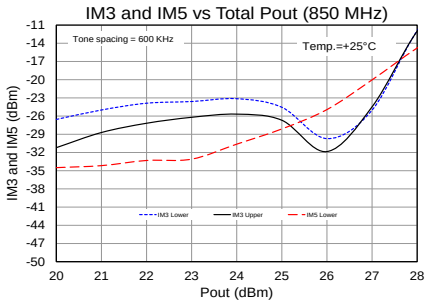


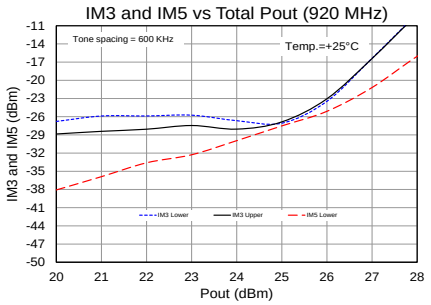


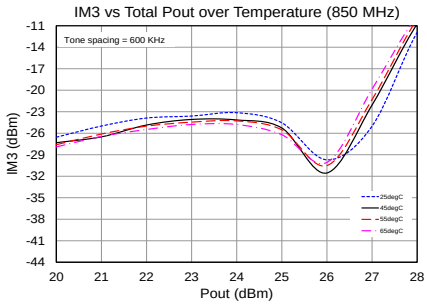


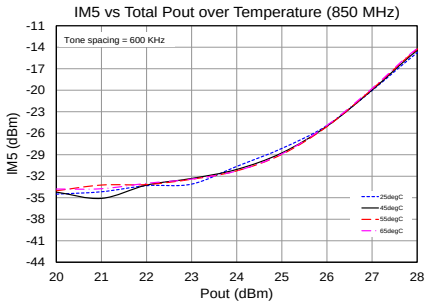


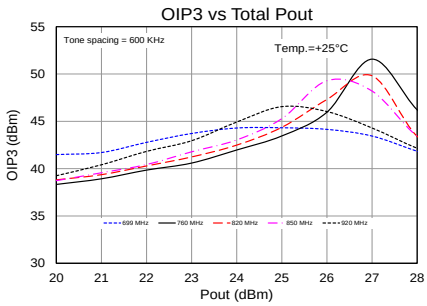










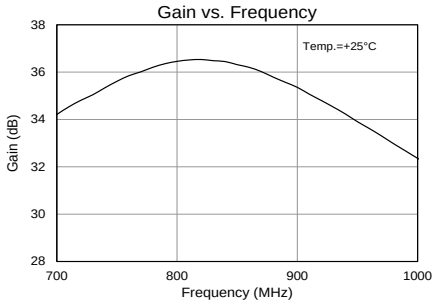


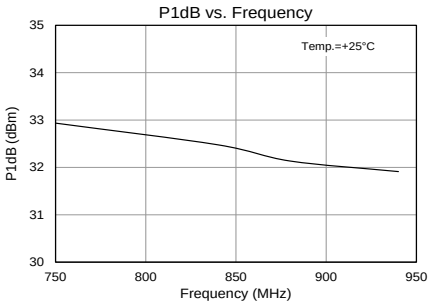
Typical Performance at Vcc = 5V

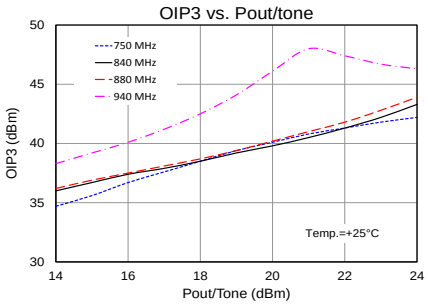
Test Conditions: V_{CC}=+5 V, Vpd=+4.3 V, Temp.=+25°C, 50Ω System

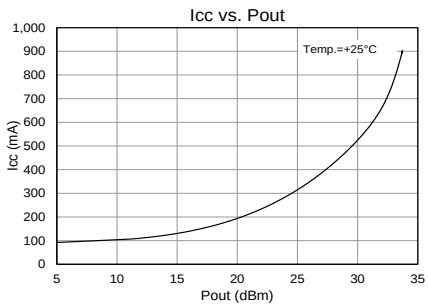
Parameter	Conditions	Typical Value				Units
Frequency		750	840	880	940	MHz
Gain		35.5	36.2	35.8	34.0	dB
Input Return Loss		-13	-9	-9	-10	dB
Output P1dB		32.9	32.5	32.1	31.9	dBm
Output IP3	Pout= +24 dBm/tone, Δf= 1 MHz	42.1	43.5	44.0	46.2	dBm
Quiescent Collector Current, I_{CQ}		87				mA

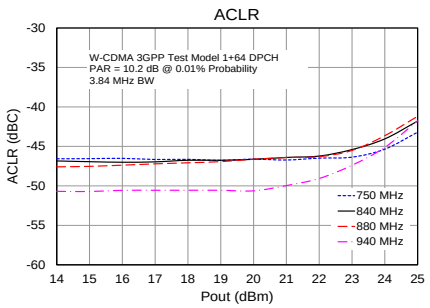
Performance Plots



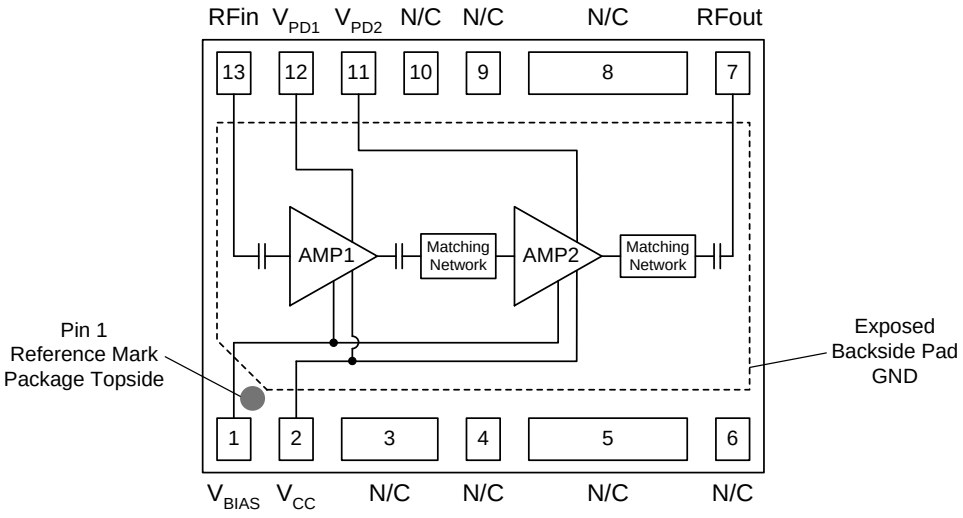








Pin Configuration and Description

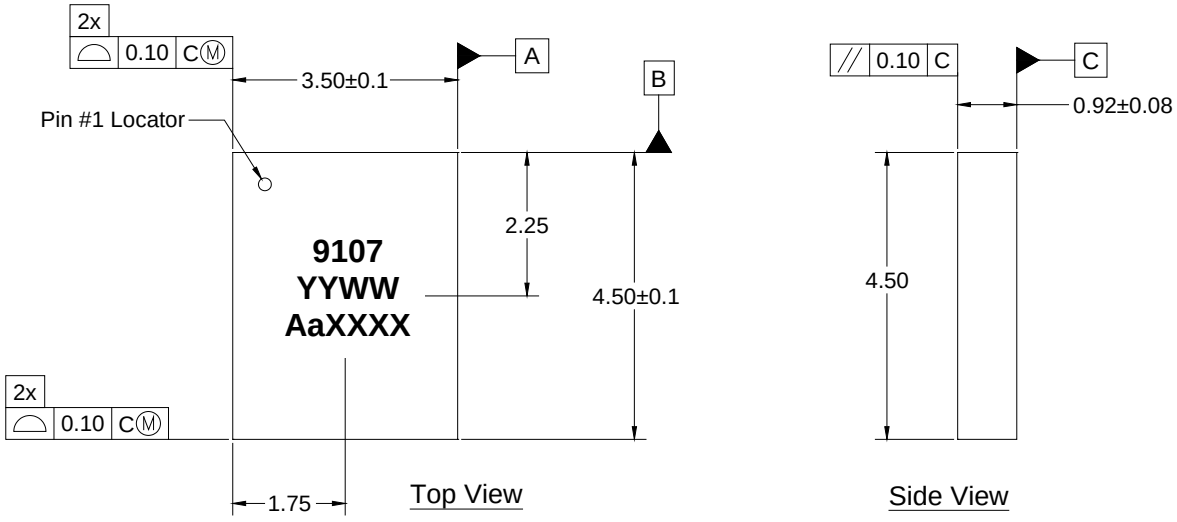


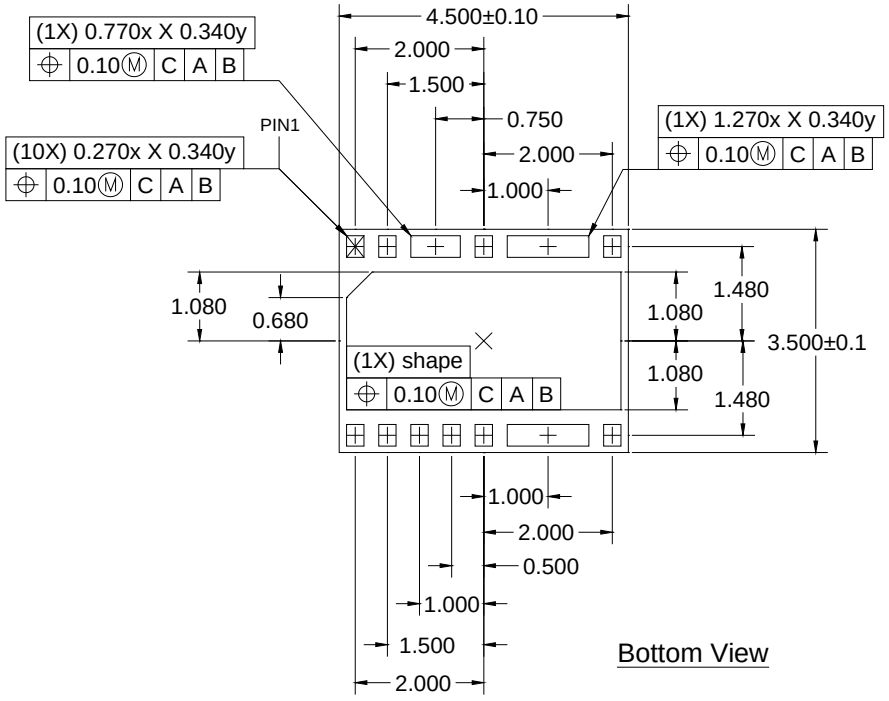
Top View

Pin No.	Label	Description
1	V_{BIAS}	Provides reference voltage for internal active biasing circuit
2	V_{CC}	DC voltage supply connection
3, 4, 5, 6, 8, 9, 10	N/C	No internal connection. Provide grounded land pads for PCB mounting integrity.
7	RF out	RF output pin. The DC is internally blocked at this pin.
11	V_{PD1}	Power down for Amp 1. This voltage adjusts for the current draw in Amp 1.
12	V_{PD2}	Power down for Amp 2. This voltage adjusts for the current draw in Amp 2.
13	RF in	RF input pin. The DC is internally blocked at this pin.
Backside Pad	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Package Marking and Dimensions

Marking: Part number – 9107
Date - YYWW
Lot code – AaXXXX

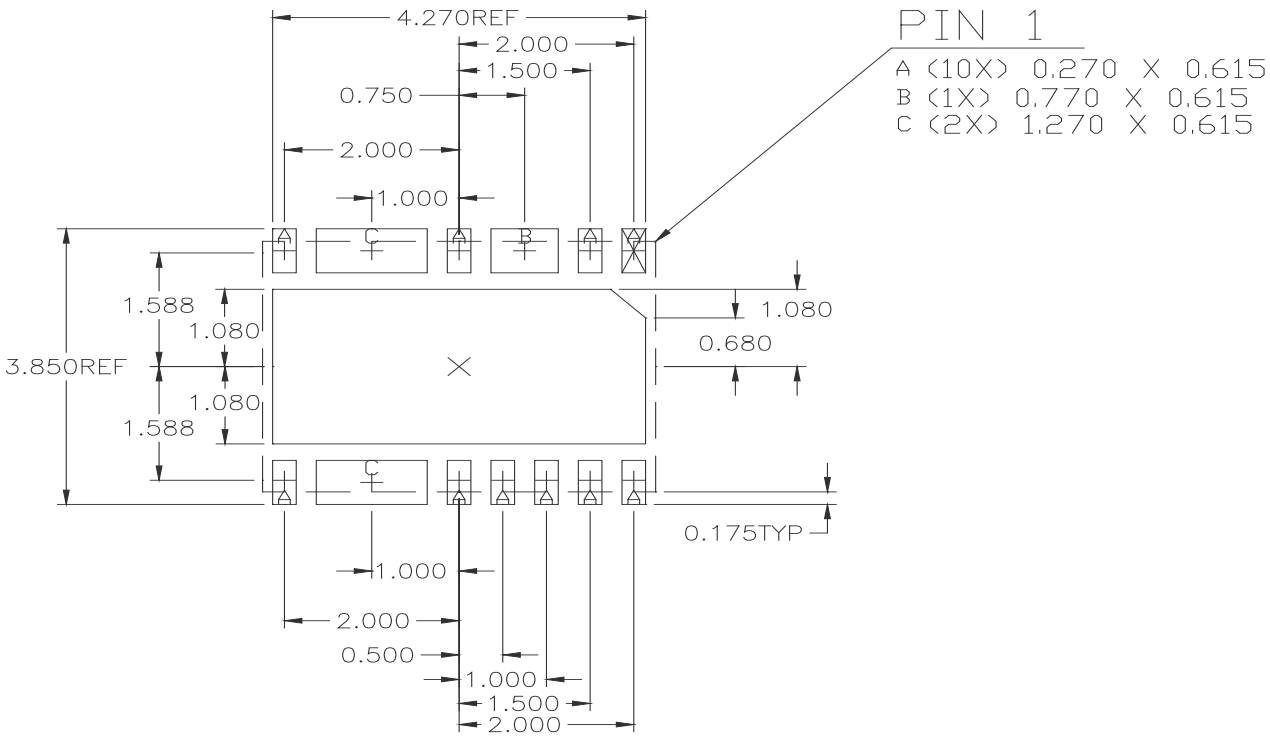




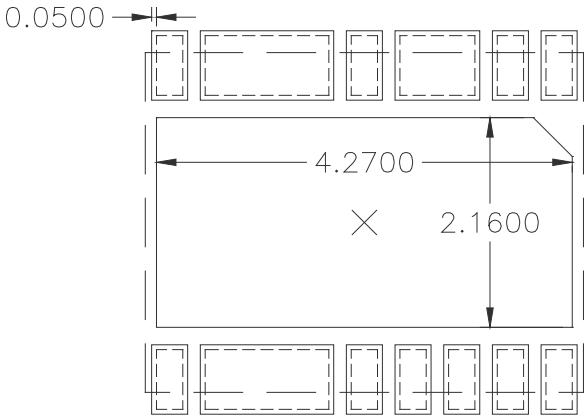
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-229.
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern

Recommend PCB land-pad pattern metallization (Top View)



Recommended PCB solder mask opening (Top View)



Notes:

1. A heat sink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 1C
Value: Passes ≥ 1000V to < 2000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: Passes ≥ 1000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 3
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead-free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.503.615.9000
Email: info-sales@triquint.com **Fax:** +1.503.615.8902

For technical questions and application information:

Email: sjcapplications.engineering@triquint.com

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