Double Pulse Test Board

$V_{DS, MAX}$	=	1200 V
$I_{D, MAX}$	=	100 A

Features

- 1200 V, 100 A Testing
- Low Series Inductance Design
- Wide, 6 oz. Copper Current Traces
- Multiple DUT and FWD Connections for Long Life
- Compatible with GeneSiC Gate Drive Mounting
- Low Resistance and Inductance Gate Drive Connection

Compatible

- TO-247 Packaged Commercial SJTs
- TO-257 Packaged High Temperature SJTs
- TO-258 Packaged High Temperature SJTs
- TO-46 Packaged High Temperature SJTs

Electrical Characteristics

Parameter	Symbol	Conditions	Value	Unit	Notes
Test Voltage Maximum	$V_{DS, MAX}$		1200	V	
Drain Current Maximum	$I_{D, MAX}$		100	A	
Capacitor Bank	C_{bank}		5.0	µF	
Parasitic Inductance	L_s	HV = 800 V, I_D = 6 A	62.5	nH	
Maximum Stored Energy	E_{max}	HV = 1200 V	3.6	J	

Overview

The GeneSiC Double Pulse Test Board is designed for performing double pulse switching tests on GeneSiC SiC Junction Transistors (SJT) as well as other three terminal switching transistors. It is designed using low ESL capacitors and PCB traces to feature a low parasitic series inductance (L_S) current path. This is necessary to record data which is most representative of the device under test (DUT) and minimize testing circuit distortions. The board is capable of reaching a maximum of 1200 V and 100 A for high power device testing. An external load inductor, DUT, and free-wheeling diode (FWD) are soldered to the board without sockets for the lowest possible contact resistance and inductance. GeneSiC pin compatible gate drive boards may be mounted directly on to the Test Board for ease of use while also having a short, low inductance path to the DUT gate pin connection.

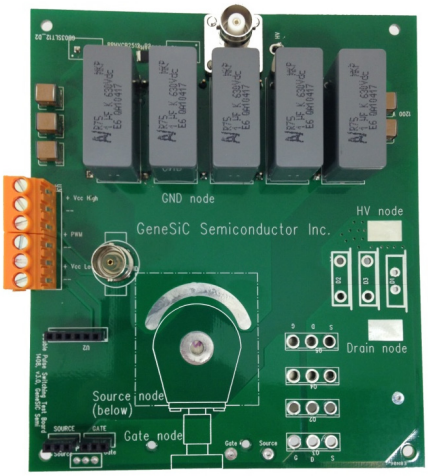


Figure 1: GeneSiC Semi Double Pulse Test Board

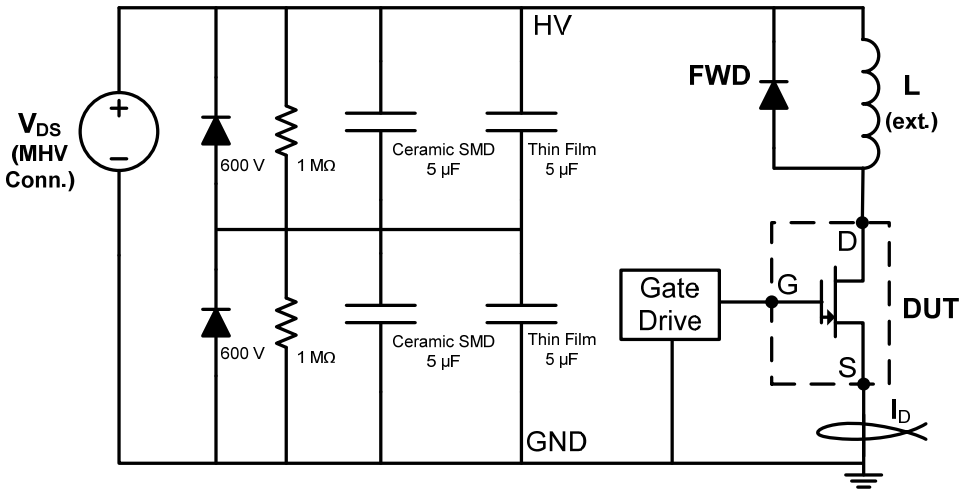


Figure 2: GeneSiC Semiconductor Switching Test Board Schematic

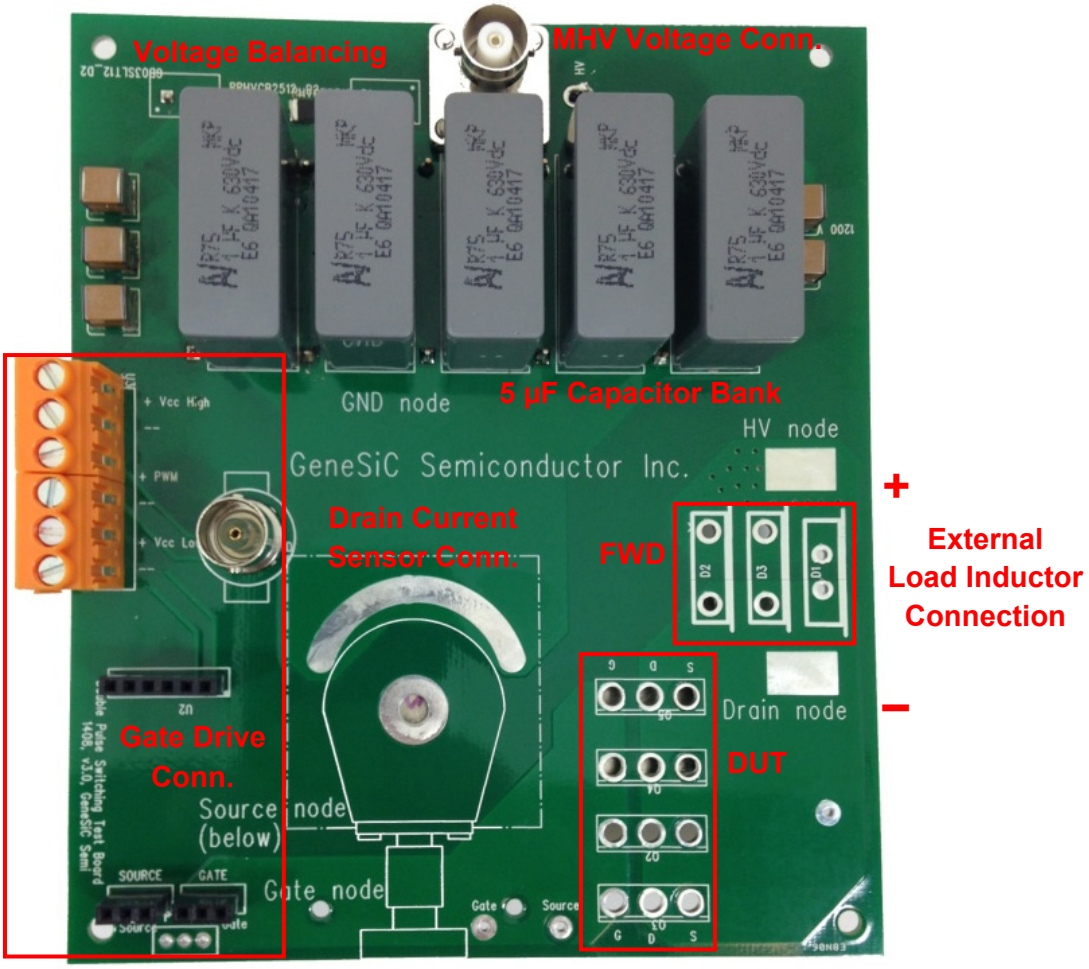


Figure 3: Switching Test Board with Labeling

MHV Voltage Connection

High voltage for testing up to 1200 V is supplied to the Test Board through a MHV coaxial connection. Voltage may be generated through a high voltage power supply of choice.

Capacitor Bank

The capacitor bank is comprised of 20, 1 µF, 630 V capacitors to store up to 3.6 J of energy to supply to the DUT. The bank includes 10 low effective series inductance (ESL) surface mount ceramic capacitors to allow DUT drain currents to rise and fall with minimal circuit interference. Thick 6 oz. copper traces on the Test Board also minimize this parasitic inductance and connect the capacitor bank to the test circuit.

Voltage Balancing Network

A voltage balancing network of two 1 MΩ, 2 W SMD resistors is used to ensure an equal potential is across the series connected capacitors on the Test Board along with two blocking rectifiers to protect against extreme overvoltage of the energy storage capacitors.

External Load Inductor Connection

A load inductor (not provided) is soldered directed to the HV and Drain nodes upon the connection pads provided. Care should be taken to ensure the voltage rating of the inductor is not exceeded. Also, if the chosen inductor value is too large the capacitor bank may drain before the inductor is fully charged to the desired test current I_D level. An inductance of $L_{load} \leq 1.0$ mH is suggested.

Device Under Test (DUT) and Free Wheeling Diode (FWD)

The DUT and FWD are to be soldered into the connection terminals with minimal lead extending from the board, extra leads extending through the Test Board should be trimmed from the package to reduce electrical noise which may distort measurement during ultra-fast, high-voltage switching which SJT devices are capable of. Devices may be connected to isolated hotplates while connected to the Test Board for high-temperature testing as desired. It is also recommended to probe any device voltages (i.e. V_{GS}, V_{DS}) as close as possible to the device for accurate measurement and minimal testing induced voltage and current ringing.

Drain Current Sensor Connection

A low inductance measurement of the DUT drain current can be made utilizing the drain current sensor connection along with the use of a Pearson Electronics Current Monitor (not provided) of the shape "J". The connection can best be made utilizing a wide metallic conductor extending from the GND node partially encasing the current monitor with a wide conductor extending through the current monitor eye-hole and connecting to the source node beneath. These two nodes, source and GND, must be connected for the Test Board to operate properly and when used in this configuration the drain current passed through a current monitor for data recording while adding minimal parasitic inductance. If the drain current is not being sensed at the Drain Current Sensor Connection in some fashion, as described here or otherwise, the two nodes must be shorted together using a wide jumper cable.

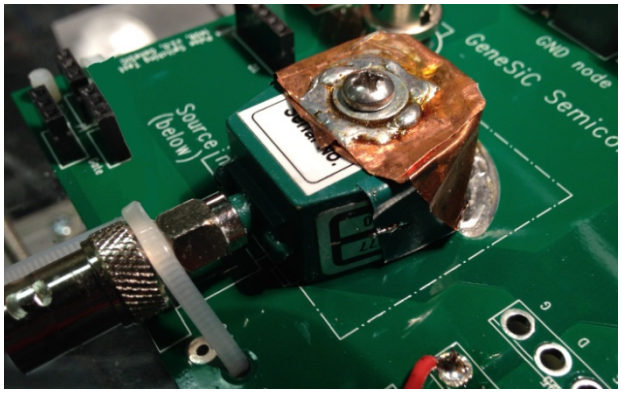


Figure 4: Drain Current Sensor Connection with Pearson Current Monitor installed using a low inductance current path.

Gate Drive Connection

The Gate Drive Connection may be used to connect a GeneSiC Gate Drive Board to the Test Board and DUT. It is designed to receive the gate drive board voltage inputs from an external supply as well as the digital gate control signal and pass them through the Test Board to the gate drive board inputs through a 6 pin, in-line header connection. The output gate connection of the gate drive board is directly fed into the Test Board gate node through a 3 pin header and is passed with a low parasitic inductance connection to the DUT gate pin along with a similar source connection return. The use of the Gate Drive Connection is optional and DUT gate driving is fully customizable to the users' specifications and preferences. The connection of any gate drive topology may be made to the Gate Drive Connection or directly to the DUT.

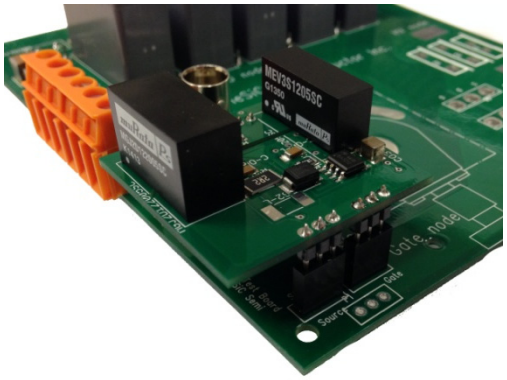


Figure 5: GeneSiC Gate Drive Board connected to the Test Board's Gate Drive Connection

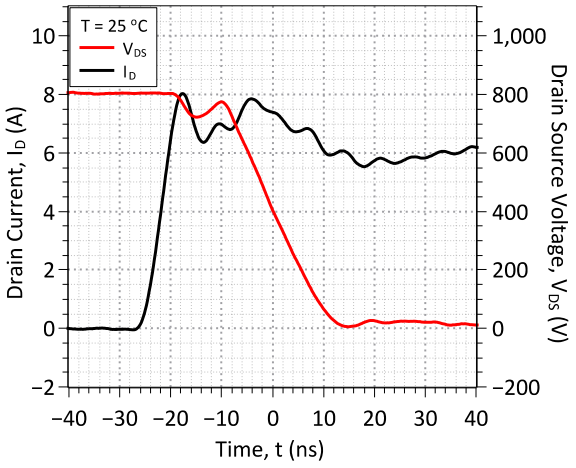


Figure 6: SJT 800V Switching Turn On Waveform

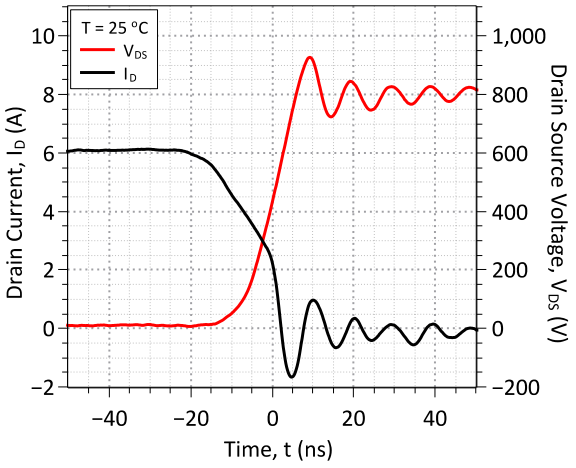
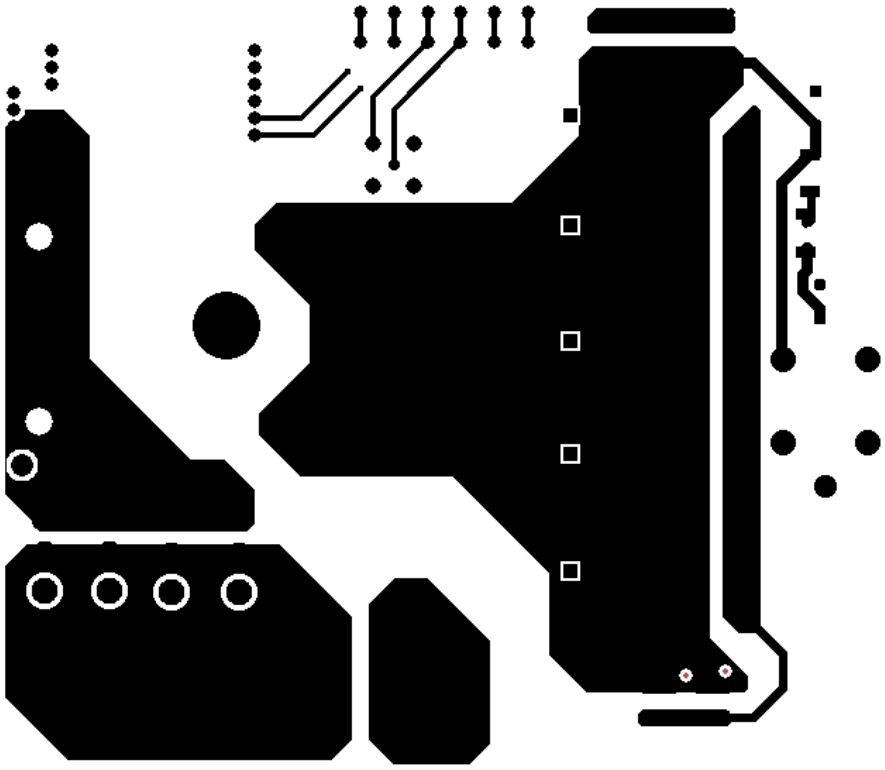


Figure 7: SJT 800V Switching Turn Off Waveform

Top Side Copper Metallization



Bottom Side Copper Metallization

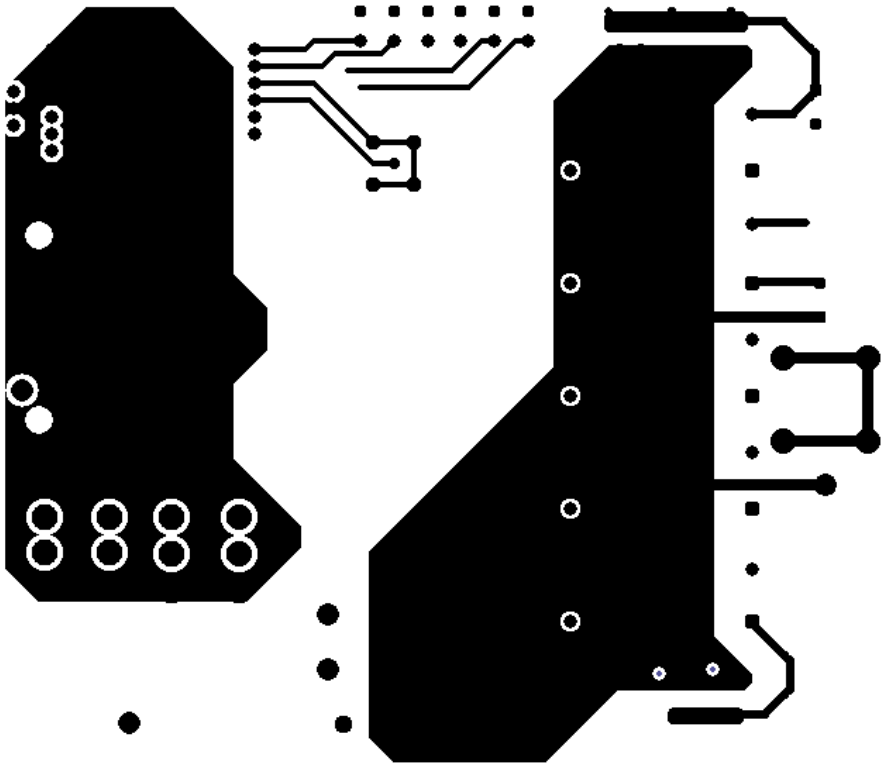


Figure 8: Test Board's top and bottom copper pours.

Revision History			
Date	Revision	Comments	Supersedes
2014/09/15	0	Initial release	

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