19A, 55V, 0.070 Ohm, N-Channel UltraFET Power MOSFETs

These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75309.

Ordering Information

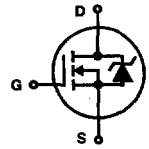
PART NUMBER	PACKAGE	BRAND
HUF75309P3	TO-220AB	75309P
HUF75309D3	TO-251AA	75309D
HUF75309D3S	TO-252AA	75309D

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-252AA variant in tape and reel, e.g., HUF75309D3ST.

Features

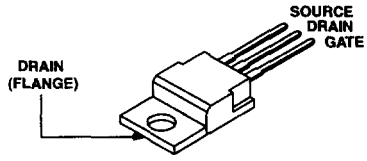
- 19A, 55V
- Simulation Models
  - Temperature Compensated PSPICE® and SABER© Models
  - SPICE and SABER Thermal Impedance Models Available on the WEB at: www.intersil.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC STYLE TO-220AB



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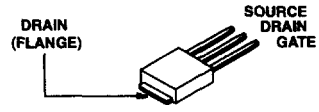

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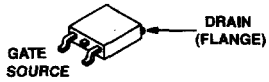

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD Handling Procedures.
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Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	55	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	55	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous (Figure 2)	I_D	19	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	E_{AS}	Figures 6, 14, 15	
Power Dissipation	P_D	55	W
Derate Above 25°C		0.37	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	°C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	°C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 11)		55	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 45V, V_{GS} = 0V, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA (Figure 10)		2	-	4	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 19A, V_{GS} = 10V (Figure 9)		-	0 .060	0.070	Ω
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)		-	-	2.7	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220		-	-	62	°C/W
		TO-251, TO-252		-	-	100	°C/W
SWITCHING SPECIFICATIONS (V_{GS} = 10V)							
Turn-On Time	t_{ON}	V_{DD} = 30V, $I_D \cong$ 19A, R_L = 1.58Ω, V_{GS} = 10V, R_{GS} = 27Ω		-	-	70	ns
Turn-On Delay Time	$t_{d(ON)}$			-	7	-	ns
Rise Time	t_r			-	39	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	24	-	ns
Fall Time	t_f			-	30	-	ns
Turn-Off Time	t_{OFF}			-	-	80	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 30V, $I_D \cong$ 19A, R_L = 1.58Ω, $I_{g(REF)}$ = 1.0mA (Figure13)	-	20	24	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	11	13.5	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	0.68	0.85	nC
Gate to Source Gate Charge	Q_{gs}			-	1.8	-	nC
Reverse Transfer Capacitance	Q_{gd}			-	5	-	nC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)	-	350	-	pF
Output Capacitance	C_{OSS}		-	150	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	39	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 19A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 19A, dI_{SD}/dt = 100A/µs	-	-	50	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 19A, dI_{SD}/dt = 100A/µs	-	-	70	nC

Typical Performance Curves

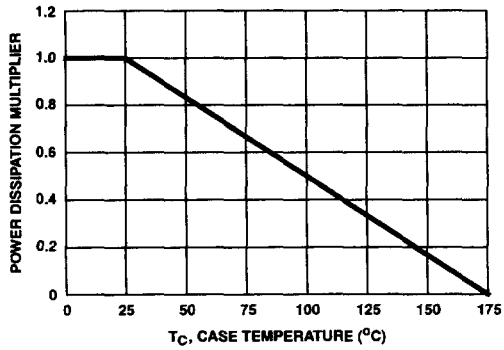


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

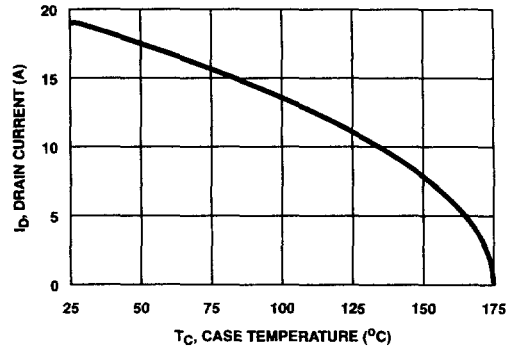


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

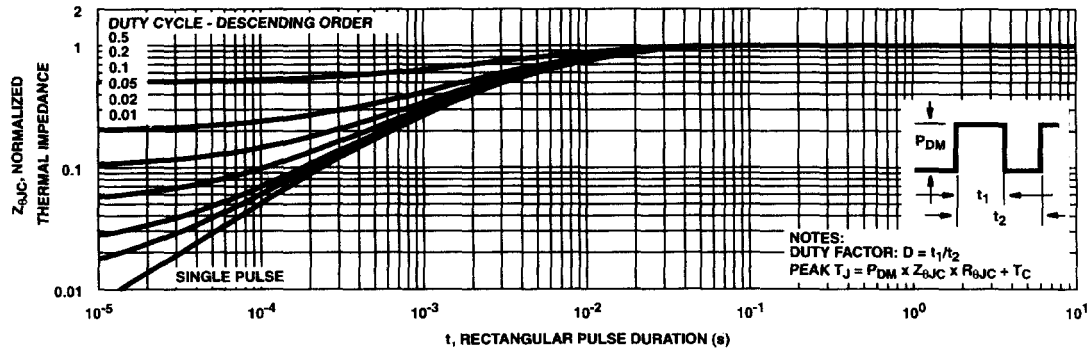


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves (Continued)

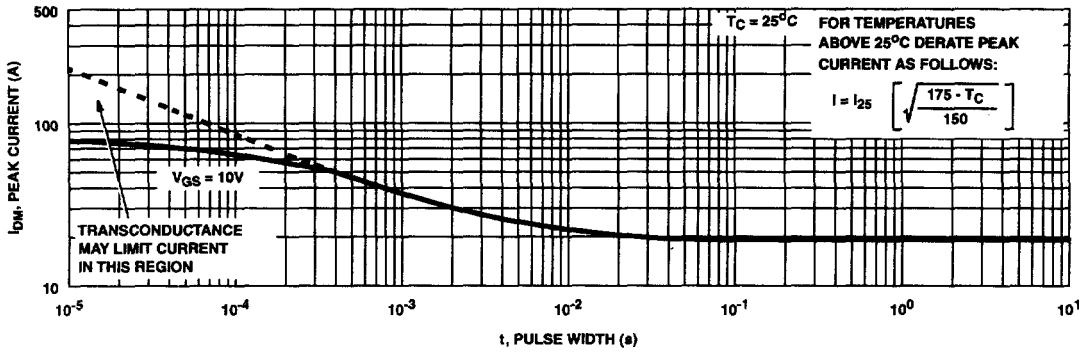


FIGURE 4. PEAK CURRENT CAPABILITY

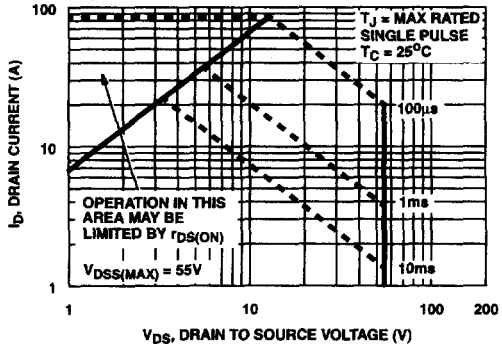
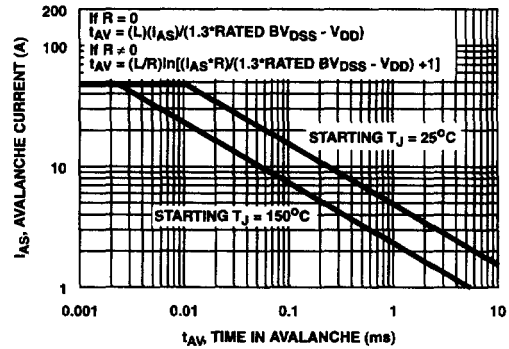


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

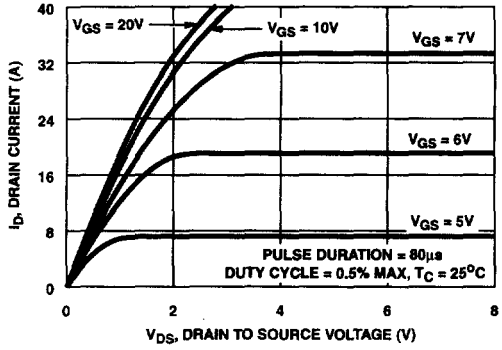


FIGURE 7. SATURATION CHARACTERISTICS

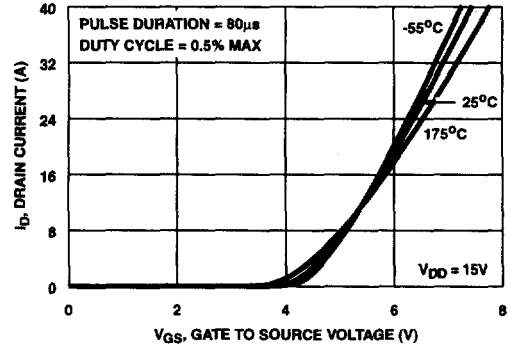


FIGURE 8. TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

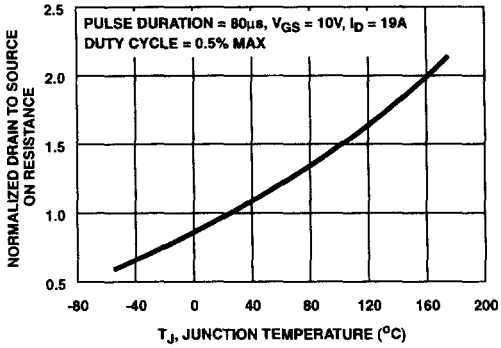


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

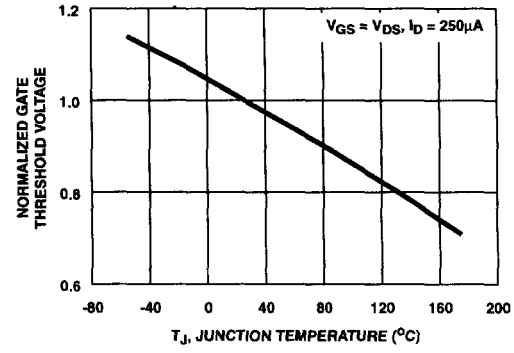


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

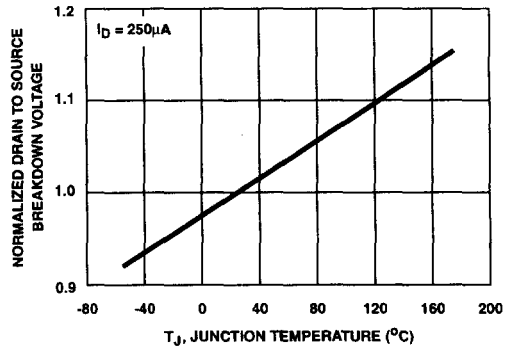


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

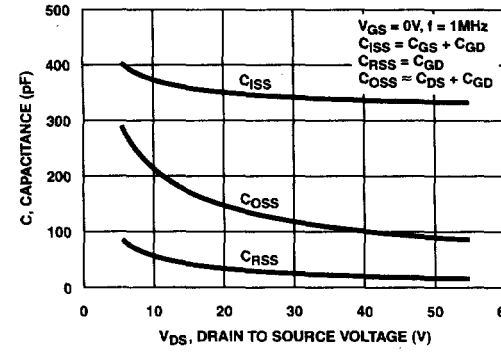
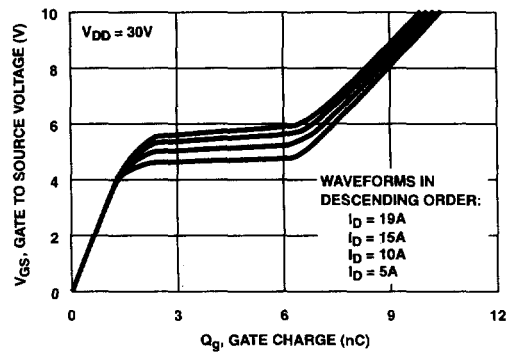


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT