M5M482128AJ,TP,RT-7,-8,-10

FAST PAGE MODE 1048576-BIT DUAL-PORT DYNAMIC RAM

DESCRIPTION

M5M482128AJ, TP, RT is a high speed 1048576-bit Dual Port Dynamic Memory equipped with a 128K x 8 Dynamic RAM Port and a 256x8 Serial Read/Write Port. High performance CMOS process using triple-layer poly-silicon and silicide technology provide both high circuit density and low power dissipation.

The Serial Read/Write Ports are connected to an internal 2048 bit Data Register through a 256 x 8 Serial Input/Output control circuit and can be serially read out or written in with a clock rate of up to 33MHz.

All reads and writes are done relative to the RAM array, thus data transfer from the RAM array to the Data Register is referred to as a Read Transfer, while data transfer from the Data Register to the RAM array is referred to as a Write Transfer.

FEATURES

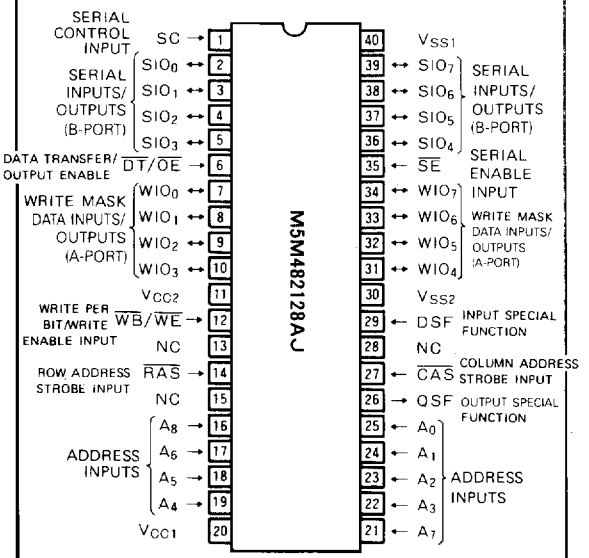
Type name	$\overline{RAS}$ Access Time (ns)	Random Read/Write Cycle Time (ns)	Serial Read Cycle Time (ns)	Random Read V_{CC} Supply Current (mA)	Serial Read/Write V_{CC} Supply Current (mA)
M5M482128 AJ, TP, RT-7	70	130	30	85	40
M5M482128 AJ, TP, RT-8	80	150	30	75	40
M5M482128 AJ, TP, RT-10	100	180	30	65	40

- Dual Port Architecture
  - RAM Port: 128K word x 8 bit
  - Serial Port: 256 word x 8 bit
- Bidirectional Data Transfer function between the RAM array and the Data Register.
- Fully Asynchronous Dual Port Accessability (Split SAM)
- Addressable Start of Serial Read/Write (Pointer Control Function)
- Write per Bit Function
- Real Time Data Transfer from the RAM Array to the Data Register
- Fast Page Mode, Hidden Refresh and $\overline{CAS}$ before $\overline{RAS}$ Refresh
- 512 cycle/8ms Refresh
- Flash write operation
- Block write operation

APPLICATION

Display equipment for personal computer/work station, Frame memory for digital TV/VCR, Videotex, Teletext, Video printer, High Speed data transmission systems

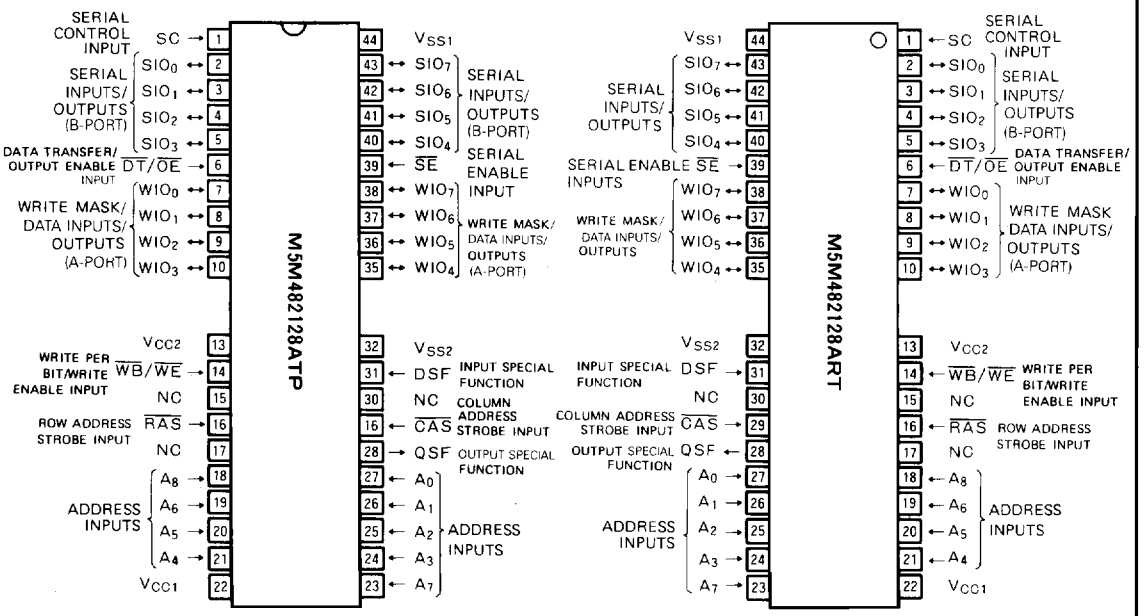
PIN CONFIGURATION (TOP VIEW)



Outline 40P0K (400 mil 40 pin SOJ)

NC: NO CONNECTION

PIN CONFIGURATION (TOP VIEW)

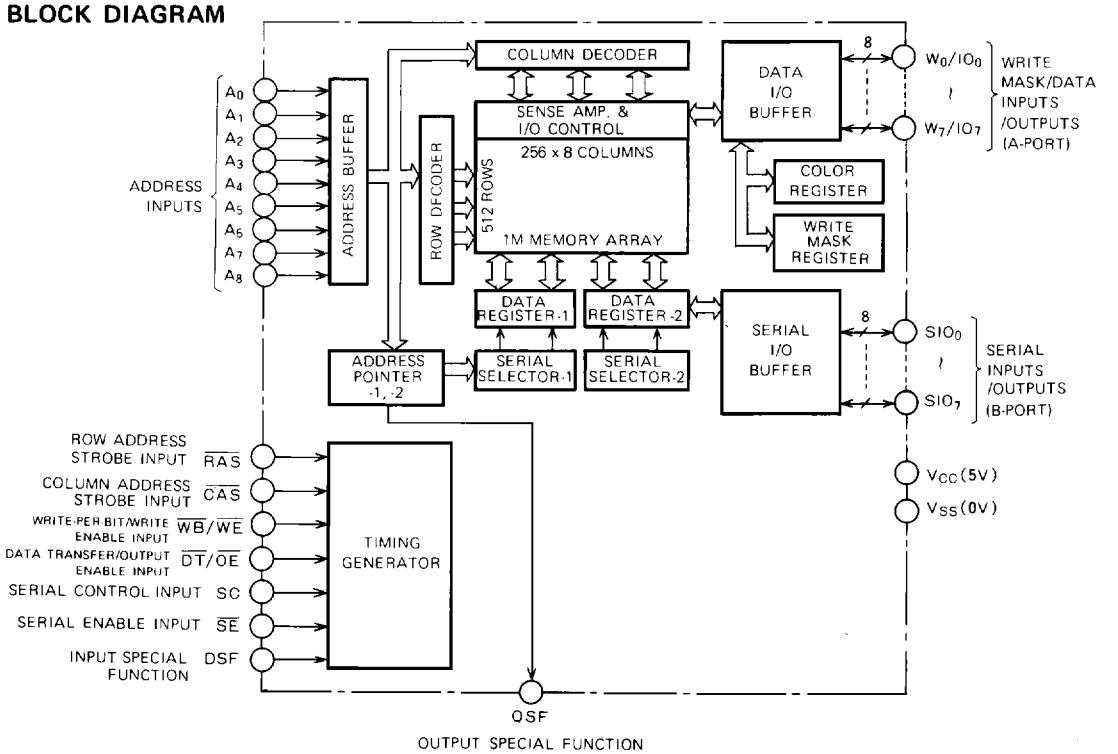


Outline 44P3W-L (400 mil 44 pin TSOP Nomal Bend Type)

Outline 44P3W-M (400 mil 44 pin TSOP Reverse Bend Type)

NC: NO CONNECTION

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin	Name	Function
$\overline{RAS}$	ROW ADDRESS STROBE INPUT	It is used as a clock which latches the row address ($A_0 \sim A_8$) to select the word line. It also latches the mask data for Write-per-bit, Flash write and Split write transfer functions when the $\overline{WB}$ level is low. $\overline{CAS}$ before $\overline{RAS}$ refresh mode is activated when preceeded by $\overline{CAS}$ falling low.
$\overline{CAS}$	COLUMN ADDRESS STROBE INPUT	It is used as a clock which latches the column address ($A_0 \sim A_7$) and initiates the reading or writing of the selected words. In the data transfer cycle, this latches the SAM Top address point. (TAP)
$A_0 \sim A_8$	ADDRESS INPUT	The M5M482128 utilizes an address multiplex method for selecting one word among the 128K-word memory cells. 9 row addresses and 8 column addresses are latched by the $\overline{RAS}$ and $\overline{CAS}$ falling edge. In the data transfer cycle, this address input is also combined with the serial access start address. (TAP)
$\overline{WB}/\overline{WE}$	WRITE-PER-BIT / WRITE ENABLE INPUT	When the $\overline{WB}/\overline{WE}$ level is low at the $\overline{RAS}$ falling edge Write-per-bit (RAM write with mask), Write transfer with MASK or Flash write with MASK cycle is selected. When it is high, normal read/write, Read transfer or Load color register cycle is selected. This clock also controls early/late write mode at the $\overline{CAS}$ falling edge.
$\overline{DT}/\overline{OE}$	DATA TRANSFER / OUTPUT ENABLE INPUT	When the $\overline{DT}/\overline{OE}$ level is low at the $\overline{RAS}$ falling edge, the data transfer cycle is selected and when it is high, RAM read/write cycle, Load color register cycle or Flash write cycle is activated according to the $\overline{WB}/\overline{WE}$ and DSF combination. In the RAM read cycle, it enables the data output (RAM port).
WIOn*	WRITE MASK / DATA INPUT/OUTPUT	These are the data input/output pins to the RAM. During RAM write-per-bit cycle, Split write transfer cycle or Flash write cycle, high data input at the $\overline{RAS}$ falling edge enables the selected-bit (row) for write operation. In the write cycle, the data is latched at the falling edge of the $\overline{CAS}$ or the $\overline{WB}/\overline{WE}$ input, whichever is the later.
SC	SERIAL CONTROL INPUT	All serial access is initiated from the SC clock rising edge. In the serial read cycle, the output data is held until the next clock rise. Also in the serial write cycle, the data is latched at the SC clock rising edge.
SIOn*	SERIAL INPUT/OUTPUT	256 x 8 word serial data input/output pins.
$\overline{SE}$	SERIAL ENABLE INPUT	This enables the serial input/output. In the write transfer cycle when $\overline{SE}$ is high at the $\overline{RAS}$ falling edge, Pseudo transfer cycle is selected, and when it is low, Write transfer cycle is selected.
DSF	INPUT SPECIAL FUNCTION	This input defines special functions such as Split read/write transfer, Flash write, Block write and Load color register. When it is set low, the device works as a basic dual-port memory except for the Normal write transfer cycle masking mode.
QSF	OUTPUT SPECIAL FUNCTION	Output indicating the serial data selector status.

Note *: n = 0 ~ 7.

128Kx8 Truth Table

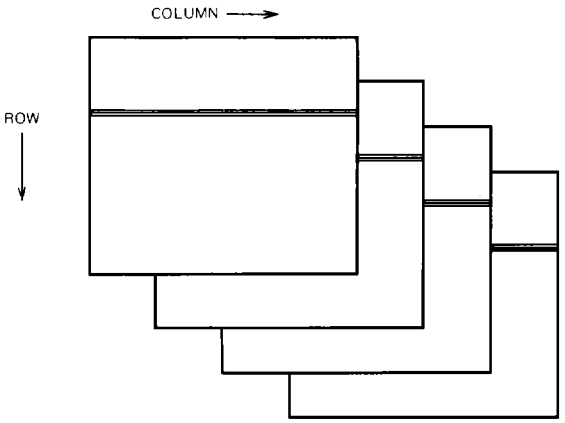
Code mnemonic	RAS falling edge							CAS falling edge				Write mask op.	Raster op.	Register			
	CAS	DT/OE	WB/WE	DSF	SE	Addr	WtOn	WB/WE	DSF	Addr	WtOn			Write mask temporary	Write mask persistant	Color	
CBR	0	0/1	0/1	0/1	—	—	—	—	—	—	—	—	—	—	—	—	C.B.R
MWT/PWT	1	0	0	0	0/1	Row/Ref	WM1	—	0	TAP	—	Yes per row	—	Load use	—	—	Wr. transfer (SE=0) Pseudo write transfer (SE=1)
	1	0	0	0	0/1	Row/Ref	WM1	—	1	TAP	—						
SWT	1	0	0	1	—	Row	WM1	—	0	TAP	—	Yes per row	—	Load use	—	—	Split write transfer with new mask
	1	0	0	1	—	Row	WM1	—	1	TAP	—						
RT	1	0	1	0	—	Row	—	—	0	TAP	—	—	—	—	—	—	Read transfer
	1	0	1	0	—	Row	—	—	1	TAP	—						
SRT	1	0	1	1	—	Row	—	—	0	TAP	—	—	—	—	—	—	Split read transfer
	1	0	1	1	—	Row	—	—	1	TAP	—						
RWNM	1	1	0	0	—	Row	WM1	*E/L	0	Col.	DQin	Yes	—	Load use	—	—	RAM write with new mask
BWNM	1	1	0	0	—	Row	WM1	—	1	Col.	Sel.	Yes	—	Load use	—	Use	Block write with new mask
FWT	1	1	0	1	—	Row	WM1	—	0	—	—	Yes per row	—	Load use	—	—	Flash write with new mask
	1	1	0	1	—	Row	WM1	—	1	—	—						
RW	1	1	1	0	—	Row	—	*E/L	0	Col.	DQin	—	—	—	—	—	Read/Write
BW	1	1	1	0	—	Row	—	—	1	Col.	Sel.	—	—	—	—	Use	Block write with no mask
LCR	1	1	1	1	—	Ref	—	*E/L	0	—	CLR.	—	—	—	—	Load	Load color reg.
	1	1	1	1	—	Ref	—	*E/L	1	—	CLR.						

* E/L: Early write/Late write ** Ref: Refresh Address

FUNCTION

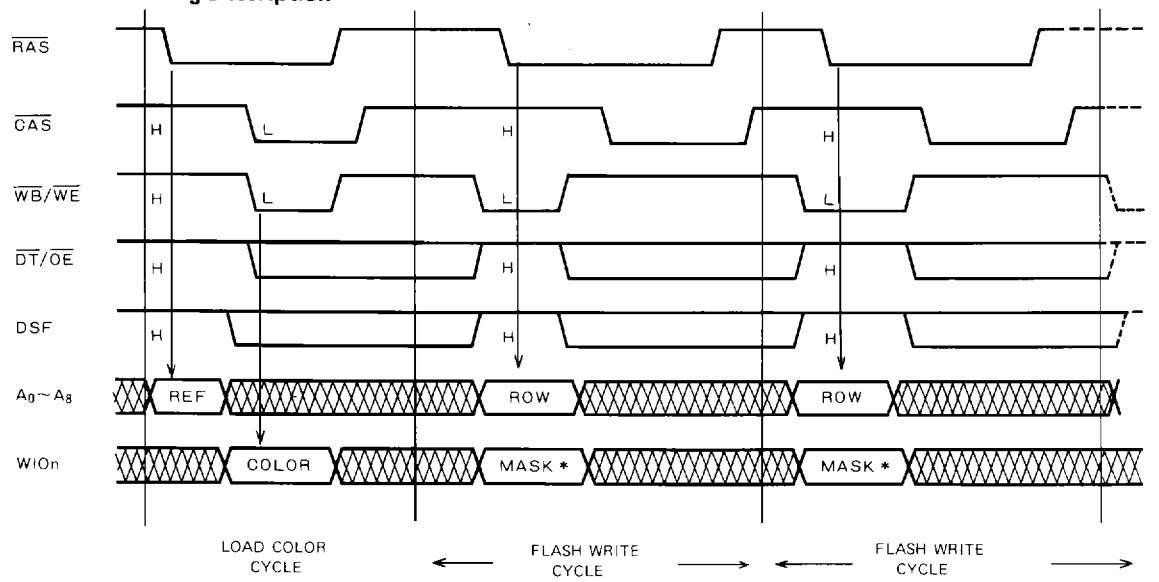
1. Flash Write

Utility: A high speed clear can be performed with flash write cycle.



* Write a color (0 or 1) to an entire row in one RAM cycle.
* Before flash write cycle, the color data must be set into an internal color register at least once.

Flash Write Timing Description

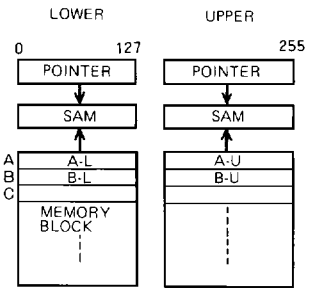


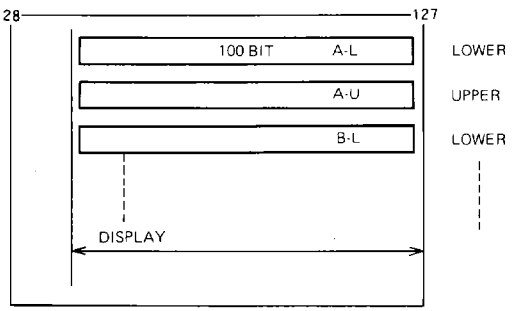
* The mask must be asserted on each flash write cycle.

2. Split Register

Utility

a. To simplify real time transfer timing (Fully asynchronous Serial Access)
b. Split Serial Register into two halves — To optimize the memory size to CRT.

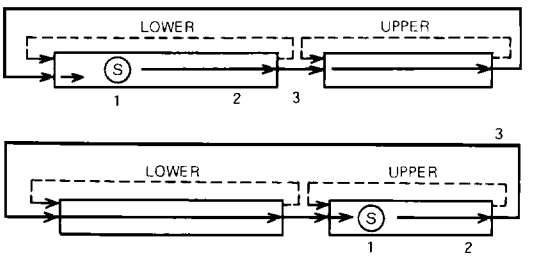




Pointer Path

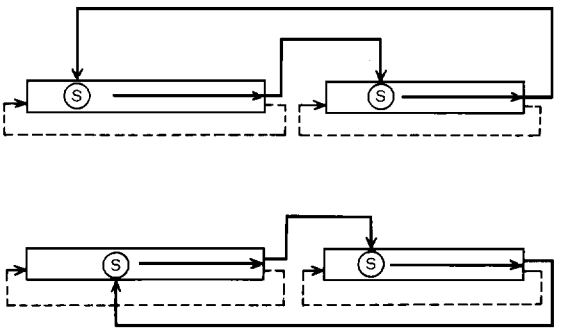
At Normal read transfer cycle

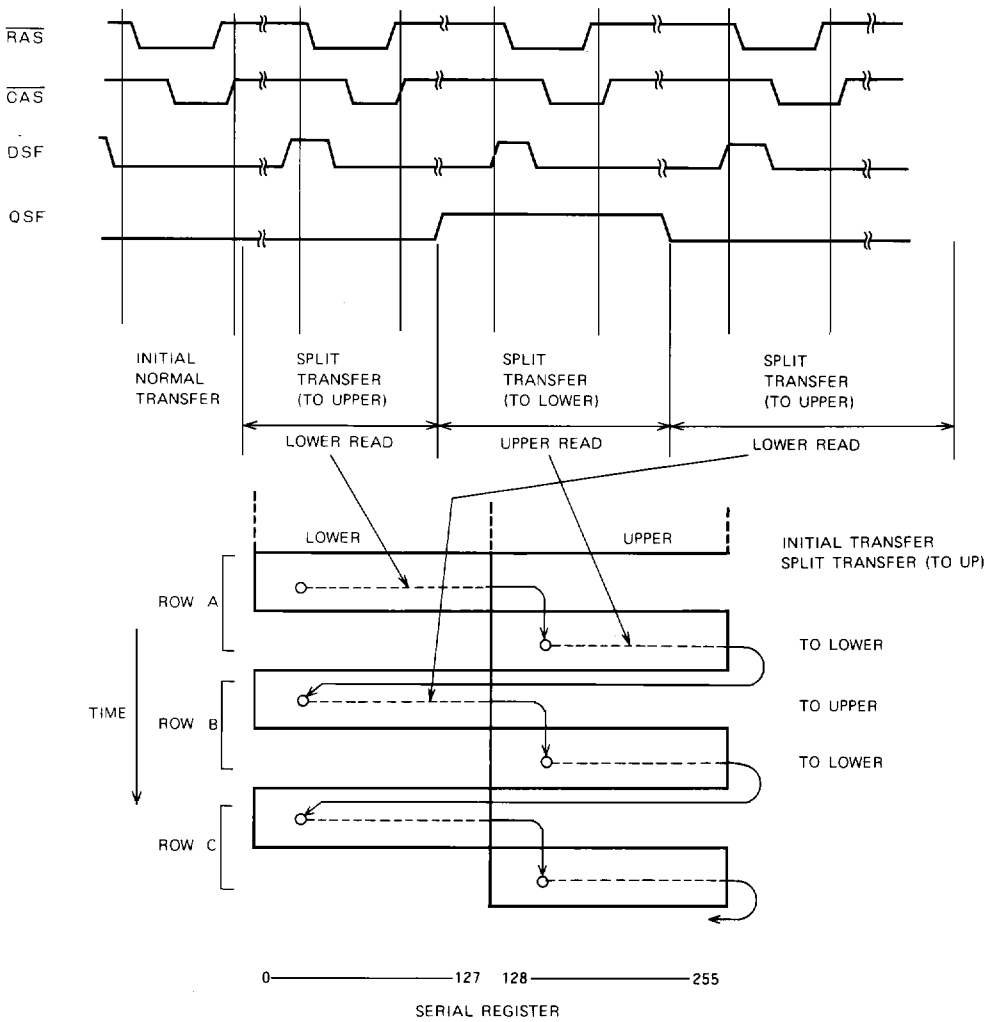
1. Transfer the data from RAM to SAM, and set the SAM start address among 256.
2. Start the Serial Read cycle.
3. Serial Read from Lower to Upper/Upper to Lower.
   (The pointer of the Lower/Upper SAM will be automatically cleared to address 0/128 after over-carried)



At Split and read transfer cycle

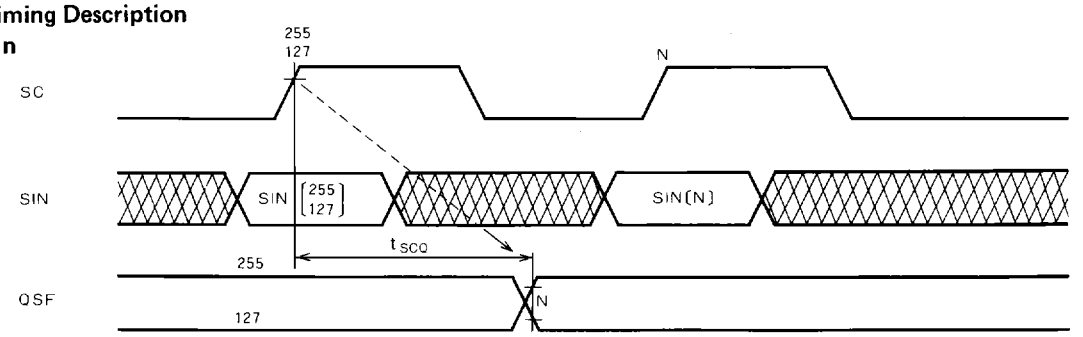
1. Normal transfer cycle must be performed prior to the split transfer cycle.
2. The data is transfered between the idle half of the SAM and the selected Row. At the same time the idle SAM's start address is set to give the next start address after the end of the busy SAM.
3. At the split transfer mode, data is transfered to the idle half of the SAM automatically. (Column A_7 is ignored.)
4. QSF indicates the busy SAM.
   (Lower Half SAM is busy: 0,
   Upper Half SAM is busy: 1)
5. Serial Read can be performed asynchronously during RAM cycle and Split transfer cycle.



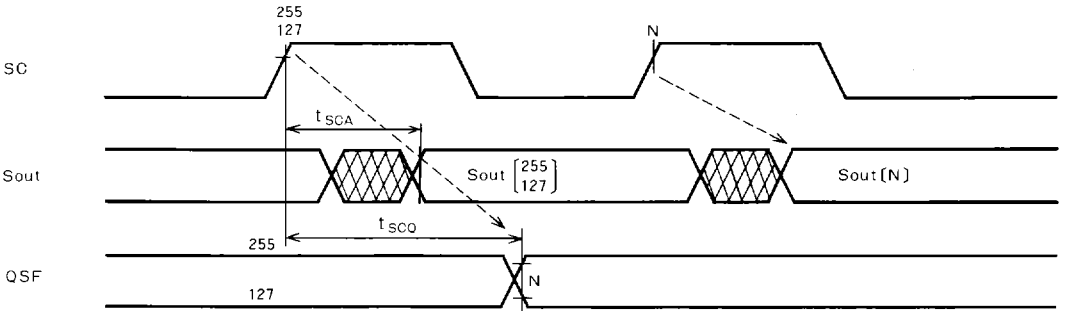


QSF Timing Description

Serial-In



Serial-Out



Data transfer mode	SIO mode	SAM TAP	Data transfer	QSF set
Normal read transfer	Output	Col. (A_0~A_7)	RAM→SAM	A_7
Normal write transfer	Input	Col. (A_0~A_7)	SAM→RAM	A_7
Pseudo write transfer	Input	Col. (A_0~A_7)	—	A_7
Split read transfer	Not effect	Col. (A_0~A_6)	RAM→SAM *1	—
Split write transfer	Not effect	Col. (A_0~A_6)	SAM→RAM *1	—

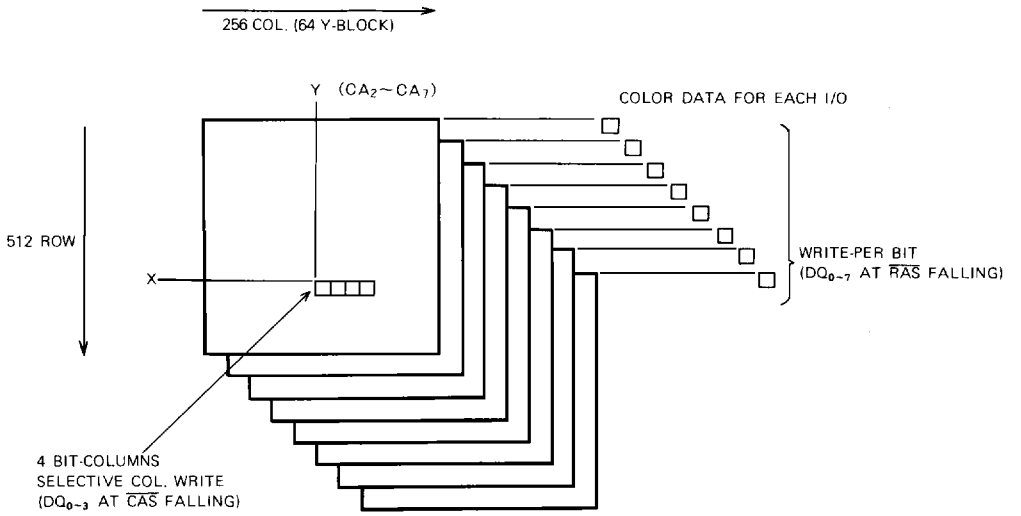
*1. If QSF = 0 then the upper half data (128 ~ 255) is transfered.
If QSF = 1 then the lower half data (0 ~ 127) is transfered.

3. Block Write

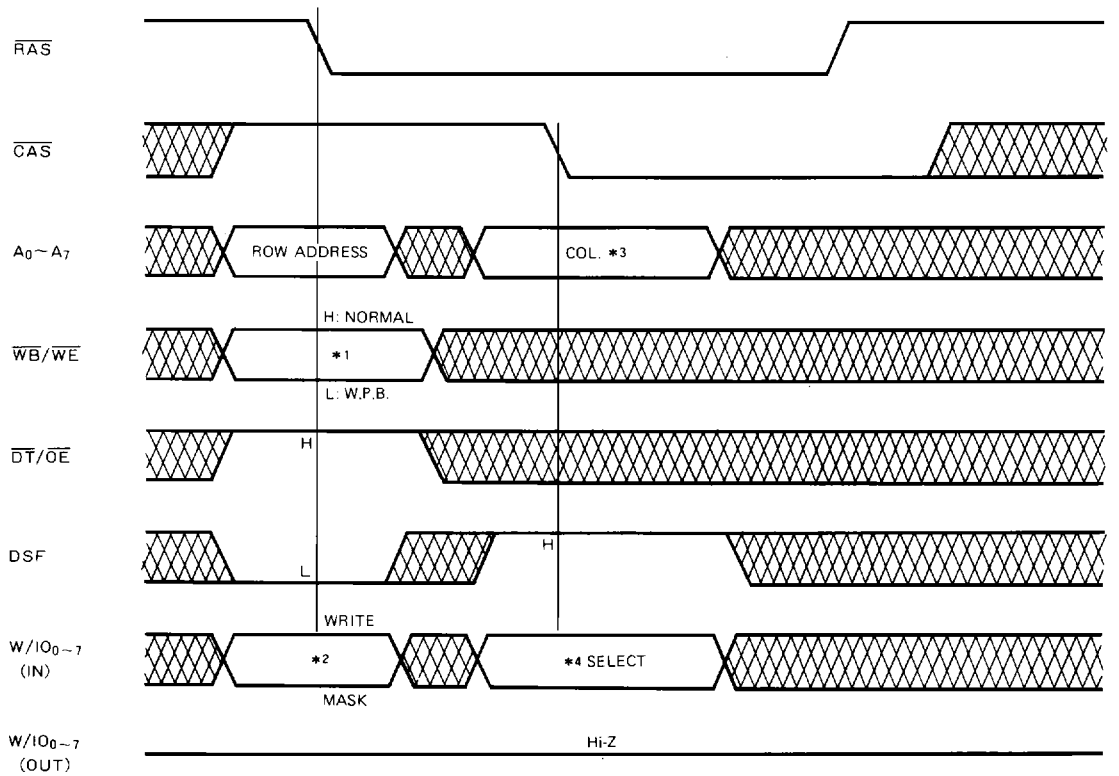
In the Block Write cycle, Data from the Color Register can be written into 4 bit-columns (which Blocks are selected with column address CA_2~CA_7) at one time. The $DQ_{0\sim3}$ the input at $\overline{CAS}$ falling edge enables a selective column write operation of the selected 4 bit-columns.
When $\overline{WB}/\overline{WE}$ is low at $\overline{RAS}$ falling edge Write-per-bit operation applies to the writing of color data.
The Color Register must be loaded prior to the Block Write cycle.

Application

Block Write operation is useful for the partial-clearing or partial-painting of a bit-map display with same color data. With the selective-column writing of data, any of the 4 bit-columns can be masked, so allowing the boundary treatment in the same cycle.



Block Write Timing Description

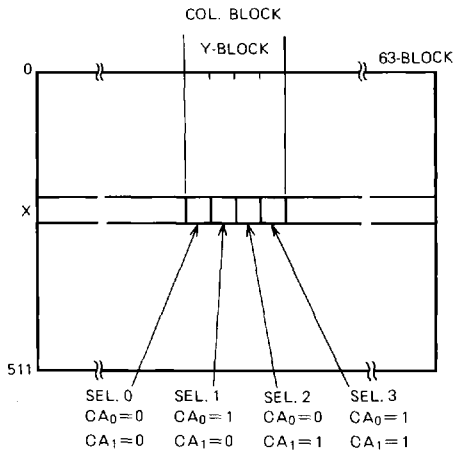


*1: H; No mask
L; Write per bit operation
*2: H; Write enable (No mask)
L; Disable (mask)
*3: Column address $CA_2 \sim CA_7$; CA_0, CA_1 = Don't care (H/L fixed)

Only when $\overline{WB}/\overline{WE}$ is low at $\overline{RAS}$ falling edge

*4: Select W/IO_0; $CA_0=0$, $CA_1=0$
W/IO_1; $CA_0=1$, $CA_1=0$
W/IO_2; $CA_0=0$, $CA_1=1$
W/IO_3; $CA_0=1$, $CA_1=1$

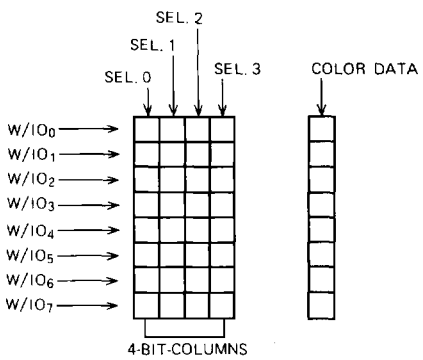
H; Write enable (no mask)
L; Disable (mask)



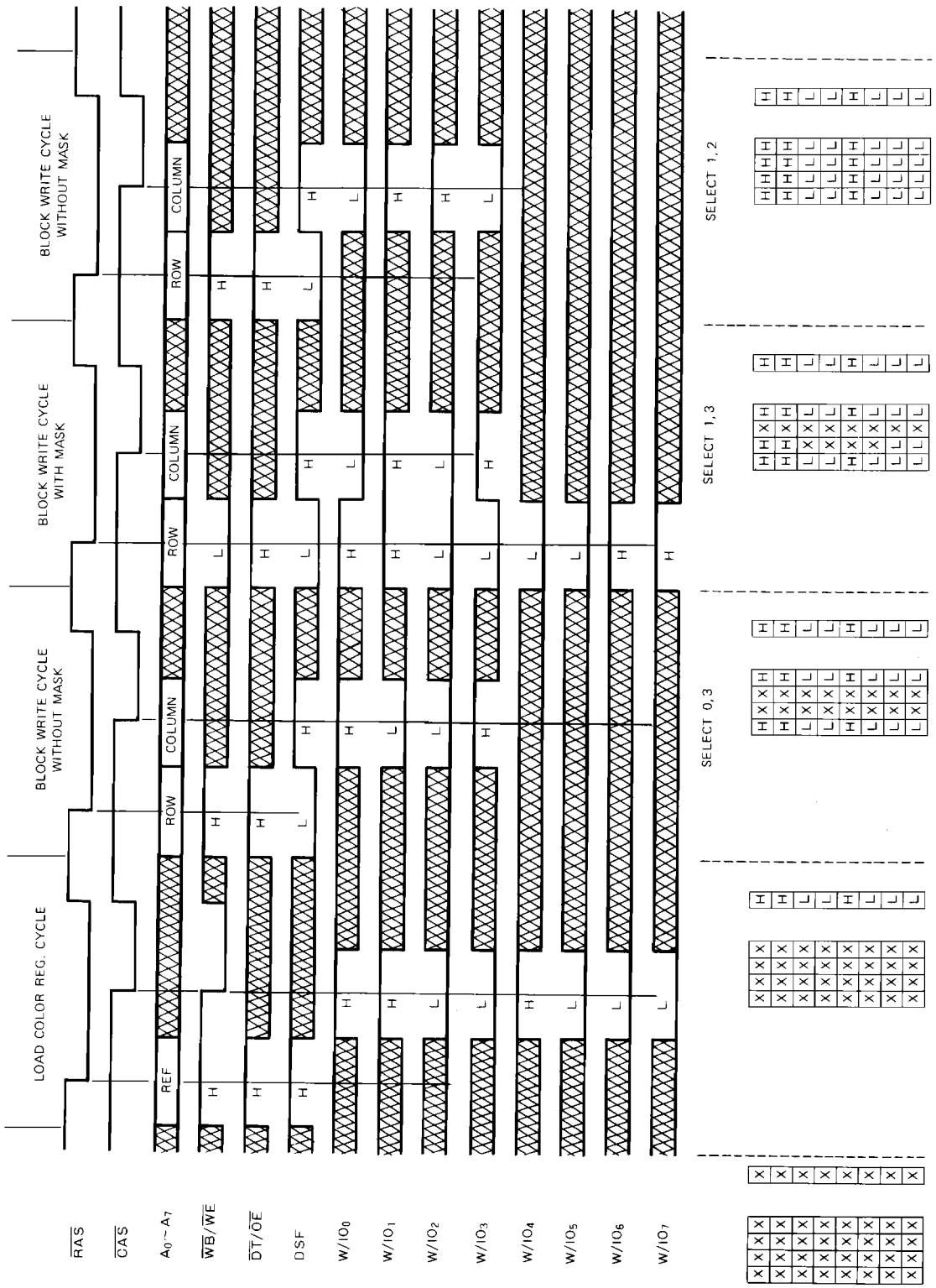
A_0, A_1 and W/IO_{4-7} at $\overline{CAS}$ falling edge, are "don't care", but must be set H or L state.

Example of Block Write Operation

'X' indicates pre-state, 'H'; high level (1), 'L'; low level (0).



Example



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1～7	V
V_I	Input voltage		−1～7	V
V_O	Output voltage		−1～7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta＝25°C	1000	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Norm	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input	2.4		6.5	V
V_{IL}	Low-level input	−1.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{OH(R)}$	High level output (RAM port)	$I_{OH(R)}$＝−1mA	2.4		V_{CC}	V
$V_{OL(R)}$	Low level output (RAM port)	$I_{OL(R)}$＝2.1mA	0		0.4	V
$V_{OH(S)}$	High level output (Serial I_O port)	$I_{OH(S)}$＝−1mA	2.4		V_{CC}	V
$V_{OL(S)}$	Low level output (Serial I_O port)	$I_{OL(S)}$＝2.1mA	0		0.4	V
I_{OZ}	Off-state output current	Q Floating 0＜V_{out}＜V_{CC}	−10		10	μA
I_I	Input current	0＜V_{in}＜V_{CC}	−10		10	μA

Note 2: Current flowing into an IC is positive, out is negative.

CAPACITANCE (Ta＝25°C, f＝1MHz, V_I＝25mVmrs)

Symbol	Pin name	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN0}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, SC, $\overline{SE}$, $\overline{DT}/\overline{OE}$, DSF	V_I＝V_{SS}, f＝1MHz, V_I＝25mVrms			7	pF
C_{IN1}	A_0～A_8				7	pF
C_O	WIO_0～WIO_7, SIO_0～SIO_7, QSF				9	pF

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			M5M482128A-7	M5M482128A-8	M5M482128A-10	
	RAM port	SAM port	Max	Max	Max	
I_{CC1}	Random R/W cycle, $\overline{RAS}$/$\overline{CAS}$ cycling, t_{RC} = min (Note 3, 4)	Standby ($\overline{SC}$ = V_{IL})	85	75	65	mA
I_{CC2}	Standby, $\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = Hi-Z		5	5	5	mA
I_{CC3}	$\overline{RAS}$ only refresh cycle, $\overline{RAS}$ = cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min (Note 3, 4)		85	75	65	mA
I_{CC4}	Page mode cycle, $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{PC} = min (Note 3, 4)		75	65	55	mA
I_{CC5}	$\overline{CAS}$ before $\overline{RAS}$ refresh, t_{RC} = min (Note 3, 4)		85	75	65	mA
I_{CC6}	Data transfer cycle, t_{RC} = min (Note 3, 4)		85	75	65	mA
I_{CC7}	Random R/W cycle, $\overline{RAS}$/$\overline{CAS}$ cycling, t_{RC} = min (Note 3, 4)	Active (t_{SCC} = min)	115	105	95	mA
I_{CC8}	Standby, $\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = Hi-Z (Note 3, 4)		40	40	40	mA
I_{CC9}	$\overline{RAS}$ only refresh cycle, $\overline{RAS}$ = cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min (Note 3, 4)		115	105	95	mA
I_{CC10}	Page mode cycle, $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{PC} = min (Note 3, 4)		105	95	85	mA
I_{CC11}	$\overline{CAS}$ before $\overline{RAS}$ refresh, t_{RC} = min (Note 3, 4)		115	105	95	mA
I_{CC12}	Data transfer cycle, t_{RC} = min (Note 3, 4)		115	105	95	mA

Note 3: I_{CC} 1, I_{CC3} ~ I_{CC12} are dependent on output loading. Specific values are obtained with the output open.
4: I_{CC} 1, I_{CC3} ~ I_{CC12} are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

SWITCH CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 12%, V_{SS} = 0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Limits						Unit
			M5M482128A-7		M5M482128A-8		M5M482128A-10		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 8)		20		20		25	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 9)		70		80		100	ns
t_{CAA}	Column address access time	(Note 6, 10)		35		40		50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 11)		40		45		55	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		20		20		25	ns
t_{CLZ}	Output low impedance from $\overline{CAS}$ low		5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	20	0	20	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	20	0	20	0	20	ns
t_{SCA}	Access time from $\overline{SC}$ high	(Note 7)		25		25		25	ns
t_{SOA}	Access time from $\overline{SE}$ low	(Note 7)	0	20	0	20	0	25	ns
t_{SOZ}	Output disable time after $\overline{SE}$ high	(Note 12)	0	20	0	20	0	20	ns
t_{SOH}	Serial output hold time after $\overline{SC}$ high		5		5		5		ns

Note 5: An initial pause of 500 μs is required after power up followed by eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock, such as $\overline{RAS}$ only refresh).
Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 8 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 1TTL loads and 50pF.
7: Measured with a load circuit equivalent to 1TTL loads and 30pF.
8: Assume that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max).
9: Assume that $t_{RCD} \geqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).
10: Assume that t_{RCD}-$t_{RAD} \geqq t_{CAA}$ (max)-t_{CAC} (min) and $t_{RCD} \geqq t_{RCD}$ (max).
11: Assume that $t_{CP} \leqq t_{CP}$(max).
12: t_{OFF}(max), t_{SOZ}(max) and t_{OEZ}(max) define the time at which output achieves high impedance state.

TIMING REQUIREMENTS ($Ta = 0 \sim 70℃$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Note 13, 14)

(1) Read, Write, Refresh, Load Color Register, Block Write, Flash Write Read/Write Transfer and Page Mode Cycles

Symbol	Parameter		Limits						Unit
			M5M482128A-7		M5M482128A-8		M5M482128A-10		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read, write cycle time		130		150		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width		70	10000	80	10000	100	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$		70		80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$		25		25		30		ns
t_{REF}	Refresh cycle time			8		8		8	ms
t_{RP}	$\overline{RAS}$ high pulse width		50		60		70		ns
t_{RCD}	Delay time $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	20	50	25	60	25	75	ns
t_{CRP}	Delay time $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 16)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		ns
t_{ASR}	Row address setup time before $\overline{RAS}$		0		0		0		ns
t_{RAH}	Row address hold time after $\overline{RAS}$		10		15		15		ns
t_{RAD}	Column address delay time from $\overline{RAS}$	(Note 17)	15	35	20	40	20	50	ns
t_{ASC}	Column address setup time before $\overline{CAS}$		0		0		0		ns
t_{CAH}	Column address hold time after $\overline{CAS}$		15		20		20		ns
t_{WSR}	$\overline{WB/WE}$ setup time before $\overline{RAS}$		0		0		0		ns
t_{RWH}	$\overline{WB/WE}$ hold time after $\overline{RAS}$		10		15		15		ns
t_{DTRS}	$\overline{DT/OE}$ setup time before $\overline{RAS}$		0		0		0		ns
t_{DTRH}	$\overline{DT/OE}$ high hold time after $\overline{RAS}$		10		15		15		ns
t_{FSR}	DSF setup time before $\overline{RAS}$		0		0		0		ns
t_{RFH}	DSF hold time after $\overline{RAS}$		10		15		15		ns
t_{FSC}	DSF setup time before $\overline{CAS}$		0		0		0		ns
t_{CFH}	DSF hold time after $\overline{CAS}$		15		20		20		ns
t_{WS}	Write mask setup time before $\overline{RAS}$		0		0		0		ns
t_{WH}	Write mask hold time after $\overline{RAS}$		10		15		15		ns
t_T	Transition time	(Note 18)	3	35	3	35	3	35	ns

Note 13: Timing requirements are assumed $t_T = 5ns$.
14: $V_{IH}(min)$ and $V_{IL}(max)$ are raference levels for measuring timing of input signals.
15: $t_{RCD}(max)$ limit ensures that $t_{RAC}(max)$ can be met. $t_{RCD}(max)$ is specified as a reference point only. If t_{RCD} is greater than $t_{RCD}(max)$, access time is controlled by t_{CAC} or t_{CAA} as shown in notes 7 or 9.
16: t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
17: $t_{RAD}(max)$ limit ensures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only. If t_{RAD} is grater than $t_{RAD}(max)$, access time is controlled by t_{CAC} or t_{CAA} as shown in notes 7 or 9.
18: t_T is measured between $V_{IH}(min)$ and $V_{IL}(max)$.

(2) Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M482128A-7		M5M482128A-8		M5M482128A-10		
			Min	Max	Min	Max	Min	Max	
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 19)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 19)	0		0		0		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time		35		40		50		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time		0		0		0		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low		20		25		25		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low		70		80		100		ns
t_{DOEL}	Delay time data to $\overline{OE}$ low		0		0		0		ns
t_{OEHD}	Delay time $\overline{OE}$ high to Data		15		15		20		ns
$t_{h(OECH)}$	$\overline{CAS}$ hold time after $\overline{OE}$ low		20		20		25		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low		20		20		25		ns

Note 19: Either t_{RCH} or t_{RRH} must be satisfied.

(3) Write Cycle (Eary Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M482128A-7		M5M482128A-8		M5M482128A-10		
			Min	Max	Min	Max	Min	Max	
t_{WCS}	Write setup time before $\overline{CAS}$	(Note 20)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$		15		15		15		ns
t_{CWL}	$\overline{CAS}$ hold time after write		20		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after write		20		20		25		ns
t_{WP}	Write pulse width		15		15		15		ns
t_{DSC}	Data setup time before $\overline{CAS}$		0		0		0		ns
t_{DHC}	Data hold time after $\overline{CAS}$		15		15		20		ns
t_{DSW}	Data setup time before write		0		0		0		ns
t_{DHW}	Data hold time after write		15		15		20		ns
t_{OEHD}	Delay time $\overline{OE}$ high to data		15		15		20		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write		15		15		20		ns

Note 20: t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} do not define the limits of operation, but are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$, early write cycle is performed with data outputs keeping high impedance state. If $t_{RWD} \geq t_{RWD(min)}$, $t_{CWD} \geq t_{CWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, read-write cycle is performed with the data of the selected address being out from the data output. If neither of the above condition is satisfied, the condition of data out (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indetermined.

(4) Read-Write and Read-Modify-Write Cycle

Symbol	Parameter	Limits						Unit
		M5M482128A-7		M5M482128A-8		M5M482128A-10		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read-write, read-modify-write cycle time	185		205		245		ns
t_{RAS}	$\overline{RAS}$ low pulse width	115	10000	125	10000	155	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	70	10000	70	10000	85	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$	115		125		155		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$	70		70		85		ns
t_{RCS}	Read setup time before $\overline{CAS}$	0		0		0		ns
t_{CWD}	Delay time $\overline{CAS}$ to write (Note 20)	40		40		50		ns
t_{RWD}	Delay time $\overline{RAS}$ to write (Note 20)	90		100		125		ns
t_{CWL}	$\overline{CAS}$ hold time after write	20		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after write	20		20		25		ns
t_{WP}	Write pulse width	15		15		15		ns
t_{DSW}	Data setup time before write	0		0		0		ns
t_{DHW}	Data hold time after write	15		15		20		ns
t_{AWD}	Delay time address to write (Note 20)	55		60		75		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$	20		20		25		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$	70		80		100		ns
t_{DOEL}	Delay-time data to $\overline{OE}$ low	0		0		0		ns
t_{OEHD}	Delay time $\overline{OE}$ high to data	15		15		20		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write	15		15		20		ns

(5) Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)

Symbol	Parameter	Limits						Unit
		M5M482128A-7		M5M482128A-8		M5M482128A-10		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Read, write cycle time	45		50		60		ns
t_{RWPC}	Read-write, read modify write cycle time	95		100		115		ns
t_{RASP}	$\overline{RAS}$ low pulse width	115	100000	135	100000	160	100000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	20	10000	25	10000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 21)	10	15	10	20	10	25	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$	25		25		30		ns

Note 21: t_{CP}(max) is specified as a reference point only. If $t_{CP}(max) \leqq t_{CP}$, access time is determined by t_{CAC}.

(6) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 22)

Symbol	Parameter	Limits						Unit
		M5M482128A-7		M5M482128A-8		M5M482128A-10		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$	15		15		20		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns

Note 22: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode

(7) Normal-Read/Normal-Write/Pseudo-Write Transfer Cycle

Symbol	Parameter	Limits						Unit
		M5M482128A-7		M5M482128A-8		M5M482128A-10		
		Min	Max	Min	Max	Min	Max	
t_{RDH}	$\overline{DT}/\overline{OE}$ low hold time after $\overline{RAS}$	10	10000	15	10000	15	10000	ns
t_{RSD}	Delay time $\overline{RAS}$ to SC	80		80		100		ns
t_{ASD}	Delay time address to SC	40		40		50		ns
t_{CSD}	Delay time $\overline{CAS}$ to SC	30		30		30		ns
t_{SDH}	SC hold time after $\overline{DT}$	15		15		15		ns
t_{RQ}	Delay time $\overline{RAS}$ to QSF		85		85		85	ns
t_{AQ}	Delay time address to QSF		40		40		40	ns
t_{CQ}	Delay time $\overline{CAS}$ to QSF		35		35		35	ns
t_{DTQ}	Delay time $\overline{DT}$ to QSF		25		25		25	ns
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ precharge time	70		80		90		ns
t_{DTW}	$\overline{DT}$ high pulse width	30		30		30		ns
t_{ES}	$\overline{SE}$ setup time before $\overline{RAS}$ low	0		0		0		ns
t_{EH}	$\overline{SE}$ hold time after $\overline{RAS}$ low	15		15		15		ns
t_{SRS}	Last SC to $\overline{RAS}$ setup time (serial input)	30		30		30		ns
t_{SRH}	$\overline{RAS}$ to first SC delay time (serial input)	20		20		20		ns
t_{SZS}	Serial input to first SC delay time (serial in → serial out)	0		0		0		ns
t_{SDZ}	Serial output turn-off delay from $\overline{RAS}$ (serial out → serial in)	10	50	10	50	10	50	ns
t_{SDP}	$\overline{RAS}$ to serial input delay time (serial out → serial in)	50		50		50		ns

(8) Real Time Read Transfer Cycle

Symbol	Parameter	Limits						Unit
		M5M482128A-7		M5M482128A-8		M5M482128A-10		
		Min	Max	Min	Max	Min	Max	
t_{RDH}	$\overline{DT}$ hold time after $\overline{RAS}$	55	10000	65	10000	80	10000	ns
t_{CDH}	$\overline{DT}$ hold time after $\overline{CAS}$	30		30		30		ns
t_{ADH}	$\overline{DT}$ hold time after address	30		30		30		ns
t_{SDD}	Delay time SC to $\overline{DT}$	5		5		5		ns
t_{SDH}	SC hold time after $\overline{DT}$	15		15		15		ns
t_{DTQ}	Delay time $\overline{DT}$ to QSF		25		25		25	ns

(9) Split Read/Write Transfer Cycle

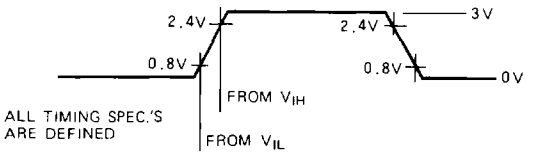
Symbol	Parameter	Limits						Unit
		M5M482128A-7		M5M482128A-8		M5M482128A-10		
		Min	Max	Min	Max	Min	Max	
t_{SCSR}	Split transfer setup time	30		30		30		ns
t_{SCHR}	Split transfer hold time	30		30		30		ns

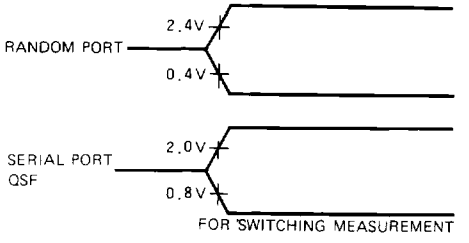
(10) Serial Read/Serial Write Cycle

Symbol	Parameter	Limits						Unit
		M5M482128A-7		M5M482128A-8		M5M482128A-10		
		Min	Max	Min	Max	Min	Max	
t_{SCC}	SC clock cycle time	30		30		30		ns
t_{SCH}	SC high pulse width	10		10		10		ns
t_{SCL}	SC low pulse width	10		10		10		ns
t_{SOP}	$\overline{SE}$ high pulse width	25		25		25		ns
t_{SOE}	$\overline{SE}$ low pulse width	25		25		25		ns
t_{SIS}	Serial input data setup time bafore SC high	0		0		0		ns
t_{SIH}	Serial input data hold time after SC high	15		15		15		ns
t_{SWIS}	$\overline{SE}$ disable setup time before SC high	5		5		5		ns
t_{SWIH}	$\overline{SE}$ disable hold time after SC high	15		15		15		ns
t_{SWS}	$\overline{SE}$ enable setup time before SC high	5		5		5		ns
t_{SWH}	$\overline{SE}$ enable hold time after SC high	15		15		15		ns
t_{SZE}	Serial input to $\overline{SE}$ delay time	0		0		0		ns
t_{SCQ}	Delay time SC to QSF		25		25		25	ns

Switching Measurement Condition

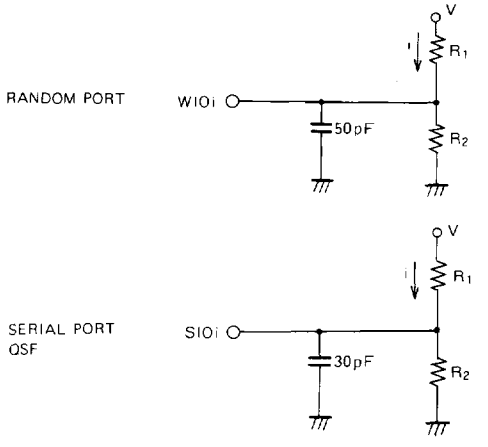
1. Input reference point





DC LEVEL OF OUTPUT IS V_{OH} = 2.4V, V_{OL} = 0.4V

3. Load condition



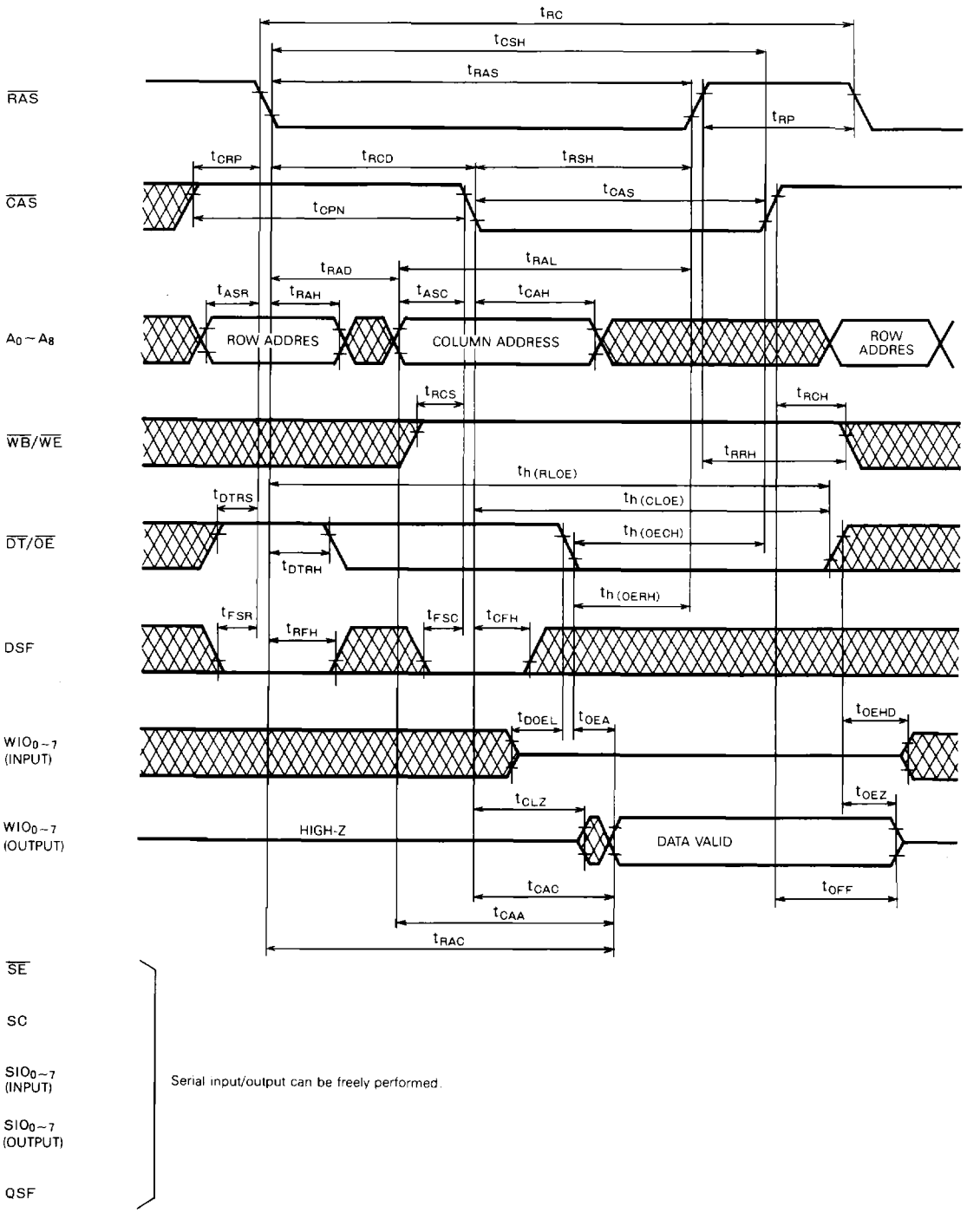
$$\left[\begin{array}{ll} V = V_{OH} + R_1 \cdot I_H & V = V_{OL} + R_1 \cdot I_L \\ V_{OH} = (I_H - I_{OH}) \cdot R_2 & V_{OL} = (I_L - I_{OL}) \cdot R_2 \\ \text{When } V = 5V,\ R_1 = 1838\,\Omega,\ R_2 = 994\,\Omega & \end{array}\right]$$

$$R_1 = \frac{V_{OH}(V - V_{OL}) - V_{OL}(V - V_{OH})}{V_{OH} \cdot I_{OL} - V_{OL} \cdot I_{OH}}$$

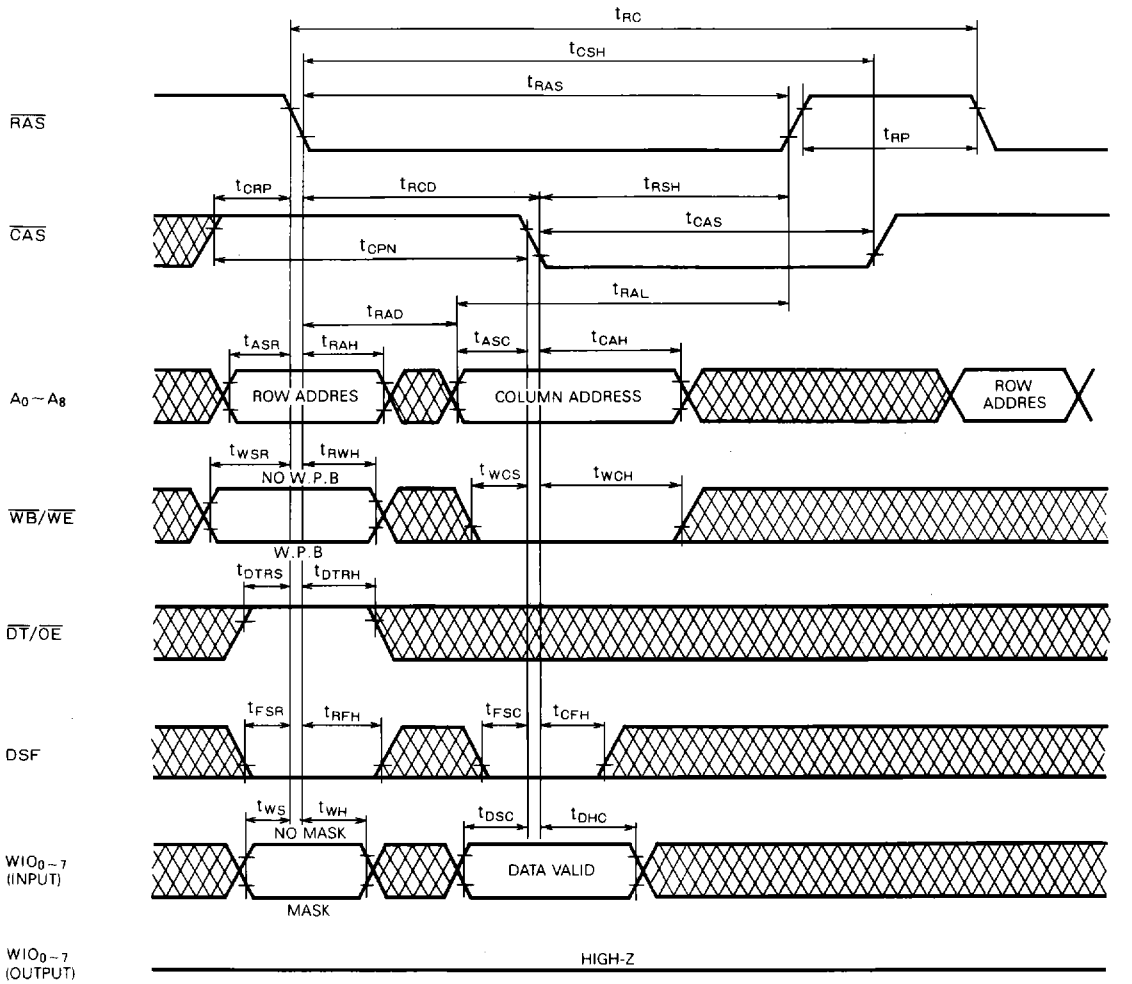
$$R_2 = \frac{V_{OH} \cdot R_1}{(V - V_{OH}) - I_{OH} \cdot R_1}$$

TIMING DIAGRAMS

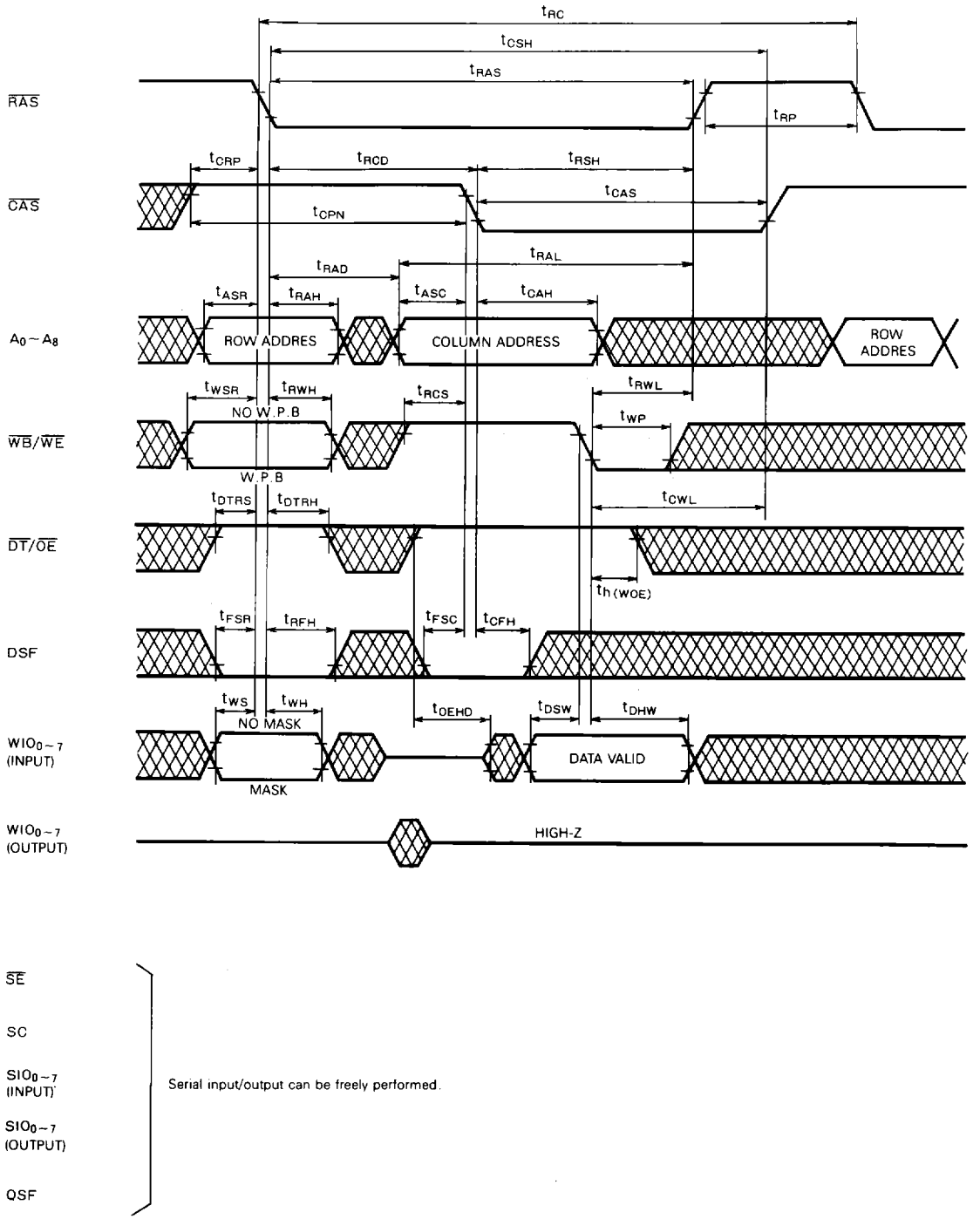
Read Cycle



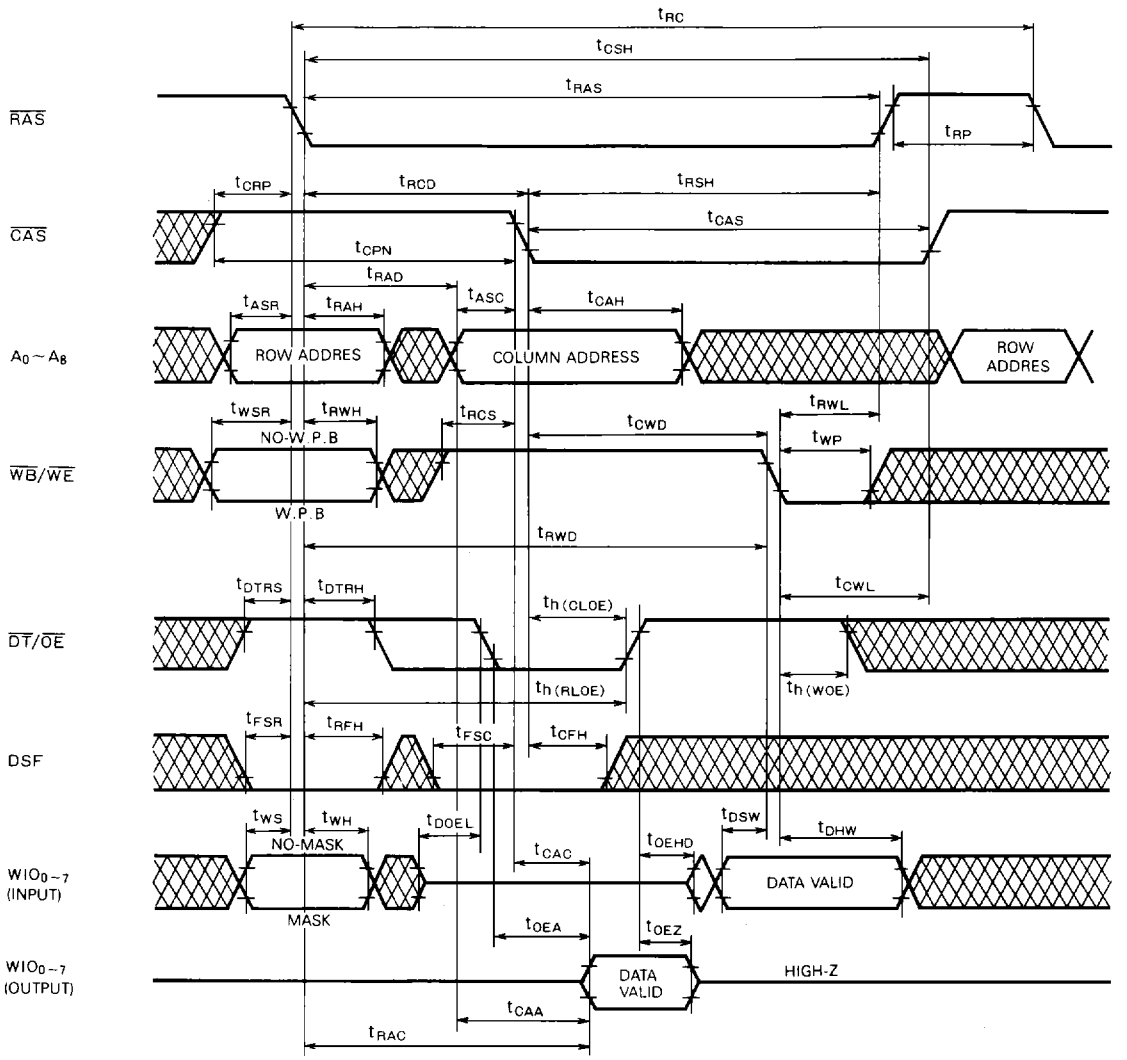
Write Cycle (Early Write)



Write Cycle (Late Write)

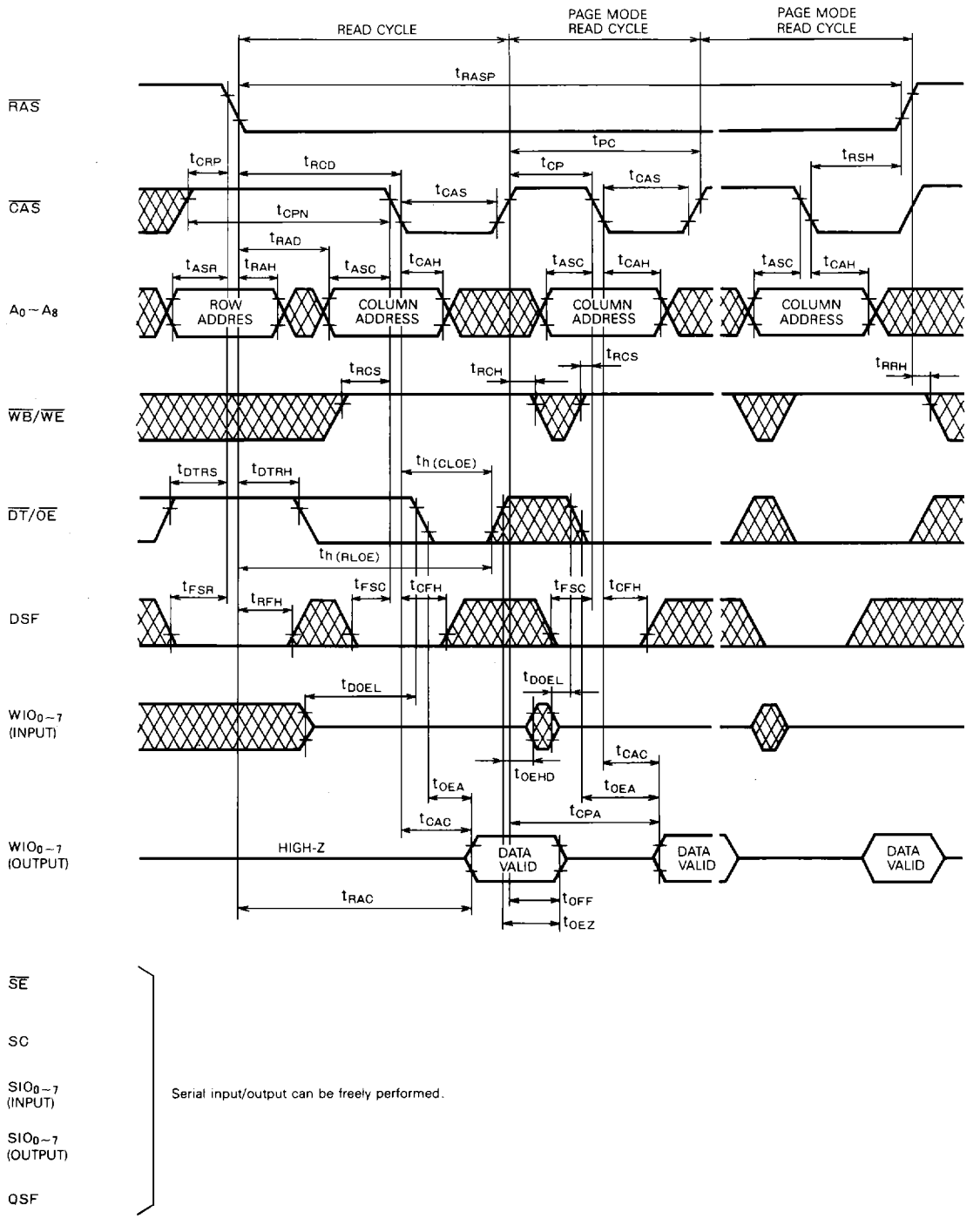


Read Modify Write Cycle

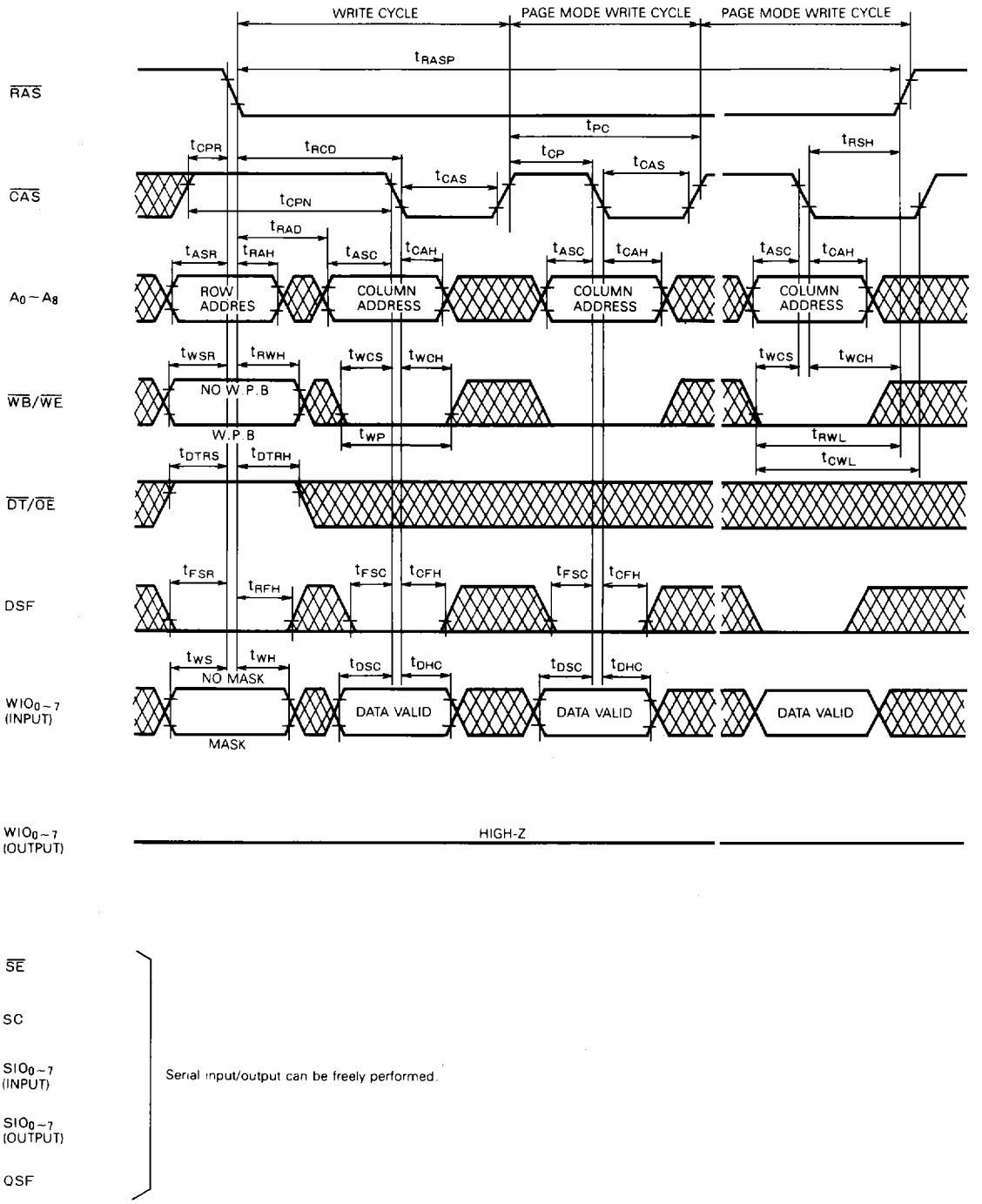


MITSUBISHI ELECTRIC

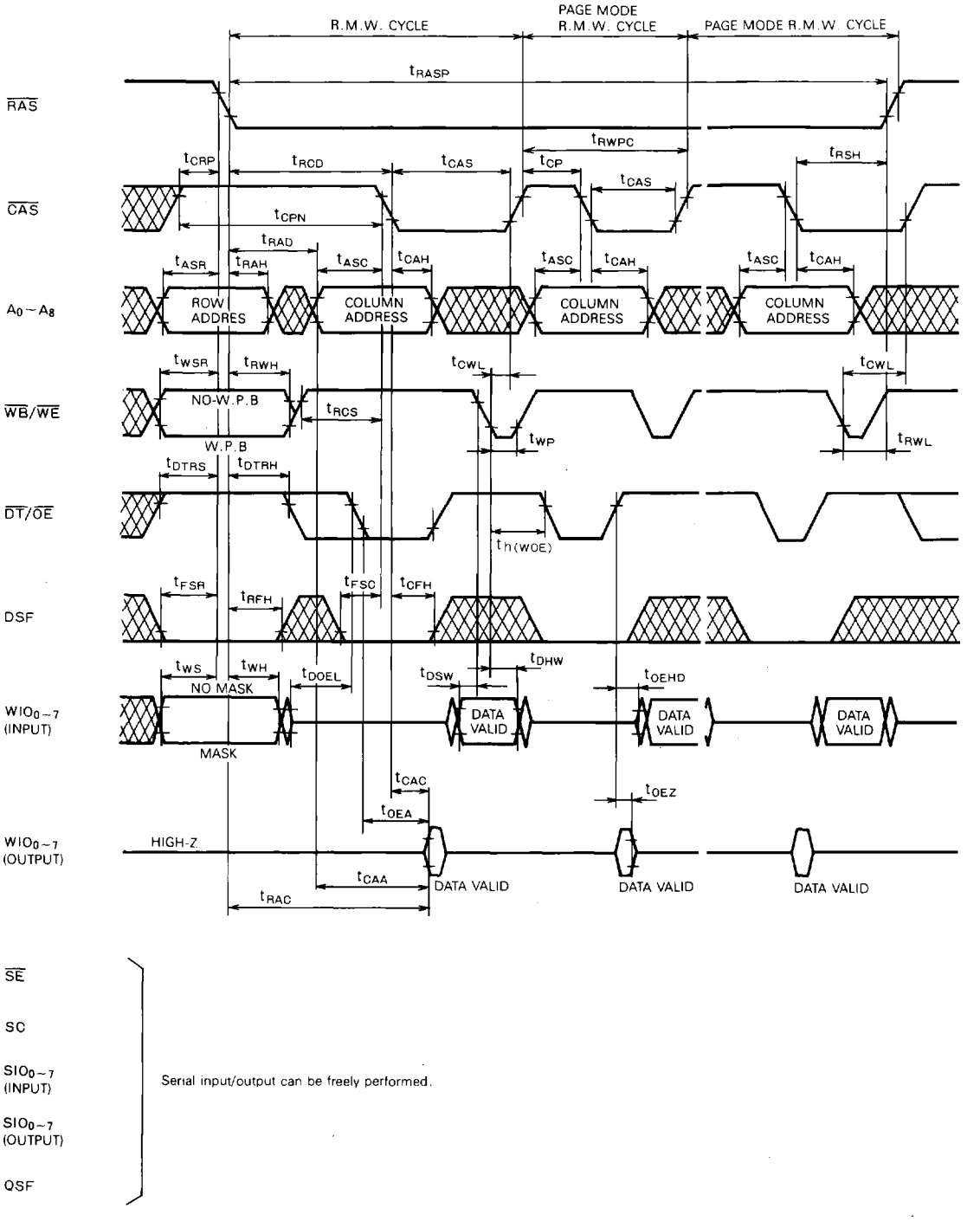
Page Mode Read Cycle



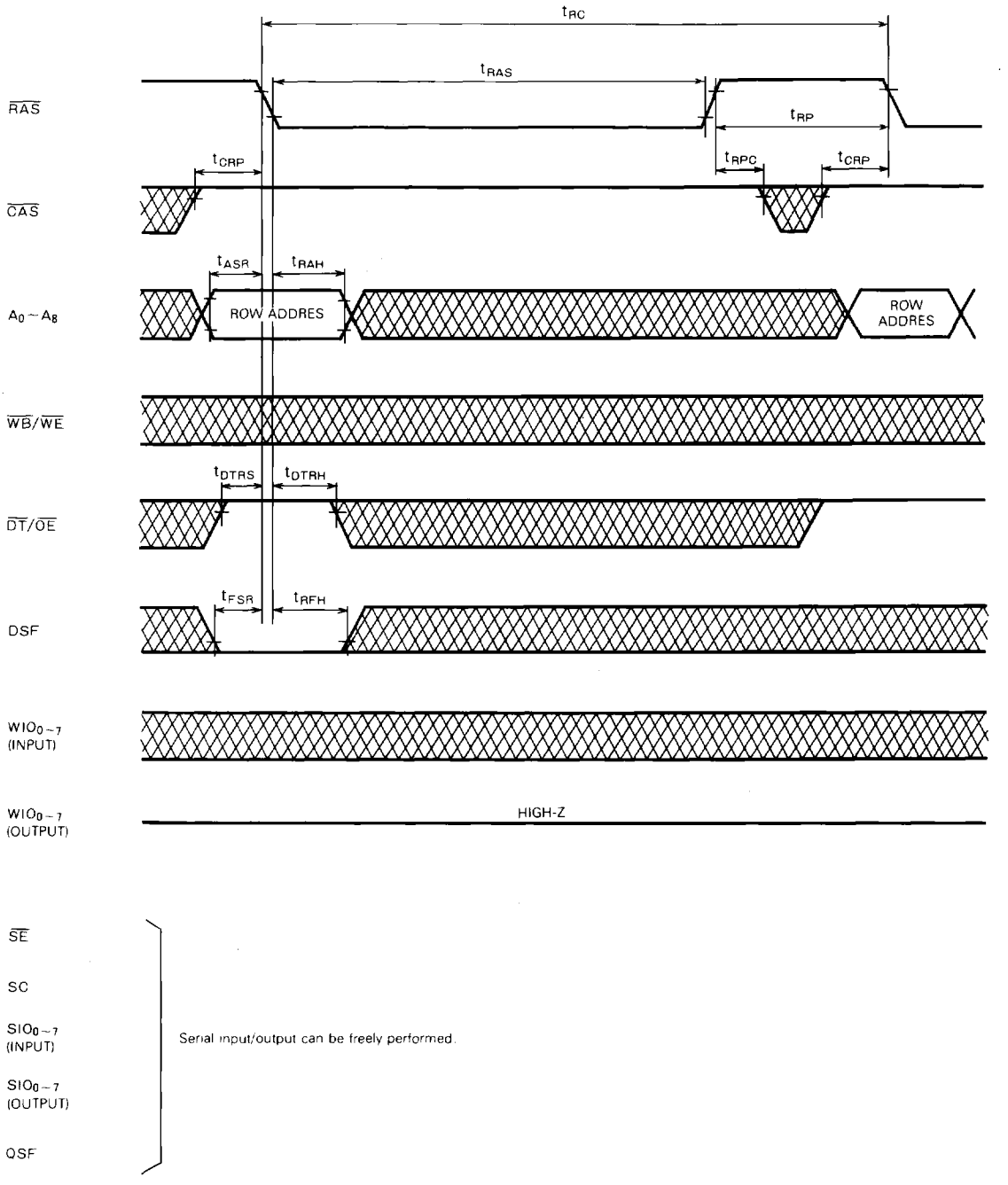
Page Mode Write Cycle (Early Write)



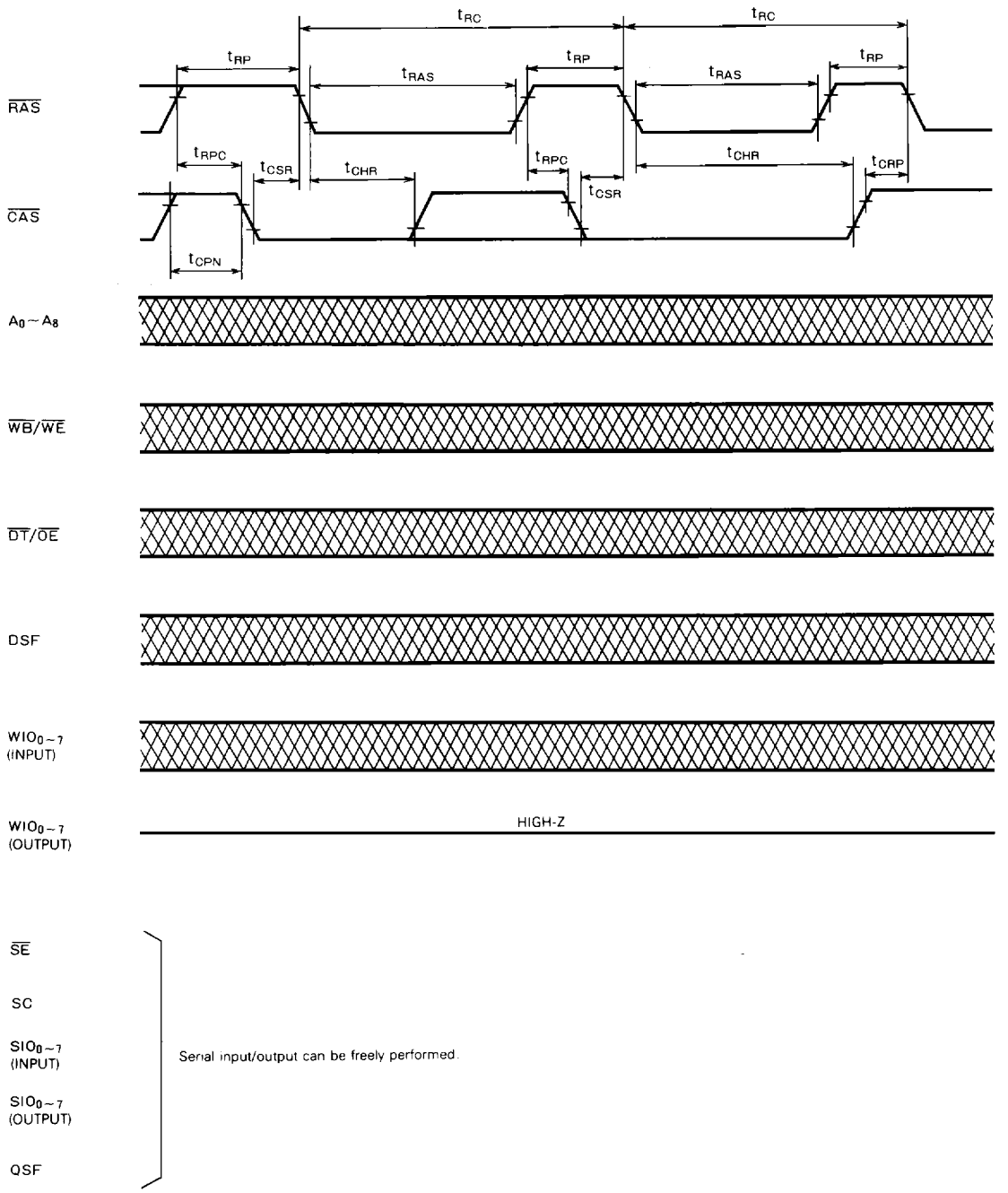
Page Mode Write Cycle (Read-Modify-Write)



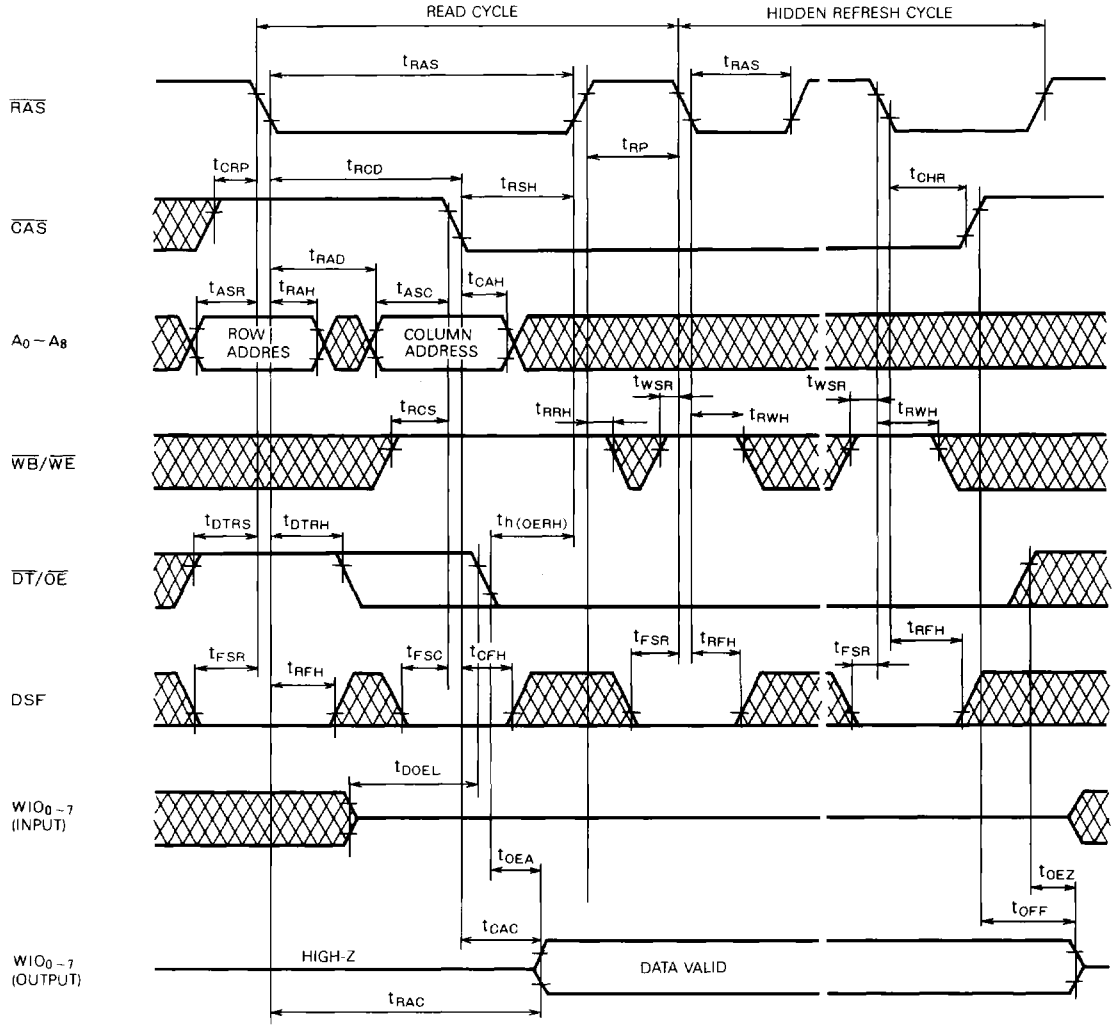
$\overline{RAS}$ Only Refresh Cycle



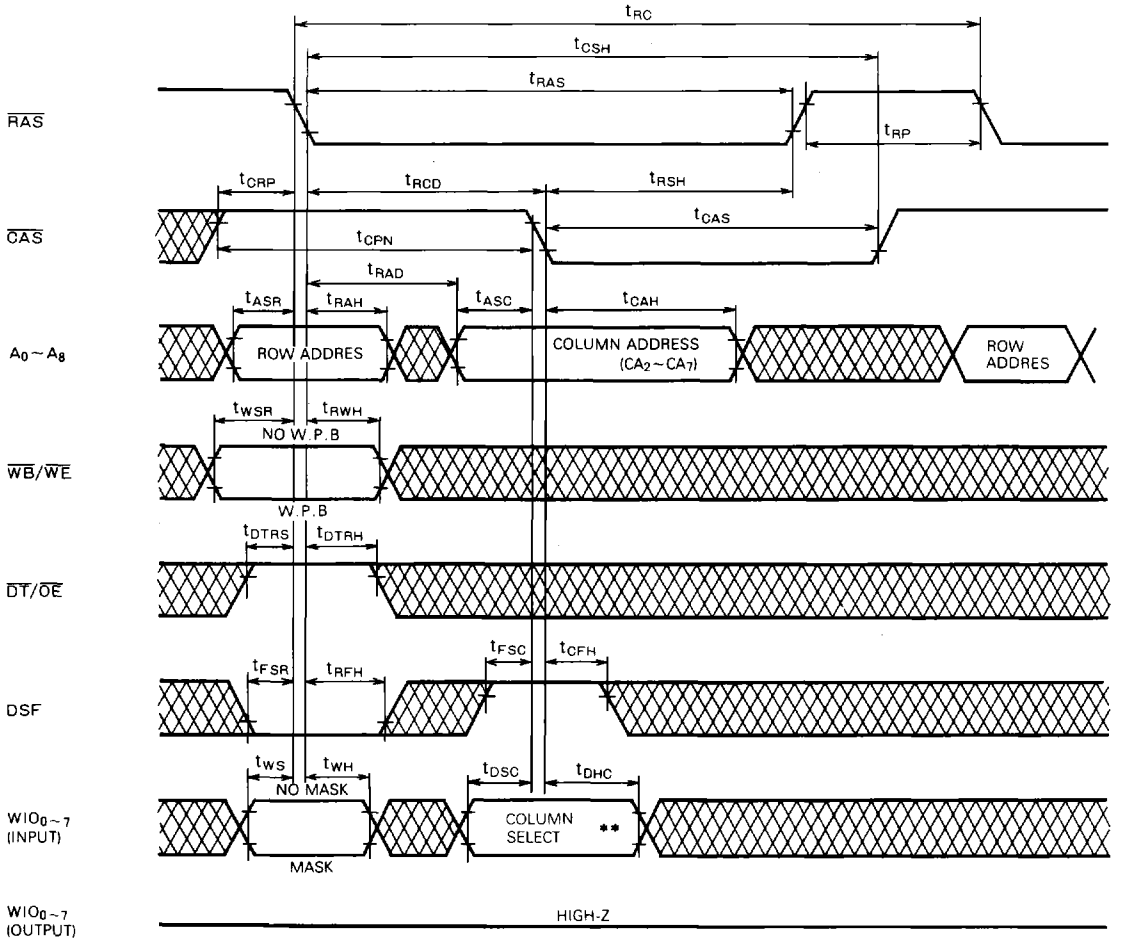
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Hidden Refresh Cycle



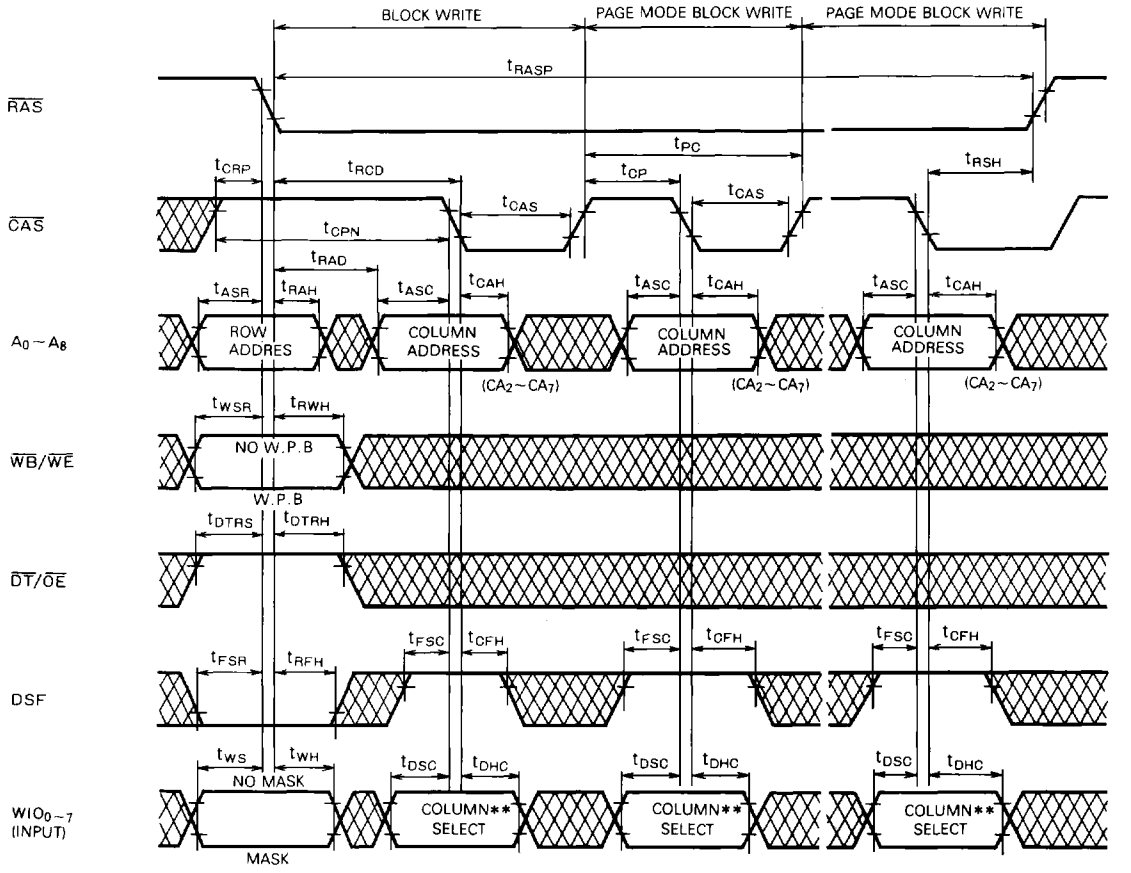
Block Write Cycle



Column select **

WIO 0	Col-0	$CA_0=0$, $CA_1=0$
WIO 1	Col-1	$CA_0=1$, $CA_1=0$
WIO 2	Col-2	$CA_0=0$, $CA_1=1$
WIO 3	Col-3	$CA_0=1$, $CA_1=1$

Page Mode Block Write Cycle



SE

SC

SIO0~7 (INPUT)

SIO0~7 (OUTPUT)

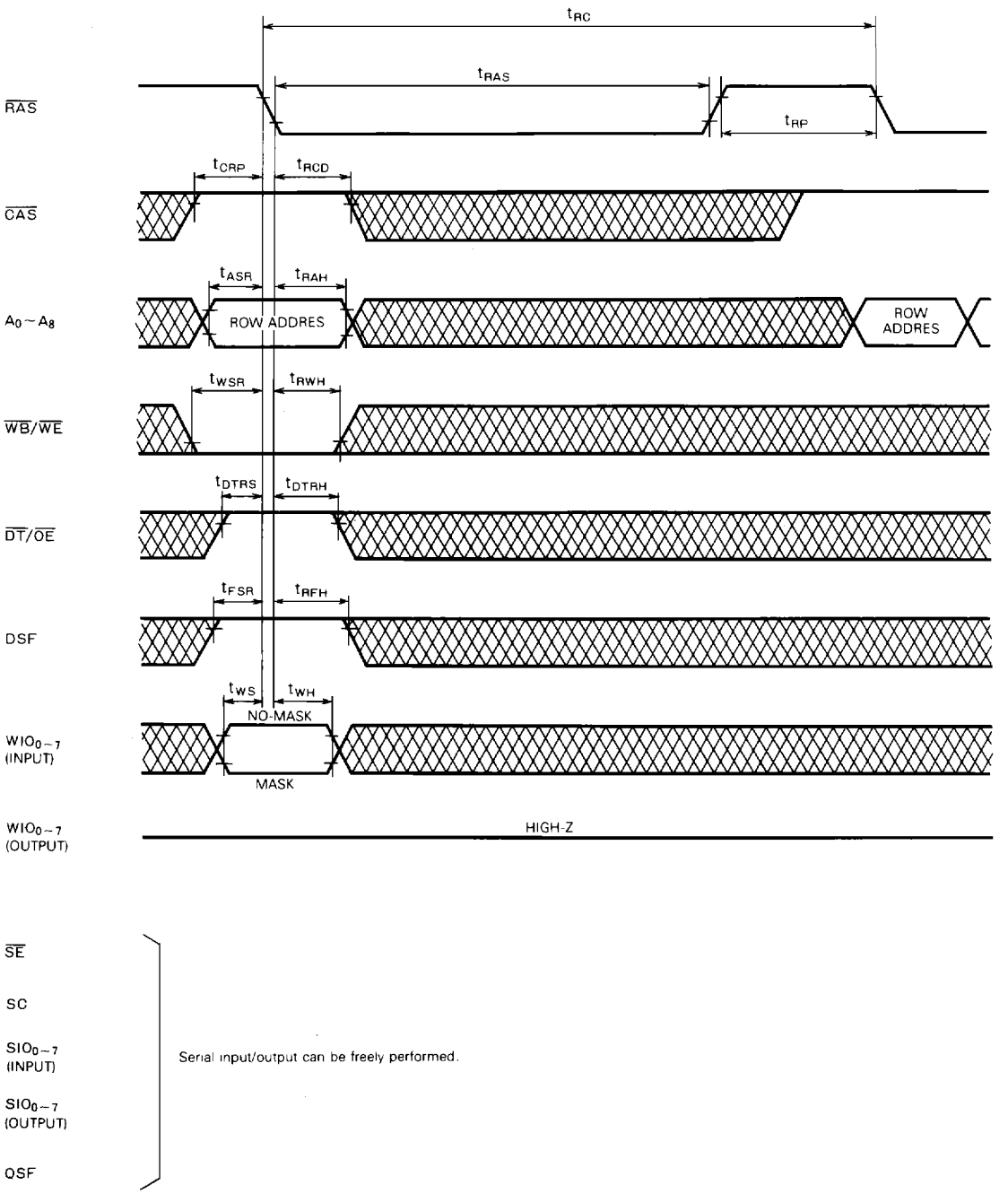
QSF

Serial input/output can be freely performed.

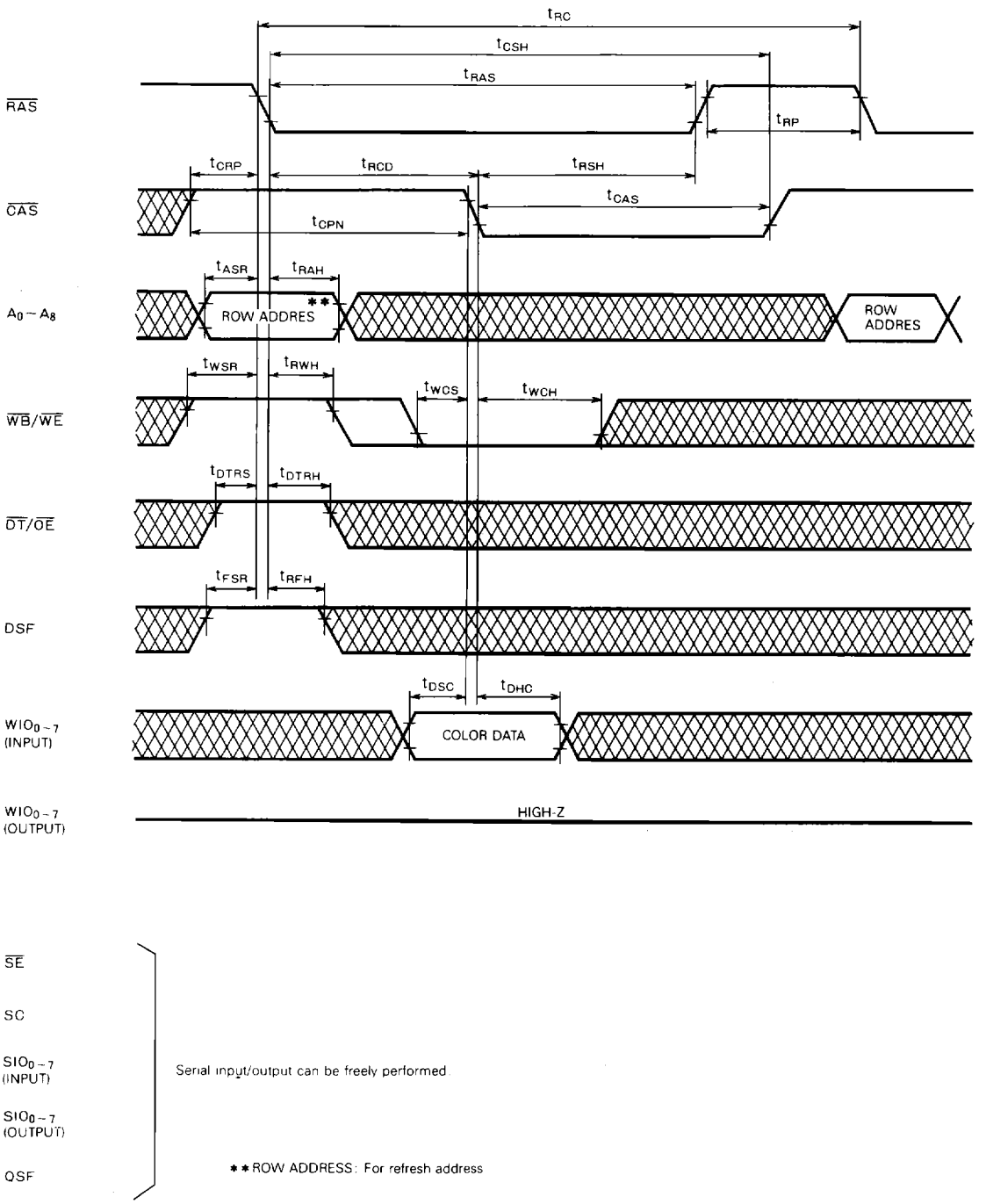
Column select **

WIO 0	Col-0	$CA_0=0$, $CA_1=0$
WIO 1	Col-1	$CA_0=1$, $CA_1=0$
WIO 2	Col-2	$CA_0=0$, $CA_1=1$
WIO 3	Col-3	$CA_0=1$, $CA_1=1$

Flash Write Cycle

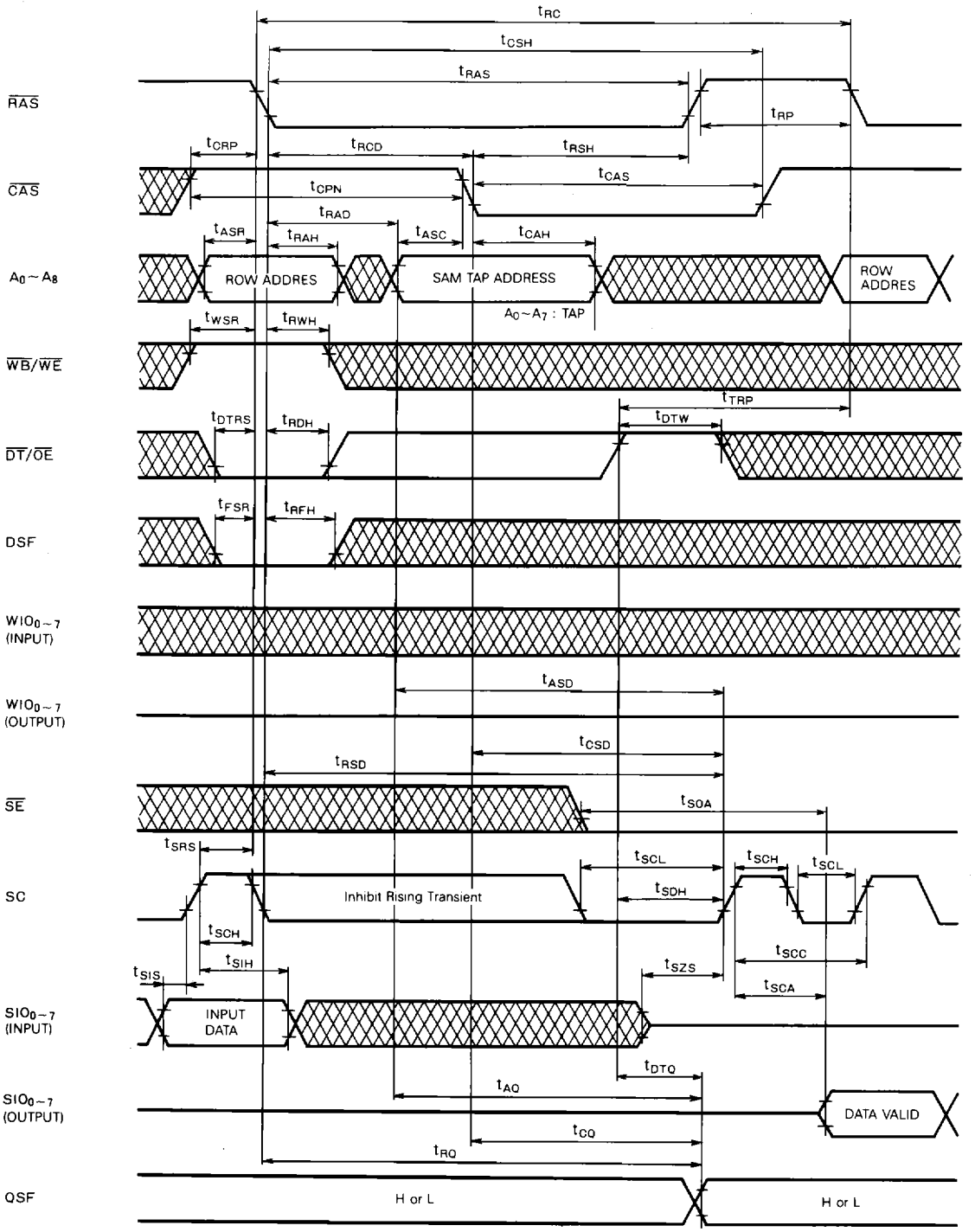


Load Color Register Cycle

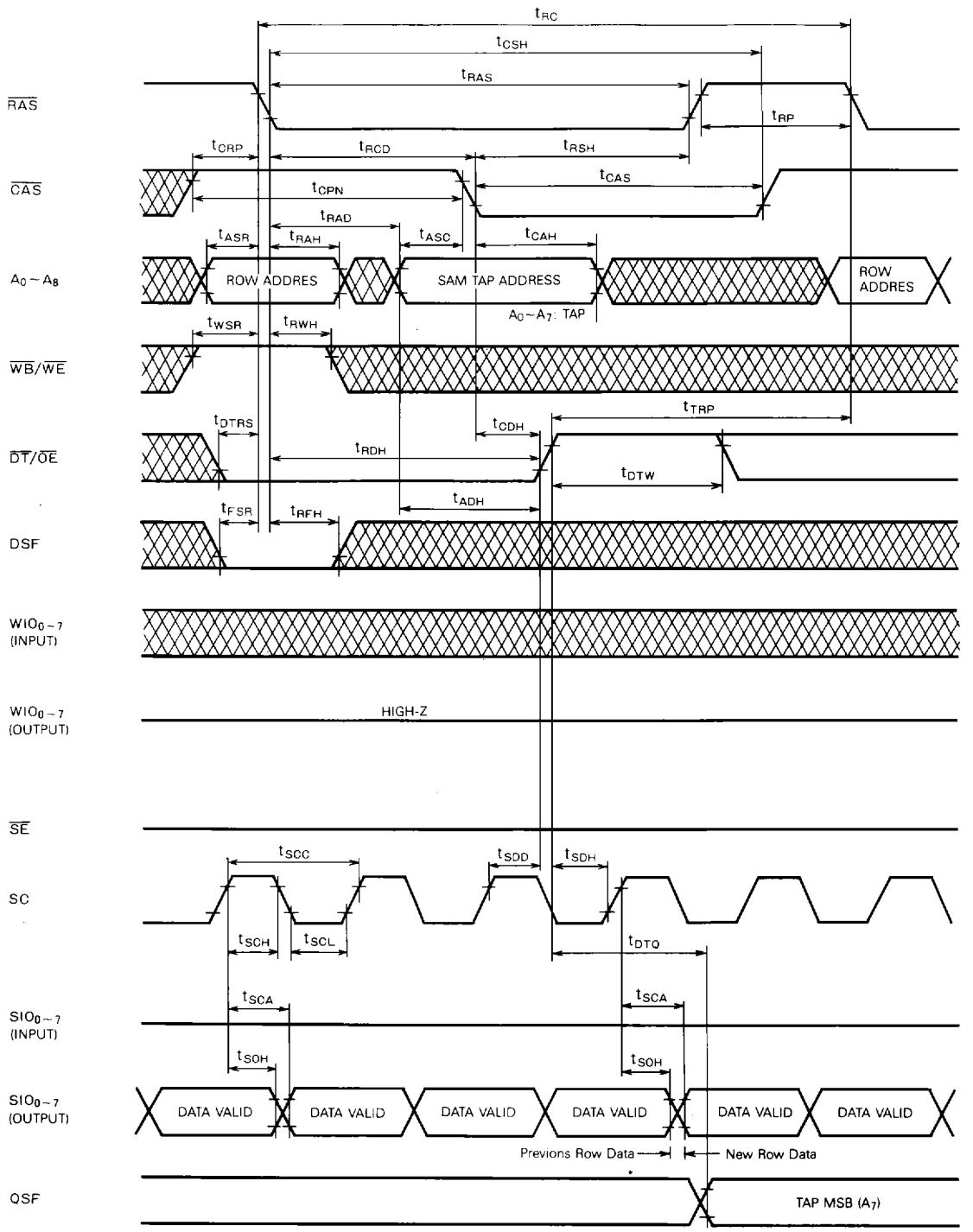


** ROW ADDRESS: For refresh address

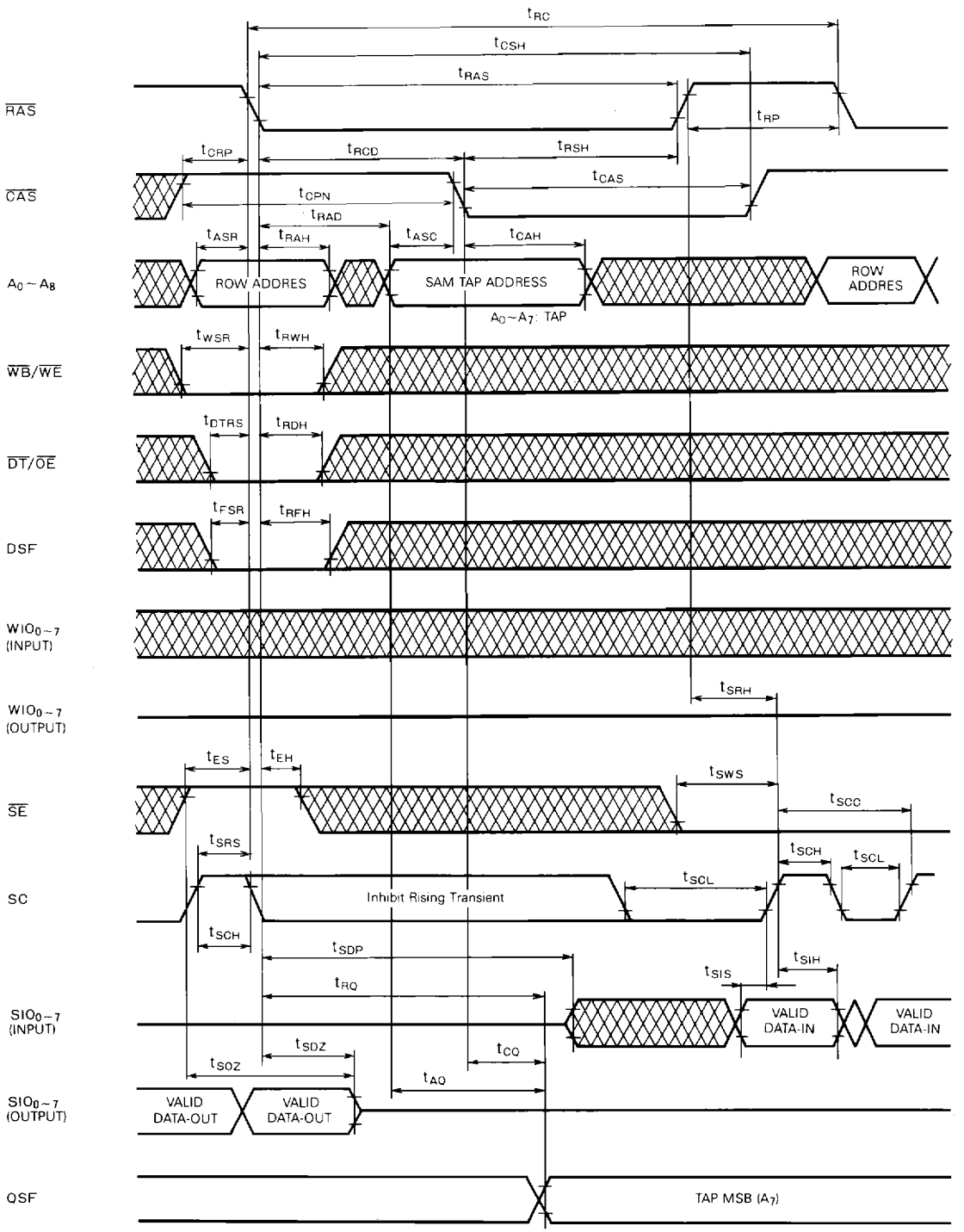
Read Transfer Cycle (Previous Transfer=Write Transfer)



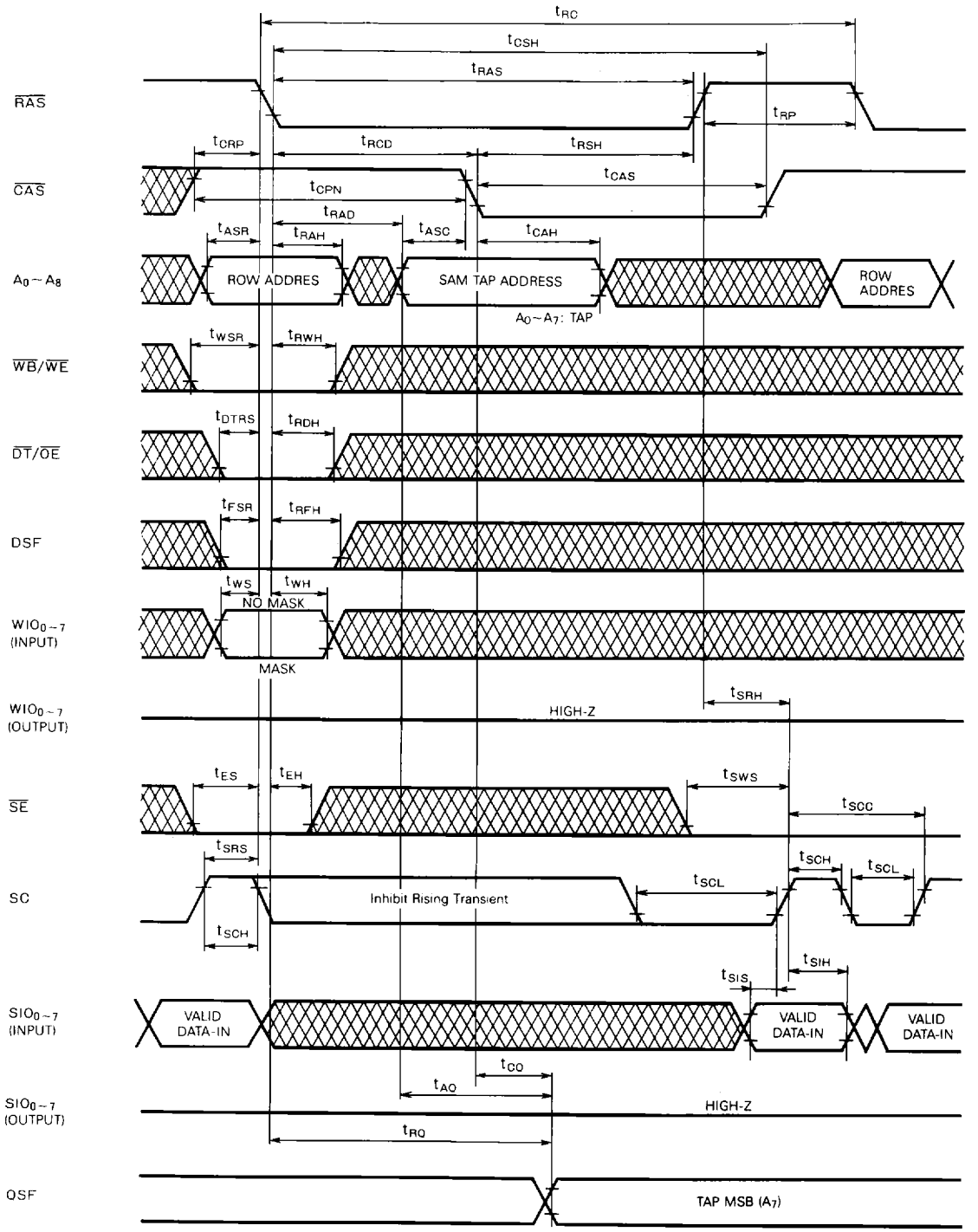
Real Time Read Transfer



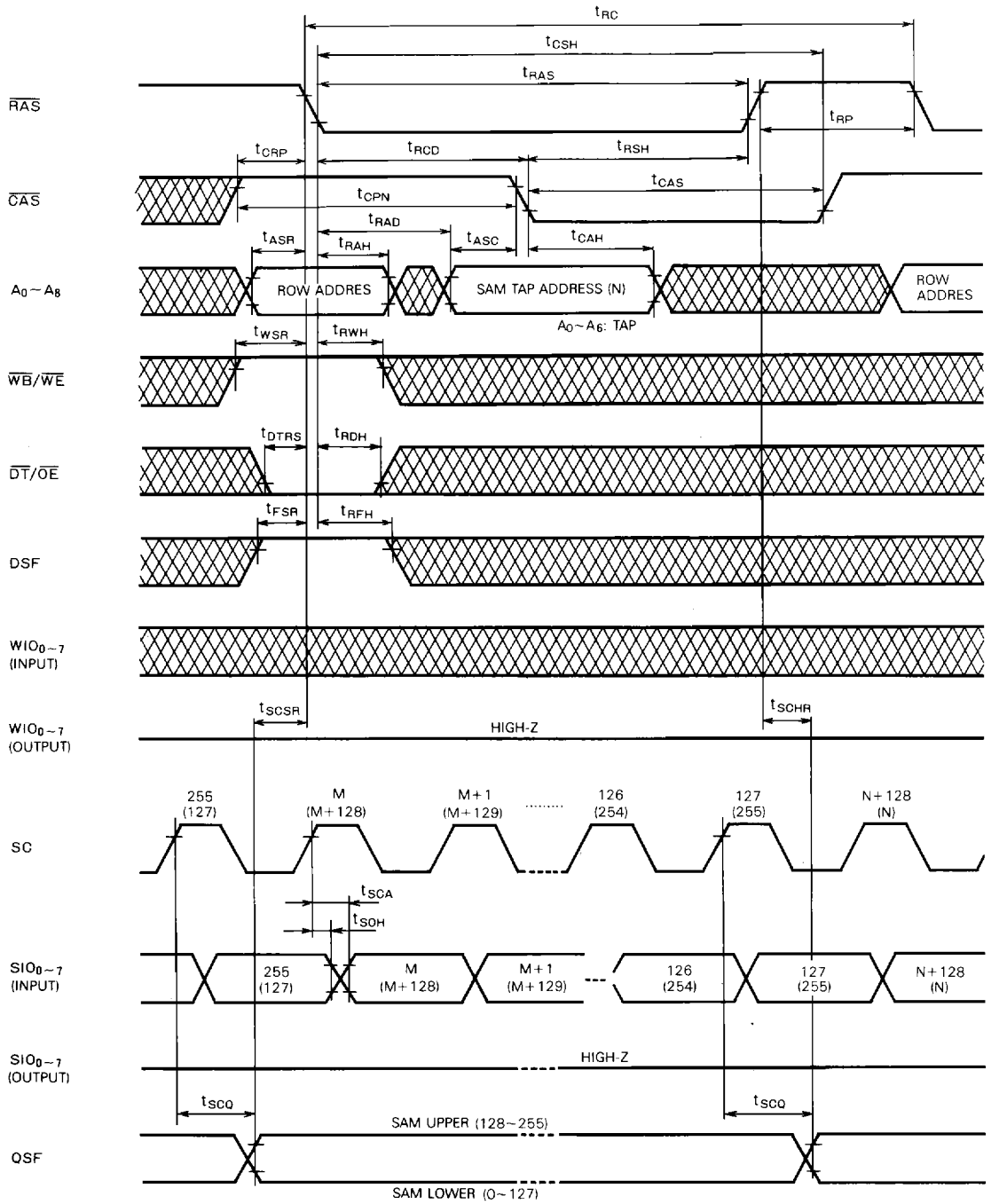
Pseudo Write Transfer Cycle



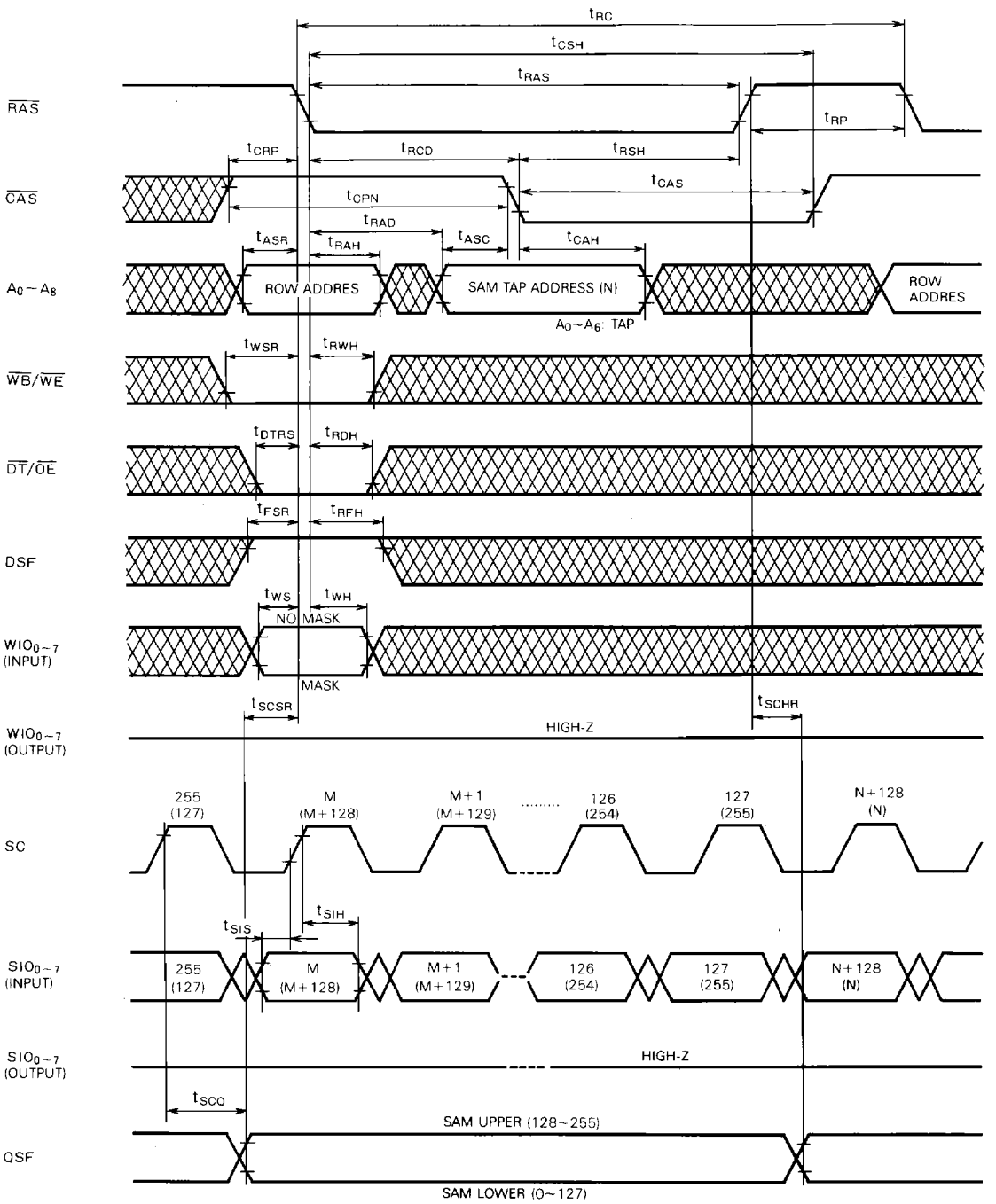
Write Transfer Cycle



Split Read Transfer Cycle



Split Write Transfer Cycle



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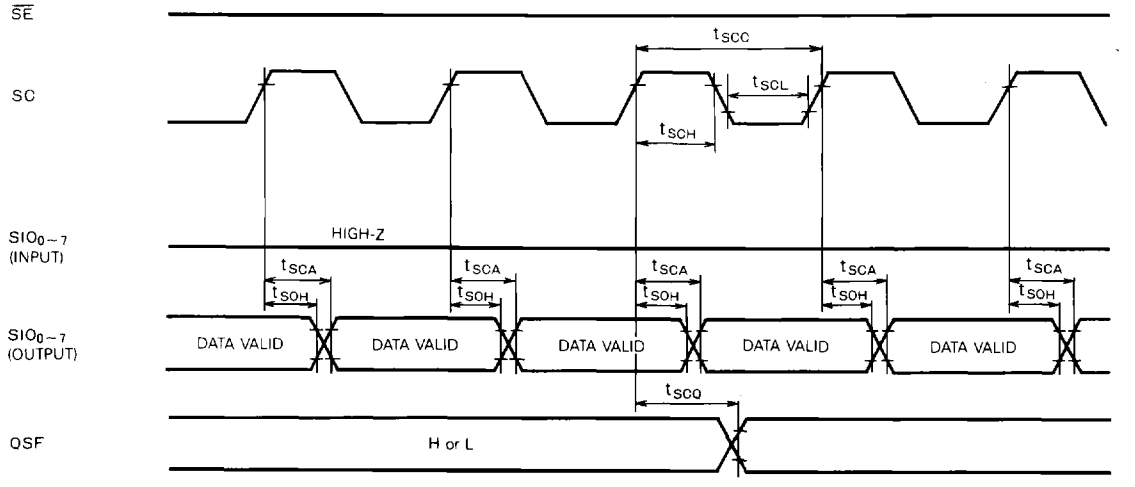
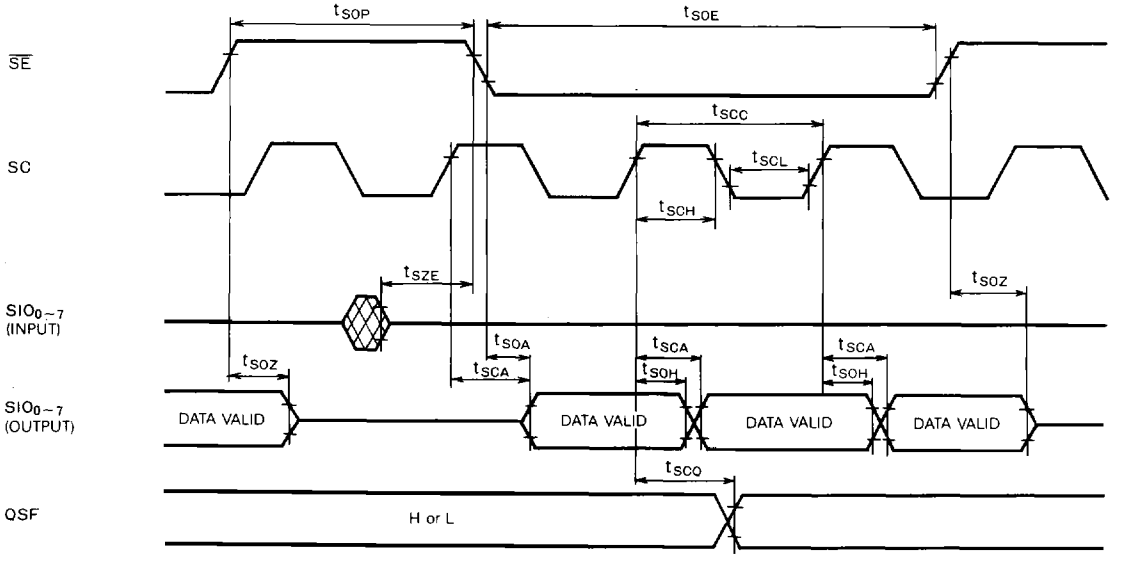
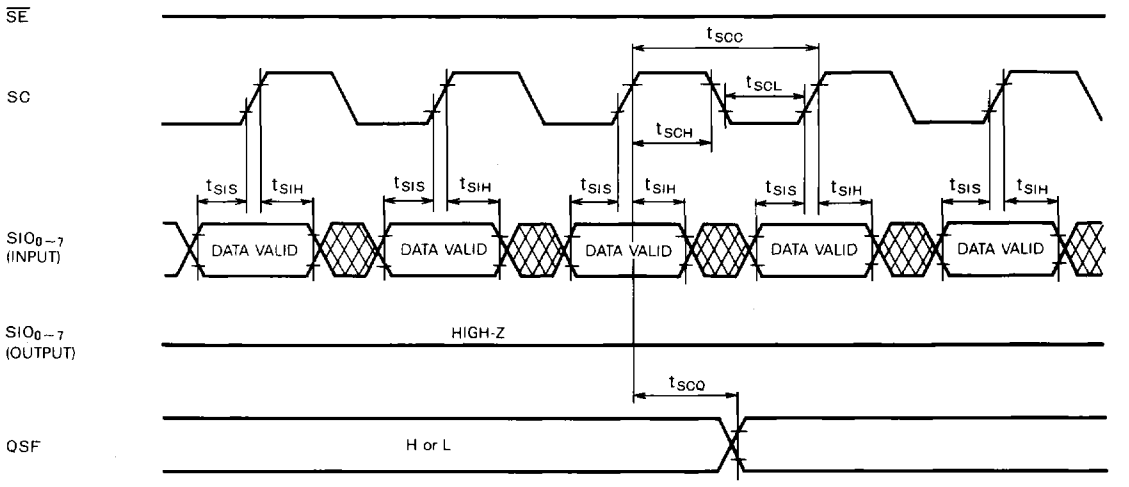
Serial Read Cycle ($\overline{SE}$=L)



Serial Read Cycle ($\overline{SE}$ Control)



Serial Write Cycle ($\overline{SE}$=L)



Serial Write Cycle ($\overline{SE}$ Control)