

MOSFETs Silicon N-channel MOS (U-MOS<sup>Ⅷ</sup>-H)

# TK100A08N1

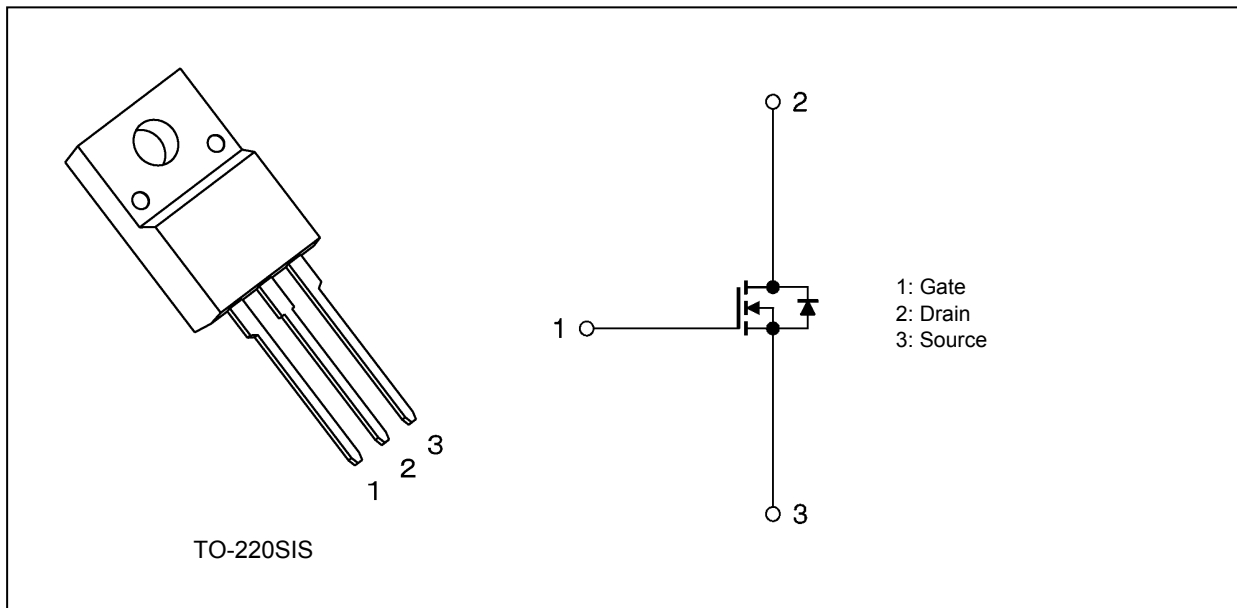
## 1. Applications

- Switching Voltage Regulators

## 2. Features

- (1) Low drain-source on-resistance:  $R_{DS(ON)} = 2.6 \text{ m}\Omega$  (typ.) ( $V_{GS} = 10 \text{ V}$ )
- (2) Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = 80 \text{ V}$ )
- (3) Enhancement mode:  $V_{th} = 2.0 \text{ to } 4.0 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 1.0 \text{ mA}$ )

## 3. Packaging and Internal Circuit



## 4. Absolute Maximum Ratings (Note) ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	80	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	
Drain current (DC)	(Silicon limit) (Note 1,2) $I_D$	214	A
Drain current (DC)	( $T_c = 25^\circ\text{C}$ ) (Note 1) $I_D$	100	
Drain current (pulsed)	( $t = 1 \text{ ms}$ ) (Note 1) $I_{DP}$	568	
Power dissipation	( $T_c = 25^\circ\text{C}$ ) $P_D$	45	W
Single-pulse avalanche energy	(Note 3) $E_{AS}$	278	mJ
Avalanche current	$I_{AR}$	100	A
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production

2011-12

**5. Thermal Characteristics**

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	2.77	°C/W
Channel-to-ambient thermal resistance	$R_{th(ch-a)}$	62.5	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Limited by silicon chip capability. Package limit is 100 A.

Note 3:  $V_{DD} = 64$  V,  $T_{ch} = 25^{\circ}\text{C}$  (initial),  $L = 21.4$   $\mu\text{H}$ ,  $I_{AR} = 100$  A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

**6. Electrical Characteristics**

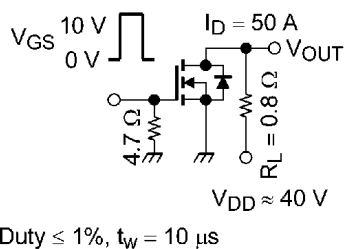
**6.1. Static Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 0.1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	80	—	—	V
Drain-source breakdown voltage (Note 4)	$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	60	—	—	
Gate threshold voltage	$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 1.0\text{ mA}$	2.0	—	4.0	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$	—	2.6	3.2	$\text{m}\Omega$

Note 4: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

**6.2. Dynamic Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	9000	—	$\text{pF}$
Reverse transfer capacitance	$C_{rss}$		—	52	—	
Output capacitance	$C_{oss}$		—	2100	—	
Gate resistance	$r_g$	—	—	3.2	—	$\Omega$
Switching time (rise time)	$t_r$	See Figure 6.2.1	—	26	—	ns
Switching time (turn-on time)	$t_{on}$		—	53	—	
Switching time (fall time)	$t_f$		—	46	—	
Switching time (turn-off time)	$t_{off}$		—	140	—	



Duty  $\leq 1\%$ ,  $t_w = 10\ \mu\text{s}$

**Fig. 6.2.1 Switching Time Test Circuit**

**6.3. Gate Charge Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} \approx 64\text{ V}, V_{GS} = 10\text{ V}, I_D = 100\text{ A}$	—	130	—	nC
Gate-source charge 1	$Q_{gs1}$		—	45	—	
Gate-drain charge	$Q_{gd}$		—	33	—	
Gate switch charge	$Q_{SW}$		—	53	—	

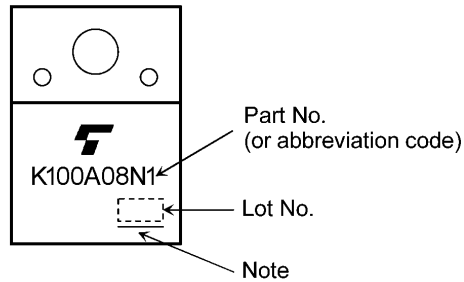
**6.4. Source-Drain Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (DC) (Note 5)	$I_{DR}$	—	—	—	100	A
Reverse drain current (pulsed) (Note 5)	$I_{DRP}$	—	—	—	568	
Diode forward voltage	$V_{DSF}$	$I_{DR} = 100\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.2	V
Reverse recovery time (Note 6)	$t_{rr}$	$I_{DR} = 100\text{ A}, V_{GS} = 0\text{ V}$ $-di_{DR}/dt = 100\text{ A}/\mu\text{s}$	—	93	—	ns
Reverse recovery charge (Note 6)	$Q_{rr}$		—	190	—	nC

Note 5: Ensure that the channel temperature does not exceed  $150^\circ\text{C}$ .

Note 6: Ensure that  $V_{DS}$  peak does not exceed  $V_{DSS}$ .

**7. Marking (Note)**



**Fig. 7.1 Marking**

Note: A line under a Lot No. identifies the indication of product Labels.

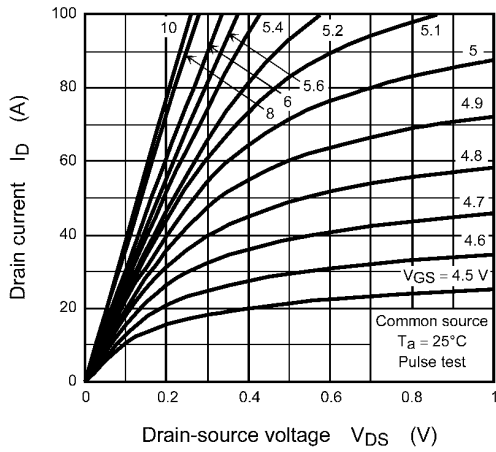
Not underlined:  $[[\text{Pb}]]/\text{INCLUDES} > \text{MCV}$

Underlined:  $[[\text{G}]]/\text{RoHS COMPATIBLE}$  or  $[[\text{G}]]/\text{RoHS } [[\text{Pb}]]$

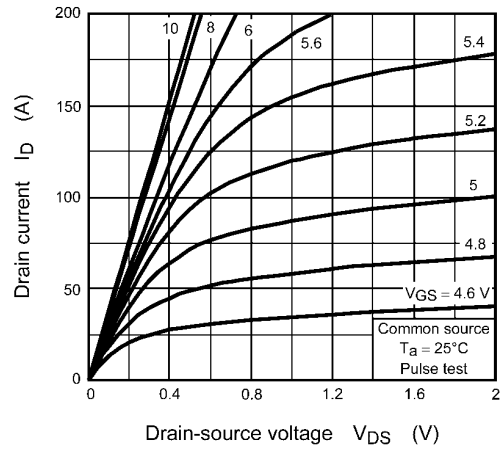
Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

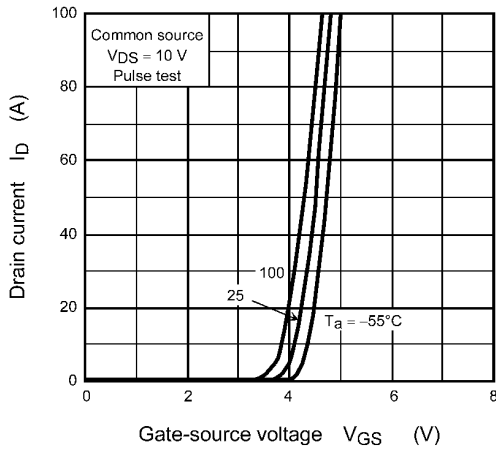
**8. Characteristics Curves (Note)**



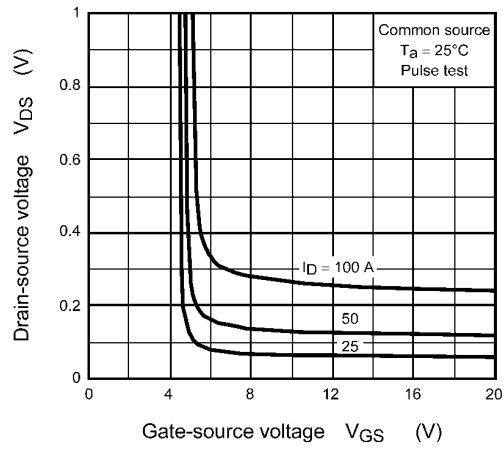
**Fig. 8.1  $I_D - V_{DS}$**



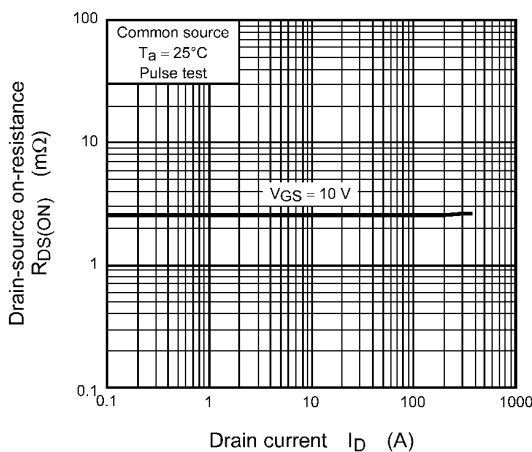
**Fig. 8.2  $I_D - V_{DS}$**



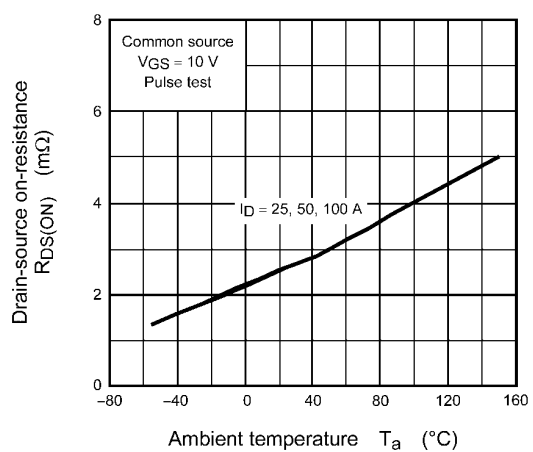
**Fig. 8.3  $I_D - V_{GS}$**



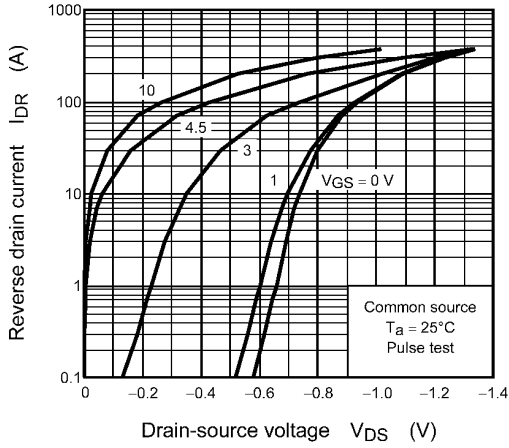
**Fig. 8.4  $V_{DS} - V_{GS}$**



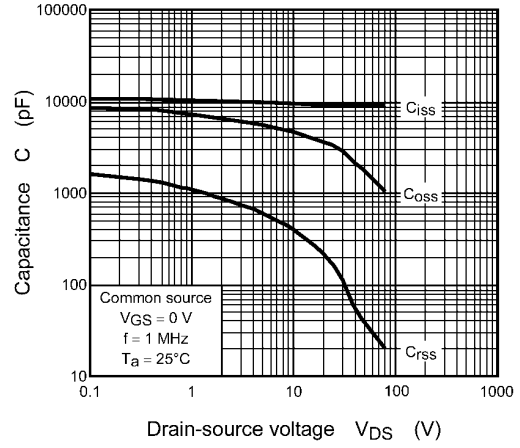
**Fig. 8.5  $R_{DS(ON)} - I_D$**



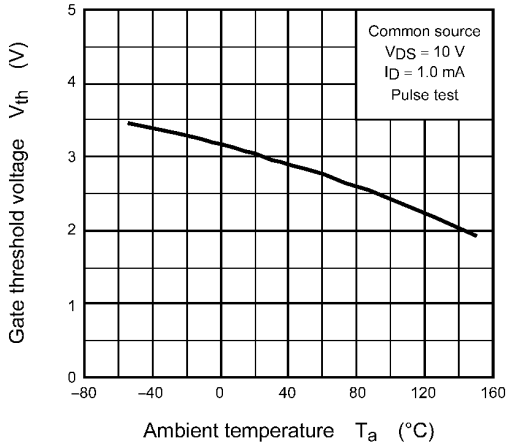
**Fig. 8.6  $R_{DS(ON)} - T_a$**



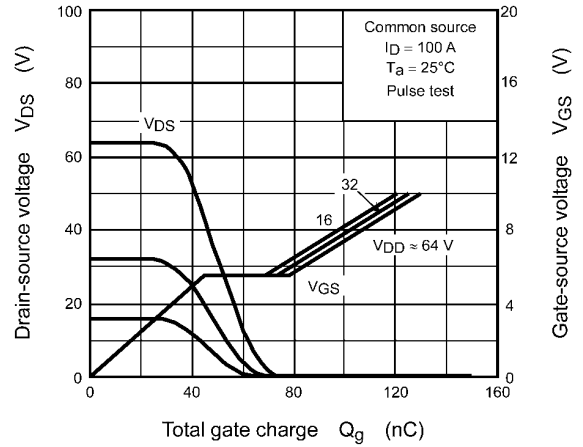
**Fig. 8.7  $I_{DR} - V_{DS}$**



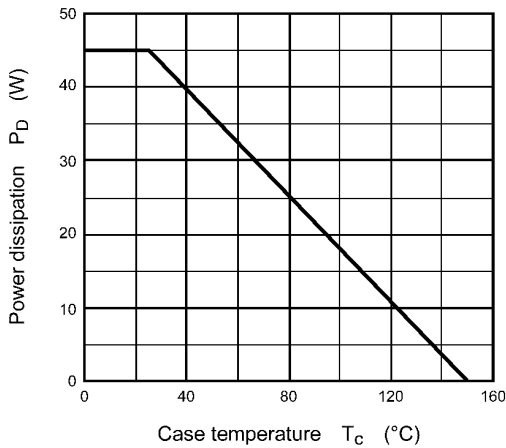
**Fig. 8.8 Capacitance -  $V_{DS}$**



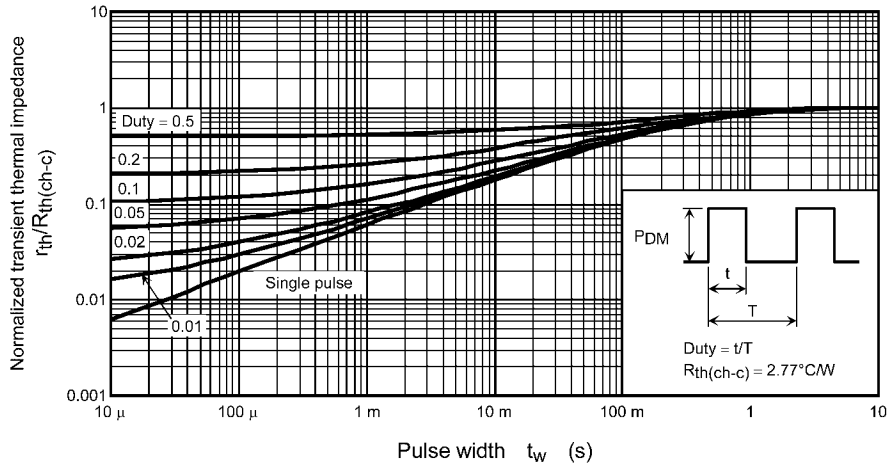
**Fig. 8.9  $V_{th} - T_a$**



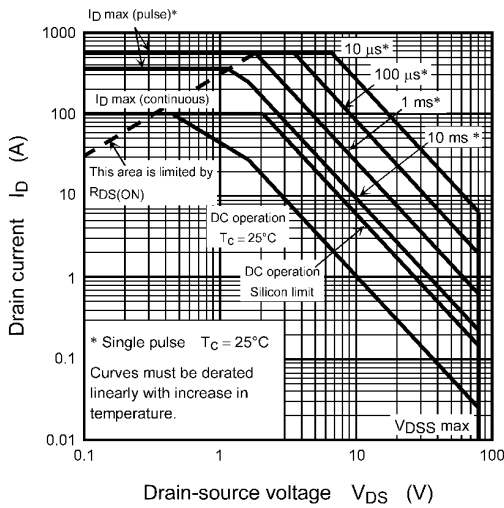
**Fig. 8.10 Dynamic Input/Output Characteristics**



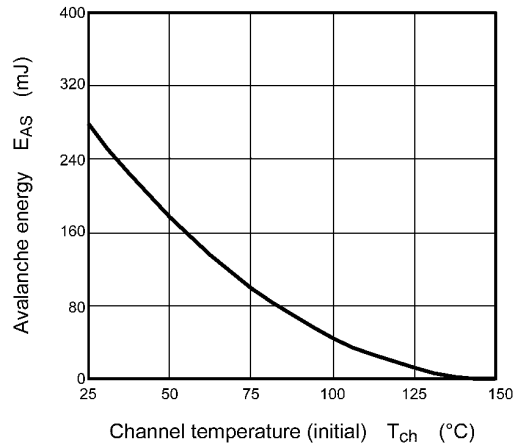
**Fig. 8.11  $P_D - T_c$   
(Guaranteed Maximum)**



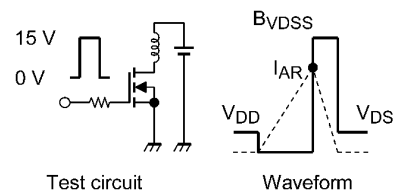
**Fig. 8.12**  $r_{th}/R_{th(ch-c)} - t_w$   
(Guaranteed Maximum)



**Fig. 8.13** Safe Operating Area  
(Guaranteed Maximum)



**Fig. 8.14**  $E_{AS} - T_{ch}$   
(Guaranteed Maximum)



$$V_{DD} = 64 \text{ V}, I_{AR} = 100 \text{ A} \quad E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left( \frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

**Fig. 8.15** Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.





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