DMN62D0LFB-7B

N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D $T_A = 25°C$
60V	2Ω @ V_{GS} = 4V	100mA
	2.5Ω @ V_{GS} = 2.5V	50mA

Description and Applications

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- DC-DC Converters
- Power management functions
- Battery Operated Systems and Solid-State Relays
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.

Features and Benefits

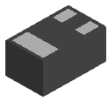
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **ESD Protected**
- **Lead Free By Design/RoHS Compliant (Note 1)**
- **"Green" Device (Note 2)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

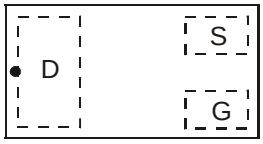
- Case: X1-DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.001 grams (approximate)

ESD PROTECTED

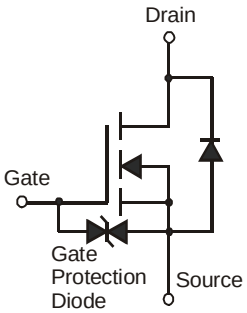
X1-DFN1006-3



Bottom View



Top View
Pin-Out



Equivalent Circuit

Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	60	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 4) V_{GS} = 4.0V	Steady State	T_A = 25°C T_A = 70°C	I_D	100 75	mA
Pulsed Drain Current (Note 5)			I_{DM}	200	mA

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Power Dissipation (Note 4)	P_D	0.47	W
Thermal Resistance, Junction to Ambient @T_A = 25°C (Note 4)	$R_{\theta JA}$	258	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics @ T_A = 25°C unless otherwise stated

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	-	-	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current T_J = 25°C	I_{DSS}	-	-	1.0	μA	V_{DS} = 60V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	-	-	±100	nA	V_{GS} = ±5V, V_{DS} = 0V
		-	-	±500	nA	V_{GS} = ±10V, V_{DS} = 0V
		-	-	±2.0	μA	V_{GS} = ±15V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(th)}$	0.6	-	1.0	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	-	1.3	2	Ω	V_{GS} = 4V, I_D = 100mA
		-	1.5	2.5		V_{GS} = 2.5V, I_D = 50mA
		-	1.9	3		V_{GS} = 1.8V, I_D = 50mA
		-	2.6	-		V_{GS} = 1.5V, I_D = 10mA
Forward Transfer Admittance	$\|Y_{fs}\|$	-	0.8	-	S	V_{DS} = 10V, I_D = 200mA
Diode Forward Voltage	V_{SD}	-	0.9	1.3	V	V_{GS} = 0V, I_S = 115mA
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	-	32	-	pF	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	-	4.4	-		
Reverse Transfer Capacitance	C_{rss}	-	2.9	-		
Gate Resistance	R_g	-	126	-	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	-	0.45	-	nC	V_{GS} = 4.5V, V_{DS} = 10V, I_D = 250mA
Gate-Source Charge	Q_{gs}	-	0.08	-		
Gate-Drain Charge	Q_{gd}	-	0.08	-		
Turn-On Delay Time	$t_{D(on)}$	-	3.4	-	ns	V_{GS} = 10V, V_{DS} = 30V, R_L = 150Ω, R_G = 25Ω, I_D = 200mA
Turn-On Rise Time	t_r	-	3.4	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	26.4	-	ns	
Turn-Off Fall Time	t_f	-	16.3	-	ns	

Notes: 4. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
5. Repetitive rating, pulse width limited by junction temperature.
6. Short duration pulse test used to minimize self-heating effect.
7. Guaranteed by design. Not subject to production testing.

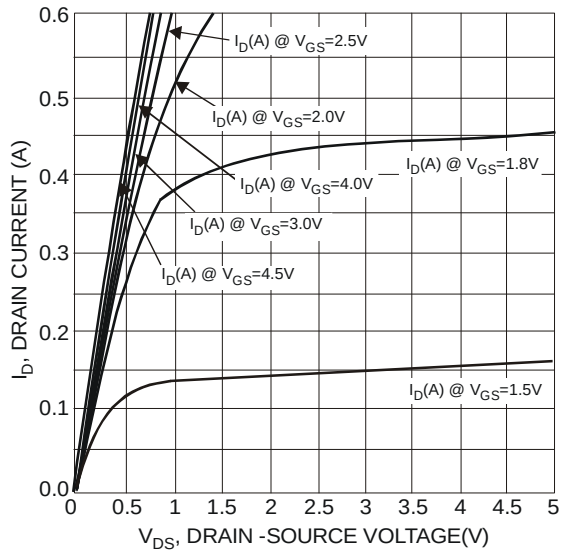


Fig. 1 Typical Output Characteristics

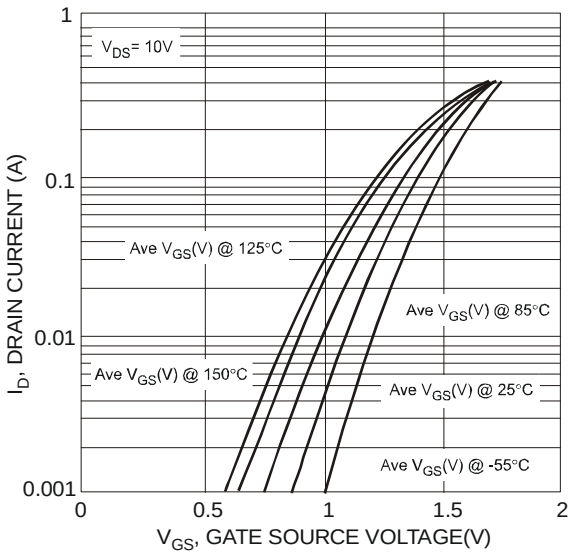


Fig. 2 Typical Transfer Characteristics

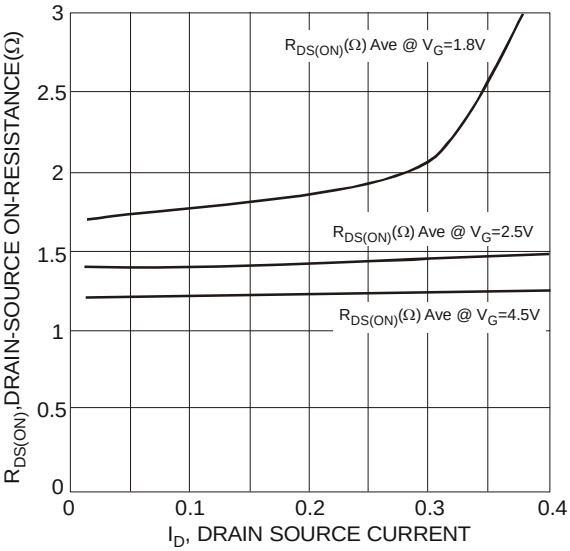


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

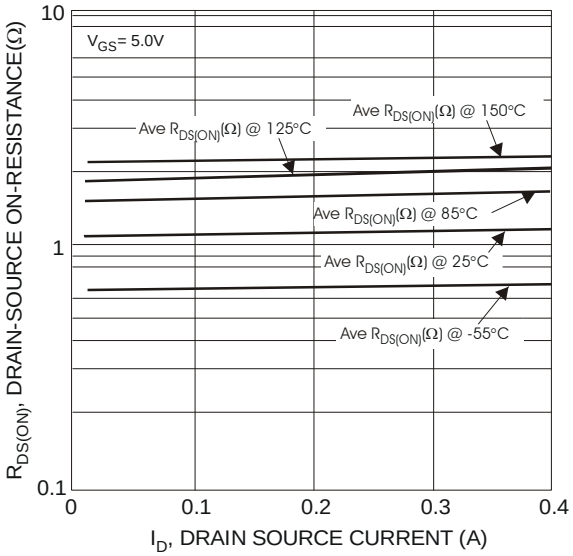


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

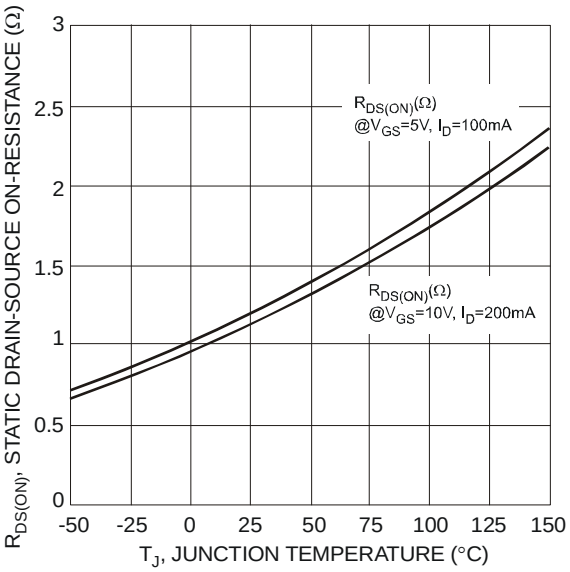


Fig. 5 On-Resistance Variation with Temperature

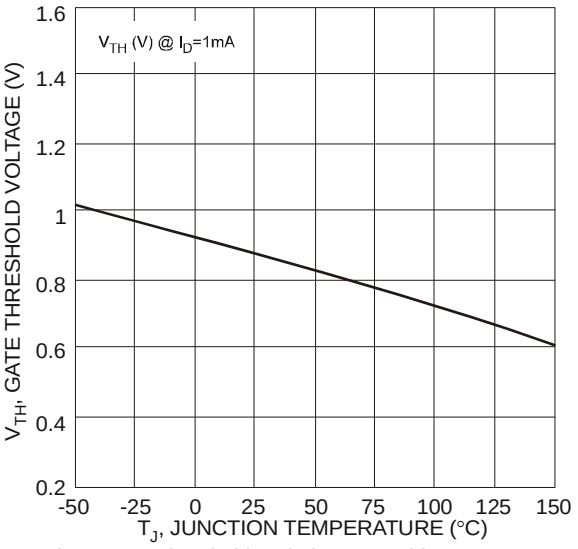


Fig. 6 Gate Threshold Variation vs. Ambient Temperature

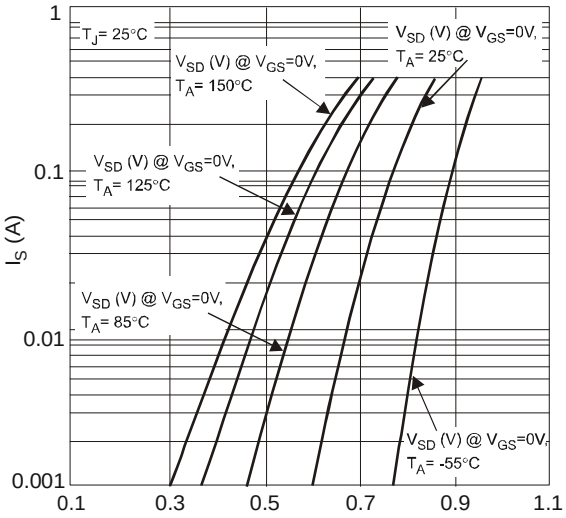


Fig. 7 Diodes Forward Voltage vs. Current

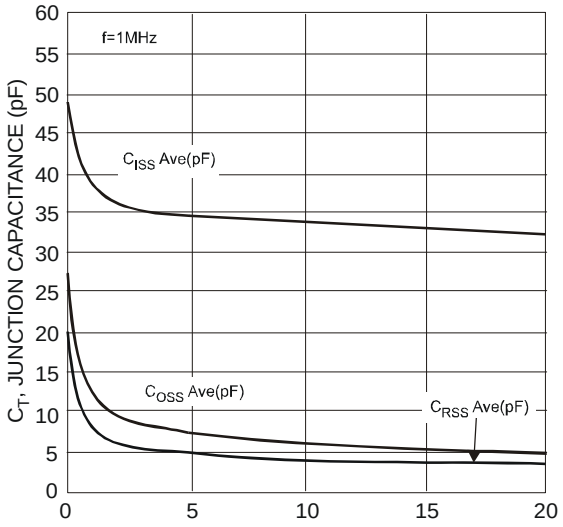


Fig. 8 Typical Junction Capacitance

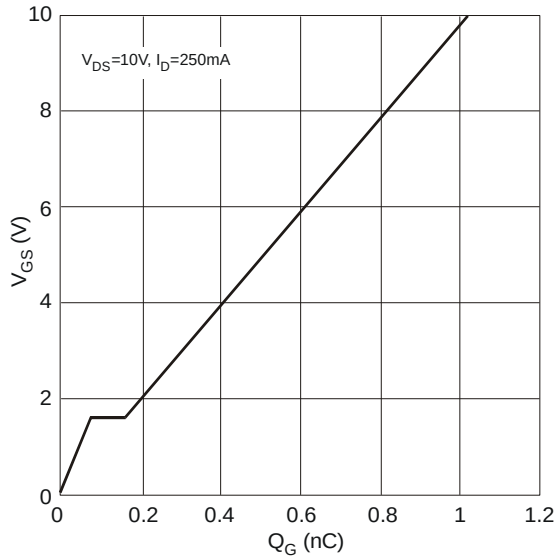


Fig. 9 Gate Charge Characteristics

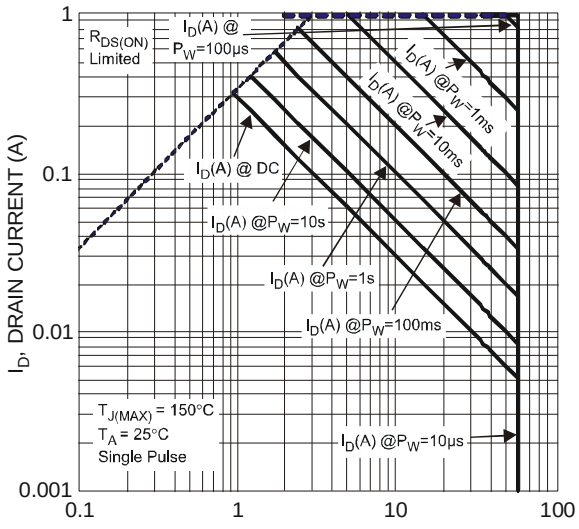


Fig. 10 SOA, Safe Operation Area

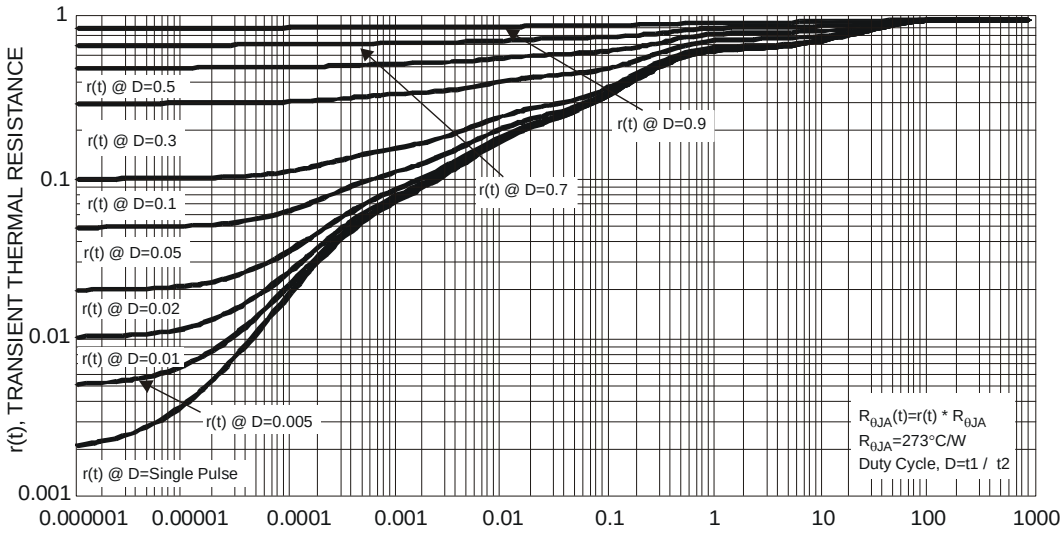
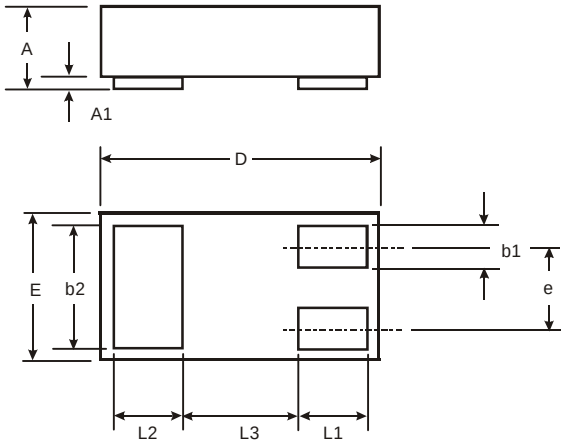


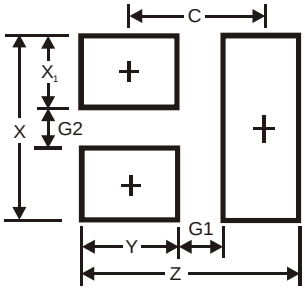
Fig. 11 Transient Thermal Resistance

Package Outline Dimensions



X1-DFN1006-3			
Dim	**Min**	**Max**	**Typ**
A	0.47	0.53	0.50
A1	0	0.05	0.03
b1	0.10	0.20	0.15
b2	0.45	0.55	0.50
D	0.95	1.075	1.00
E	0.55	0.675	0.60
e	—	—	0.35
L1	0.20	0.30	0.25
L2	0.20	0.30	0.25
L3	—	—	0.40
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
Z	1.1
G1	0.3
G2	0.2
X	0.7
X1	0.25
Y	0.4
C	0.7