Compact, High Efficiency, High Power Flash/Torch LED Driver with Dual Interface

ADP1653

FEATURES

- Small 6.4 mm × 7.2 mm solution
- 2.2 µH power inductor
- 92% peak efficiency
- Tx masking within 50 µs
- 2.1 A, 12 V power switch
- Pin-selectable interface: 2-bit logic or I²C®
- Programmable flash and torch current
  - Up to 200 mA in torch mode
  - Up to 500 mA in flash mode
- Programmable indicator LED current up to 20 mA
- Programmable timer register: up to 820 ms flash timeout
- 2.75 V to 5.5 V input voltage range
- Low noise, 1.2 MHz PWM operation
- Safety features
  - Interrupt output pin
  - Fault condition register
  - Short-circuit protection
  - Output overvoltage protection
  - Thermal overload protection
  - Integrated current limit and soft start
- Small 3 mm × 3 mm, 16-lead LFCSP footprint

APPLICATIONS

Camera-enabled cellular phones, smart phones
Digital still cameras, camcorders, PDAs

GENERAL DESCRIPTION

The ADP1653 is a very compact, high efficiency, high power, camera-flash LED driver optimized for cellular phones. The device's high efficiency and dynamic LED current control improve flash brightness and picture quality in dimly lit environments. Efficiency peaks at 92% and is higher than charge pump solutions over the Li-Ion battery range.

The device has a dual-mode interface that is configurable to 2-bit logic or an I²C interface. The indicator and high power LED currents are programmable with external resistors or through the I²C interface. To maximize overall flash brightness, the ADP1653 offers an input to reduce flash LED current in less than 50 µs, referred to as the Tx mask. Tx masking reduces battery stress by scaling back flash LED current during an RF transmission.

The ADP1653 solution requires only four external components in I²C mode and fits in a 6.4 mm × 7.2 mm space. The part integrates multiple safety features such as soft start, flash timeout, output current limit, thermal protection, and overvoltage protection.

The ADP1653 operates over the −40°C to +125°C junction temperature range.

TYPICAL OPERATING CIRCUIT

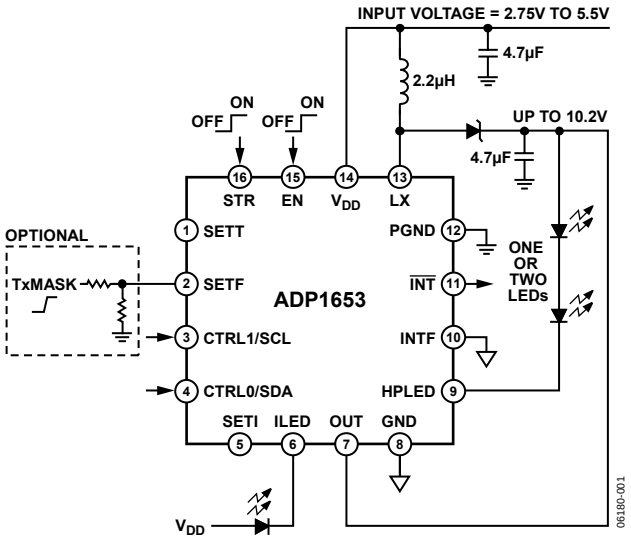

Figure 1.

PCB LAYOUT

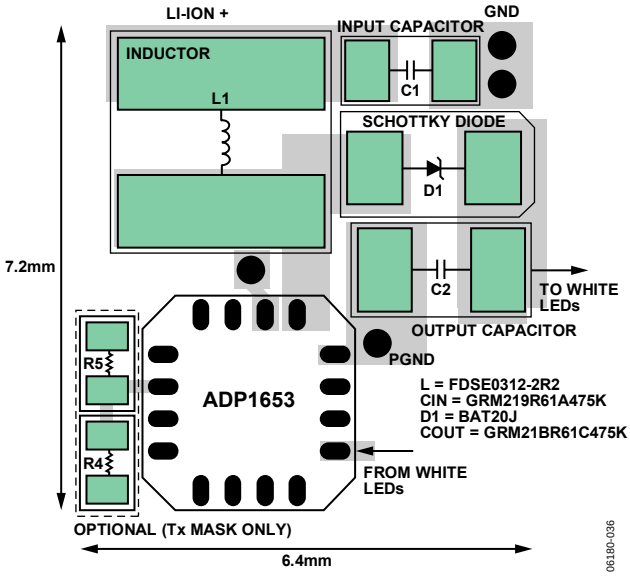

Figure 2.

Rev. A

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REVISION HISTORY

1/07—Revision A: Initial Version

SPECIFICATIONS

V_{DD} = 3.0 V to 5.5 V, T_J = −40°C to +125°C, unless otherwise noted.[1]

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY					
Input Voltage Range[2]		3.0		5.5	V
Undervoltage Lockout Threshold	V_{DD} rising	2.80	2.9	2.95	V
	V_{DD} falling	2.58	2.7	2.75	V
Shutdown Current	EN = GND, T_J = −40°C to +85°C		0.1	1	µA
Soft Power-Down Current	INTF = 0, EN = V_{DD}, ILED register = 0, HPLED register = 0, T_J = −40°C to +85°C		19	45	µA
	INTF = 1, EN = V_{DD}, (CTRL1, CTRL0) = (0, 0), T_J = −40°C to +85°C		19	45	µA
Operating Current[3]	INTF = 0, EN = V_{DD}, ILED register = 001, HPLED register = 0		500	700	µA
	INTF = 1, (CTRL1, CTRL0) = (0, 1), R_{SETI} = 200 kΩ		500	700	µA
	INTF = 0, EN = V_{DD}, HPLED register = 00001		1.6	3	mA
	INTF = 1, (CTRL1, CTRL0) = (1, x)		1.6	3	mA
LX Leakage	T_J = −40°C to +85°C		0.05	0.5	µA
HPLED Leakage	T_J = −40°C to +85°C		0.03	0.5	µA
THERMAL SHUTDOWN					
Thermal Shutdown Threshold	T_J rising		155		°C
INPUTS					
EN, STR, CTRL1/SCL, CTRL0/SDA					
Input Logic Low Voltage	T_J = −40°C to +85°C			0.54	V
	T_J = −40°C to +125°C			0.48	V
Input Logic High Voltage	T_J = −40°C to +85°C	1.26			V
	T_J = −40°C to +125°C	1.27			V
SETI, SETT, SETF					
Input Logic High Voltage		1.4			V
INTF					
Input Logic Low Voltage[4]				$V_{DD}/2 - 0.6$	V
Input Logic High Voltage[4]		$V_{DD}/2 + 0.6$			V
$\overline{INT}$ OUTPUT					
Logic Low Output Voltage	I_{SINK} = −3 mA			0.4	V
Logic High Leakage Current			0.05	0.5	µA
SETI, SETT, SETF REFERENCE VOLTAGE		1.19	1.22	1.24	V
INDICATOR LED					
INTF = 1, SETI Current Source	R_{SETI} = 25 kΩ	14.5	17.5	21.5	mA
	R_{SETI} = 200 kΩ	2.0	2.5	3.0	mA
INTF = 0	ILED register = 1 (001 binary), SETI = V_{DD}	2.0	2.5	3.0	mA
	ILED register = 7 (111 binary), SETI = V_{DD}	14.5	17.5	21.5	mA
WHITE LED DRIVER					
LX					
Switching Frequency		1.1	1.2	1.3	MHz
Current Limit		1.8	2.1	2.45	A
On Resistance			250	420	mΩ
OUT					
Soft Start Ramp			18		V/ms
Overvoltage Threshold	V_{DD} rising	9.8	10.15	10.5	V
Bias Current[5]	V_{OUT} = 10 V			12	µA

Parameter	Conditions	Min	Typ	Max	Unit
HPLED					
Regulation Voltage[6]	Boost active, two high power LEDs (HPLEDs) in series	0.23	0.32	0.42	V
Regulation Current					
INTF = 1, Torch Mode	RSETT = 50 kΩ or SETT = V_{DD}	110	125	145	mA
	RSETT = 125 kΩ	35	50	60	mA
Flash Mode	RSETF = 50 kΩ	460	500	550	mA
	RSETF = 500 kΩ	35	50	60	mA
INTF = 0, Flash Mode	HPLED register = 11111 (binary), SETF = V_{DD}	460	500	550	mA
	HPLED register = 11000 (binary), SETF = V_{DD}	365	395	435	mA
Torch Mode	HPLED register = 00110 (binary), SETF = V_{DD}	110	125	145	mA
	HPLED register = 00001 (binary), SETF = V_{DD}	38	50	60	mA
Step Size for HPLED LSB Change	SETF = V_{DD}		15		mA
Maximum Flash Timeout	INTF = 0 or 1, 983,040 × oscillator cycles		820		ms
SETF RESPONSE (TRANSMIT MASKING FUNCTION)[7]					
	HPLED current = 335 mA to 140 mA		22		µs
	HPLED current = 140 mA to 335 mA		24		µs

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). Typical values are at T_A = 25°C, V_{DD} = 3.6 V.
[2] This is the V_{DD} input voltage range over which the rest of the specifications are valid. The part operates as expected until V_{DD} goes below the UVLO threshold.
[3] This is the current into the V_{DD} pin. Additional current can flow into the indicator LED or HPLED, depending on the mode selected.
[4] INTF should be tied to GND (INTF = 0) for I²C interface or to V_{DD} (INTF = 1) for hardwire interface. All other digital inputs are 1.8 V compatible.
[5] This bias current is active only when the high power LED and/or indicator LED functions are enabled.
[6] This specification is not valid during minimum on-time operation of the boost converter (one LED case) when excess voltage is dropped across the HPLED pin.
[7] This specification is not production tested but is based on bench evaluation. It is based on the typical two-LED application circuit using a 100 kΩ resistor from SETF to GND, and a 160 kΩ resistor to a 1.8 V Tx mask logic signal with <1 µs rise/fall time. HPLED register = 11001 (binary). The inductor current has settled to within ±5% of final value.

I²C TIMING SPECIFICATIONS

Table 2.

Parameter	Min	Max	Unit	Description
f_{SCL}		400	kHz	SCL clock frequency
t_{HIGH}	0.6		µs	SCL high time
t_{LOW}	1.3		µs	SCL low time
$t_{SU, DAT}$	100		ns	Data setup time
$t_{HD, DAT}$[1]	0	0.9	µs	Data hold time
$t_{SU, STA}$	0.6		µs	Setup time for repeated start
$t_{HD, STA}$	0.6		µs	Hold time for start/repeated start
t_{BUF}	1.3		µs	Bus free time between a stop and a start condition
$t_{SU, STO}$	0.6		µs	Setup time for stop condition
t_R	20 + 0.1 C_B	300	ns	Rise time of SCL and SDA
t_F	20 + 0.1 C_B	300	ns	Fall time of SCL and SDA
t_{SP}	0	50	ns	Pulse width of suppressed spike
C_B[2]		400	pF	Capacitive load for each bus line

[1] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} minimum of the SCL signal) to bridge the undefined region of the SCL falling edge.
[2] C_B is the total capacitance of one bus line in picofarads.

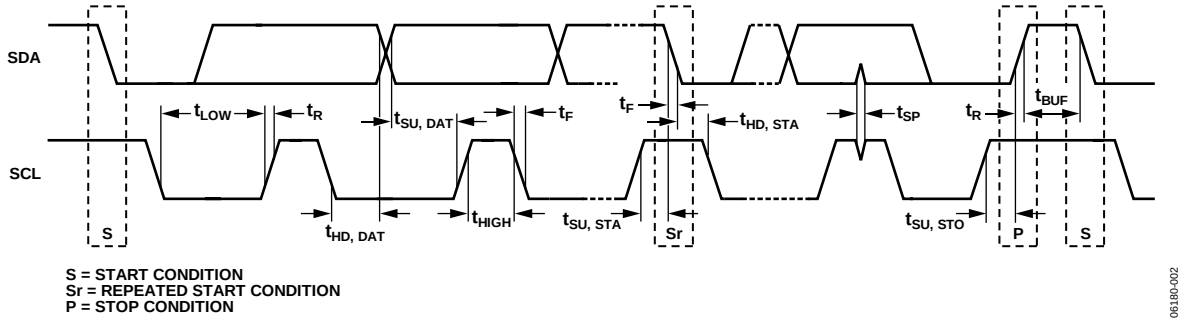

Figure 3. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD}, CTRL0/SDA, CTRL1/SCL, INTF, EN, SETI, SETT, SETF, STR, HPLED to GND	−0.3 V to +6 V
$\overline{INT}$, ILED to GND	−0.3 V to + (V_{DD} + 0.3 V)
LX, OUT to GND	−0.3 V to +12 V
PGND to GND	−0.3 V to +0.3 V
Operating Ambient Temperature Range	−40°C to +125°C[1]
Operating Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

[1] In applications where high power dissipation and poor thermal resistance are present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(MAX)}$) is dependent on the maximum operating junction temperature ($T_{J(MAXOP)}$ = 125°C), the maximum power dissipation of the device ($P_{D(MAX)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), using the following equation: $T_{A(MAX)} = T_{J(MAXOP)} - (\theta_{JA} \times P_{D(MAX)})$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

THERMAL RESISTANCE

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is dependent on the application and board layout. In applications where high maximum power dissipation exists, attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. For more information, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP).*

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP	44	°C/W
Maximum Power Dissipation	1	W

BOUNDARY CONDITION

Natural convection, 4-layer board, exposed pad soldered to the PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

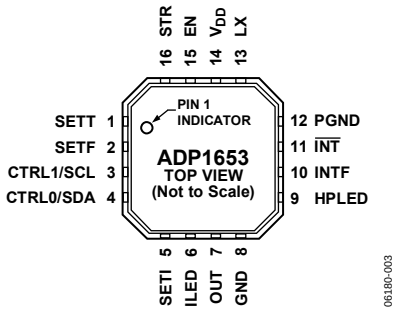

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SETT	Set Torch Input (2-Bit Logic Interface Only). SETT programs the high power LED current in torch mode. An external resistor connected between SETT and ground sets the torch current. When SETT is tied high, the current is internally set to 125 mA. In I²C mode, this pin is regarded as a no connect.
2	SETF	Set Flash Input. SETF programs the high power LED (HPLED) current in flash mode and allows for transmit blanking of the LED. In 2-bit logic interface mode, an external resistor connected between SETF and ground sets the flash current. If SETF is tied high, the current is set internally to 500 mA. In I²C mode, the flash current scales with both the external resistor and the internal HPLED bits in the output select register. If SETF is tied high, an internal 50 kΩ resistor combined with the HPLED bits set the HPLED current.
3	CTRL1/SCL	Serial Interface Clock Input. In 2-bit logic interface mode, CTRL1 is the second input bit of the digital interface. In I²C mode, SCL is the clock input of the I²C-compatible serial interface.
4	CTRL0/SDA	Serial Interface Data Input. In 2-bit logic interface mode, CTRL0 is the first input bit of the digital interface. In I²C mode, SDA is the data input/output of the I²C-compatible serial interface.
5	SETI	Set Indicator Input (2-Bit Logic Interface Only). SETI programs the indicator LED current. An external resistor connected between SETI and ground sets the indicator LED (ILED) current. If SETI is tied high, the current is internally set to 10 mA. In I²C mode, this pin is regarded as a no connect.
6	ILED	Indicator LED Input. Connect the cathode of the indicator LED to the ILED pin. Connect the anode to the battery or to a voltage rail greater than the LED forward voltage.
7	OUT	White LED Output Voltage. OUT senses the output voltage of the white LED step-up converter. At startup, the ADP1653 limits the rate of increase of the voltage at OUT (soft start) to prevent excessive input inrush current. The OUT pin features a comparator to detect an overvoltage condition if the LED string is open circuited. Connect the anode of the white LED(s) to OUT. Connect a 3.3 µF or greater capacitor between OUT and PGND.
8	GND	Analog/Digital Ground. Connect GND to PGND at the LFCSP paddle.
9	HPLED	High Power LED Current Regulator. HPLED regulates the current of the high power LED(s). Connect the cathode of the white LED string to HPLED.
10	INTF	Interface Input. INTF selects the 2-pin interface mode. INTF is driven high to enable CTRL1 and CTRL0 for 2-bit logic interface mode. INTF is driven low to enable SDA and SCL for I²C interfacing.
11	$\overline{INT}$	Active Low Interrupt Output. $\overline{INT}$ is an open-drain output that transitions from high to low to signal that a fault condition has occurred. $\overline{INT}$ should be connected via a pull-up resistor (for example, 10 kΩ to 100 kΩ) to the I/O supply rail and directly to the system processor. When an interrupt is detected, the system processor can read the FAULT register, using the I²C interface for details on the fault condition.
12	PGND	Power Ground for Internal Switching FET.
13	LX	White LED Switch Node. LX drives the inductor of the white LED step-up converter. An inductor and diode connected to LX powers the white LEDs.
14	V_{DD}	Supply Input. Connect the battery between V_{DD} and PGND. Bypass V_{DD} to PGND with a 4.7 µF or greater capacitor.
15	EN	Enable Input. Driving EN high turns on the ADP1653. Driving EN low disables the ADP1653 and reduces the input current to less than 1 µA. When EN is high, disabling the LEDs puts the part into sleep mode, dropping the input current to less than 45 µA.
16	STR	Strobe Control Input (I²C Interface Only). Driving STR high enables the flash function of the white LED. STR also enables the watchdog timer to prevent overstressing the white LEDs.

Table 6. Mode Selection

Pin Mnemonic	Value	INTF = 0 (I^2C Interface)	INTF = 1 (2-Bit Logic Interface)
CTRL0/SDA		SDA	CTRL1, CTRL0 = 0, 0 (ADP1653 disabled)
CTRL1/SCL		SCL	CTRL1, CTRL0 = 0, 1 (ADP1653 indicator LED)
			CTRL1, CTRL0 = 1, 0 (ADP1653 torch mode)
			CTRL1, CTRL0 = 1, 1 (ADP1653 flash mode)
EN	Low	ADP1653 disabled	ADP1653 disabled
	High	ADP1653 enabled	ADP1653 enabled
STR	Low	Flash disabled	Ignored
	High	Flash enabled	Ignored
$\overline{INT}$	Low	Fault condition	Fault condition
	High	Normal operation	Normal operation
SETI	Resistor	Ignored[1]	SETI resistor sets indicator LED current[2]
	High	I^2C sets ILED current	ILED current = 10 mA
SETT	Resistor	Ignored[1]	SETT resistor sets torch current[2]
	High	I^2C sets torch current	Torch current = 125 mA
SETF	Resistor	SETF resistor(s) and I^2C set flash current and torch current[3]	SETF resistor(s) set flash current[2]
	High	I^2C sets flash current	Flash current = 500 mA

[1] If a resistor is present on SETI or SETT in I^2C mode, it is ignored. Both pins should be tied high when operating in I^2C mode.
[2] If a resistor is present, the current is set by this resistor. If a resistor is not present, the pin must be tied high and a default internal current set.
[3] If a resistor is present on SETF in I^2C mode, the output current scales with both the I^2C setting and the external reference current. The SETF resistor scales both the flash mode and torch mode currents.

TYPICAL PERFORMANCE CHARACTERISTICS

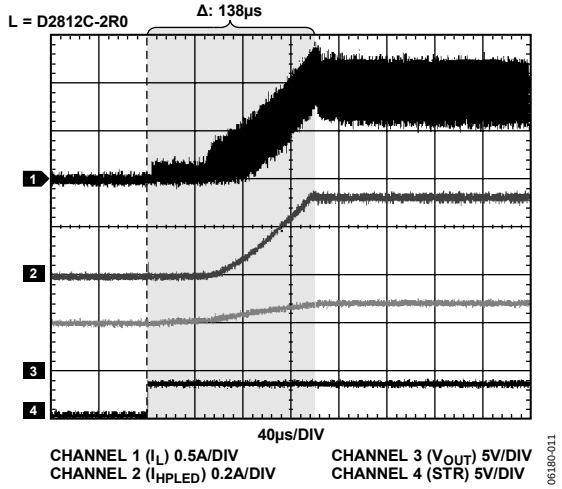

Figure 5. Startup, Two LEDs Flash Mode, LED Current = 335 mA, V_{DD} = 3.2 V

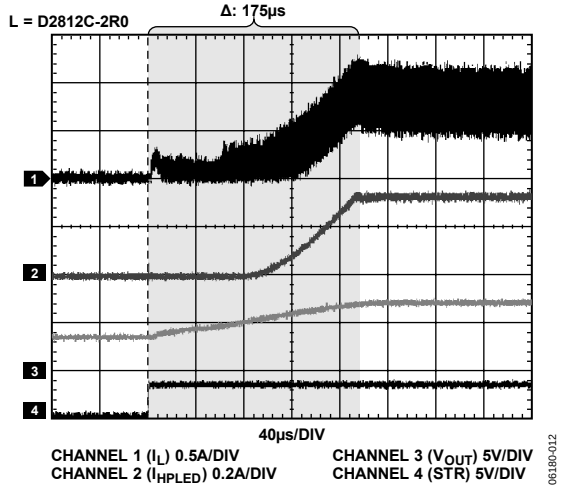

Figure 6. Startup, Two LEDs Flash Mode, LED Current = 335 mA, V_{DD} = 3.6 V

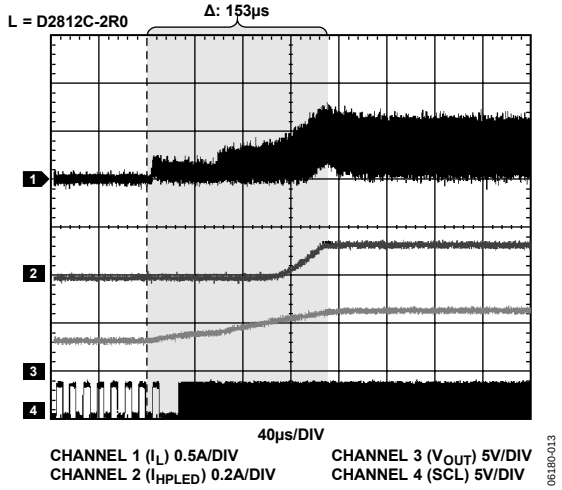

Figure 7. Startup, Two LEDs Torch Mode, LED Current = 130 mA, V_{DD} = 3.2 V

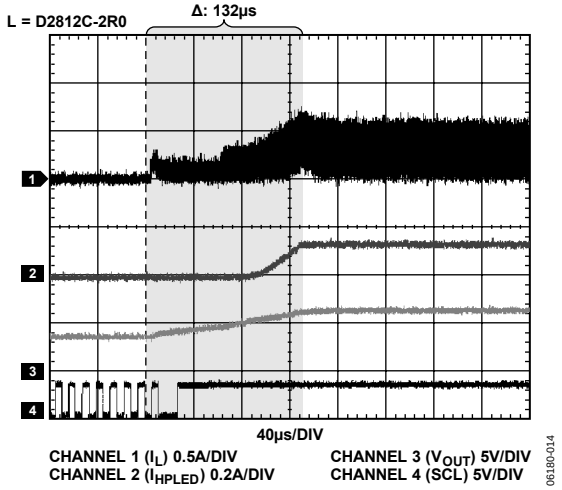

Figure 8. Startup, Two LEDs Torch Mode, LED Current = 130 mA, V_{DD} = 3.6 V

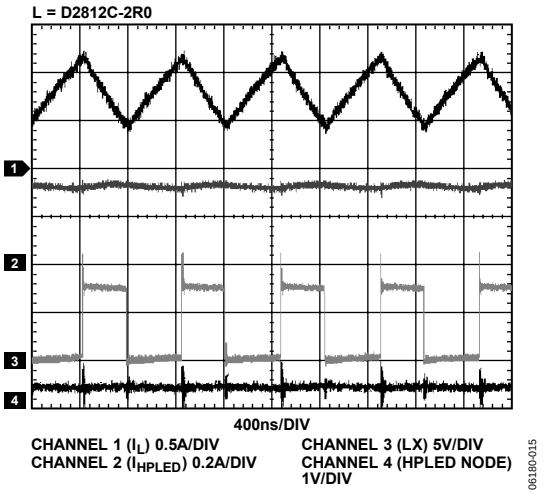

Figure 9. Inductor Current, Two LEDs Flash Mode, LED Current = 335 mA, V_{DD} = 3.6 V

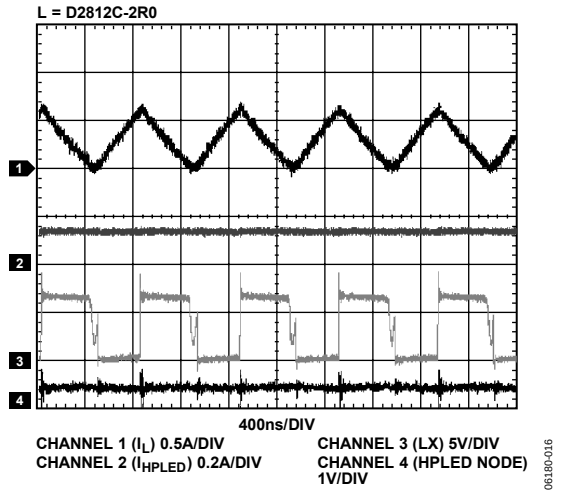

Figure 10. Inductor Current, Two LEDs Torch Mode, LED Current = 130 mA, V_{DD} = 3.6 V

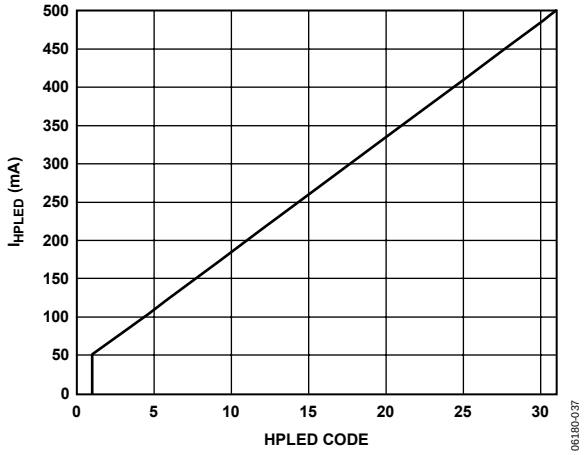

Figure 11. HPLED Current vs. HPLED Code, I²C Mode, SETF = V_{DD}

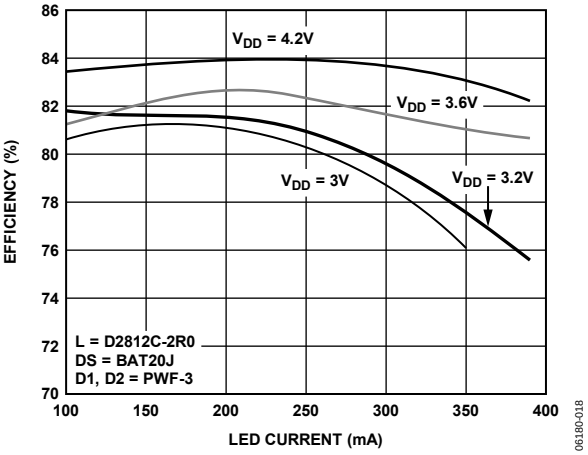

Figure 12. Efficiency P_{LED}/P_{IN}, Two High Power White LEDs in Series

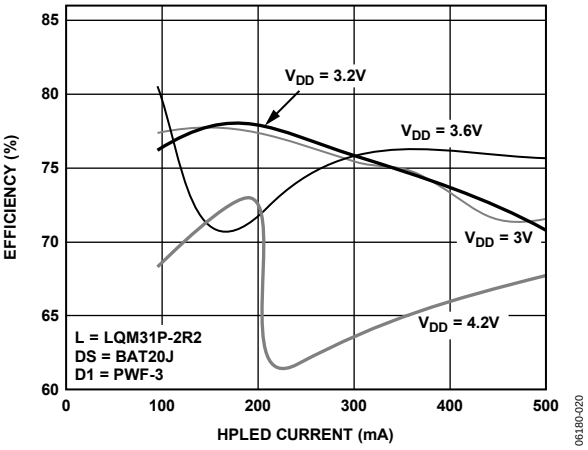

Figure 13. Efficiency P_{LED}/P_{IN}, One High Power White LED

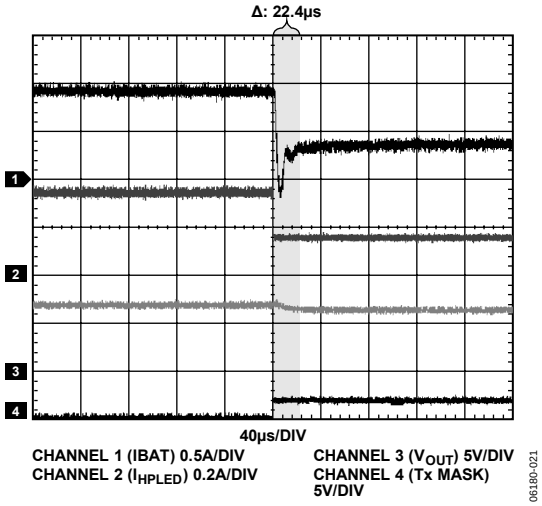

Figure 14. Tx Masking Response, Tx Mask 0 V to1.8 V, IHPLED = 335 mA to 140 mA, V_{DD} = 3.2 V

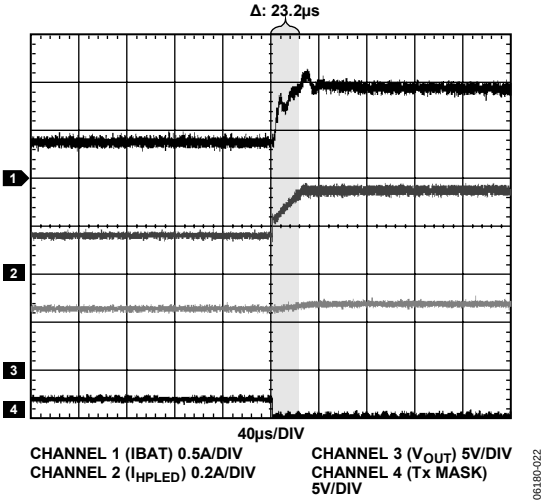

Figure 15. Tx Masking Response, Tx Mask 0 V to1.8 V, I_{HPLED} = 140 mA to 335 mA, V_{DD} = 3.2 V

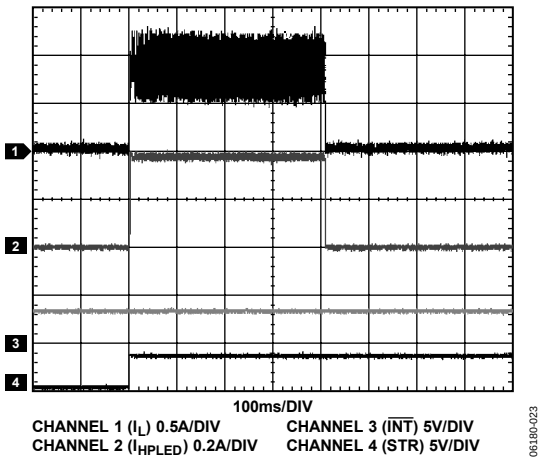

Figure 16. Flash Timed Mode, Two LEDs, Timer = 820 ms, I_{HPLED} = 380 mA, V_{DD} = 3.6 V

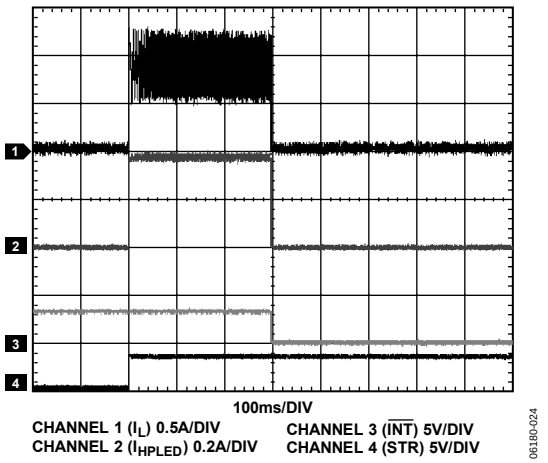

Figure 17. Flash Untimed Mode, Two LEDs, Timer = 300 ms, I_{HPLED} = 380 mA, V_{DD} = 3.6 V

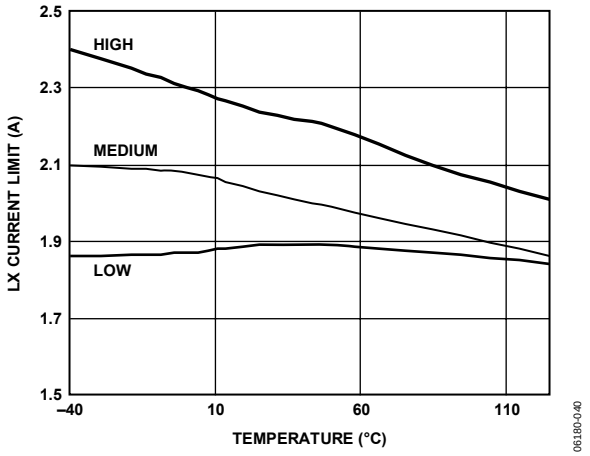

Figure 18. Typical Current Limit vs. Temperature; Low, Medium, and High Current Limit Parts

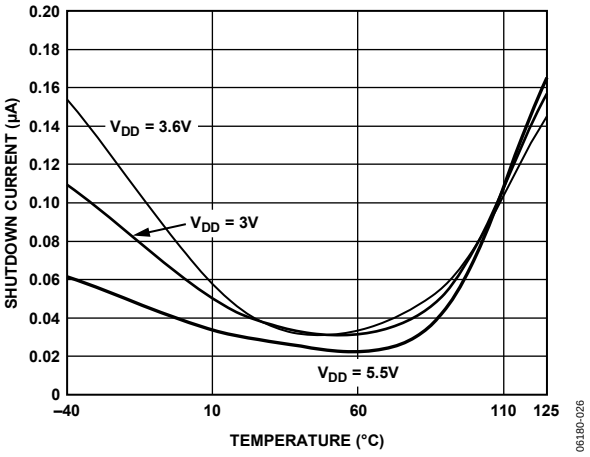

Figure 19. Shutdown Current vs. Temperature, EN = 0 V

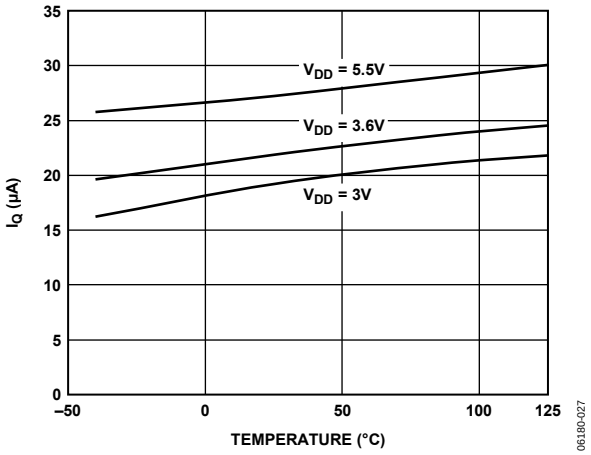

Figure 20. Quiescent Current vs. Temperature, EN = V_{DD}, LED Functions Disabled

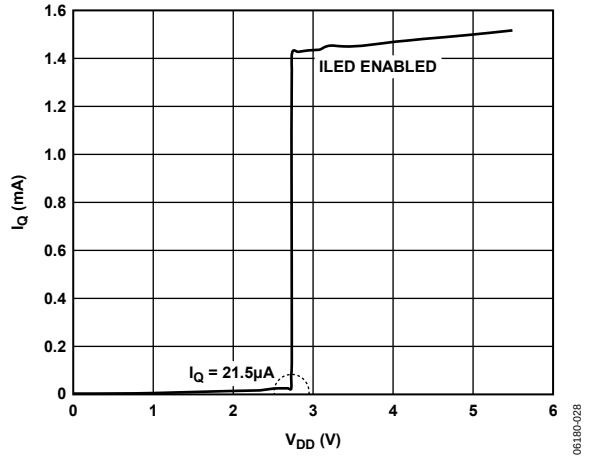

Figure 21. Quiescent Current vs. Temperature, V_{DD} Swept from 5.5 V to 0 V, ILED Active at 2.5 mA Until UVLO Threshold

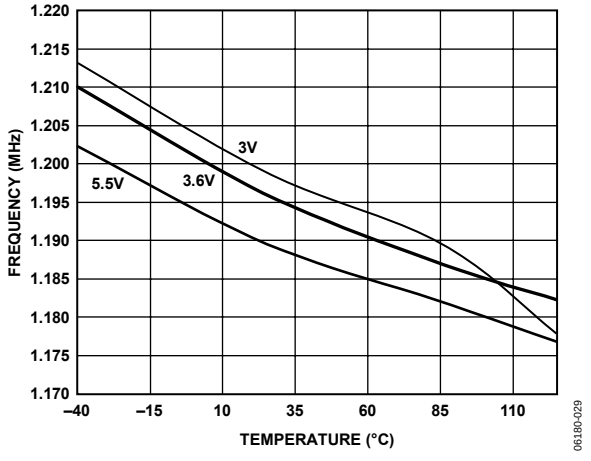

Figure 22. Oscillator Frequency vs. Temperature vs. V_{DD}

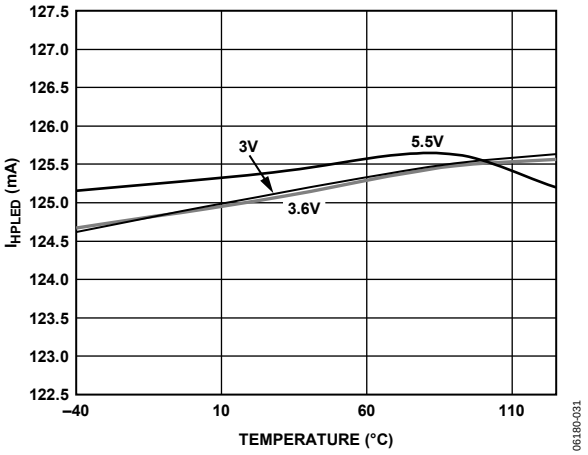

Figure 23. HPLED Regulation, Set at 125 mA, HPLED Register = 00110 (Binary), SETF = V_{DD}

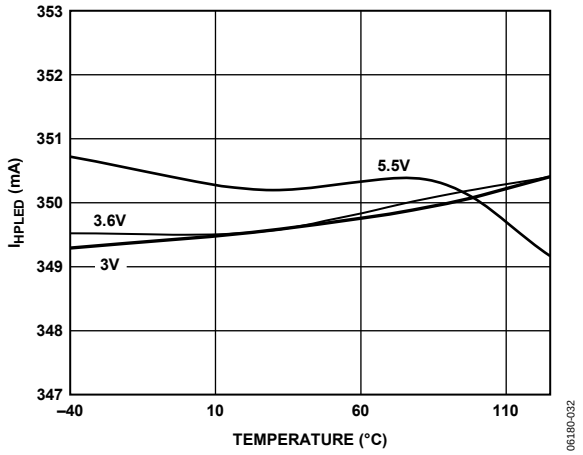

Figure 24. HPLED Regulation, Set at 350 mA, HPLED Register = 10101 (Binary), SETF = V_{DD}

THEORY OF OPERATION

The ADP1653 is a high power, white LED driver ideal for driving white LEDs for use as a camera flash. The ADP1653 includes a step-up converter and a current regulator suitable for powering one, or up to three, high power, white LEDs. A second lower current sink allows an indicator LED to be driven with 2.5 mA to 17.5 mA current.

The ADP1653 responds to a 2-pin control interface that can operate in two separate pin-selectable modes. Tying the INTF pin high enables a 2-bit logic hardwire interface. Tying the INTF pin low enables the I^2C interface.

WHITE LED DRIVER

The ADP1653 drives a step-up converter to power typically one or two series-connected, high power LEDs. The white LED driver regulates the high power LED current for accurate brightness control. The ADP1653 uses an integrated NFET current regulator that drops the voltage when the power LED forward voltage is less than the battery voltage.

When the required LED voltage is greater than the battery voltage, the NFET current regulator voltage at the HPLED pin is approximately 320 mV, and the step-up converter applies the appropriate voltage to OUT, allowing the LED to conduct the regulated current.

When the white LED is turned on, the step-up converter output voltage slew is limited to 18 V/ms to prevent excessive battery current while charging the output capacitor. The output voltage of the step-up converter is sensed at OUT. If the output voltage exceeds the 10.15 V (typical) limit, the white LED converter turns off to indicate that a fault condition has occurred through the $\overline{INT}$ output and system registers. This feature prevents damage due to an overvoltage if the white LED string fails with an open-circuit condition.

Setting the LED regulation currents depends on the 2-pin control interface used, as described in the following sections.

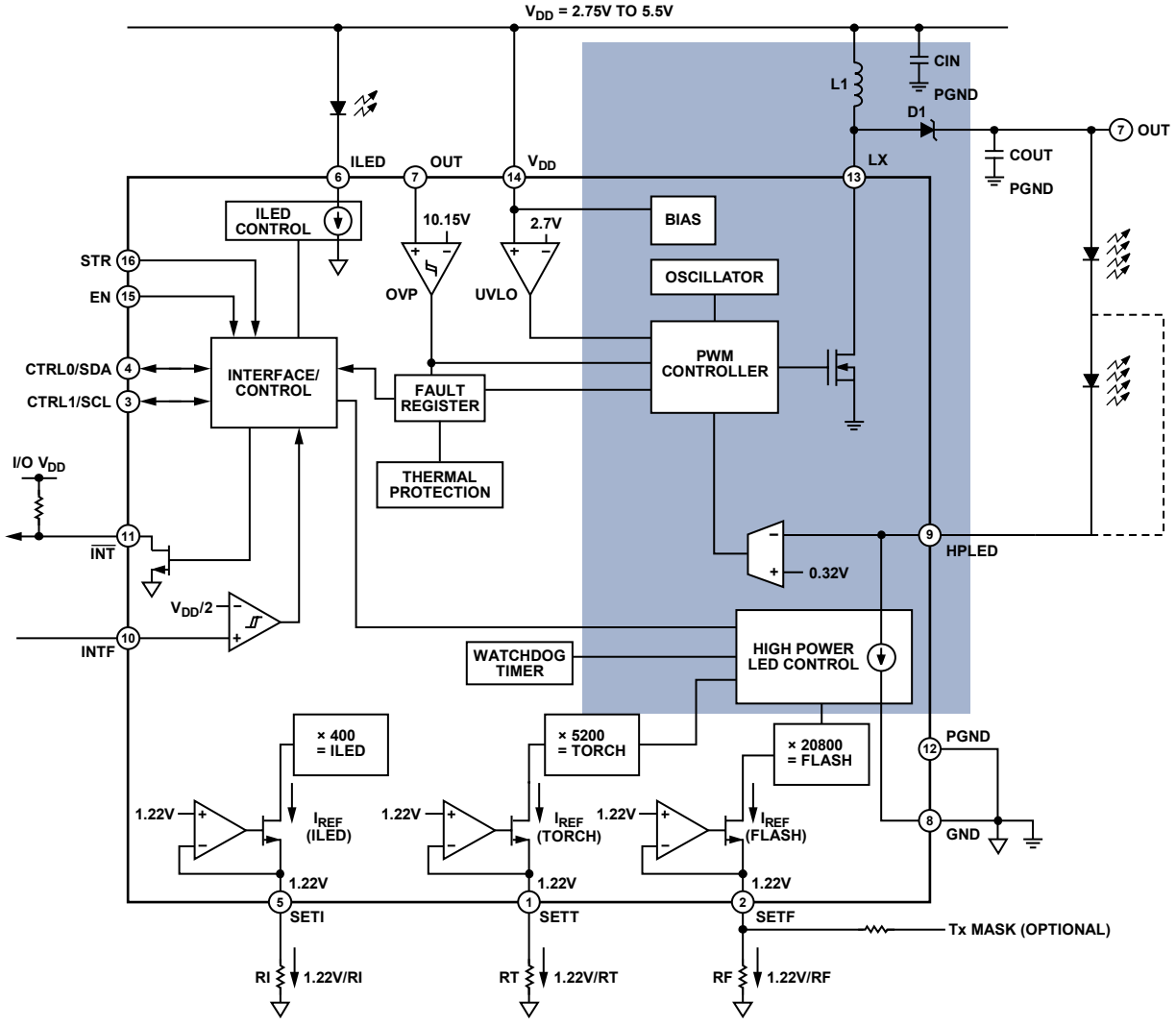

Figure 25. Detailed Block Diagram

2-BIT LOGIC INTERFACE MODE (INTF = 1)

In 2-bit logic interface mode, the two control pins, CTRL1 and CTRL0, select whether the part is disabled or operating in indicator LED mode, torch mode, or flash mode, as outlined in Table 7.

Table 7. 2-Bit Logic Interface Mode Selection

INTF = 1	CTRL1	CTRL0	LED Current Setting Pin	Default Current (SETx = H)
Disabled	0	0	–	–
ILED	0	1	SETI	ILED = 10 mA
Torch	1	0	SETT	HPLED = 125 mA
Flash	1	1	SETF	HPLED = 500 mA

The LED current levels for indicator LED mode, torch mode, and flash mode operation are set with separate external resistors tied between ground and the SETI, SETT, and SETF pins, respectively. The resulting reference current into each SETx pin is equal to 1.22 V/R_{SETx}. The reference current multiplied by a fixed ratio sets the relevant LED current.

Table 8. Reference Current to LED Current Scaling

INTF = 1	CTRL1	CTRL0	LED Current
Disabled	0	0	–
ILED	0	1	I_{REF}(SETI) × 400
Torch	1	0	I_{REF}(SETT) × 5200
Flash	1	1	I_{REF}(SETF) × 20,800

Alternatively, a default internal current setting is used by tying the SETx pin high. The default current for each mode of operation approximately equals the current obtained with a 50 kΩ resistor tied from the SETx pin to ground.

Consequently, the LED current resulting from an external resistor SETx is given by the following equation:

$$I_{LED} = I_{DEFAULT} \times \frac{50\,\text{k}\Omega}{R_{SETx}} \quad (1)$$

where $I_{DEFAULT}$ is the LED current resulting from tying the SETx pin high.

The values of $I_{DEFAULT}$ are given in Table 7 for indicator LED mode (SETI), torch mode (SETT), and flash mode (SETF) operation. For accurate LED current settings, the minimum SETx resistor values should be 25 kΩ (SETI, SETT) or 50 kΩ (SETF).

The flash current can be quickly reduced with an external logic signal (typically 1.8 V logic) by adding a second external resistor from the SETF pin to the logic signal. Bringing this digital input from low to high toggles the flash from normal to reduced current mode by reducing the reference current supplied to the ADP1653 via the SETF pin (see the Applications Information section).

I²C INTERFACE MODE (INTF = 0)

The ADP1653 includes an I²C-compatible serial interface for control of LED current, as well as for readback of system status registers. The I²C chip address is 0x60 (0110 0000 (binary) in write mode).

Figure 26 illustrates the I²C write sequence. The subaddress content selects which of the four ADP1653 registers is written to. Figure 27 shows the I²C read sequence. The ADP1653 sends the data from the register denoted by the subaddress. In this case, the fault register is read (REG3).

The register definitions are shown in Figure 28. The lowest bit number (0) represents the least significant bit, and the highest bit number (7) represents the most significant bit.

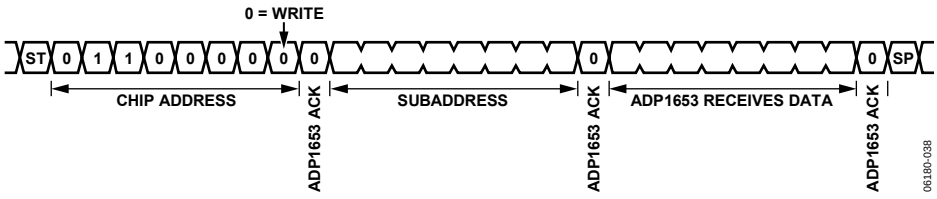

Figure 26. I²C Write Sequence

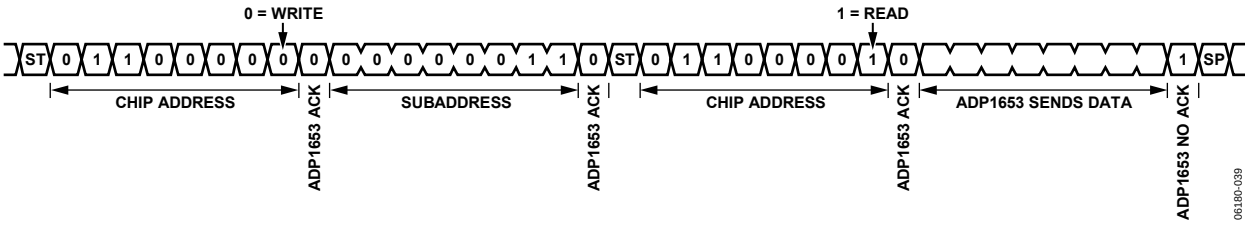

Figure 27. I²C Read Sequence

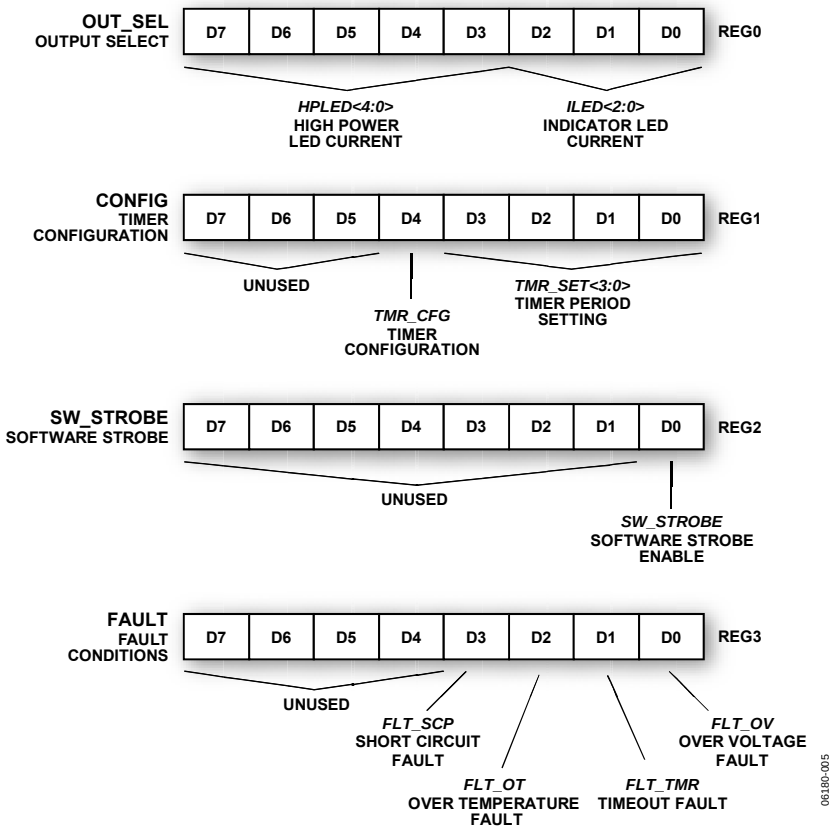

Figure 28. I²C Register Assignments

The LED regulation current levels are controlled by writing to the ILED and HPLED registers. If the ILED register is set to 0, the ILED regulator is turned off and no current flows through the indicator LED. If the ILED register is programmed from 1 (001 binary) to 7 (111 binary), the indicator LED is continuously on, with a current scaled to the register setting given by

$$I_{ILED} = 2.5\ \text{mA} \times Code \quad (2)$$

where *Code* is the ILED register setting. Therefore, the ILED current can be programmed between 2.5 mA and 17.5 mA, using the full range of codes.

If the HPLED register is set to 0, the HPLED regulator is turned off, and no current flows through the high power LED(s). If the HPLED register is programmed from 1 (00001 binary) to 11 (01011 binary), the regulator is in torch mode, and the HPLED remains continuously on, independent of the state of STR. If the HPLED register is programmed between 12 (01100 binary) and 31 (11111 binary), the HPLED regulator remains off until enabled through the strobe input (STR) or a software strobe command. To program a desired HPLED current with SETF tied high, use the following equation:

$$I_{HPLED} = 35\ \text{mA} + Code \times 15\ \text{mA} \quad (3)$$

where *Code* is the HPLED register setting.

Therefore, the HPLED torch current can be programmed between 50 mA and 200 mA for Code 1 to Code 11, and the HPLED flash current can be programmed between 215 mA and 500 mA for Code 12 to Code 31.

Additionally, the HPLED current can be adjusted with an external resistor. This feature is primarily intended for limiting the LED flash current in handset applications when the phone's power amplifier transmits, but it can also be used to modify the HPLED current settings. If an external SETF resistor is present, the HPLED current is given by

$$I_{HPLED} = (35\ \text{mA} + Code \times 15\ \text{mA}) \times \frac{50\ \text{k}\Omega}{R_{SETF}} \quad (4)$$

TURNING ON THE FLASH AND WATCHDOG TIMER

A watchdog timer is always active in flash mode to prevent overstress of the HPLED.

In 2-bit logic interface mode, users select flash operation by setting the CTRL1 pin and the CTRL0 pin high. The watchdog timer in this mode is fixed at 0.82 sec. Bringing the CTRLx pins to another state terminates the flash. If the state of the CTRLx pins remains high for longer than 0.82 sec, flash is automatically disabled by the watchdog timer, and the interrupt pin ($\overline{\text{INT}}$) goes low to indicate a fault.

In I²C mode, users select flash operation by programming the HPLED register between 12 (01100 binary) and 31 (11111 binary). The flash does not turn on until a strobe command is given by either pulling the STR pin high or by writing a software strobe command to the appropriate I²C register.

There are additional settings for the watchdog timer in I²C mode. The strobe command operates in one of two watchdog timer modes, timed flash and user-controlled flash, that are controlled via the state of the timeout configuration (TMR_CFG) bit of the CONFIG register. If TMR_CFG is set (1), the flash operates in timed mode. In timed flash, a rising edge on STR turns on the flash. The flash remains on until the internal timeout occurs, which is set by the TMR_SET bits of the CONFIG register, according to the following equation:

$$t_{FLASH} = 820\text{ ms} - Code \times 54.6\text{ ms} \quad (5)$$

where *Code* ranges from 0 (0000 binary) to 15 (1111 binary), allowing for flash periods ranging from 54 ms to 820 ms.

If TMR_CFG is not set (0), the flash operates in user-controlled timer mode. In user-controlled timer mode, the flash remains on as long as STR is held high. If STR remains high longer than T_{FLASH} (if TMR_SET = 0, t_{FLASH} = 820 ms), the flash is turned off and a fault is set in the watchdog timeout (FLT_TMR) bit of the FAULT register.

The ADP1653 also offers a software strobe option, allowing the user to turn on the flash directly through the I²C interface without pulling the STR pin high. Setting the SW_STROBE register bit to 1 initiates a flash cycle. The strobe can operate in either timed or user-controlled mode, as previously described.

SAFETY FEATURES

Interrupts

For critical system conditions, such as output overvoltage, watchdog timeout, and overtemperature conditions, the ADP1653 indicates that an interrupt event has occurred by asserting the active-low interrupt output $\overline{INT}$. $\overline{INT}$ is an open-drain output and should be pulled up to the I/O voltage rail by using a resistor.

In I²C interface mode, the system baseband processor can read the fault register through the I²C interface to determine the nature of the fault condition after sensing that $\overline{INT}$ has gone low. Users can clear a fault by writing 0x00 to the OUT_SEL register. This brings $\overline{INT}$ high and clears the FAULT register.

In 2-bit logic interface mode, $\overline{INT}$ goes low for the same fault conditions, but I²C register readback is not available. To clear a fault, set CTRL1 and CTRL0 low.

Overvoltage Fault

The ADP1653 contains a comparator at the OUT pin that monitors the voltage from the high power LED(s) to PGND. If the voltage exceeds 10.15 V (typical), the ADP1653 shuts down (I_Q < 45 µA) and $\overline{INT}$ goes low. In I²C mode, Bit D0 in the FAULT register (FLT_OV) is read back as high. The ADP1653 is disabled, and $\overline{INT}$ remains low until the fault is cleared.

Timeout Fault

If the 2-bit logic interface is used, the maximum duration for flash being enabled (CTRL1/CTRL0 =1) is preset to 820 ms. If CTRL1 and CTRL0 remain high for longer than 820 ms, $\overline{INT}$ goes low and the ADP1653 is disabled.

In I²C mode, if TMR_CFG is not set (0), and STR remains high for longer than t_{FLASH} (see Equation 5), $\overline{INT}$ goes low and the FLT_TMR bit in the FAULT register is read back as high. The ADP1653 is disabled, and $\overline{INT}$ remains low until the fault is cleared.

Overtemperature Fault

If the junction temperature of the ADP1653 rises above 155°C, a thermal protection circuit shuts down the LED driver and brings $\overline{INT}$ low. In I²C mode, Bit D2 (FLT_OT) of the FAULT register is read back as high. The ADP1653 is disabled, and $\overline{INT}$ remains low until the fault is cleared.

Short-Circuit Fault

The HPLED pin features short-circuit protection that disables the ADP1653 if it detects a short circuit to ground at the cathode of the LED(s). The ADP1653 monitors the HPLED voltage once the part is enabled in torch mode. If after 820 ms the HPLED pin remains grounded, a short circuit is detected. $\overline{INT}$ goes low, and Bit D3 (FLT_SCP) of the FAULT register is read back as high.

Input Undervoltage

The ADP1653 includes an input undervoltage lockout circuit. If the battery voltage drops below the 2.7 V (typical) input UVLO threshold, the ADP1653 shuts down and the input current drops to less than 45 µA to prevent deep discharge of the battery. In this case, the system register information is lost, and when power is reapplied, a power-on reset circuit resets the registers to their default conditions.

Current Limit

The internal LX switch limits battery current by ensuring that the peak inductor current does not exceed 2.1 A (typical). If the SETI, SETT, or SETF pins accidentally connect to ground, reference current is limited to a maximum of 1 mA.

APPLICATIONS INFORMATION

FLASH-CURRENT FOLDBACK DURING TRANSMIT PULSE

The ADP1653 allows a fast, 1.8 V logic-enabled foldback of the flash current, typically enabled shortly before an RF transmit pulse. This feature extends the life of the battery by preventing overstress of the battery cell. It also extends the life of the phone by reducing the maximum instantaneous system current that can occur, allowing a lower battery operating voltage limit.

2-Bit Logic Interface Mode (INTF = 1)

In 2-bit logic interface mode, the flash current is set with an external resistor. The 1.22 V reference voltage is buffered to the SETF pin, generating a reference current across an external SETF resistor. This reference current is multiplied by a fixed gain to set the flash current in the HPLED.

A 1.8 V compatible logic signal selects normal or reduced flash current by adjusting the reference current, as shown in Figure 29 and Figure 30.

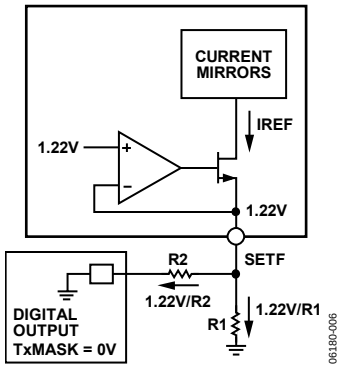

Figure 29. Flash Mode Current Foldback
(Normal Operation with R2 Grounded Through Digital Control Signal)

Full-current flash mode has a reference current of

$$I_{REF\_0} = \frac{1.22\,\text{V}}{R1 // R2} = \frac{1.22\ \text{V} \times (R1 + R2)}{R1 \times R2} \quad (6)$$

The reference current is multiplied by a fixed gain to give the actual flash current (see Table 8).

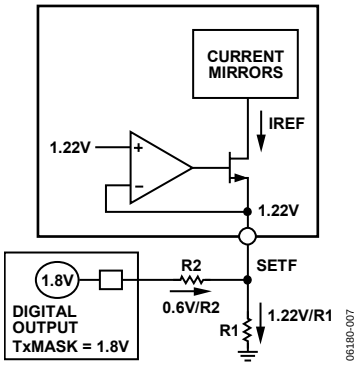

Figure 30. Flash Mode Current Foldback with 1.8 V Signal Applied to R2

A logic high to R2 changes the direction of the current in R2.

$$I_{REF} = I_{R1} - I_{R2} \quad (7)$$

$$I_{REF} = \frac{1.22\,\text{V}}{R1} - \frac{V_{Tx\ mask} - 1.22\,\text{V}}{R2} \quad (8)$$

$$I_{HPLED} = I_{REF} \times 20{,}800 \quad (9)$$

The ratio of full flash current to reduced flash current for a 1.8 V logic signal is approximately

$$\frac{Full\ Flash}{Reduced\ Flash} = \frac{R2 + R1}{R2 - \frac{R1}{2}} \quad (10)$$

If R1 = R2 = 100 kΩ, maximum flash current is 500 mA, and reduced flash current is 125 mA.

I²C Mode (INTF = 0)

To allow flash current foldback in I²C mode, the user should connect a resistor between SETF and ground, and another resistor from SETF to the logic input, as shown in Figure 29 and Figure 30. Operation is the same as for the 2-bit logic interface mode, except the flash current is additionally scaled by setting the HPLED bits in the OUT_SEL register.

Full-current flash mode (Tx mask = 0 V) has a flash current of

$$I_{HPLED} = (35\ \text{mA} + Code \times 15\ \text{mA}) \times \frac{50\ \text{k}\Omega}{R_{SETF}} \quad (11)$$

where:

R_{SETF} is a parallel combination of R1 and R2.
Code is the HPLED register setting.

Bring the Tx mask voltage high for reduced reference current. Therefore, the reduced LED current is I_{HPLED} (see Equation 13).

$$I_{REF} = \frac{1.22\ \text{V}}{R1} - \frac{V_{Tx\ mask} - 1.22\,\text{V}}{R2} \quad (12)$$

$$I_{HPLED} = (35\,\text{mA} + Code \times 15\,\text{mA}) \times \frac{50\ \text{k}\Omega \times I_{REF}}{1.22\ \text{V}} \quad (13)$$

EXTERNAL COMPONENT SELECTION

Selecting the Inductor

The ADP1653 step-up converter increases the battery voltage to allow driving one, two, or three LEDs, whose combined voltage drop is higher than the battery voltage plus the 0.32 V (typical) current source headroom voltage. This allows the converter to regulate the HPLED current over the entire battery voltage range and with a wide variation of LED forward voltage.

Users should choose an inductor value such that the inductor ripple current is approximately 2/5th of the maximum dc input load current. In general, lower inductance values have higher saturation current and lower series resistance for a given physical size. For most applications, an inductor in the range of 1.5 µH to 3.3 µH works well.

To determine the inductor ripple current, users should first calculate the switch duty cycle for the step-up converter, which is determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and Schottky forward voltage (V_F). V_{OUT} equals the LED voltage drop plus 320 mV (typical) overhead for the HPLED current regulator.

$$\frac{V_{IN}}{V_{OUT}+V_F}=1-D \tag{14}$$

Solving for D

$$D=1-\frac{V_{IN}}{V_{OUT}+V_F}=\frac{V_{OUT}+V_F-V_{IN}}{V_{OUT}+V_F}$$

The HPLED (output) current is regulated as low as 50 mA (torch mode) and as high as 500 mA (flash mode). The maximum dc input current is related to the maximum dc output current by the following equation:

$$I_{IN(MAX)}=I_{OUT(MAX)}\times\left(\frac{V_{OUT}}{V_{IN}}\right)\times\frac{1}{\eta} \tag{15}$$

where η is efficiency (assume $\eta \approx 0.80$ in the two-LED case).

Choose the initial inductor value by using the equation

$$L=\frac{V_{IN}}{\Delta I_L\times f_{SW}}\left(\frac{V_{OUT}+V_F-V_{IN}}{V_{OUT}+V_F}\right) \tag{16}$$

where:

L is the inductor value (reduce L to reduce solution size).
f_{SW} is the switching frequency.
ΔI_L is the inductor ripple current, typically 2/5th of the maximum dc input current.
V_F is the forward voltage of the Schottky diode.

The inductor saturation current should be greater than the sum of the dc input current and half the inductor ripple current. A reduction in the effective inductance due to saturation increases the inductor current ripple but improves loop stability, reducing the amount of output capacitance required. Ensure that the peak inductor current (dc + 1/2 of inductor ripple) is less than the LX minimum current limit (1.5 A).

Selecting the Input Capacitor

The ADP1653 requires an input bypass capacitor to supply transient currents while maintaining constant input and output voltage. The input capacitor carries the input ripple current, allowing the input power source to supply only the dc current. Use an input capacitor with sufficient ripple current rating to handle the inductor ripple. A 4.7 µF X5R/X7R ceramic capacitor rated for 6.3 V is the minimum recommended input capacitor. Increased input capacitance reduces the amplitude of the switching frequency ripple on the battery. Because of the dc bias characteristics of ceramic capacitors, a 0603, 6.3 V X5R/X7R, 10 µF ceramic capacitor is preferable.

Selecting the Diode

The ADP1653 is a nonsynchronous boost and, as such, requires an external Schottky rectifier to conduct the inductor current to the output capacitor and HPLEDs when the LX switch is off. Ensure that the Schottky peak current rating is greater than the maximum inductor current. Choose a diode with an average current rating that is significantly larger than the maximum LED current. To prevent thermal runaway, derate the Schottky rectifier to ensure reliable operation at high junction temperatures. To achieve the best efficiency, select a Schottky diode with a low V_F.

Selecting the Output Capacitor

The output capacitor maintains the output voltage and supplies the HPLED current when the LX switch is on. It also stabilizes the loop. A 4.7 µF, 16 V X5R/X7R ceramic capacitor is generally recommended. The minimum required capacitance for loop stability for the two-LED and one-LED cases is shown in Figure 31 and Figure 32, respectively. Choose a capacitor with a capacitance greater than the minimum shown in Figure 31 and Figure 32 for the worst case dc bias voltage and temperature condition.

Note that dc bias characterization data is available from capacitor manufacturers and should be taken into account when selecting input and output capacitors.

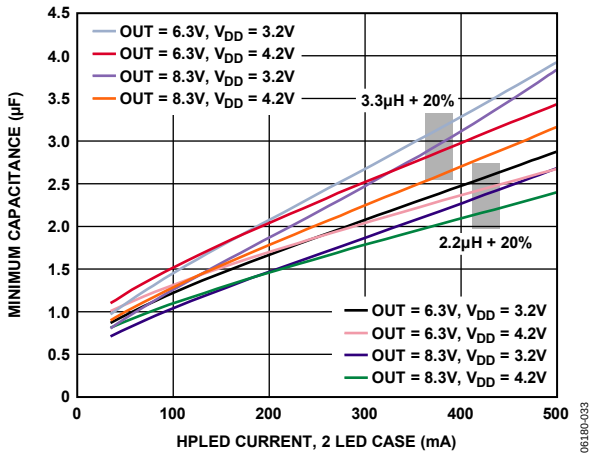

Figure 31. Minimum Output Capacitance for L = 3.3 µH + 20% and L = 2.2 µH + 20% for Two-LED Designs

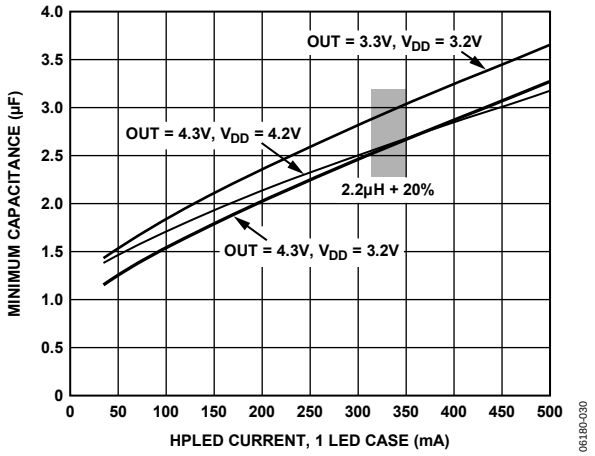

Figure 32. Minimum Output Capacitance for L = 2.2 µH + 20% for One-LED Design

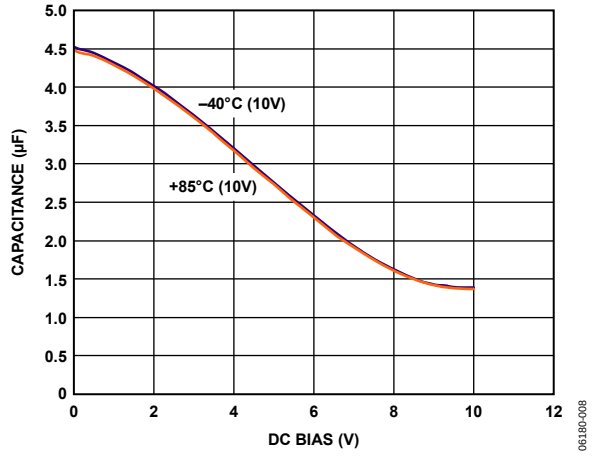

Figure 33. DC Bias Characteristic of a 10 V, 4.7 µF Ceramic Capacitor

PCB BOARD LAYOUT

Good PCB layout is important to maximize efficiency and to minimize noise and electromagnetic interference (EMI). An example PCB layout is shown in Figure 34. Refer to the following guidelines for adjustment to the suggested layout.

The high current paths are shown in Figure 35. Place components that are on high current paths first. To minimize large current loops, place the input capacitor, inductor, Schottky diode, and output capacitor as close as possible to each other and to the ADP1653 using wide tracks (use shapes where possible).

Use separate analog and power ground planes. The analog ground plane is used to ground the SETI, SETT, and SETF resistors and for any digital connections (that is, INTF = 0 = AGND).

Use the power ground plane to ground the power components. Connect the input capacitor, output capacitor, and the PGND pin (Pin 12) to the PGND plane. If it is not possible to make the PGND plane continuous, use a number of low inductance vias to connect the planes. Connect the AGND and PGND planes at the paddle or close to the paddle of the ADP1653.

The SETI, SETT, and SETF resistors set a small reference current that generates the LED current. To minimize noise and current error, connect the SETI, SETT, and SETF resistors as close as possible to the ADP1653. Connect the other end of the resistors directly to the AGND plane.

Connect the output capacitor to the high power LED(s), using a wide, low resistance trace. Connect the bottom of the LED string back to the HPLED pin (Pin 9) with a wide trace. The GND pin (Pin 8) is connected to the source of the current regulator NFET. Ensure that there is a low impedance back to the battery for the high power LED current by connecting the GND pin to the PGND plane with a low impedance via(s) close to the GND pin.

The OUT pin is used for soft start and contains a comparator for overvoltage protection. Connect the output capacitor back to the OUT pin (Pin 7) with a direct trace. The trace does not need to be wide.

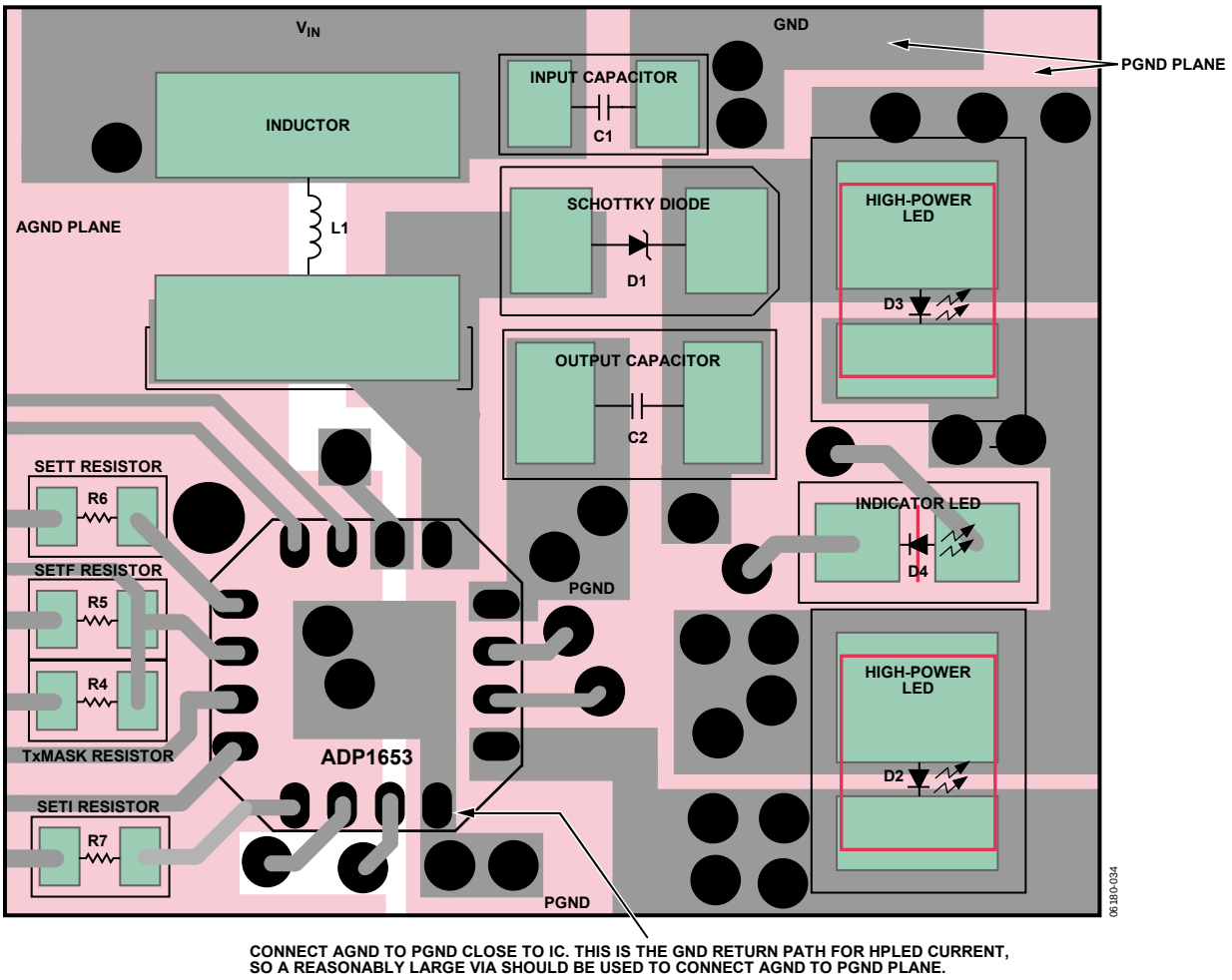

Figure 34. Example Layout of ADP1653 Driving Two White LEDs, Pink = GND Layer, Gray/Green = Top Layer (a One-LED Layout Is Similar)

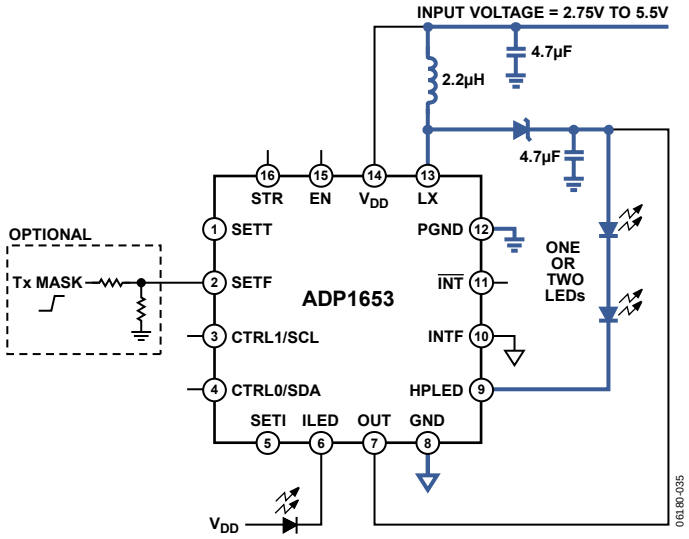

Figure 35. Typical Applications Circuit (High Current Lines Are Shown in Bold)

OUTLINE DIMENSIONS

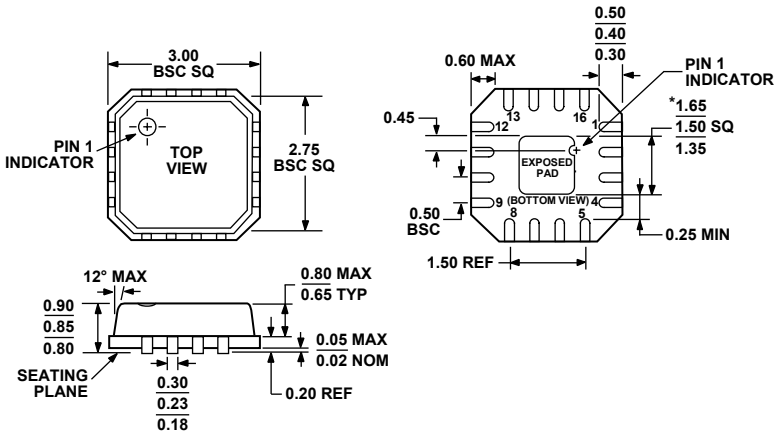

Figure 36. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm x 3 mm Body, Very Thin Quad (CP-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADP1653ACPZ-R2[1]	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-3	L3H
ADP1653ACPZ-R7[1]	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-3	L3H
ADP1653-EVALZ[1]		Evaluation Board		

[1] Z = Pb-free part.

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