TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

4,194,304-WORD BY 1-BIT/1,048,576-WORD BY 4-BIT CMOS STATIC RAM

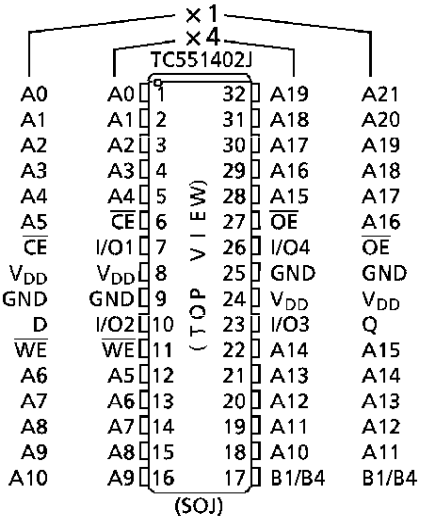
DESCRIPTION

The TC551402J is a 4,194,304-bit high speed static random access memory (SRAM), it is possible to change the organization between 4,194,304 words by 1 bit and 1,048,576 words by 4 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 5 V power supply. Chip enable ($\overline{CE}$) can be used to place the device in a low-power mode, and output enable ($\overline{OE}$) provides fast memory access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are isolated and directly TTL compatible. The TC551402J is available in a plastic 32-pin SOJ package (400 mil width) for high density surface assembly.

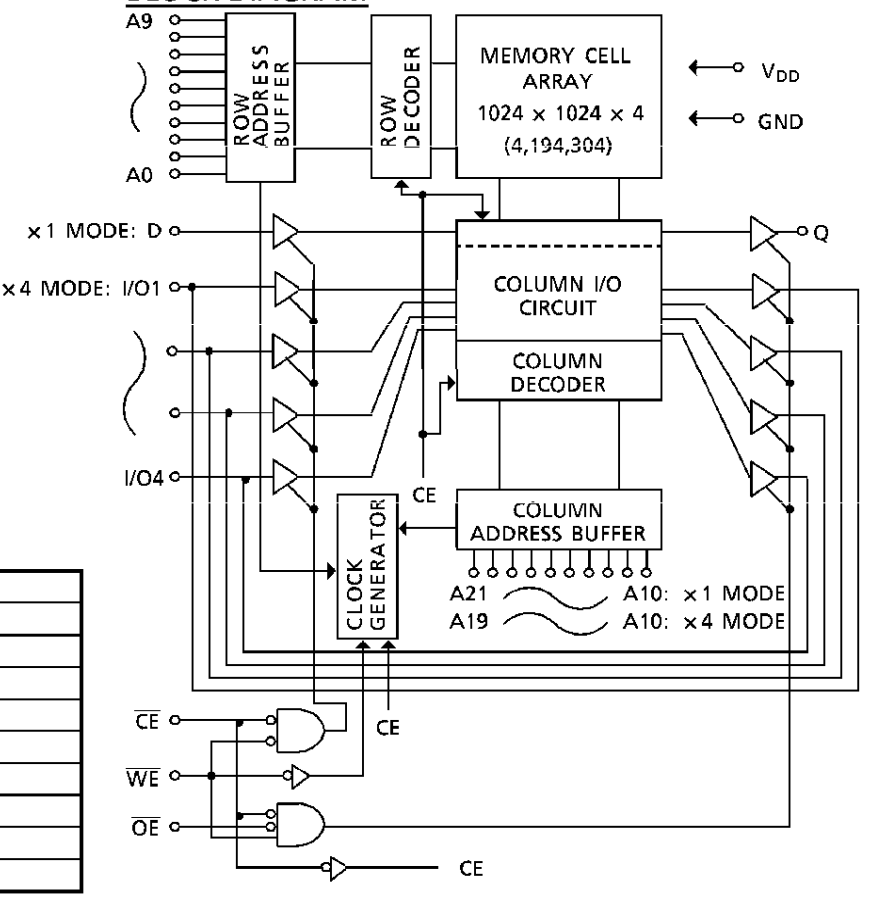
FEATURES

- Fast access time (the following are maximum values)
  TC551402J-22 : 22 ns
  TC551402J-25 : 25 ns
- Low-power dissipation
  (the following are maximum values)
  Operating: 180 mA (22 ns type)
  Operating: 160 mA (25 ns type)
  Standby : 10 mA (all devices)
- Single power supply voltage:
  TC551402J-22 : 5V±5%
  TC551402J-25 : 5V±10%
- Fully static operation
- All inputs and outputs are TTL compatible
- Separate inputs and outputs (×1 Mode),
  Common data input and output (×4 Mode)
- Output buffer control using $\overline{OE}$
- Package :
  SOJ32-P-400-1.27A (Weight : 1.22 g typ)

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAME

A0 to A21	Address Inputs
I/O1 to I/O4	Data Inputs/Outputs
D	Data Input
Q	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+ 5 V)
GND	Ground
B1/B4	Bit Function

961001EBA1

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	− 0.5 to 7.0	V
V_{IN}	Input Terminal Voltage	− 2.0* to 7.0	V
$V_{I/O}$	I/O Terminal Voltage	− 0.5* to V_{DD} + 0.5	V
V_{OUT}	Output Terminal Voltage	− 0.5* to V_{DD} + 0.5	V
P_D	Power Dissipation	1.0	W
Tsolder	Soldering Temperature (10 s)	260	°C
Tstrg	Storage Temperature	− 65 to 150	°C
Topr	Operating Temperature	− 10 to 85	°C

*: − 3 V with a pulse width of 10 ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER		MIN	TYP	TYP	UNIT
V_{DD}	Power Supply Voltage	-22	4.75	5.0	5.25	V
		-25	4.5	5.0	5.5	
V_{IH}	Input High Voltage		2.2	−	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage		− 0.5 *	−	0.8	V

*: − 3 V with a pulse width of 10 ns

DC CHARACTERISTICS (Ta = 0° to 70°C, -22 : V_{DD} = 5V ± 5%, -25 : V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	TYP	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{DD}		−	−	± 10	μA
I_{OH}	Output High Current	V_{OH} = 2.4 V		− 4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V		8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 V to V_{DD}		−	−	± 10	μA
I_{DDO}	Operating Current	tcycle = Minimum Cycle, $\overline{CE}$ = V_{IL}, Iout = 0 mA, Other Inputs = V_{IH} or V_{IL}	-22	−	−	180	mA
			-25	−	−	160	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} Other Inputs = V_{IH} or V_{IL}		−	−	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2 V Other Inputs = V_{DD} − 0.2 V or 0.2 V		−	−	10	

CAPACITANCE (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	8	pF
$C_{I/O}$, C_{OUT}	D_{OUT} Capacitance	V_{OUT} = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

TRUTH TABLE

MODE		B1/B4	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	POWER
×1 MODE	Read	H	L	L	H	Dout	I_{DDO}
	Write	H	L	×	L	Din	I_{DDO}
	Output Disabled	H	L	H	H	High - Z	I_{DDO}
	Standby	H	H	×	×	High - Z	I_{DDS}
×4 MODE	Read	L	L	L	H	Dout	I_{DDO}
	Write	L	L	×	L	Din	I_{DDO}
	Output Disabled	L	L	H	H	High - Z	I_{DDO}
	Standby	L	H	×	×	High - Z	I_{DDS}

×: "H" or "L"

TC551402J is possible to change the organization of bit mode between 4M words by one bit and 1M words by four bits with input level of pin condition B1/B4.

"4M × 1 Mode" is performed on when pin B1/B4 is held on "V_{IH} level". On the other hand "1M × 4 Mode" is requires B1/B4 be connected to "V_{IL} level".

Input level of B1/B4 condition must be set at the same time of power on. Any of change of input level B1/B4, high or low, is prohibited after power on.

AC CHARACTERISTICS (Ta = 0° to 70°C (Note 4), -22 : V_{DD} = 5V ± 5%, -25 : V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC551402J-22		TC551402J-25		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	22	–	25	–	ns
t_{ACC}	Address Access Time	–	22	–	25	
t_{CO}	Chip Enable Access Time	–	22	–	25	
t_{OE}	Output Enable Access Time	–	12	–	12	
t_{COE}	Output Enable Time from Chip Enable	5	–	5	–	
t_{COD}	Output Disable Time from Chip Enable	–	10	–	10	
t_{OEE}	Output Enable Time from Output Enable	1	–	1	–	
t_{ODO}	Output Disable Time from Output Enable	–	10	–	10	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	
t_{PD}	Chip Deselection to Power Down Time	–	22	–	25	

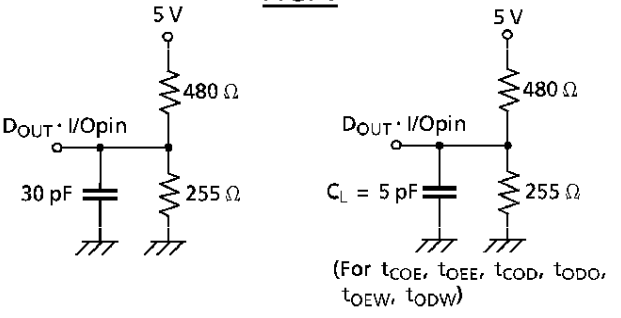
WRITE CYCLE

SYMBOL	PARAMETER	TC551402J-22		TC551402J-25		UNIT
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	22	–	25	–	ns
t_{WP}	Write Pulse Width	13	–	13	–	
t_{AW}	Address Valid to End of Write	20	–	20	–	
t_{CW}	Chip Enable to End of Write	20	–	20	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{OEW}	Output Enable Time from Write Enable	1	–	1	–	
t_{ODW}	Output Disable Time from Write Enable	–	10	–	10	
t_{DS}	Data Setup Time	12	–	12	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC TEST CONDITION

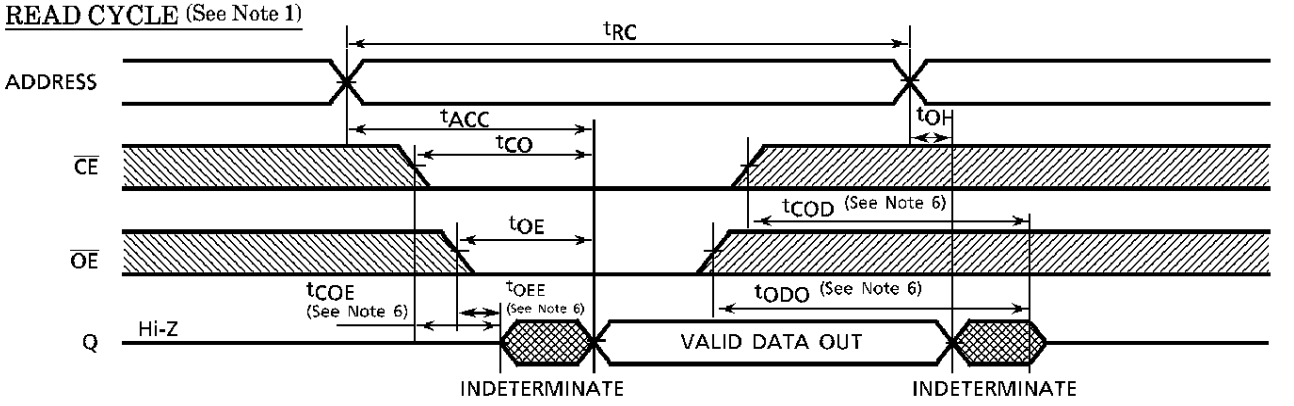
Input Pulse Levels	3.0 V, 0.0 V
Input Pulse Rise and Fall Time	3 ns
Input Timing Measurement Reference Levels	1.5 V
Output Timing Measurement Reference Levels	1.5 V
Output Load	Fig. 1

FIG. 1

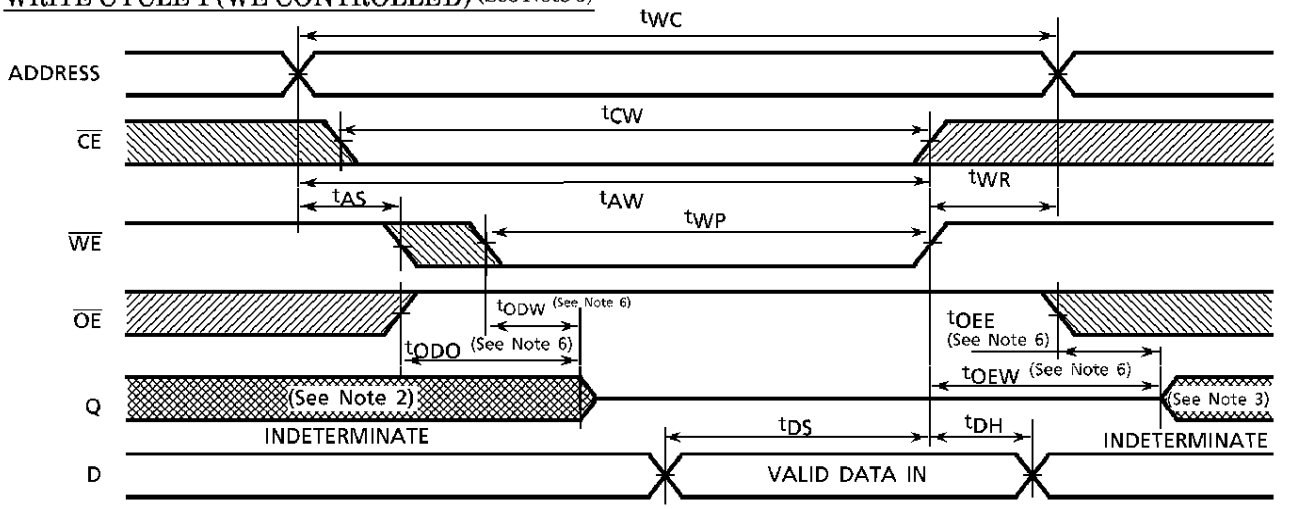


TIMING DIAGRAMS

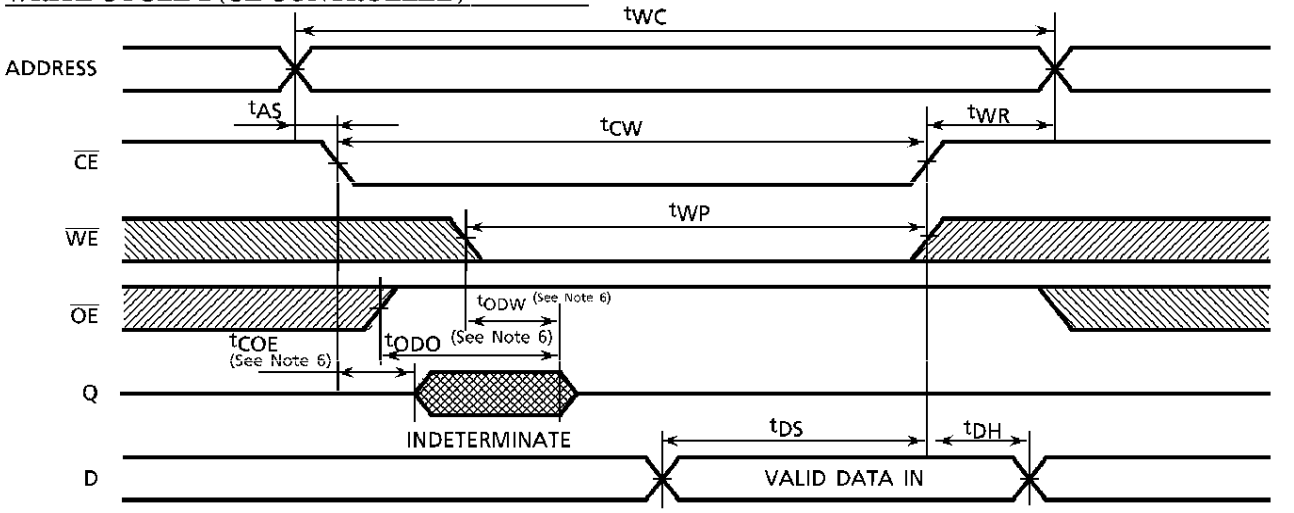
READ CYCLE (See Note 1)



WRITE CYCLE 1 ($\overline{WE}$ CONTROLLED) (See Note 5)



WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 5)



Note: (1) Operating temperature (Ta) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2) $\overline{WE}$ remains HIGH for Read Cycle.

(3) If $\overline{CE}$ goes LOW coincident with or after $\overline{WE}$ goes LOW, the outputs will remain at high impedance.

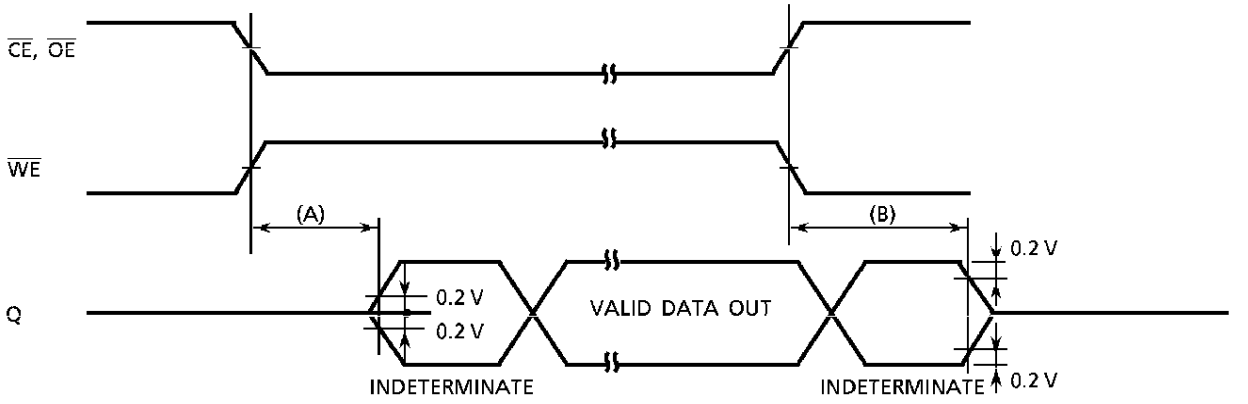
(4) If $\overline{CE}$ goes HIGH coincident with or before $\overline{WE}$ goes HIGH, the outputs will remain at high impedance.

(5) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig. 1.

(A) t_{COE}, t_{OEE}, t_{OEW} ····· Output Enable Time

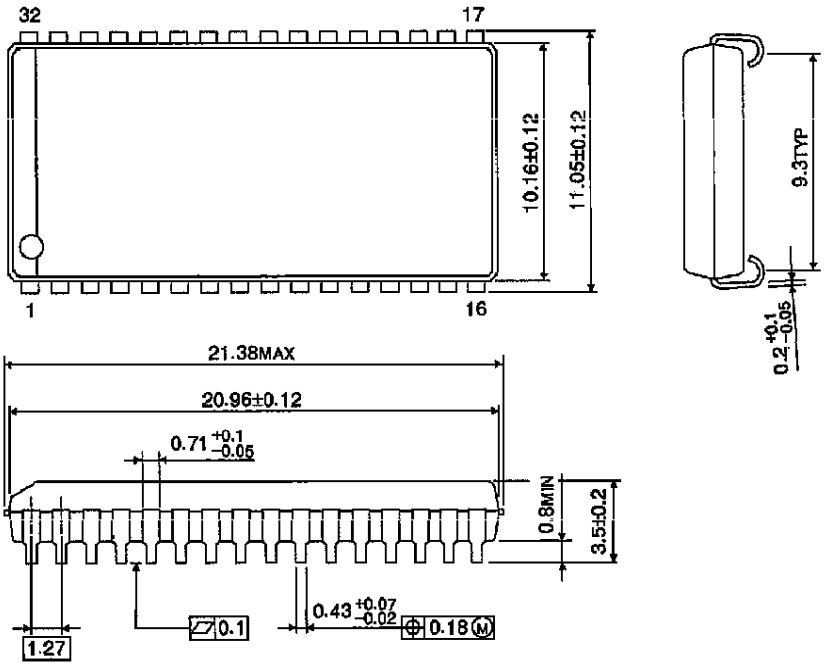
(B) t_{COD}, t_{ODO}, t_{ODW} ····· Output Disable Time



PACKAGE DIMENSIONS

Plastic SOJ (SOJ32-P-400-1.27A)

Units in mm



Weight: 1.22 g (typ)